Computer Architecture Lab
Assignment 3

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1 Introduction

This assignment involves developing a single cycle processor simulator for the ToyRISC ISA.

2 Benchmarks

Benchmarks for the provide sample programs in the current processor simulator are as follows,

Program	Static Instructions	Dynamic Instuctions	Cycles	IPC	Frequency (GHz)
Descending	21	277	277	1.0	0.2
Even Odd	9	6	6	1.0	0.2
Fibonacci	21	78	78	1.0	0.2
Palindrome	16	49	49	1.0	0.2
Prime	16	29	29	1.0	0.2

2.1 Static Instructions

This metric measures the number of static instruction present in the program.

2.2 Dynamic Instructions

This metric measures the number of dynamic instructions executed during the simulation of the program on the processor.

2.3 Cycles

This metric measure the number of cycles required to complete execution of the program.

2.4 IPC

This metric measure the Instructions Executed per Cycle during the simulation.

2.5 Frequency

This metric measures the frequency in GHz of instructions executed in the simulation. We currently assume that all stages take exactly 1 nanosecond to execute.