Computer Architecture Lab Assignment 4

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1 Introduction

This assignment involves developing a pipelined processor simulator for the ToyRISC ISA.

2 Benchmarks

Benchmarks for the provide sample programs in the current processor simulator are as follows,

Program	Static Instructions	Dynamic Instuctions	Cycles	IPC	Frequency (GHz)	Stalls	Incorrect Branches
Descending	21	368	129	2.852713	0.2	192	88
Even Odd	9	7	4	1.75	0.2	14	0
Fibonacci	21	96	36	2.6667	0.2	68	16
Palindrome	16	57	28	2.0357	0.2	79	7
Prime	16	35	13	3.6923	0.2	28	5

2.1 Static Instructions

This metric measures the number of static instruction present in the program.

2.2 Dynamic Instructions

This metric measures the number of dynamic instructions executed during the simulation of the program on the processor.

2.3 Cycles

This metric measure the number of cycles required to complete execution of the program.

2.4 IPC

This metric measure the Instructions Executed per Cycle during the simulation.

2.5 Frequency

This metric measures the frequency in GHz of instructions executed in the simulation. We currently assume that all stages take exactly 1 nanosecond to execute.

2.6 Stalls

The number of dynamic instructions for which the stage did not do any operation (i.e. no. of bubbles)

2.7 Incorrect Branches

The number of dynamic branch instructions for which the branch taken was incorrect, and 2 bubbles had to be added into the pipeline in OF and IF stages, invalidating the present instructions in them.

2.8 Observations

The IPC of the pipelined processor is higher than that of the single cycle processor. The IPC is inversely proportional to the number of stalls and incorrect branches; also, IPC is directly proportional to number of dynamic instructions. The frequency remains the same. These facts can be observed from the above benchmarked data.