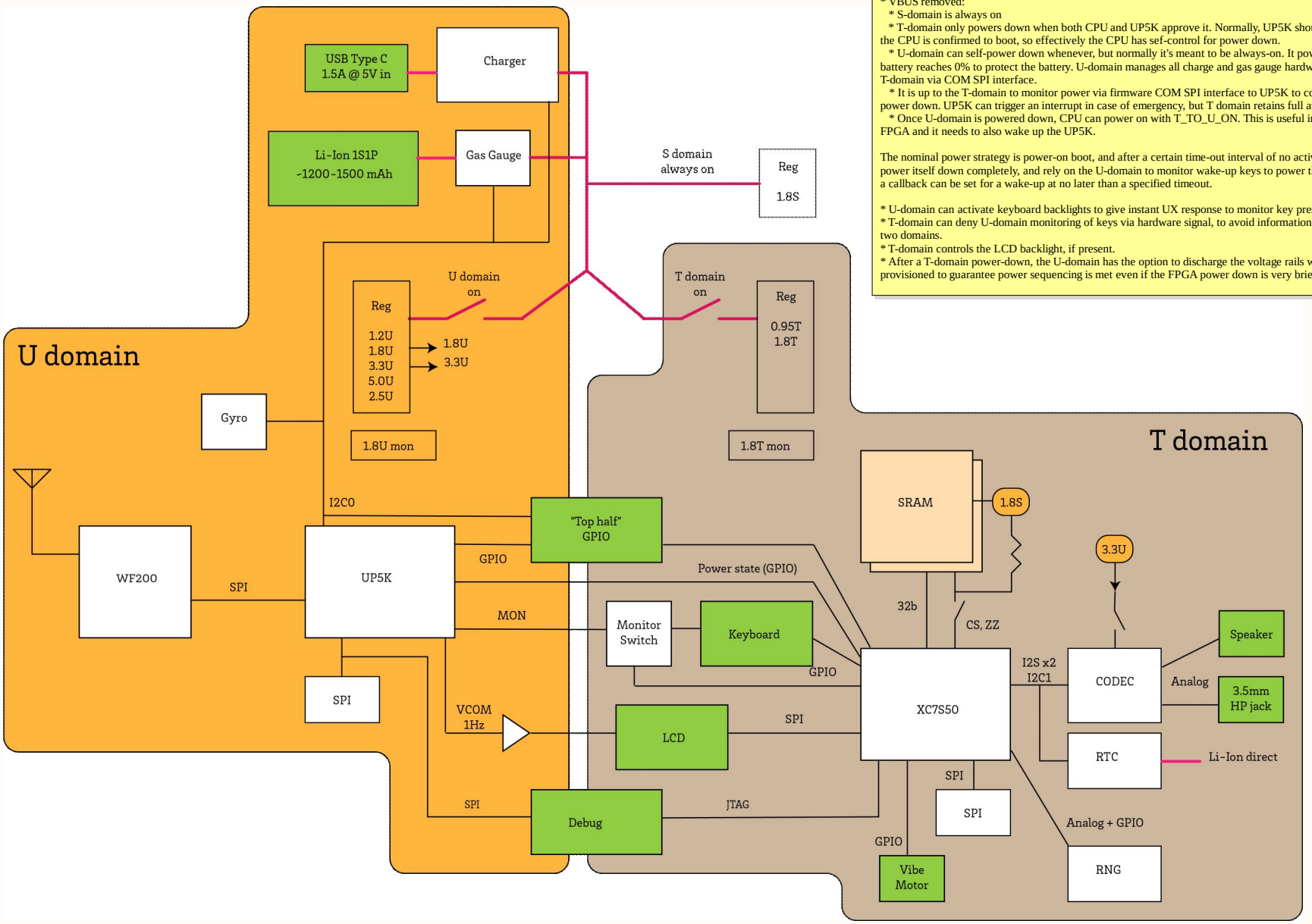
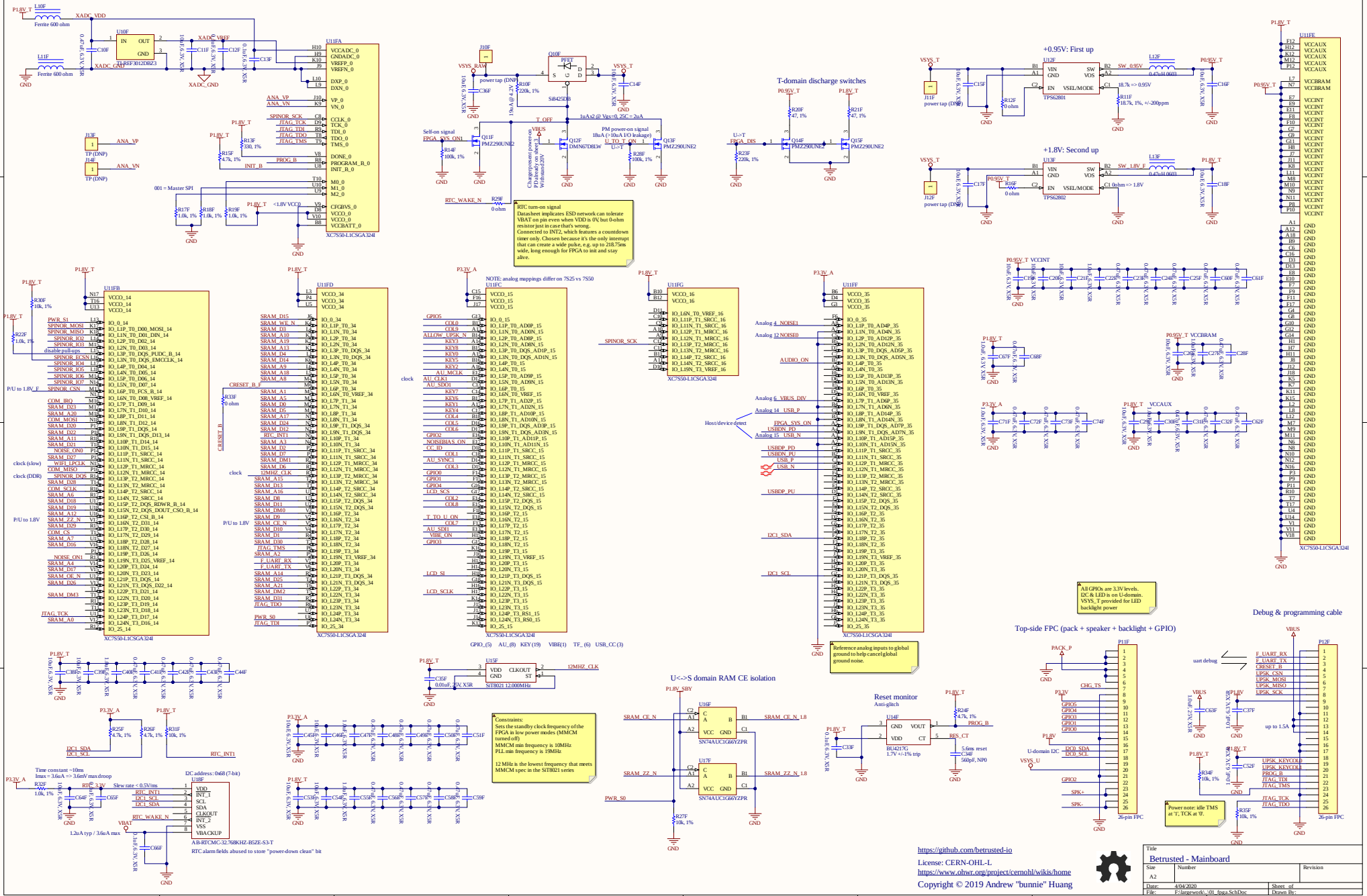


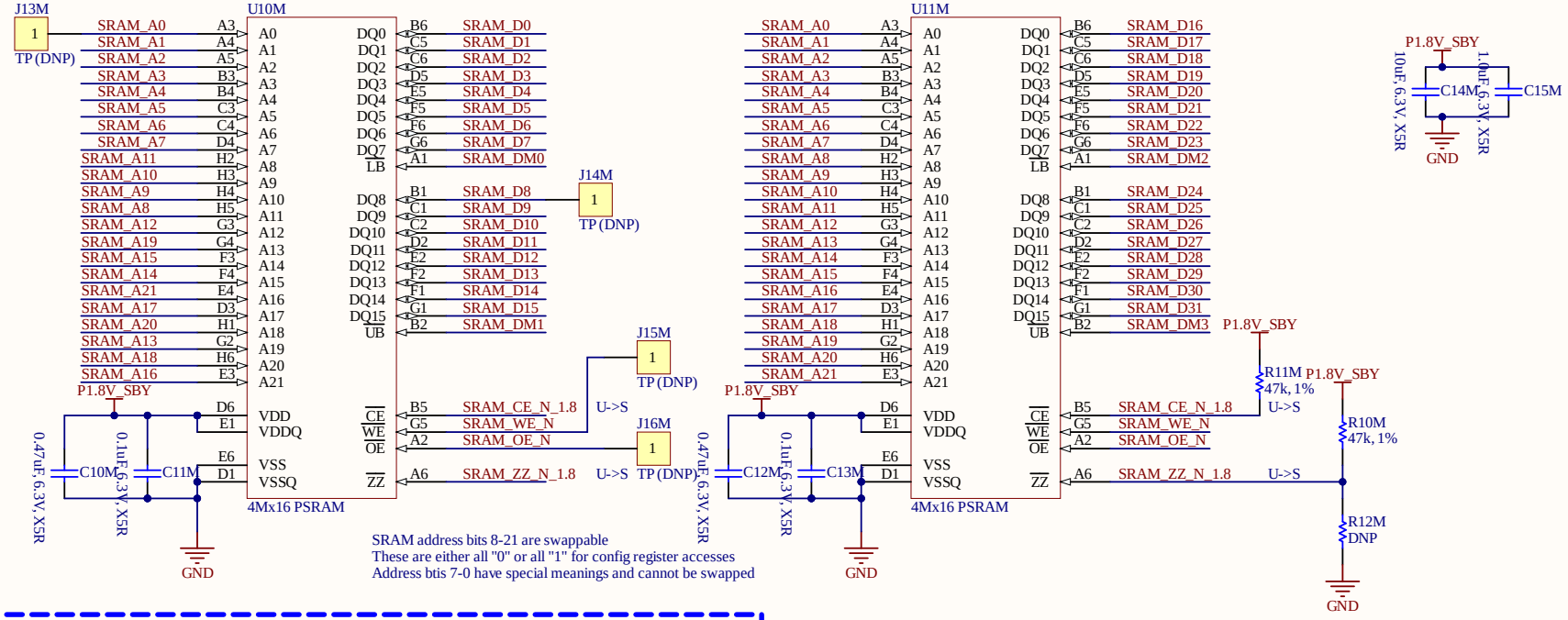
https://github.com/betrusted-io

Title	Betrusted - Mainboard	
Size: A	Number:	Revision:
Date: 4/04/2020		Sheet of
File: F:\largework\..\00_map.SchDoc		Drawn By:

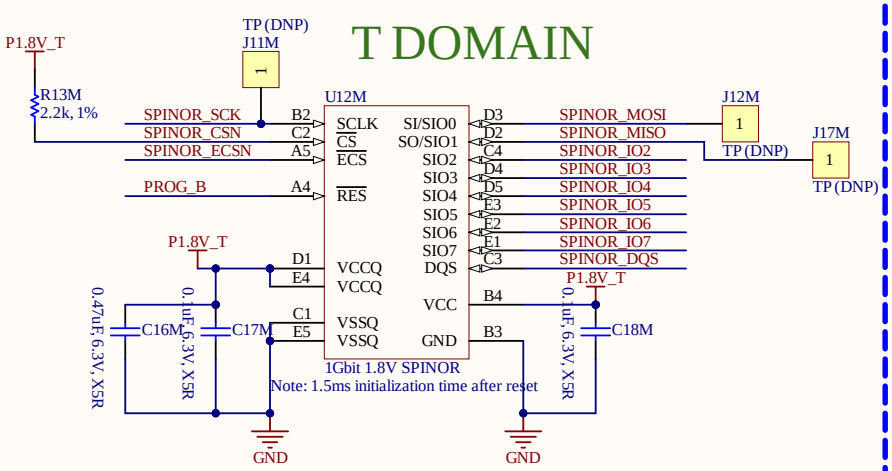
T DOMAIN


U11FA
U11FB
U11FC
U11FD
U11FE
U11FF
U11FG
XC7S50-1CSGA324I
T-domain discharge switches
+0.95V: First up
+1.8V: Second up
RTC turn-on signal
Datasheet implicates ESD network can tolerate VBAT on pin even when VDD is 0V, but 0-ohm resistor just in case that's wrong.
Connected to INT2, which features a countdown timer only. Chosen because it's the only interrupt that can create a wide pulse, e.g. up to 218.75ms wide, long enough for FPGA to init and stay alive.
All GPIOs are 3.3V levels.
I2C & LED is on U-domain.
VSYS_T provided for LED backlight power
Reference analog inputs to global ground to help cancel global ground noise.
Constraints:
Sets the standby clock frequency of the FPGA in low power modes (MMCM turned off)
MMCM min frequency is 10MHz
PLL min frequency is 19MHz
12 MHz is the lowest frequency that meets MMCM spec in the SiT8021 series
U<->S domain RAM CE isolation
Reset monitor
Anti-glitch
Top-side FPC (pack + speaker + backlight + GPIO)
Debug & programming cable
Power note: idle TMS at '1', TCK at '0'.
AB-RTCMC-32.768KHZ-B5ZE-S3-T
RTC alarm fields abused to store "power-down clean" bit
https://github.com/betrusted-io
License: CERN-OHL-L
https://www.ohwr.org/project/cernohl/wikis/home
Copyright © 2019 Andrew "bunnie" Huang
Title
Betrusted - Mainboard
Size
A2
Number
Revision
Date: 4/04/2020
File: F:\largework_\01_fpga.SchDoc
Sheet of
Drawn By:

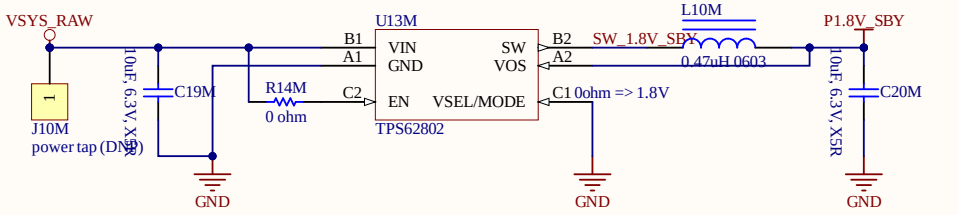
T-SBY DOMAIN



T DOMAIN

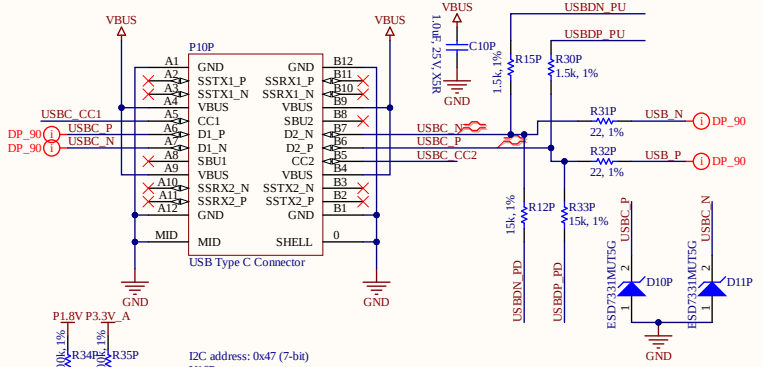


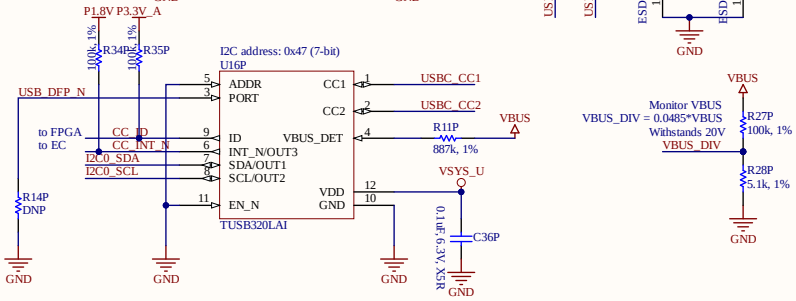
+1.8V_SBY: always on

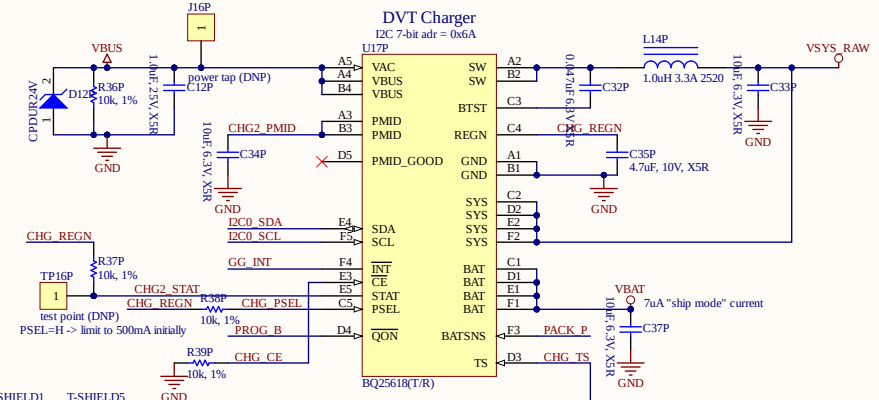


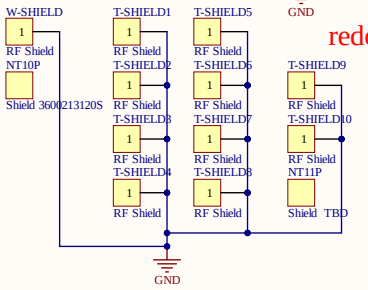
Title: Betrusted - Mainboard		
Size: A4	Number:	Revision:
Date: 4/04/2020		Sheet of
File: F:\largework\..\02_memory.SchDoc		Drawn By:

U DOMAIN

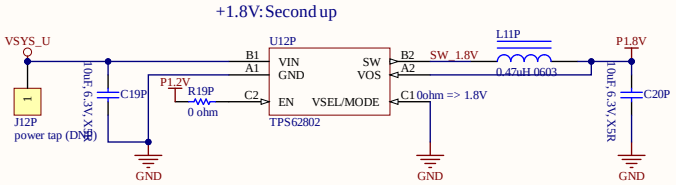


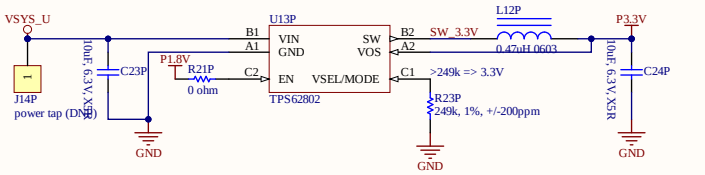


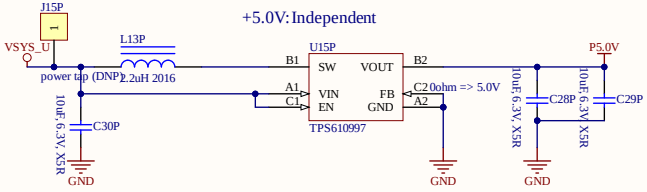


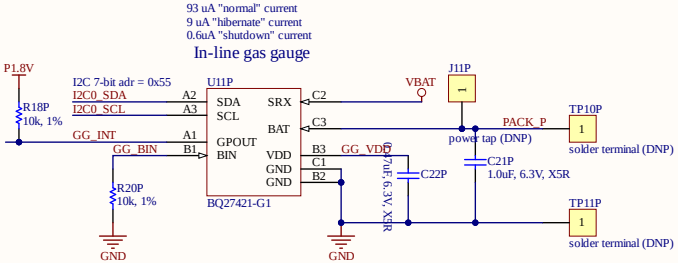


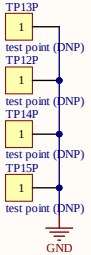
redo firmware for charger

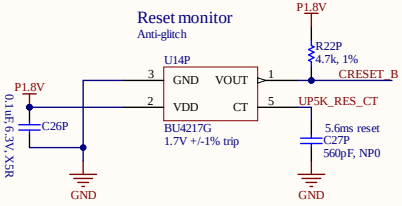


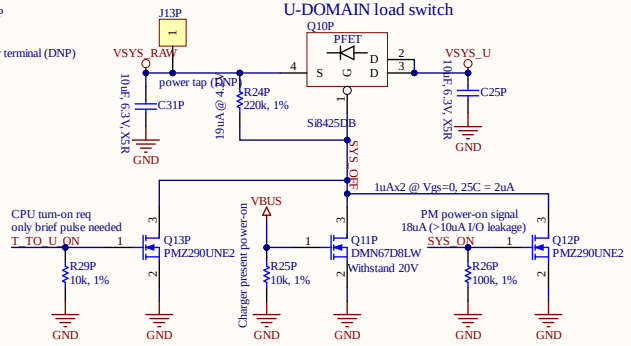










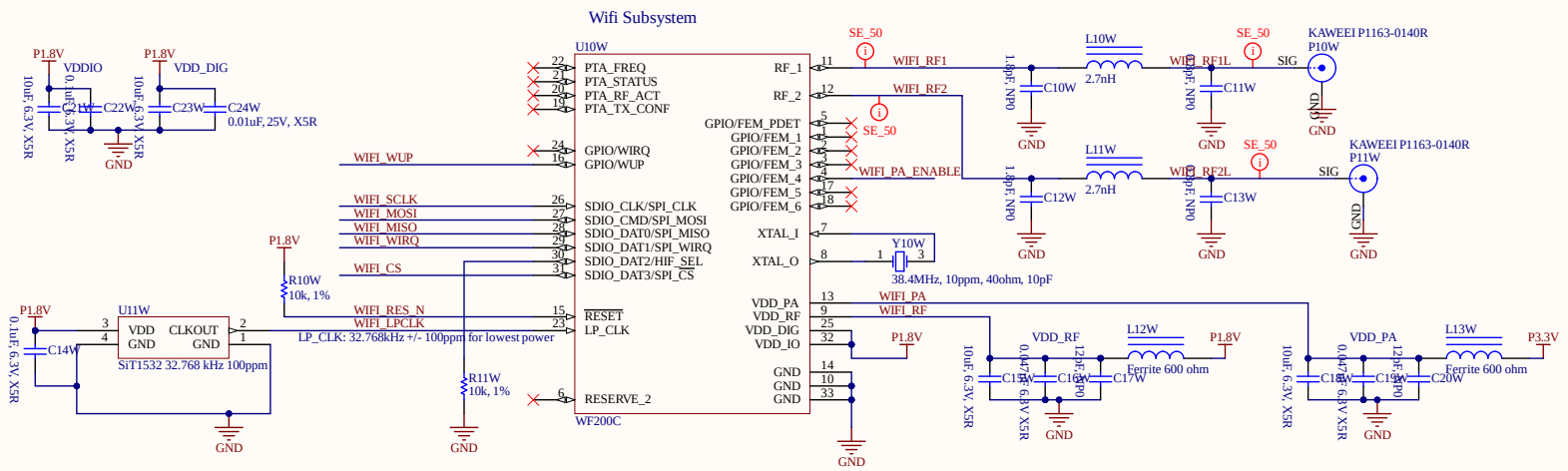


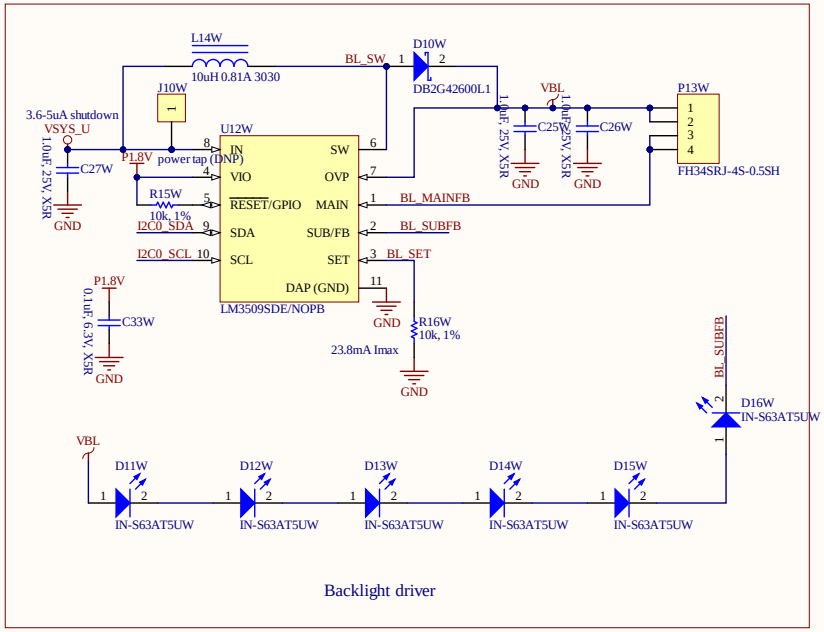
Behavior:

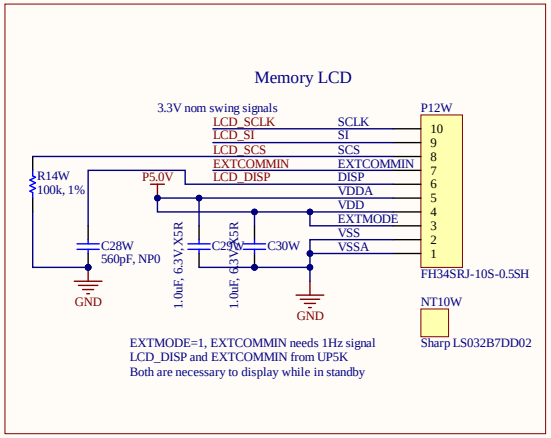
Charger present => always connect VBAT
(260ms to override auto-shutdown if battery is not present)
CPU => must drive system on transistor, or else power down by default

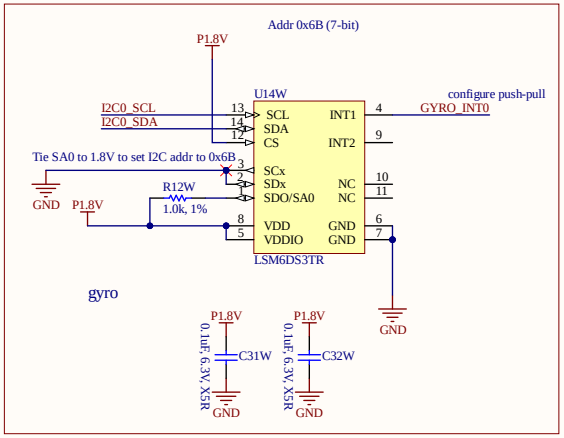
Title	Betrusted - Mainboard		
Size	Number		Revision
A3			
Date:	4/04/2020	Sheet of	
File:	F:\largework\..\03_power.SchDoc	Drawn By:	

U DOMAIN



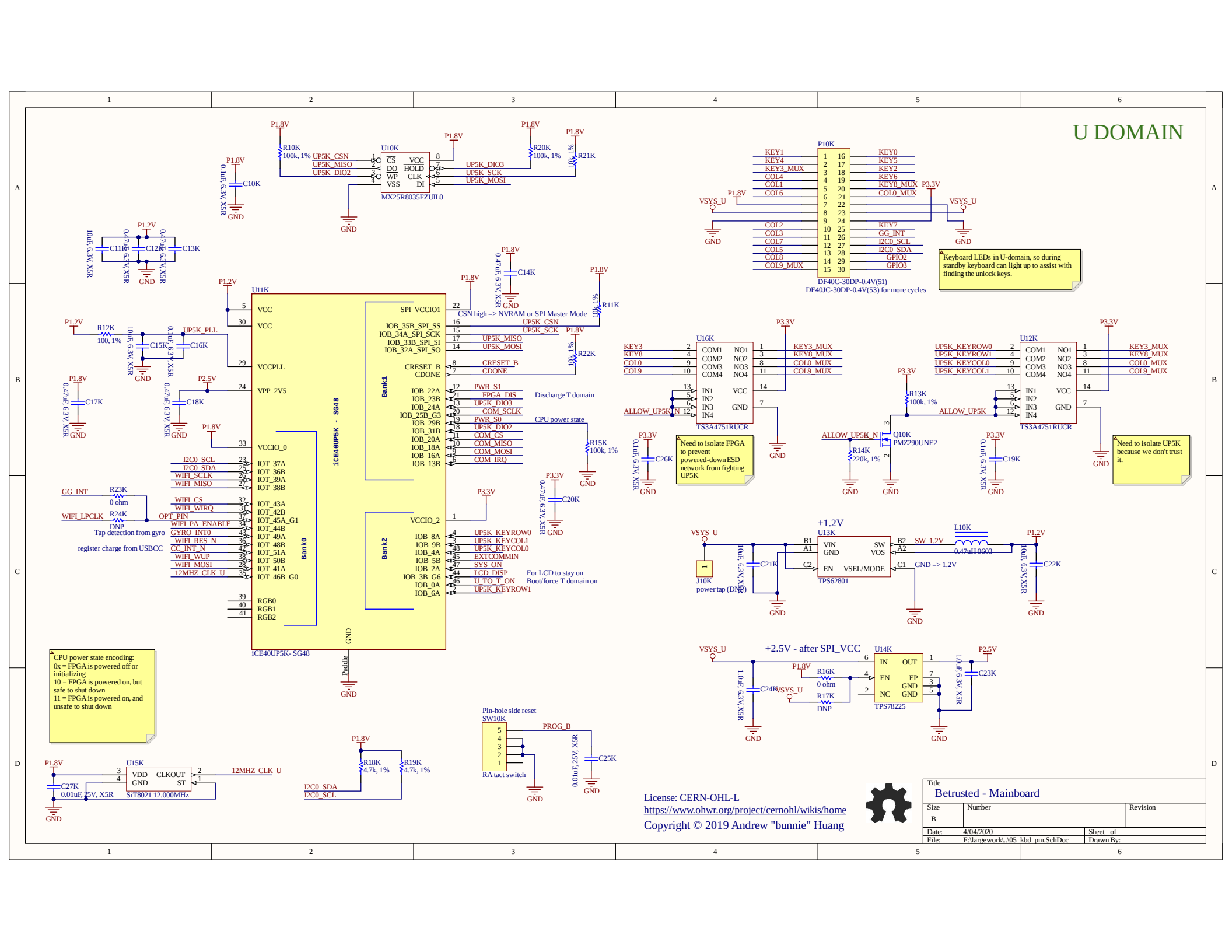




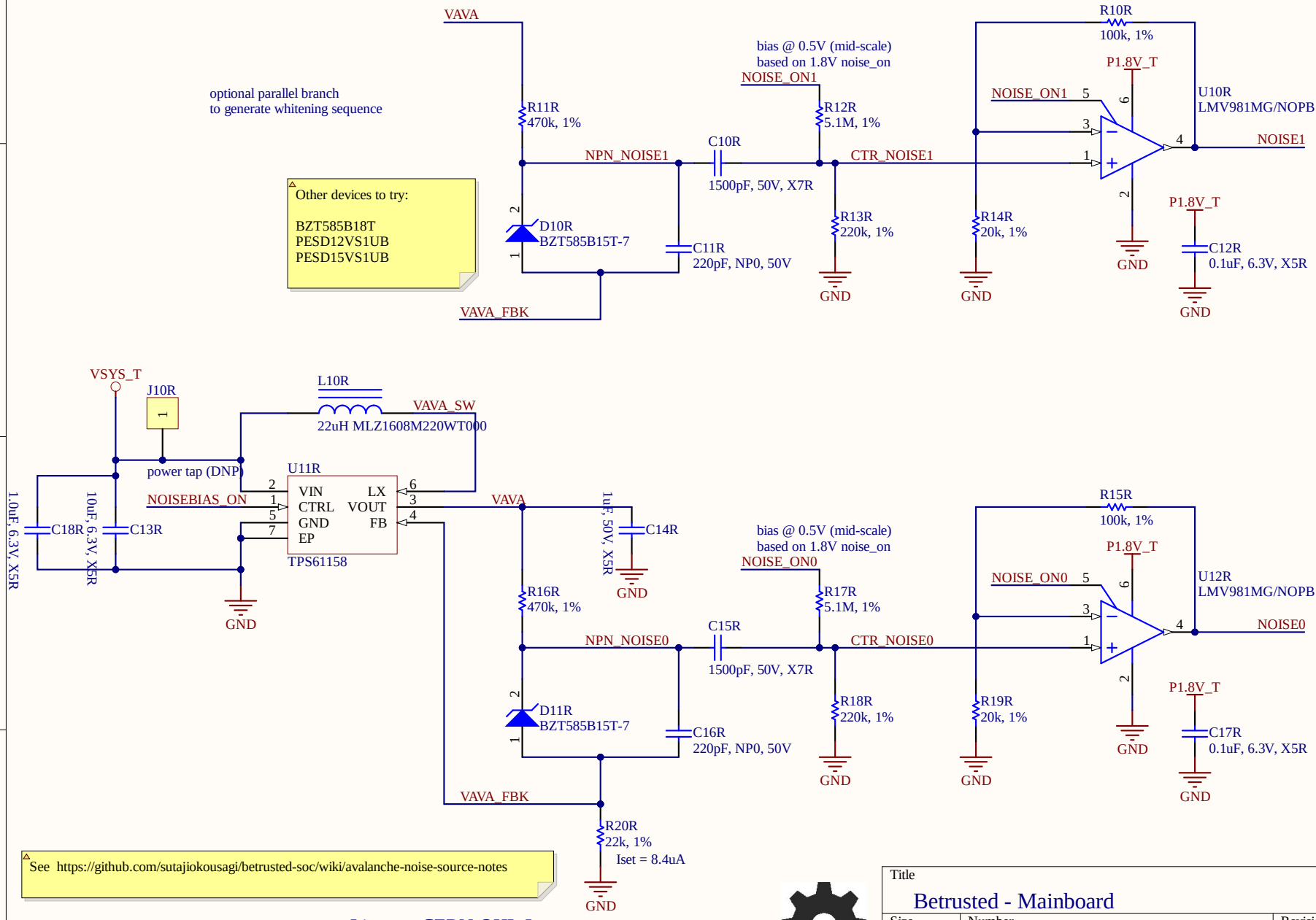


Title: Betrusted - Mainboard		
Size: B	Number:	Revision:
Date: 4/04/2020		Sheet of
File: F:\largework\..\04_io.SchDoc		Drawn By:

U DOMAIN

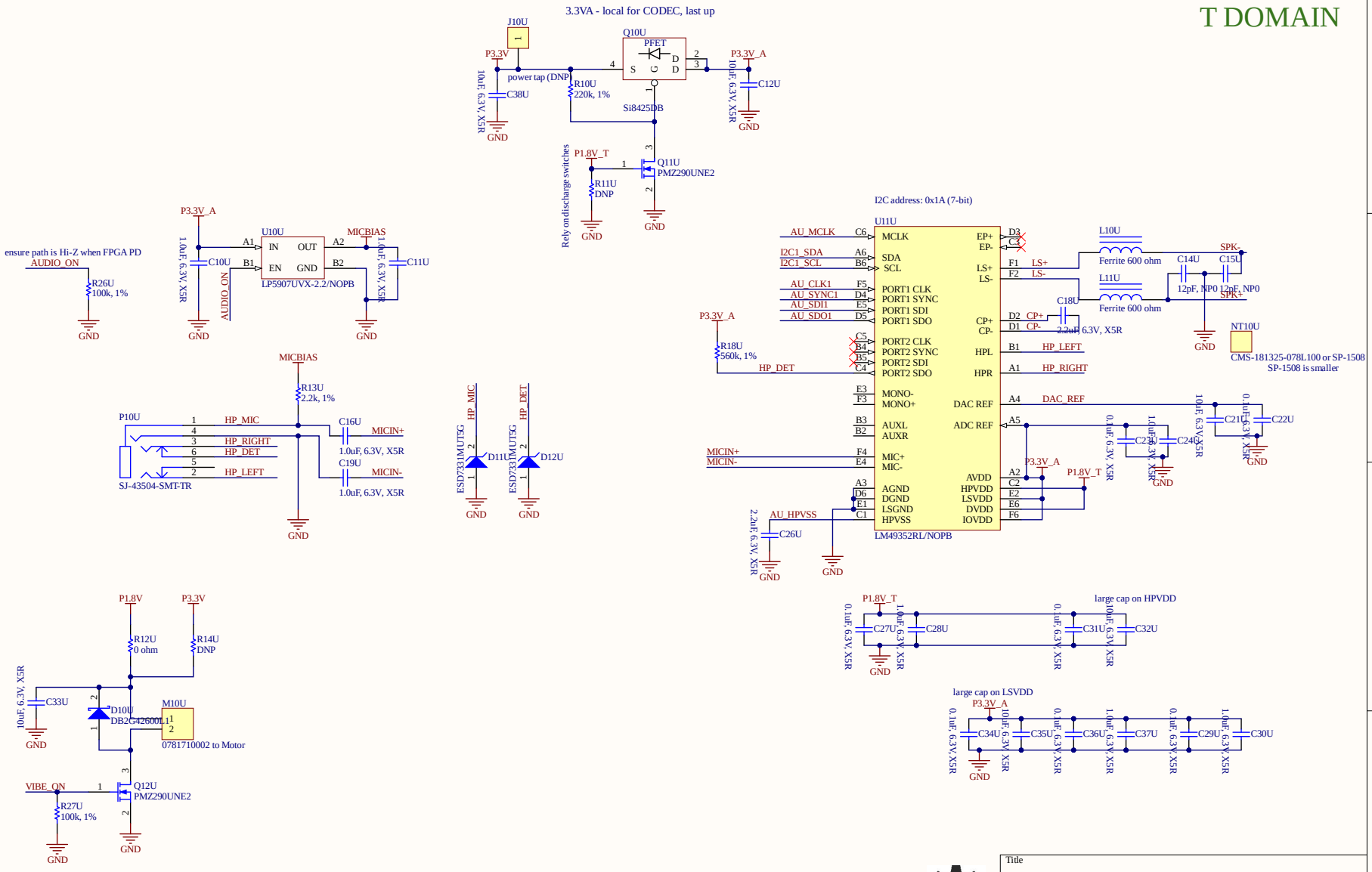

U10K
MX25R8035FZUIL0
U11K
iCE40UP5K - SG48
iCE40UP5K- SG48
P10K
DF40C-30DP-0.4V(51)
DF40JC-30DP-0.4V(53) for more cycles
Keyboard LEDs in U-domain, so during standby keyboard can light up to assist with finding the unlock keys.
U16K
TS3A4751RUCR
Need to isolate FPGA to prevent powered-down ESD network from fighting UP5K
U12K
TS3A4751RUCR
Need to isolate UP5K because we don't trust it.
Q10K
PMZ290UNE2
CSN high => NVRAM or SPI Master Mode
Discharge T domain
CPU power state
For LCD to stay on
Boot/force T domain on
Tap detection from gyro
register charge from USBCC
J10K
power tap (DNP)
U13K
TPS62801
+1.2V
L10K
0.47uH 0603
GND => 1.2V
U14K
TPS78225
+2.5V - after SPI_VCC
U15K
SiT8021 12.000MHz
SW10K
RA tact switch
Pin-hole side reset
CPU power state encoding:
0x = FPGA is powered off or initializing
10 = FPGA is powered on, but safe to shut down
11 = FPGA is powered on, and unsafe to shut down
License: CERN-OHL-L
https://www.ohwr.org/project/cernohl/wikis/home
Copyright © 2019 Andrew "bunnie" Huang
Title
Betrusted - Mainboard
Size
B
Number
Revision
Date: 4/04/2020
Sheet of
File: F:\largework\..\05_kbd_pm.SchDoc
Drawn By:

T DOMAIN



Title: Betrusted - Mainboard		
Size: A	Number:	Revision:
Date: 4/04/2020		Sheet of
File: F:\largework\..\06_rng.SchDoc		Drawn By:

T DOMAIN



Title: Betrusted - Mainboard		
Size: B	Number:	Revision:
Date: 4/04/2020	Sheet of	
File: F:\largework\..\07_ux.SchDoc	Drawn By:	