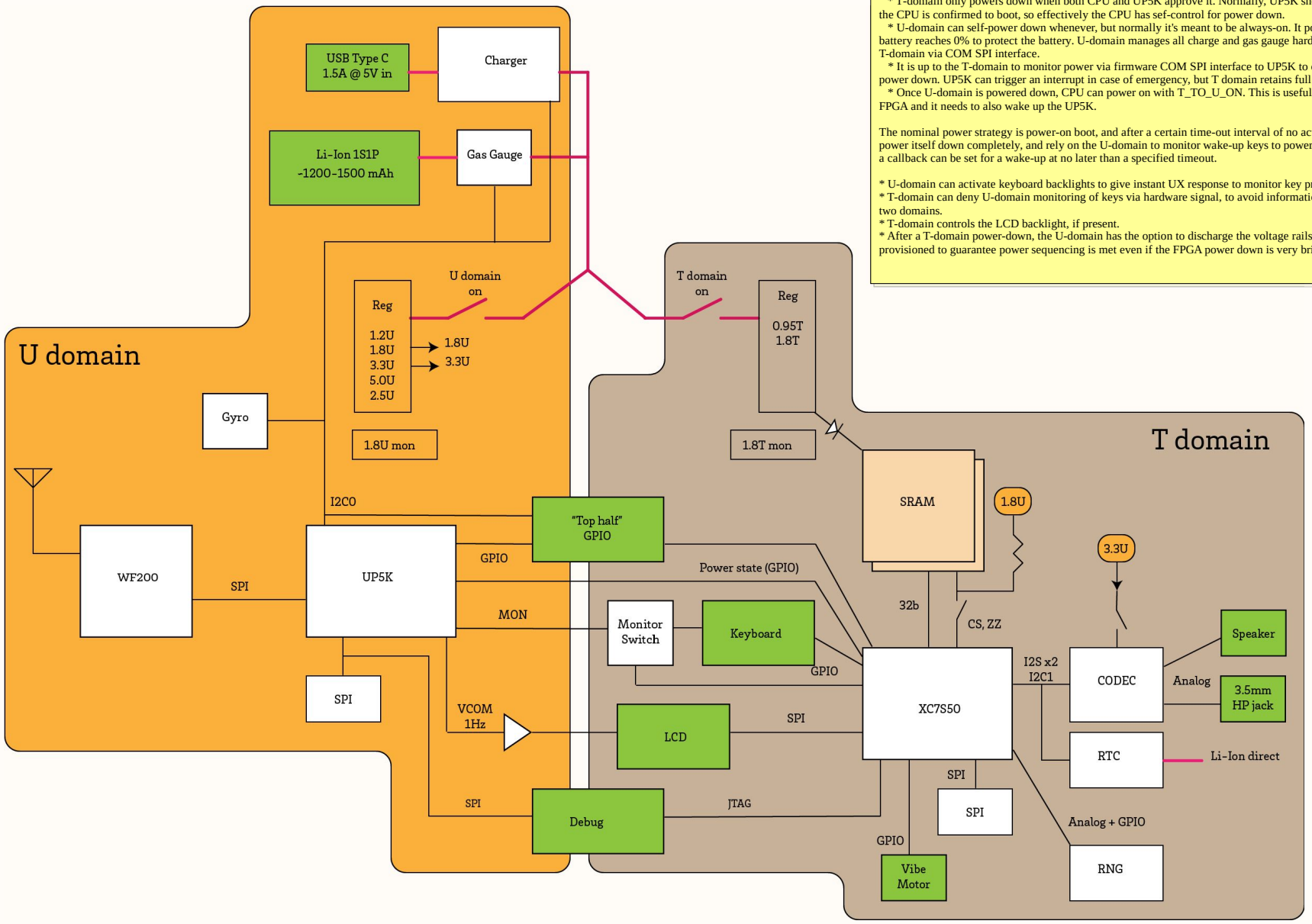
Power sequencing:

* START with all systems off.
* VBUS (external power) applied, both U and T domains power on, and cannot be powered off until VBUS is removed. However, devices can still go into a power-saving mode on their own.
* VBUS removed:
  * T-domain only powers down when both CPU and UP5K approve it. Normally, UP5K should cut its override once the CPU is confirmed to boot, so effectively the CPU has sef-control for power down.
  * U-domain can self-power down whenever, but normally it's meant to be always-on. It powers off only when the battery reaches 0% to protect the battery. U-domain manages all charge and gas gauge hardware, and reports status to T-domain via COM SPI interface.
  * It is up to the T-domain to monitor power via firmware COM SPI interface to UP5K to coordinate on the 0% power down. UP5K can trigger an interrupt in case of emergency, but T domain retains full authority to ignore it.
  * Once U-domain is powered down, CPU can power on with T_TO_U_ON. This is useful in case RTC wakes up FPGA and it needs to also wake up the UP5K.

The nominal power strategy is power-on boot, and after a certain time-out interval of no activity, the FPGA will power itself down completely, and rely on the U-domain to monitor wake-up keys to power the FPGA domain up, or a callback can be set for a wake-up at no later than a specified timeout.

* U-domain can activate keyboard backlights to give instant UX response to monitor key press.
* T-domain can deny U-domain monitoring of keys via hardware signal, to avoid information leakage between the two domains.
* T-domain controls the LCD backlight, if present.
* After a T-domain power-down, the U-domain has the option to discharge the voltage rails with FPGA_DIS. This is provisioned to guarantee power sequencing is met even if the FPGA power down is very brief.



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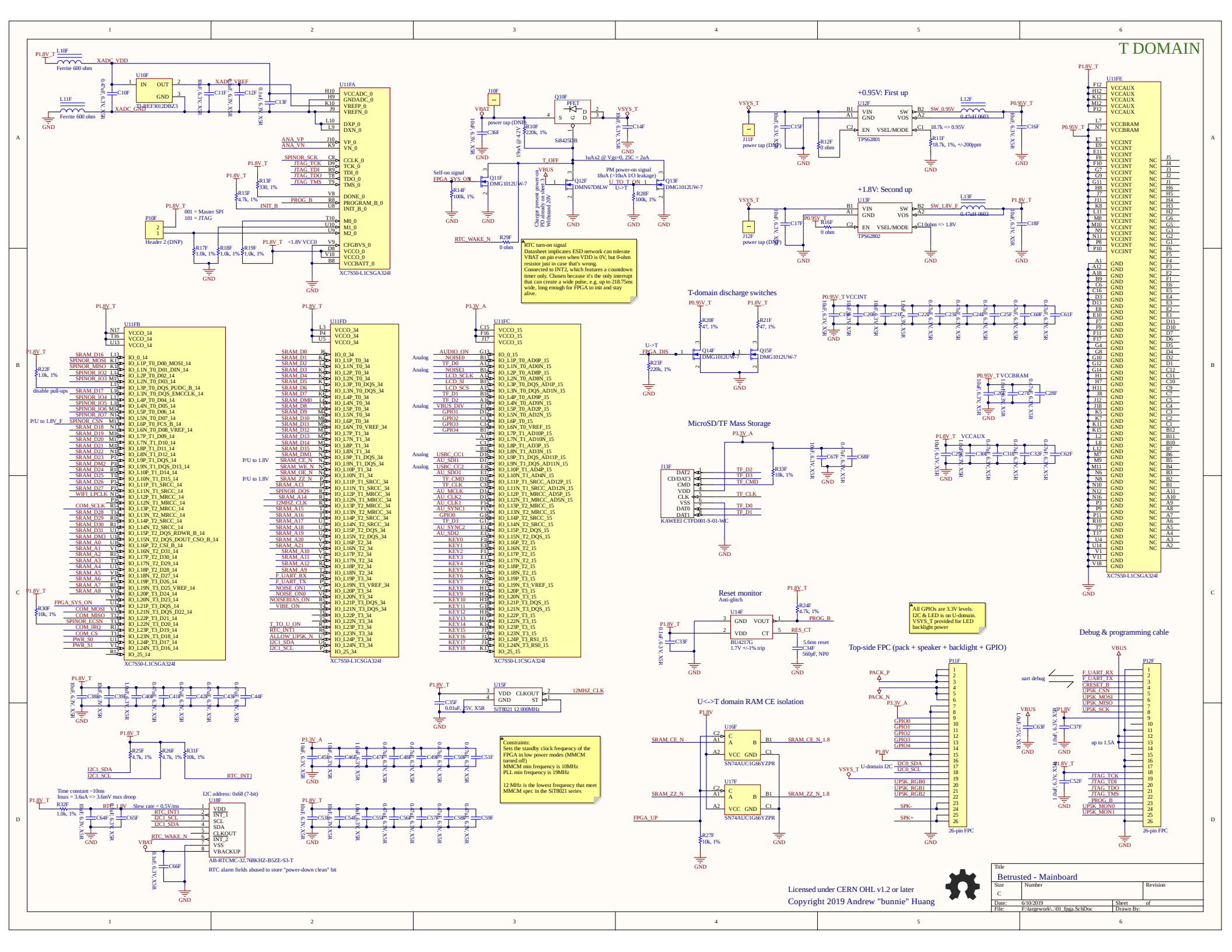
T DOMAIN


P1.8V_T
L10F
Ferrite 600 ohm
XADC_VDD
U10F
IN
OUT
GND
U-REF3012DBZ3
XADC_VREF
L11F
XADC_GND
C10F
C11F
C12F
C13F
U11FA
VCCADC_0
GNDADC_0
VREFP_0
VREFN_0
DXP_0
DXN_0
VP_0
VN_0
CCLK_0
TCK_0
TDI_0
TDO_0
TMS_0
DONE_0
PROGRAM_B_0
INIT_B_0
M0_0
M1_0
M2_0
CFGBVS_0
VCCO_0
VCCBATT_0
XC7S50-L1CSGA324I
ANA_VP
ANA_VN
SPINOR_SCK
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
R13F
330, 1%
R15F
4.7k, 1%
PROG_B
INIT_B
P10F
001 = Master SPI
101 = JTAG
Header 2 (DNP)
R17F
1.0k, 1%
R18F
1.0k, 1%
R19F
1.0k, 1%
<1.8V VCCO
R29F
0 ohm
RTC_WAKE_N
J10F
VBAT
power tap (DNP)
Q10F
PFET
Si8425DB
R10F
220k, 1%
C36F
C14F
VSYS_T
T_OFF
1uAx2 @ Vgs=0, 25C = 2uA
Self-on signal
FPGA_SYS_ON
Q11F
DMG1012UW-7
R14F
100k, 1%
Q12F
DMN67D8LW
Q13F
DMG1012UW-7
R28F
100k, 1%
VBUS
Charger present power-on
PD already on sheet
Withstand 20V
PM power-on signal
18uA (>10uA I/O leakage)
U->T
RTC turn-on signal
Datasheet implicates ESD network can tolerate VBAT on pin even when VDD is 0V, but 0-ohm resistor just in case that's wrong.
Connected to INT2, which features a countdown timer only. Chosen because it's the only interrupt that can create a wide pulse, e.g. up to 218.75ms wide, long enough for FPGA to init and stay alive.
+0.95V: First up
J11F
power tap (DNP)
U12F
TPS62801
L12F
0.47uH 0603
SW_0.95V
R12F
0 ohm
R11F
18.7k, 1%, +/-200ppm
18.7k => 0.95V
P0.95V_T
C15F
C16F
+1.8V: Second up
J12F
power tap (DNP)
U13F
TPS62802
L13F
0.47uH 0603
SW_1.8V_F
R16F
0 ohm
C10ohm => 1.8V
C17F
C18F
U11FE
VCCAUX
VCCBRAM
VCCINT
NC
GND
XC7S50-L1CSGA324I
T-domain discharge switches
U->T
FPGA_DIS
R20F
47, 1%
R21F
47, 1%
Q14F
DMG1012UW-7
Q15F
DMG1012UW-7
R23F
220k, 1%
VCCINT
C19F
C20F
C21F
C22F
C23F
C24F
C25F
C60F
C61F
VCCBRAM
C26F
C27F
C28F
MicroSD/TF Mass Storage
J13F
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
KAWEEI CTFD001-S-01-WC
TF_D2
TF_D3
TF_CMD
TF_CLK
TF_D0
TF_D1
R33F
10k, 1%
C67F
C68F
VCCAUX
C29F
C30F
C31F
C32F
C62F
U11FB
U11FC
U11FD
VCCO_14
VCCO_15
VCCO_34
IO_0_14
IO_0_15
IO_0_34
SRAM_D16
SPINOR_MOSI
SPINOR_MISO
SPINOR_IO2
SPINOR_IO3
SPINOR_IO4
SPINOR_IO5
SPINOR_IO6
SPINOR_IO7
SPINOR_CSN
SRAM_D17
SRAM_D18
SRAM_D19
SRAM_D20
SRAM_D21
SRAM_D22
SRAM_D23
SRAM_D24
SRAM_D25
SRAM_D26
SRAM_D27
WIFI_LPCLK_N
COM_SCLK
SRAM_D28
SRAM_D29
SRAM_D30
SRAM_D31
SRAM_DM3
SRAM_A0
SRAM_A1
SRAM_A2
SRAM_A3
SRAM_A4
SRAM_A5
SRAM_A6
SRAM_A7
SRAM_A8
FPGA_SYS_ON
COM_MOSI
COM_MISO
SPINOR_ECSN
COM_IRQ
COM_CS
PWR_S0
PWR_S1
R22F
1.0k, 1%
disable pull-ups
P/U to 1.8V_F
R30F
10k, 1%
SRAM_D0
SRAM_D1
SRAM_D2
SRAM_D3
SRAM_D4
SRAM_D5
SRAM_D6
SRAM_D7
SRAM_DM0
SRAM_D8
SRAM_D9
SRAM_D10
SRAM_D11
SRAM_D12
SRAM_D13
SRAM_D14
SRAM_D15
SRAM_DM1
SRAM_CE_N
SRAM_WE_N
SRAM_OE_N
SRAM_ZZ_N
SRAM_A13
SPINOR_DQS
SRAM_A14
12MHZ_CLK
SRAM_A15
SRAM_A16
SRAM_A17
SRAM_A18
SRAM_A19
SRAM_A20
SRAM_A21
SRAM_A10
SRAM_A11
SRAM_A12
SRAM_A9
F_UART_RX
F_UART_TX
NOISE_ON1
NOISE_ON0
NOISEBIAS_ON
VIBE_ON
T_TO_U_ON
RTC_INT1
ALLOW_UP5K_N
I2C1_SDA
I2C1_SCL
P/U to 1.8V
AUDIO_ON
NOISE0
TF_D0
NOISE1
LCD_SCLK
LCD_SI
LCD_SCS
TF_D1
TF_D2
VBUS_DIV
GPIO1
GPIO2
GPIO3
GPIO4
USBC_CC1
AU_SDI1
USBC_CC2
AU_SDO1
TF_CMD
TF_CLK
AU_MCLK
AU_CLK2
AU_CLK1
AU_SYNC1
GPIO0
TF_D3
AU_SYNC2
AU_SDI2
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
KEY7
KEY8
KEY9
KEY10
KEY11
KEY12
KEY13
KEY14
KEY15
KEY16
KEY17
KEY18
Analog
XC7S50-L1CSGA324I
Reset monitor
Anti-glitch
U14F
BU4217G
1.7V +/-1% trip
R24F
4.7k, 1%
PROG_B
RES_CT
5.6ms reset
C34F
560pF, NP0
C33F
All GPIOs are 3.3V levels.
I2C & LED is on U-domain.
VSYS_T provided for LED backlight power
Top-side FPC (pack + speaker + backlight + GPIO)
P11F
PACK_P
PACK_N
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
I2C0_SDA
I2C0_SCL
U5K_RGB0
U5K_RGB1
U5K_RGB2
SPK-
SPK+
26-pin FPC
Debug & programming cable
P12F
uart debug
F_UART_RX
F_UART_TX
CRESET_B
U5K_CSN
U5K_MOSI
U5K_MISO
U5K_SCK
up to 1.5A
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
PROG_B
U5K_MON0
U5K_MON1
26-pin FPC
U15F
SiT8021 12.000MHz
12MHZ_CLK
C35F
0.01uF, 25V, X5R
Constraints:
Sets the standby clock frequency of the FPGA in low power modes (MMCM turned off)
MMCM min frequency is 10MHz
PLL min frequency is 19MHz
12 MHz is the lowest frequency that meet MMCM spec in the SIT8021 series
U<->T domain RAM CE isolation
U16F
SN74AUC1G66YZPR
SRAM_CE_N
SRAM_CE_N_1.8
U17F
SRAM_ZZ_N
SRAM_ZZ_N_1.8
FPGA_UP
R27F
10k, 1%
U-domain I2C
R25F
4.7k, 1%
R26F
4.7k, 1%
R31F
10k, 1%
I2C1_SDA
I2C1_SCL
RTC_INT1
Time constant ~10ms
Imax = 3.6uA => 3.6mV max droop
RTC 1.8V
Slew rate < 0.5V/ms
R32F
1.0k, 1%
C64F
C65F
I2C address: 0x68 (7-bit)
U18F
VDD
INT_1
SCL
SDA
CLKOUT
INT_2
VSS
VBACKUP
AB-RTCMC-32.768KHZ-B5ZE-S3-T
C66F
RTC alarm fields abused to store "power-down clean" bit
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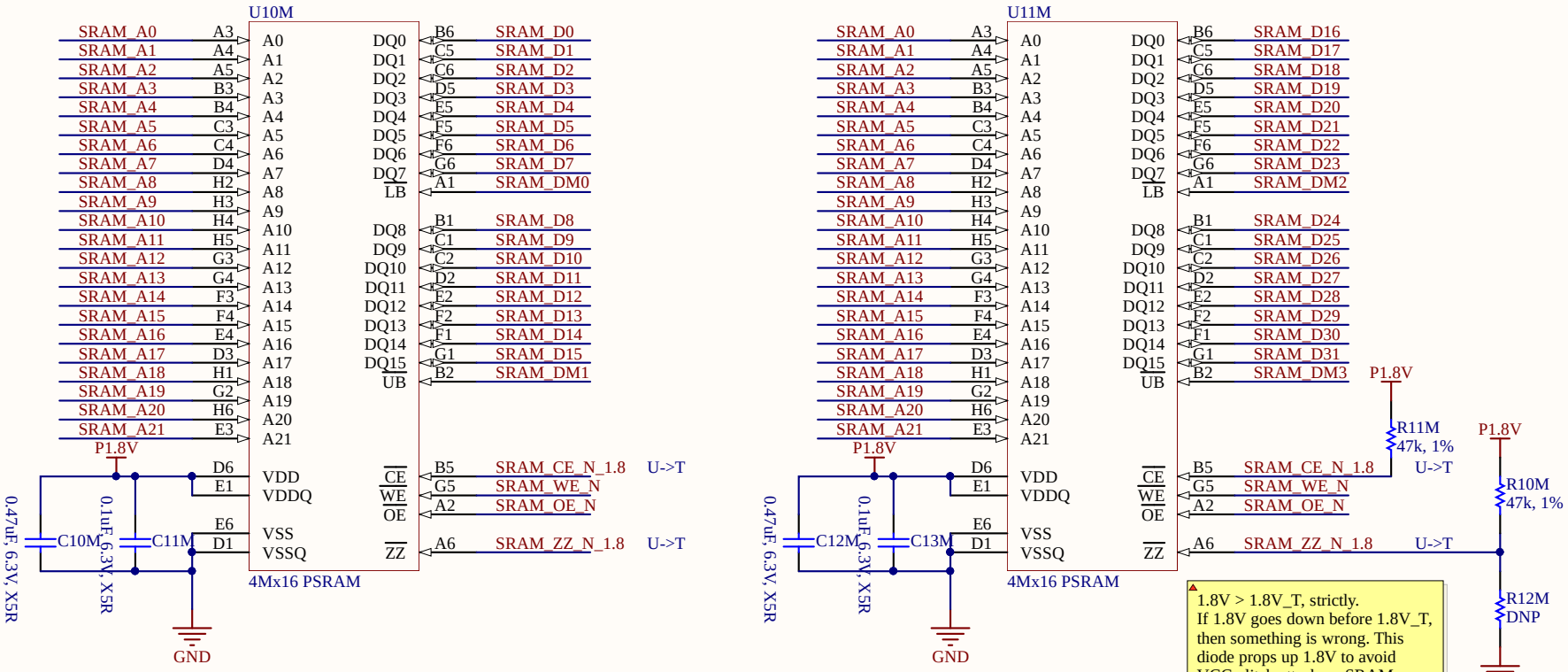
U DOMAIN



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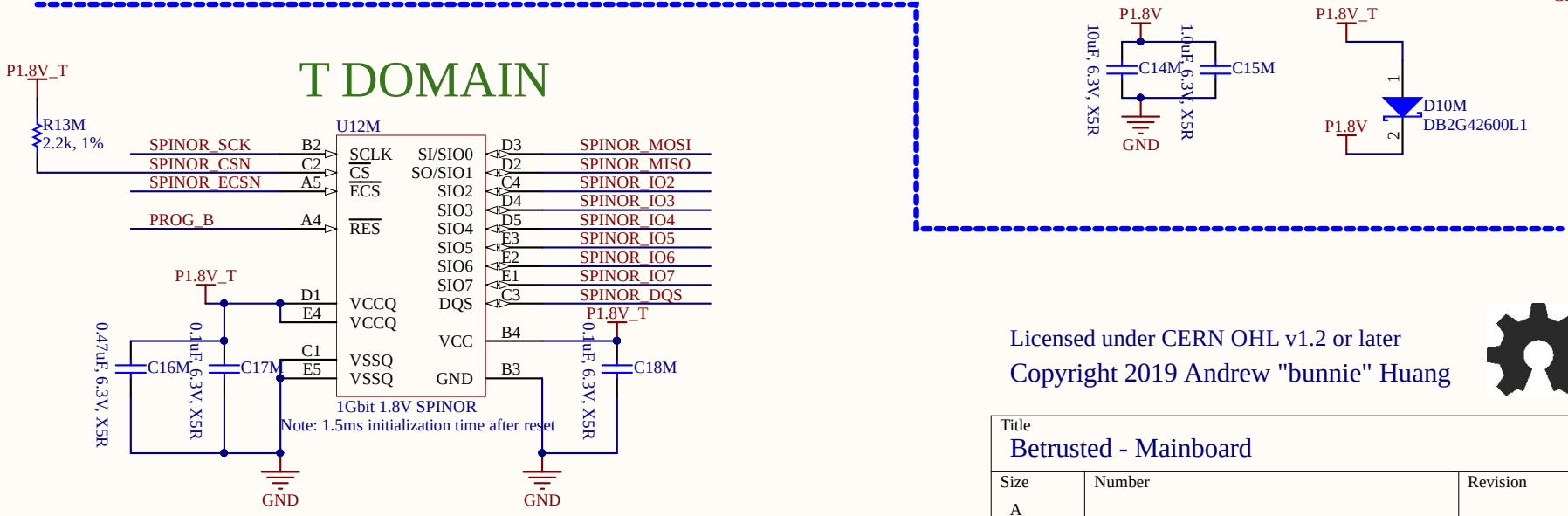

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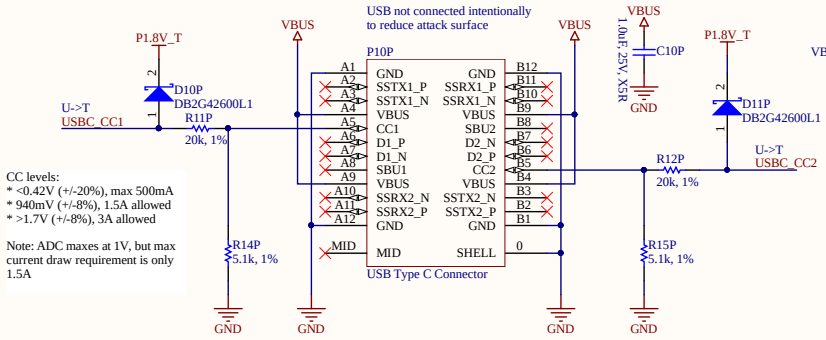
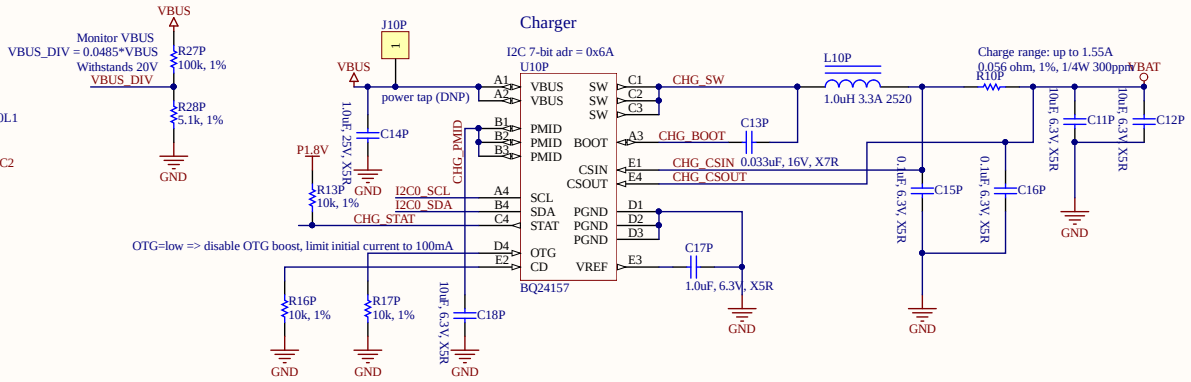
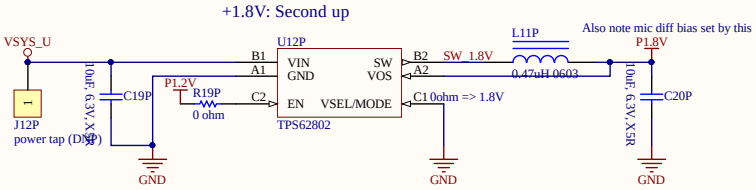
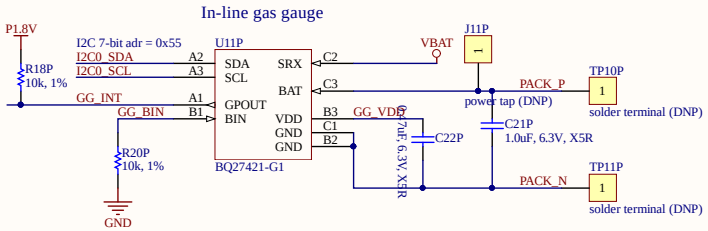
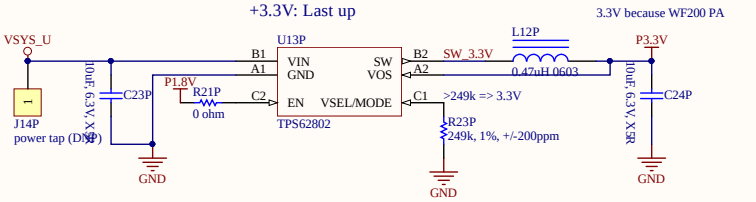
U DOMAIN

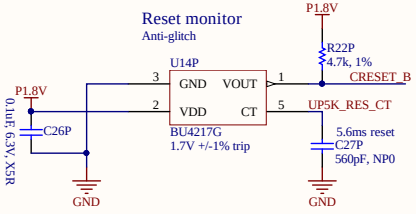


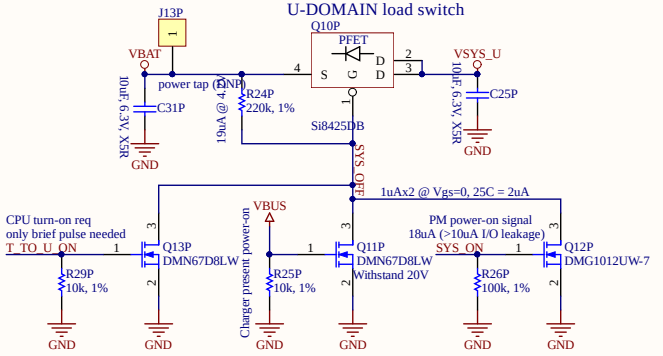


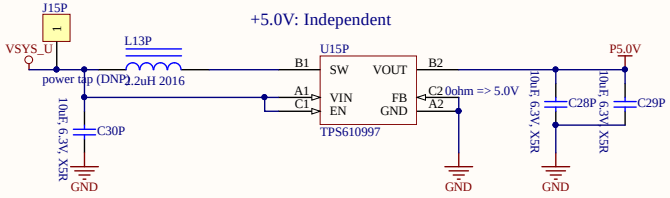


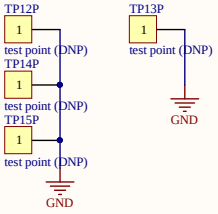












Behavior:

Charger present => always connect VBAT
(260ms to override auto-shutdown if battery is not present)
CPU => must drive system on transistor, or else power down by default

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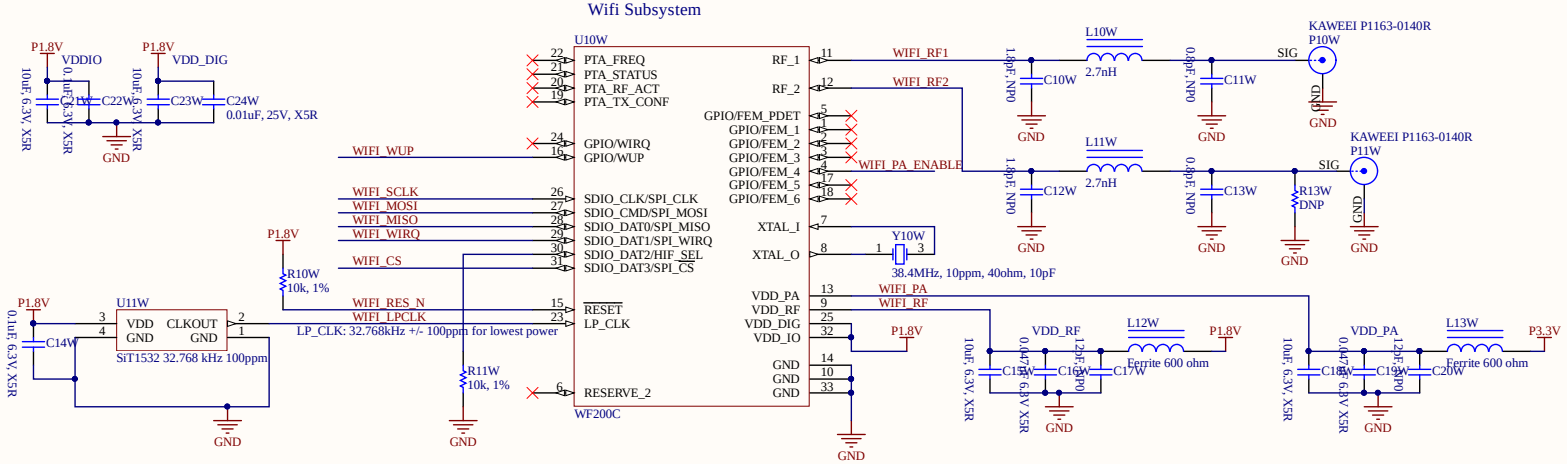
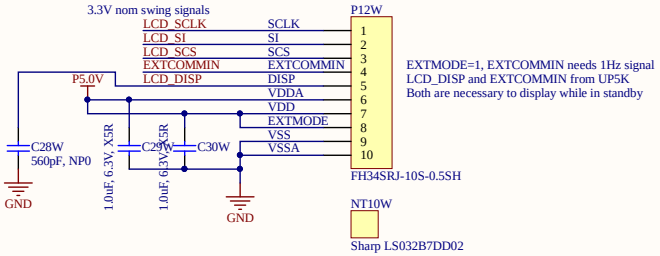
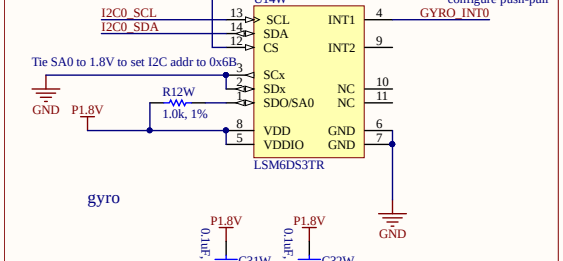
U DOMAIN

Wifi Subsystem



Memory LCD





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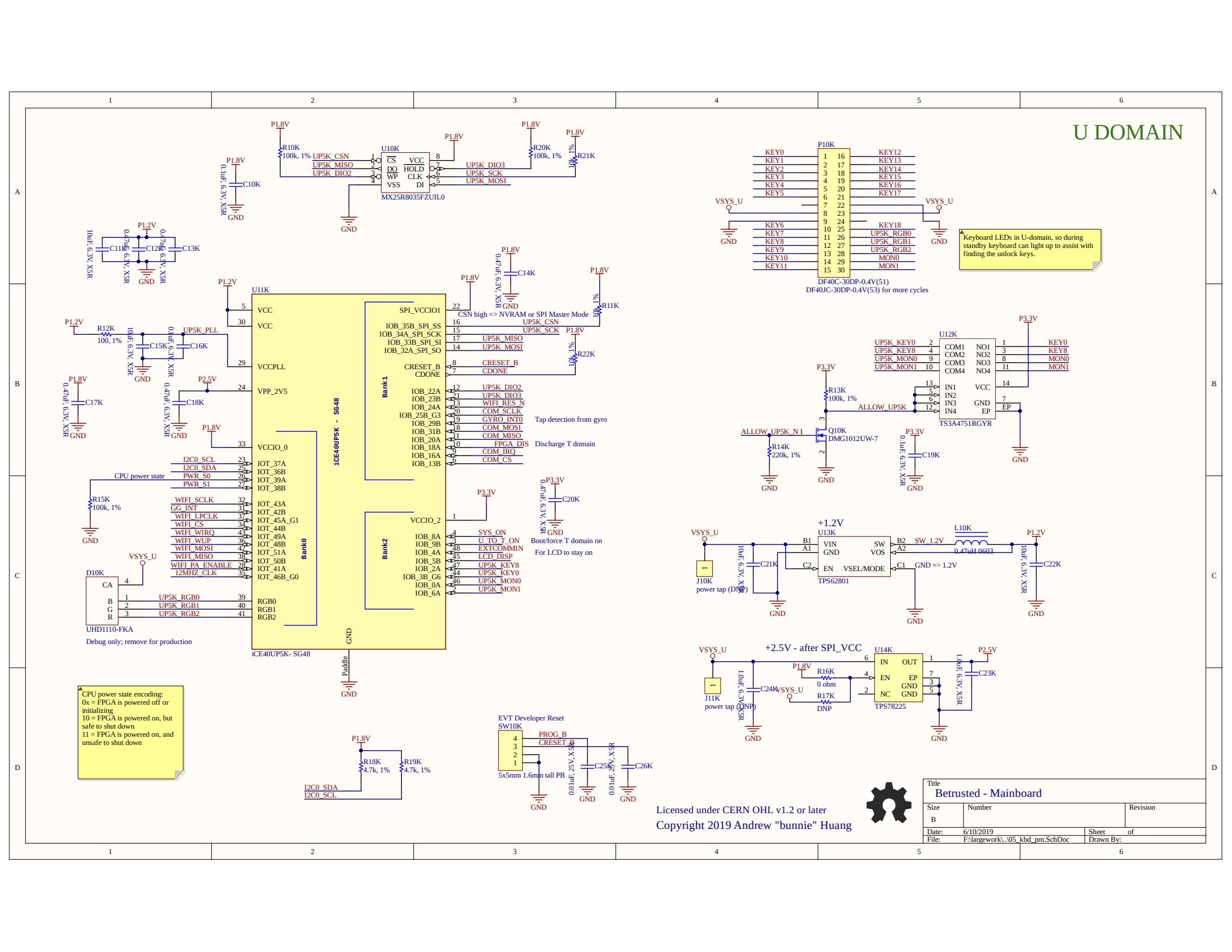
U DOMAIN
U10K
MX25R8035FZUIL0
U11K
iCE40UP5K - SG48
iCE40UP5K- SG48
Bank0
Bank1
Bank2
P10K
DF40C-30DP-0.4V(51)
DF40JC-30DP-0.4V(53) for more cycles
Keyboard LEDs in U-domain, so during standby keyboard can light up to assist with finding the unlock keys.
U12K
TS3A4751RGYR
Q10K
DMG1012UW-7
+1.2V
U13K
TPS62801
L10K
0.47uH 0603
J10K
power tap (DNP)
+2.5V - after SPI_VCC
U14K
TPS78225
J11K
power tap (DNP)
CSN high => NVRAM or SPI Master Mode
Tap detection from gyro
Discharge T domain
Boot/force T domain on
For LCD to stay on
CPU power state
CPU power state encoding:
0x = FPGA is powered off or initializing
10 = FPGA is powered on, but safe to shut down
11 = FPGA is powered on, and unsafe to shut down
D10K
UHD1110-FKA
Debug only; remove for production
EVT Developer Reset
SW10K
5x5mm 1.6mm tall PB
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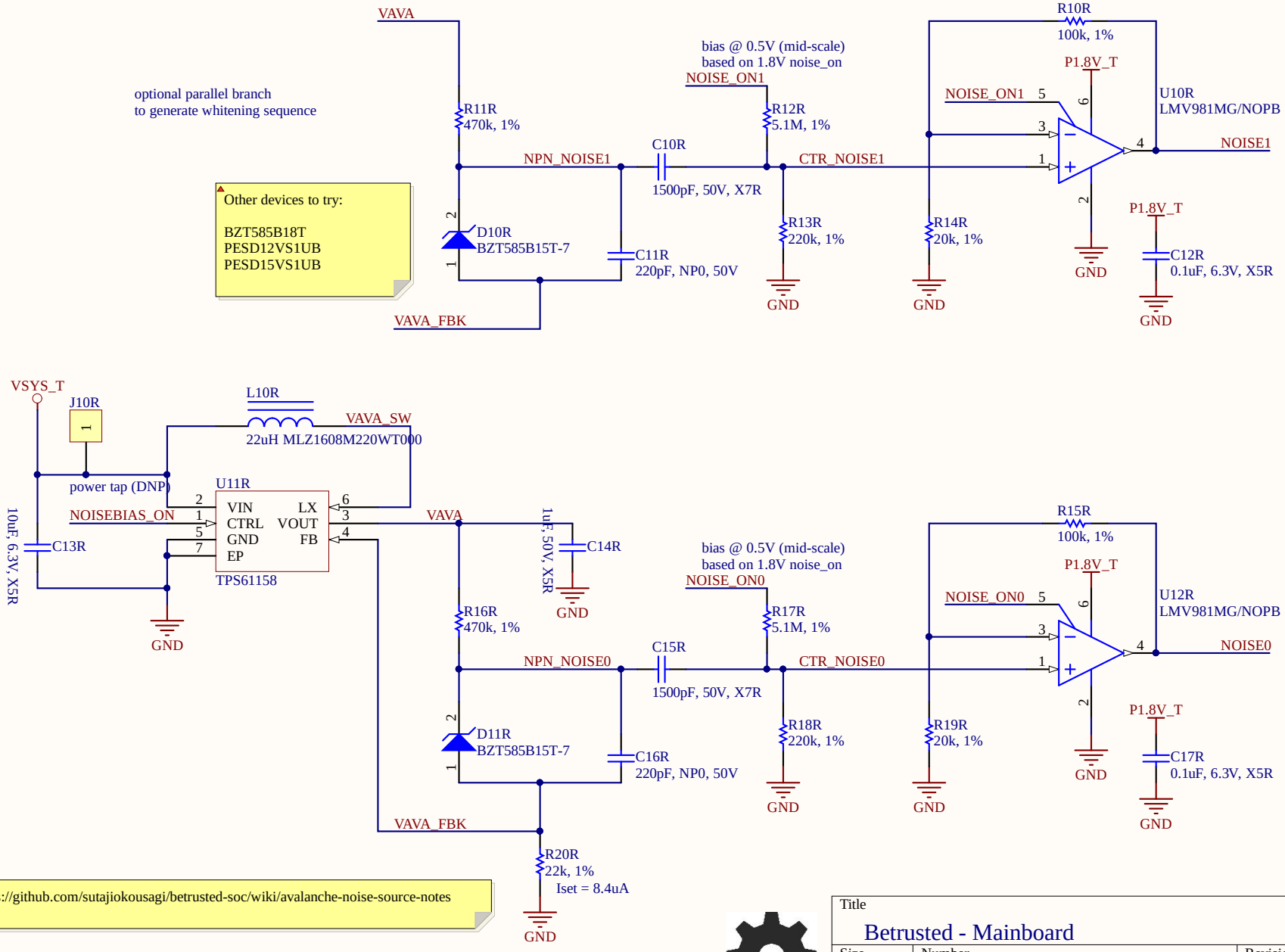
T DOMAIN



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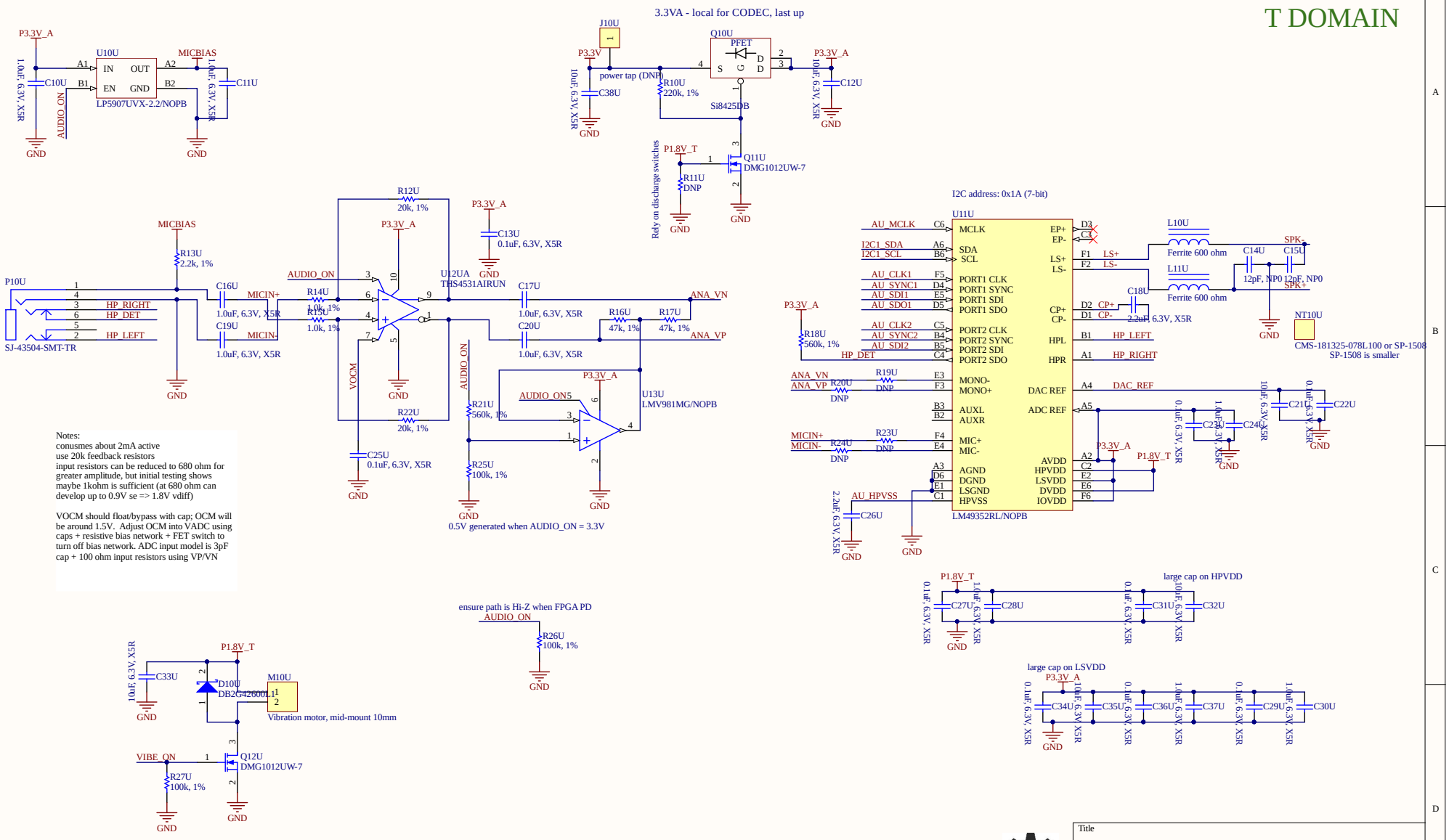
T DOMAIN



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