Design of Digital Circuits: Lab Report		
Lab 1: Drawing Basic Circuits		
Date	08.03.2019	Grade
Names	David Zollikofer	
	Sven Pfiffner	Lab session / lab room
		Fri. 10:00 | E 26.1

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and other required material. Only one of the members of each group should submit. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

Exercise 1

(a) Assume that we were only using 2-input AND gates and 2-input XNOR gates to create our comparator in Part 1 in this week's lab manual. How many of each gate would you use for a comparator of width 8, 16, 32 and 64 bits? What is the logic depth in each case?

Note: the logic depth of a combinational circuit is defined as the number of logic gates in the longest signal path (path from input to output).

Comparator Width	2-input XNOR gates	2-input AND gates	Logic depth
8 bits	8	15	4
16 bits	16	31	5
32 bits	32	63	6
64 bits	64	127	7

Original circuit:

The circuit has to compare each digit of the two inputs. So we definitely need n - XNOR gates for a comparator of width n.

(b) Given the comparator width is N, derive general expressions for calculating the following:

(i) The number of 2-input XNOR gates

N	We compare each of the N digits with a distinct 2-input-XNOR-gate

(ii) The number of 2-input AND gates

$\sum_{k=0}^{\log_2(N)} 2^k$	After we have halfed the outputs with the XNOR's, each remaining logical layer contains half as many AND's as outputs.

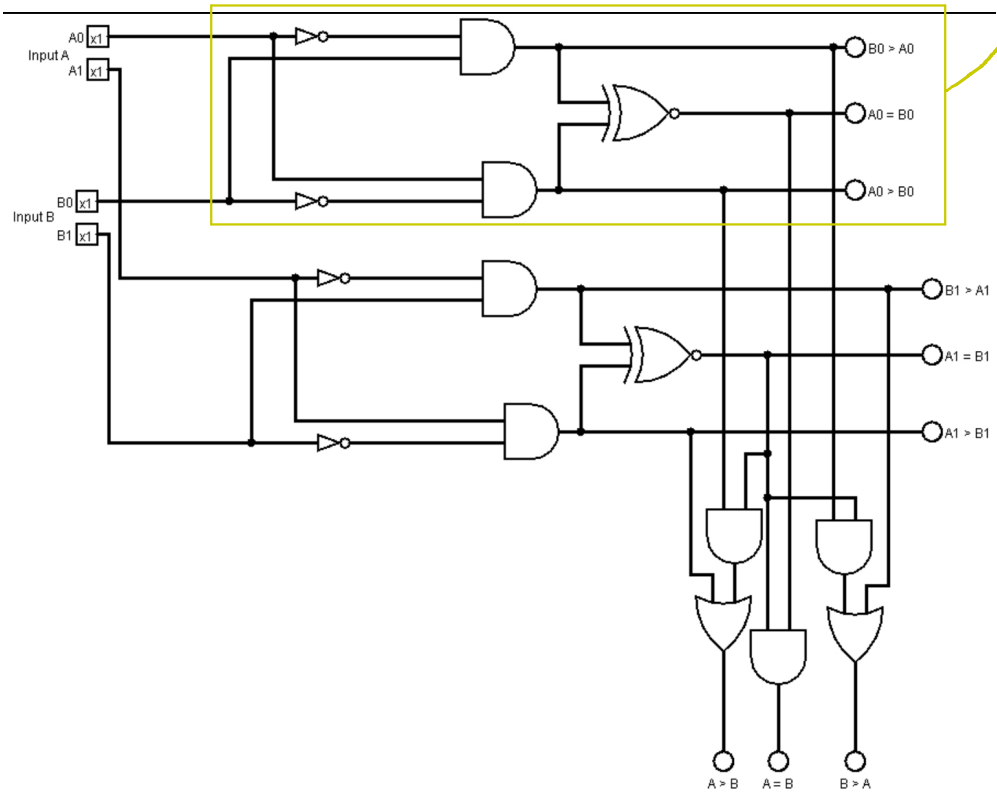
(iii) The logic depth

$1 + \log_2(N)$	Because we have a total of 2N inputs and would like to have 1 output, and because we can half the number of outputs in each layer, we end up with $1 + \log_2(N) = \log_2(2N)$ layers.

Remember: $A < B : O_3$, $A = B : O_2$, $A > B : O_1$

Exercise 2

Use two instances of the 1-bit comparator we designed in Part 2 in this week's lab to implement a 2-bit comparator. Draw the schematic of your design.



Exercise 3

What is the logic depth of each of the output ports in the circuit of Exercise 2?

O_1 : Depth 5

O_2 : Depth 4

O_3 : Depth 5