Design of Digital Circuits: Lab Report		
Lab 2: Mapping Your Circuit to FPGA		
Date	15.03.2019	Grade
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		Fri:10-12 | E 26.3

You have to submit this report via Moodle.

Use a zip file or tarball that contains the report and any other required material. Only one member from each group should submit the report. All members of the group will get the same grade.

The name of the submitted file should be *Lab1_LastName1_LastName2.zip* (or *.tar*), where *LastName1* and *LastName2* are the last names of the members of the group.

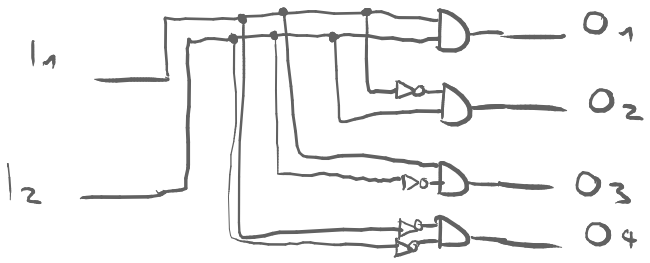
Exercise 1. Decoder

In this part, you will design a Decoder module and implement it using built-in logic gates (e.g., AND, OR, NOT, ...) in Verilog. Here is the description of a 2-input Decoder:

- 2 inputs and 4 outputs
- Exactly one of the outputs is 1 and all others are 0
- The one output that is logically 1 is the output corresponding to the input pattern that the logic circuit is supposed to detect

Map the inputs to two switches on the board, and map outputs to 4 LEDs on the board. Map your design to the FPGA and check the correctness of your design. Include your Verilog codes files and the constraint file in your report submission.

Notes : Use gate level logic to implement this circuit



Exercise 2. Multiplexer

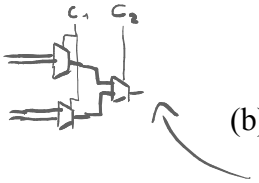
(a) Design a multiplexer with these features:

- Selects one of the *2* inputs to connect it to the output
- Needs a 1-bit control input

We call this multiplexer a 2:1 MUX

Notes: This should easily be accomplishable if working with behaviour level design.

⇒ Ternary operation if (c) then out[1] else out[2] } output = c? out[1] : out[2]



(b) Use several instances of your 2:1 MUX to design a 4:1 MUX. Map your design to your FPGA board, with input and output ports of your choice, and check the functionality of your circuit.

Include your Verilog files and constraint file in your submission.

Feedback

If you have any comments about the exercise please add them here: mistakes in the text, difficulty level of the exercise, or anything that will help us improve it for the next time.

We encountered an error where vivado could not find the constraints file. After some research we figured out that one has to check "set as target constraints file" on the desired .xdc. However, this was not mentioned in the excercise.