Lab Report 6

Testing the FSM from Lab 4

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In order to make the simulation a bit more interesting and have it complete withing seconds rather than hours on our computer we have changed the code for our clock divider from:

```verilog
module clk_div(input clock, input reset, output clock_en);
    reg [24:0] clk_count;
    always @ (posedge clock)
        begin
            if(reset)
                clk_count <= 0;
            else
                clk_count <= clk_count+1;
        end
        assign clock_en = &clk_count;
endmodule
```

to

```verilog
module clk_div(input clock, input reset, output clock_en);
    reg [4:0] clk_count;
    always @ (posedge clock)
        begin
            if(reset)
                clk_count <= 0;
            else
                clk_count <= clk_count+1;
        end
        assign clock_en = &clk_count;
endmodule
```

This allows us to make the simulation go faster and actually see what is going on in the simulation window with our own eyes. However we would like to point out that this does not change the outcome of the simulation in any significant way (except for the time it takes to transition from state to state).

We have taken the testbench code from lab 6 but we have heavily adapted it. One one hand, this report does not require that we automatically check the state transitions with testvectors, but instead want's us to focus on the

Results:

When we run the testbench we get the following output: (a copy of the output that is not annotated can also be found in this folder):

First we issue the reset. This doesn't really have any visible effects on the output, but resets the FSM.

We the press the left button for a nanosecond. This doesn't cause the FSM to immediately enter the sequence to the left. Instead, internally the FSM's nextState will be set to the first state to the left and only after the slow clock has a rising edge the left sequence starts (this explains the gap between the moment when left is pressed and the sequence starts).

After the left sequence has finished we wait a bit and do the same to the right.
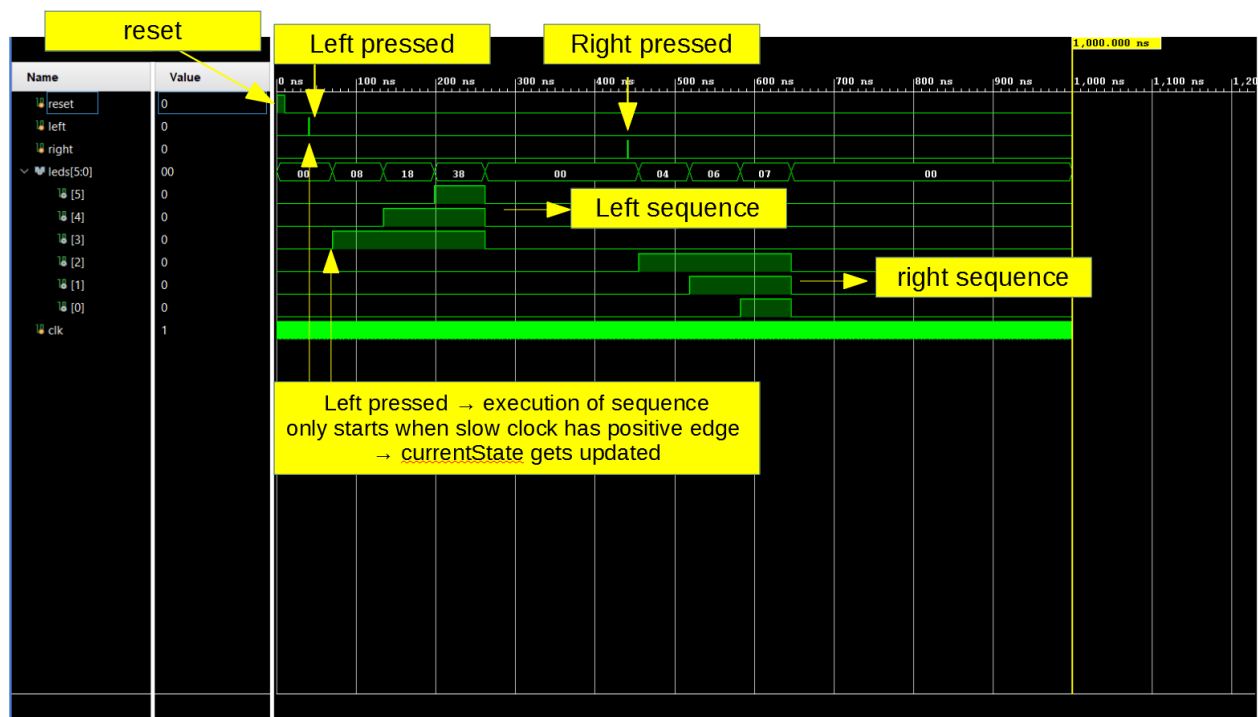
For completeness sake we have also added a picture showing only the right sequence (since this is what you are asking for in the report.)

If you have any questions feel free to send us a quick email.