Experiment #2 - Clock Adjusting and Monitoring

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I. Clock Adjusting Unit

A. Look at tables and figs 1 and 2

TABLE1. SCENARIO1 WITH FIXED SETPERIOD VALUE

Ring Oscillator Frequency	Desired Frequency	Final Parallel Loads	Initial Parallel Loads	Setperiod
20 MHz	400KHz	205	1	125

TABLE2. SCENARIO2 WITH FIXED SETPERIOD VALUE

Ring Oscillator Frequency	Desired Frequency	Final Parallel Loads	Initial Parallel Loads	Setperiod
18 MHz	400KHz	214	205	125

II. Clock Monitoring Unit

A. Look at tables and figs 3, 4 and 5

TABLE3. SCENARIO1 WITH DIFFERENT PSISET VALUES

Internal FRO	Desired Frequency	Final Parallel Loads	Final frequency	PSIset
20 MHz	554KHz	219	548KHz	70

TABLE4. SCENARIO1 WITH DIFFERENT PSISET VALUES

Internal FRO	Desired Frequency	Final Parallel Loads	Final frequency	PSIset
20 MHz	400KHz	205	396KHz	125

TABLE5. SCENARIO1 WITH DIFFERENT PSISET VALUES

Internal FRO	Desired Frequency	Final Parallel Loads	Final frequency	PSIset
20 MHz	312KHz	192	312KHz	180

B. Fro_min = 30, Duration of external oscillator = 50, 100, 5000 and 6000 ns.(look at Fig6)

III. Noise Eliminator unit

A. As you can see in figure 7, noise eliminator works correctly.

B. As you can see in figure 8, when we issue power mode flag our main clock will be external ring oscillator output otherwise it will be PSI(noise eliminated and adjusted internal oscillator).

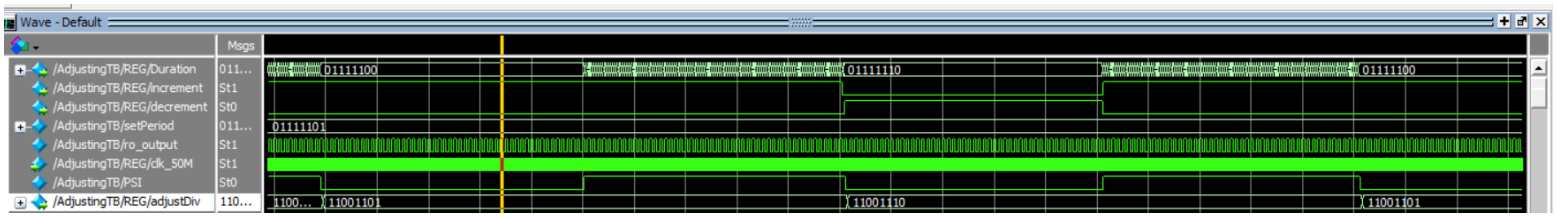

Fig. 1 Scenario 1

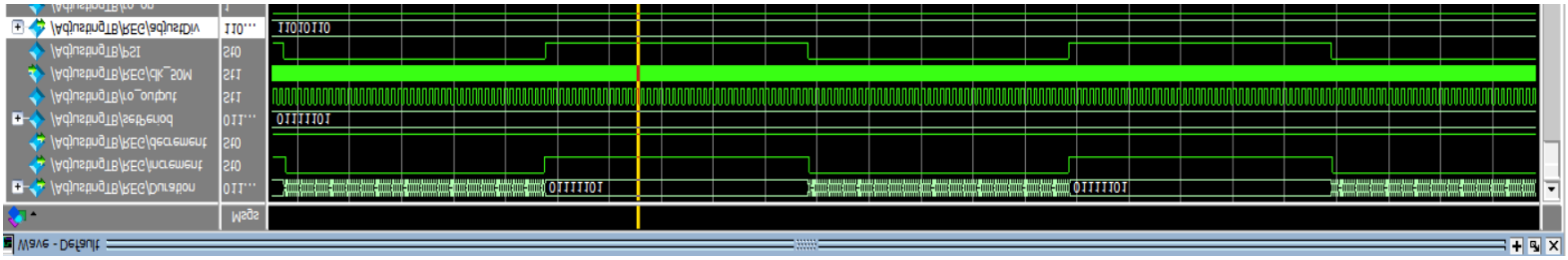

Fig. 2 Scenario 2

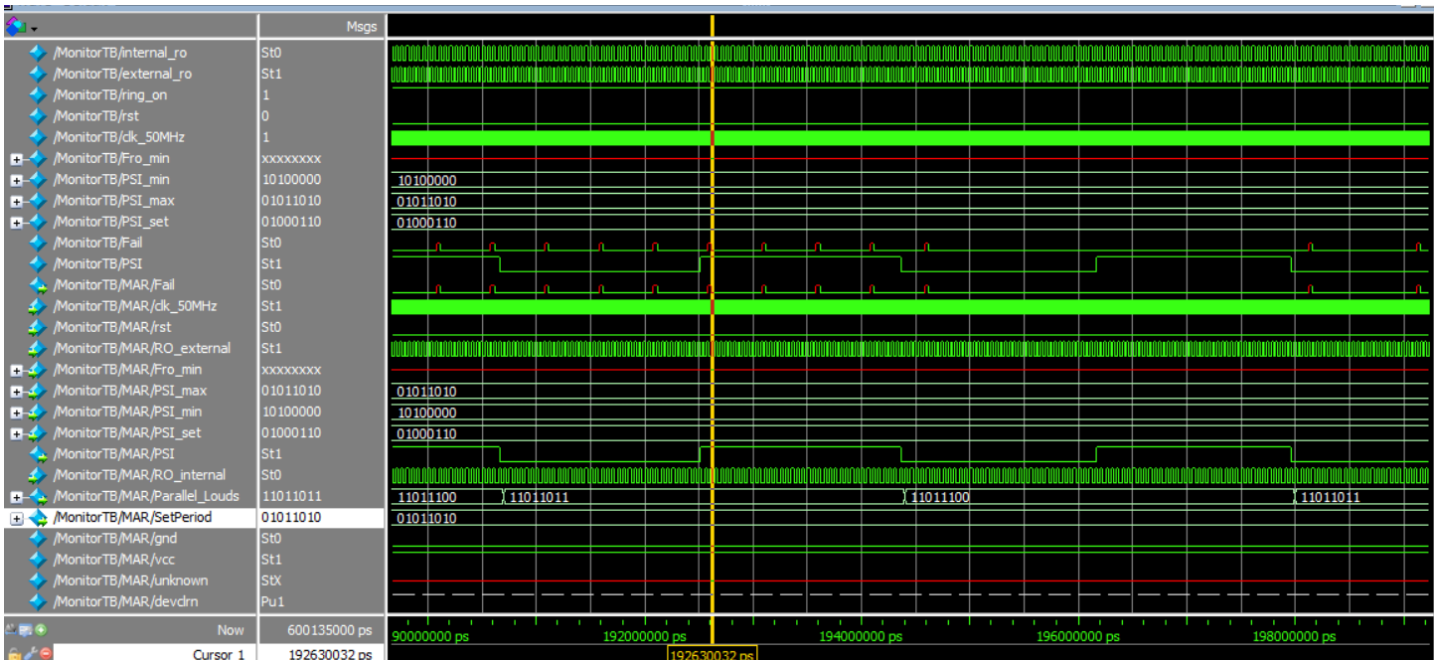

Fig. 3 Scenario 1

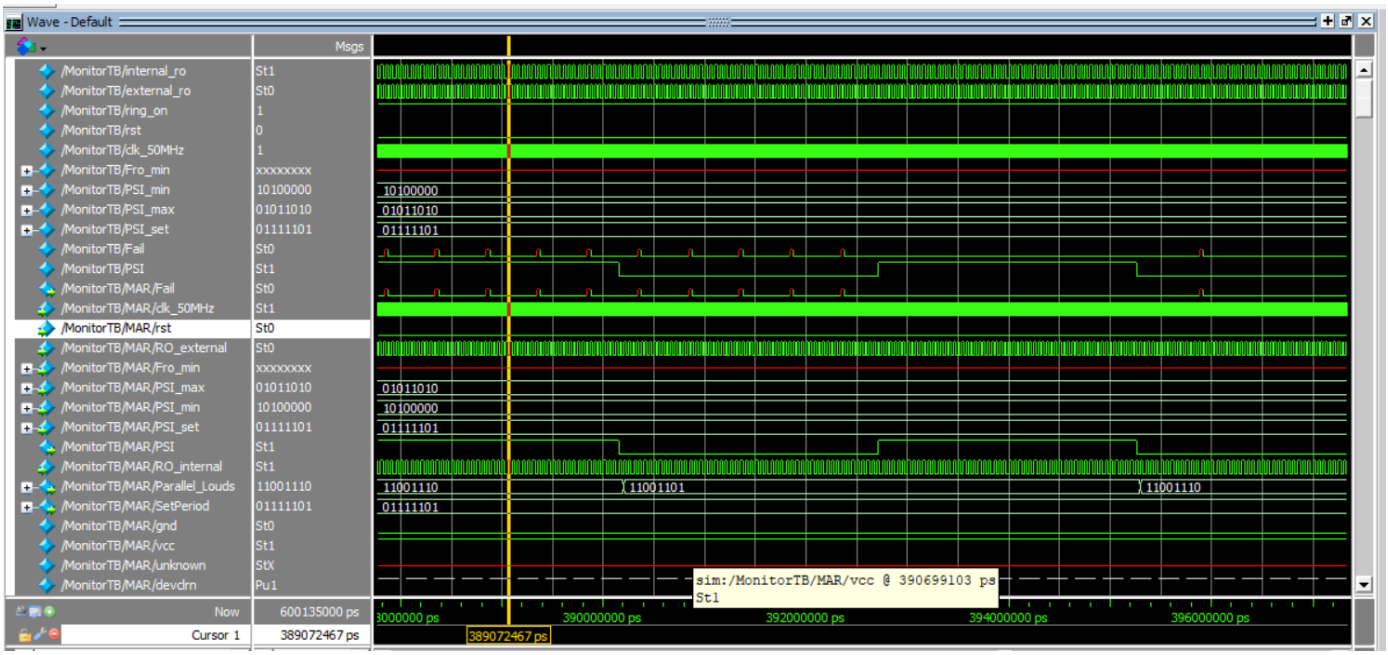

Fig. 4 Scenario 1

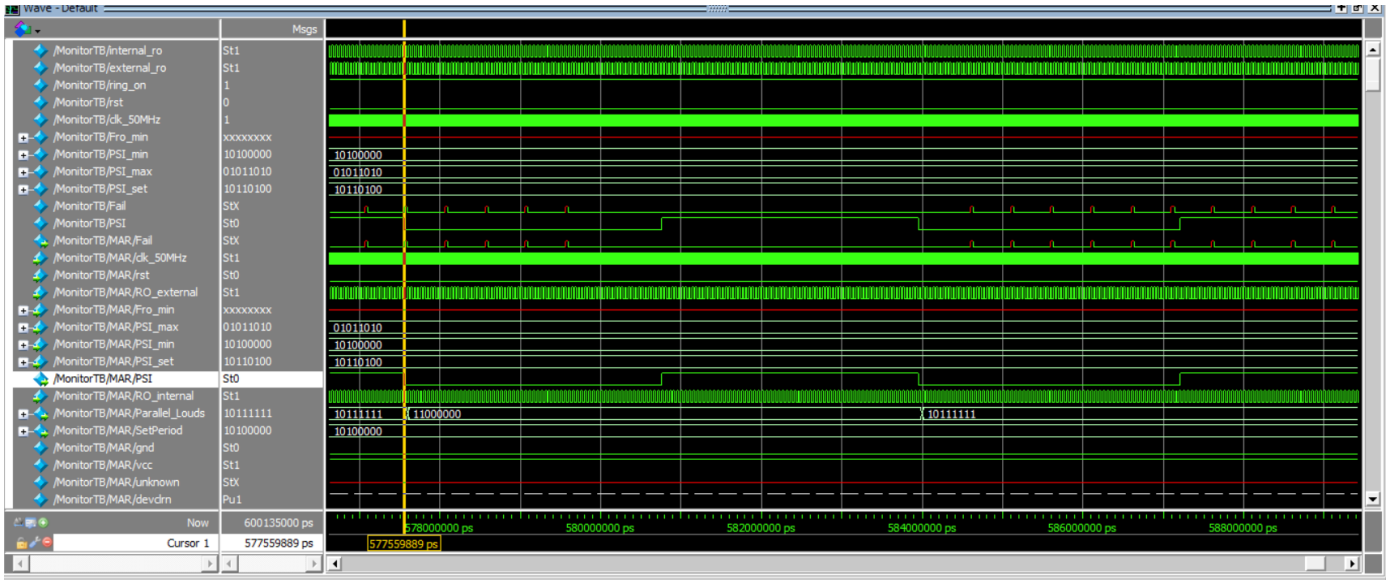

Fig. 5 Scenario 1

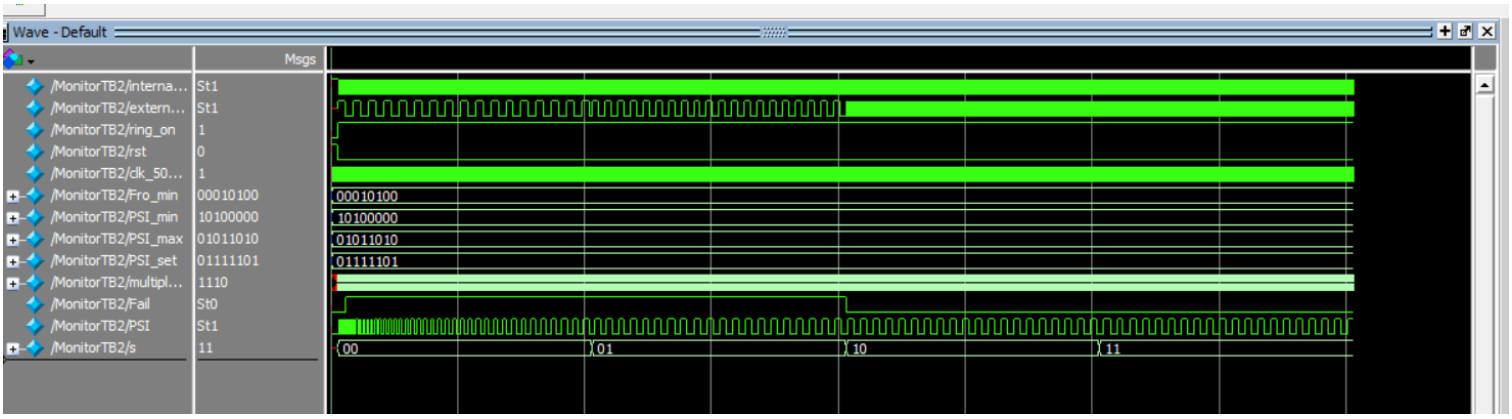

Fig. 6 Verify second task of clock monitoring unit

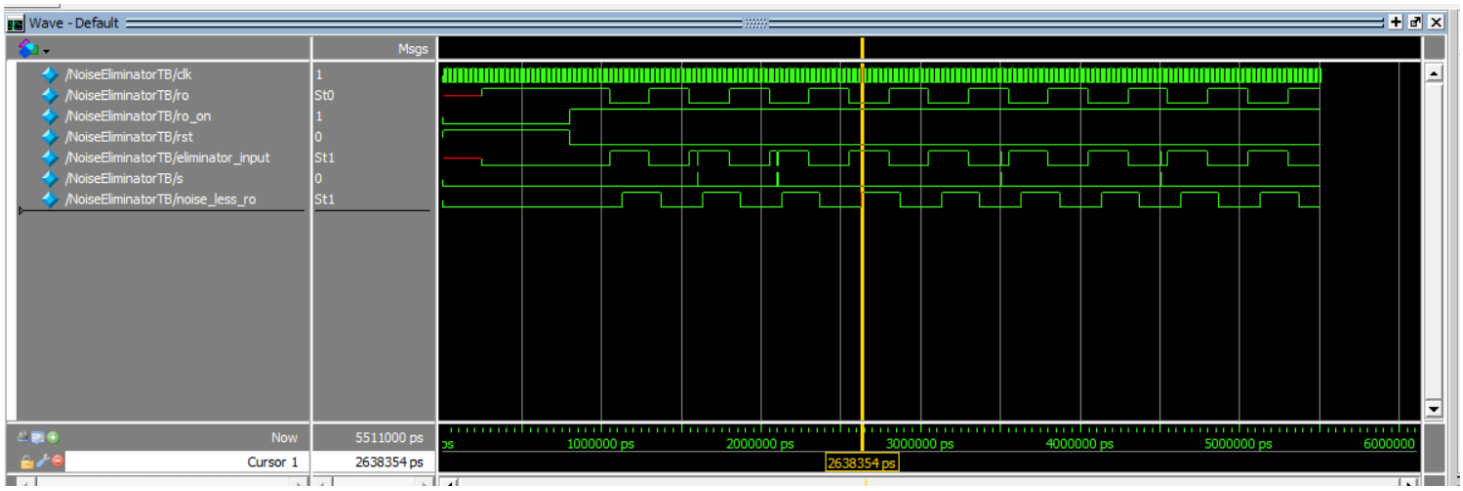

Fig. 7 Noise Eliminator waveform

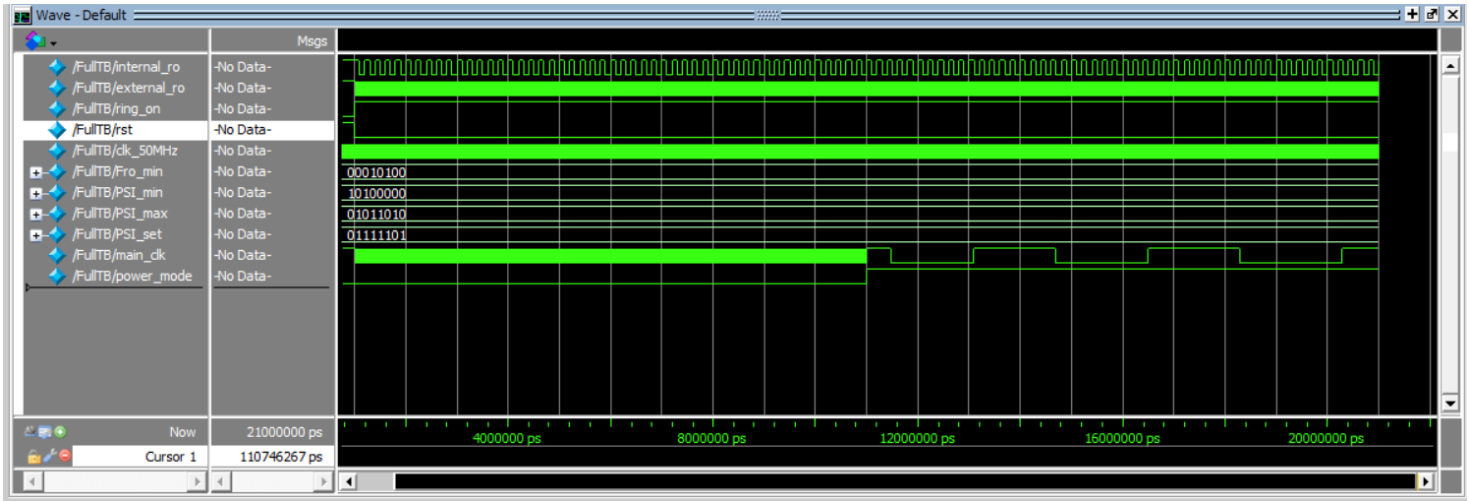

Fig. 8 Full Design waveform