

# Experiment #4 – Integrated System

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2) As you can see in figure 4 maximum frequency of this accelerator is equal to 135.01MHz.

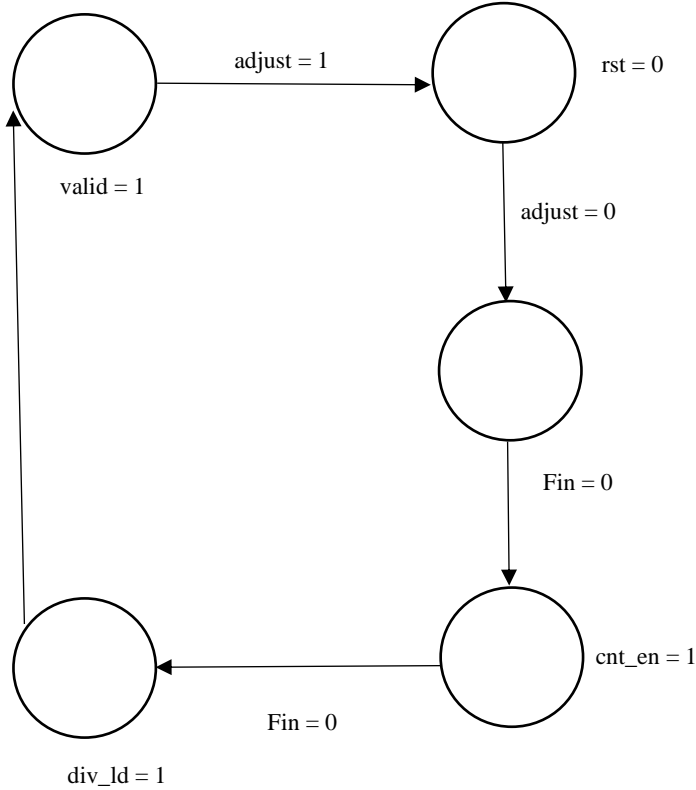
## B. Exponential Accelerator Wrapper:

1) Exponential Accelerator Wrapper Controller State diagram:

I. FREQUENCY MULTIPLIER  
 $f_{in} * 2^n = f_{ref} / k \rightarrow 1 / T_{in} * 2^n = 1 / (T_{ref} * k) \rightarrow$

$$k = T_{in} / (T_{ref} * 2^n)$$

### A. State Diagram of the Controller:



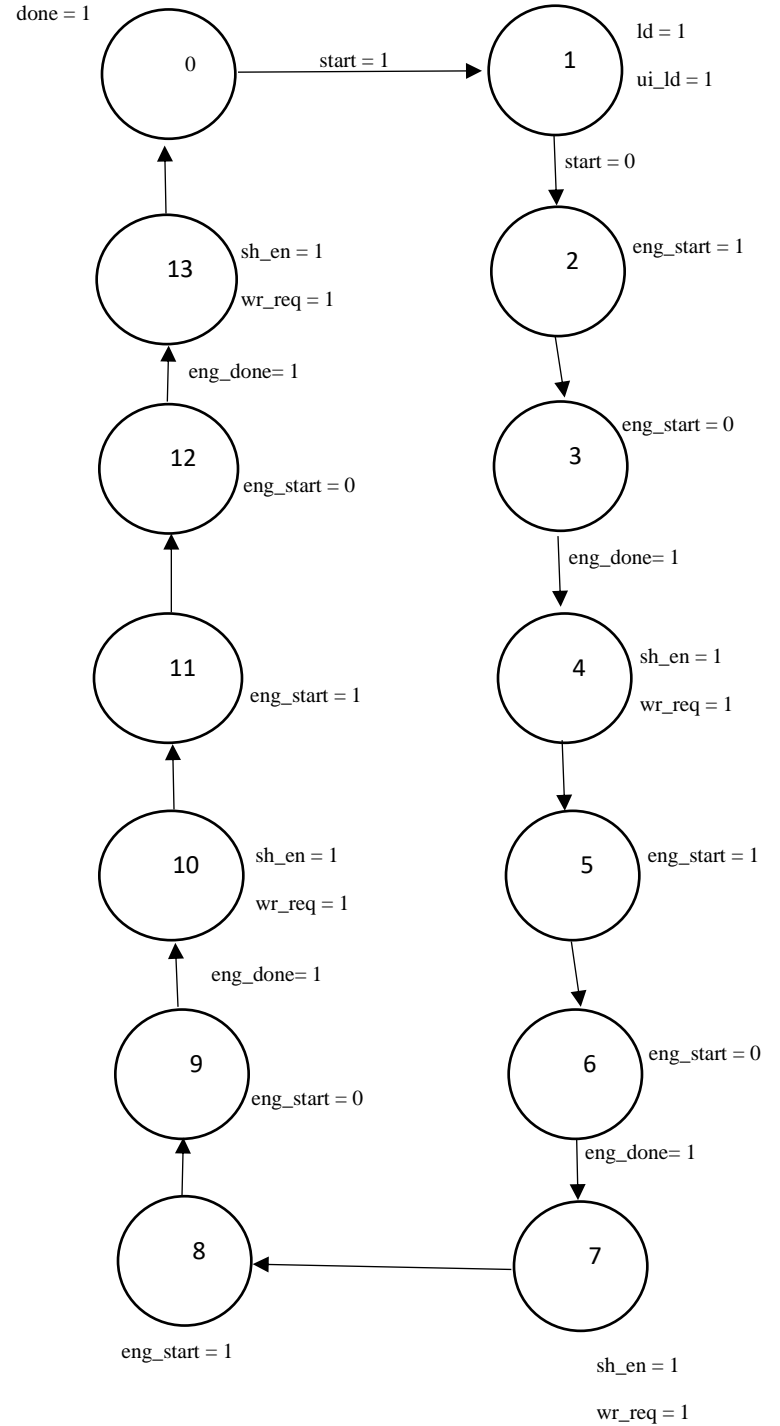
### B. Simulate results:

In all of wave forms InFreq = 1MHz  
 Look at figures 1, 2 and 3.

## II. EXPONENTIAL ACCELERATOR

### A. Exponential Engine:

- 1) As you can see in figure 4 if we set
  - ◇ x = 0: answer will be 1
  - ◇ x = 1: answer will be e ~ 2.718
  - ◇ x = 0.5: answer will be  $e^{0.5} \sim 1.648$



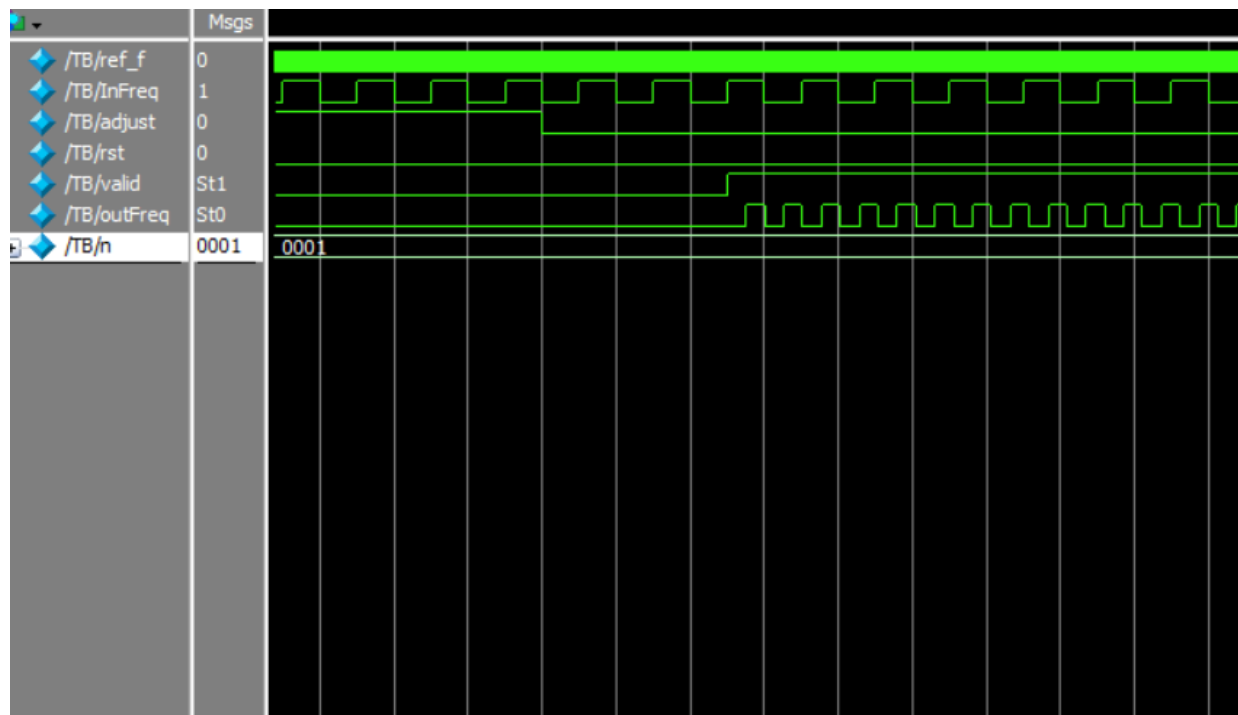


Fig. 1  $n=1$ , outFreq frequency = 2MHz

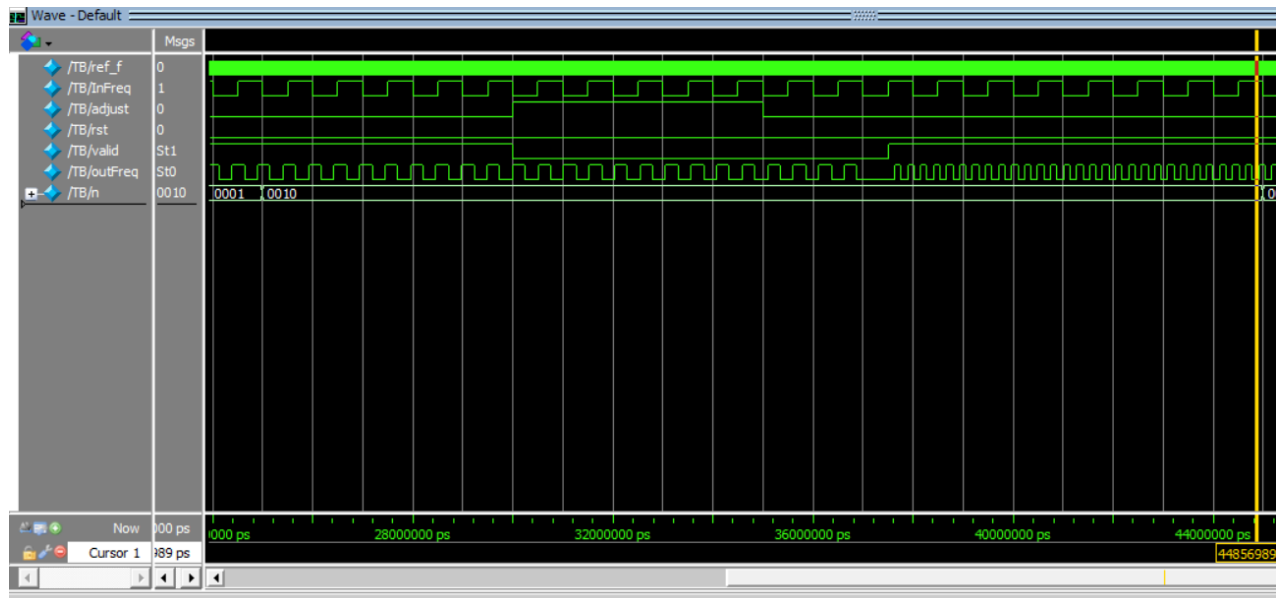


Fig. 2  $n = 2$ , outFreq frequency = 4MHz

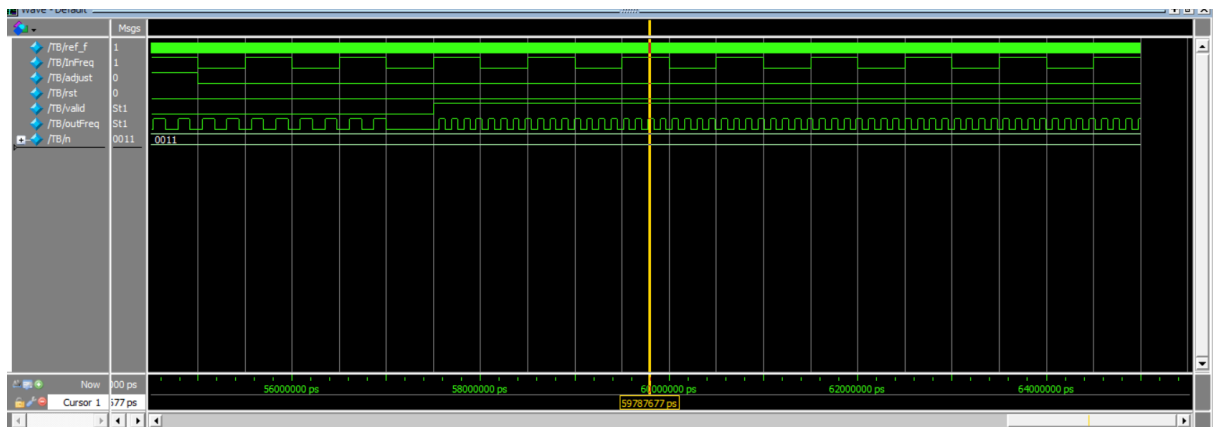


Fig. 3  $n = 4$ , outFreq frequency = 8MHz

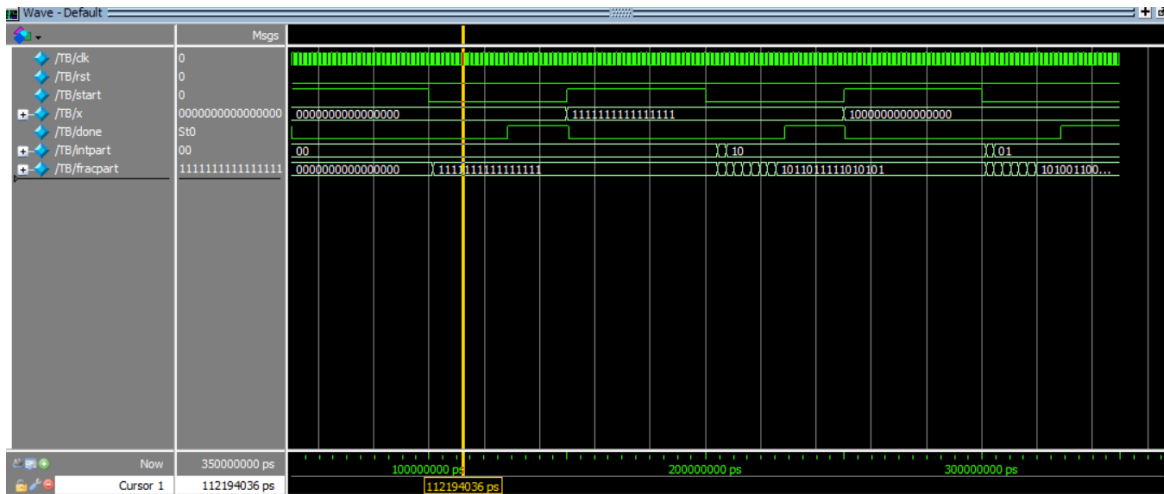


Fig. 4 simulate accelerator waveform

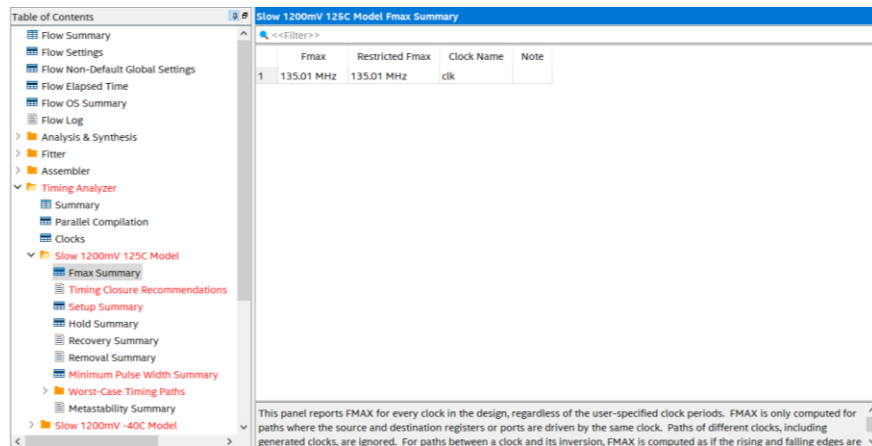


Fig. 5 Accelerator maximum frequency

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Slow 1200mV 125C Model Fmax Summary

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	Fmax	Restricted Fmax	Clock Name	Note
1	132.22 MHz	132.22 MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always

Fig. 6 Wrapper maximum frequency

2) According to figure 6 its maximum frequency = 132.22MH

### III. INTEGRATED CIRCUIT

1) MultFactor <= 661 → n <= 5