Experiment #1 - Clock and Periodic Signal Generation

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I. Clock Generation using ICs and Analog Components

A. *Ring Oscillator*

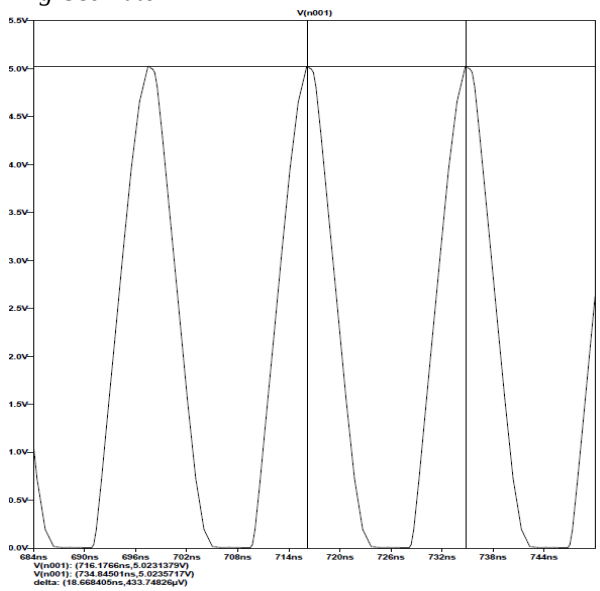

Fig. 1 Output waveform

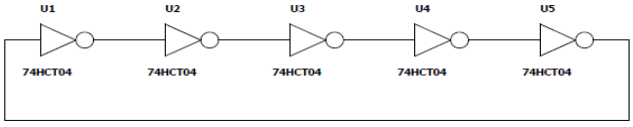

Fig. 2 Circuit simulated

1) Propagation Delay of the Chain: 18,67ns

2) Delay of a Single Inverter: 1.867ns

TABLE I
74HCT04 Propagation Delays

Symbol	Parameter	Test Conditions	V_{CC}	T_A = +25°C			-40°C to +85°C	-40°C to +125°C	Unit
				Min	Typ	Max	Max	Max	
t_{PD}	Propagation Delay A_N to Y_N	Figure 1 C_L = 50pF	4.5V	–	12	22	24	29	ns
t_t	Transition time	Figure 1 C_L = 50pF	4.5V	–	7	29	29	29	ns

B. *LM555 Timer*

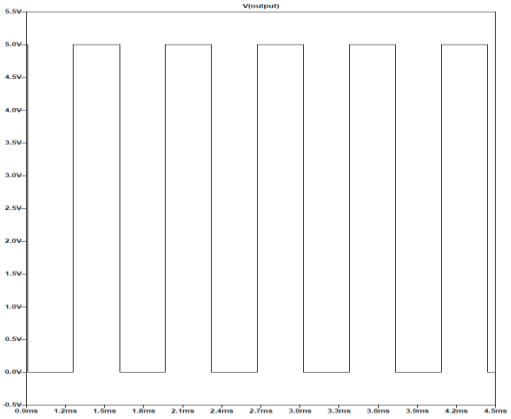

Fig. 3 Output waveform

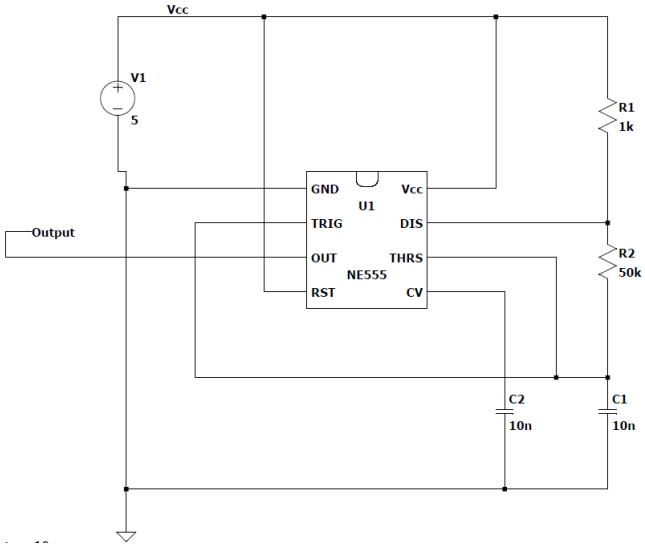

Fig. 4 Circuit

First of all we need to add a voltage power generator(V1) and connect it to GND and Vcc port to generate continuous rectangular pulse then we just need to calculate clock and duty cycle frequency using waveform.

1) Clock Frequency & Duty Cycle: 1.416KHz, 50.15%

2) Produce Different Clock Frequencies: Related waveform for each resistor shown below.

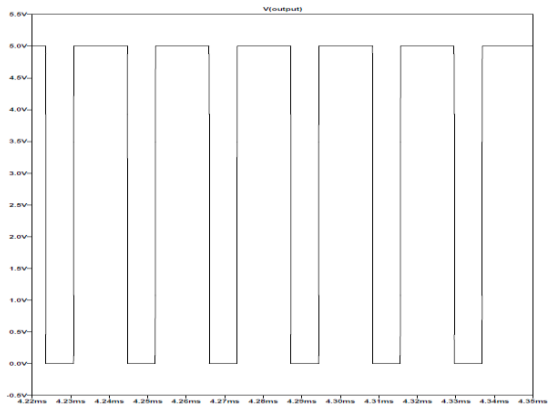

Fig. 5 R2 = 1Kohm

◊ Clock frequency:

- Expected: 1 / 0.693 * (3Kohm) * 10nF = 48.1KHz
- Simulated result: 1 / 21.203us = 47.16KHz

◊ Duty cycle:

- Expected: 2/3 = 66.66%
- Simulated result: 65.51%

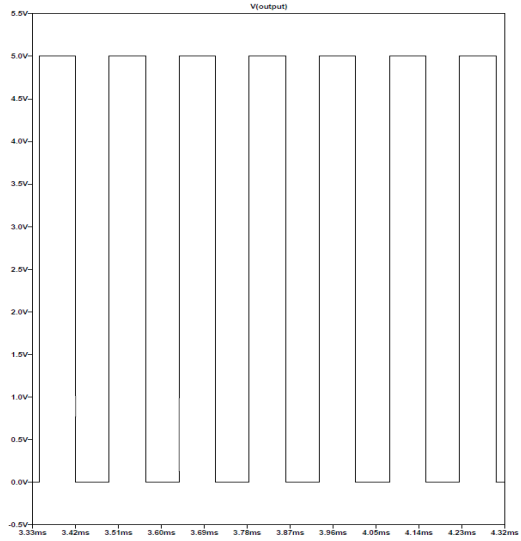

Fig. 6 R2 = 10Kohm

◊ Clock frequency:

- Expected: 1 / 0.693 * (21Kohm) * 10nF = 6.87KHz
- Simulated result: 1 / 146.90us = 6.8KHz

◊ Duty cycle:

- Expected: 11/21 = 52.38%
- Simulated result: 51.95%

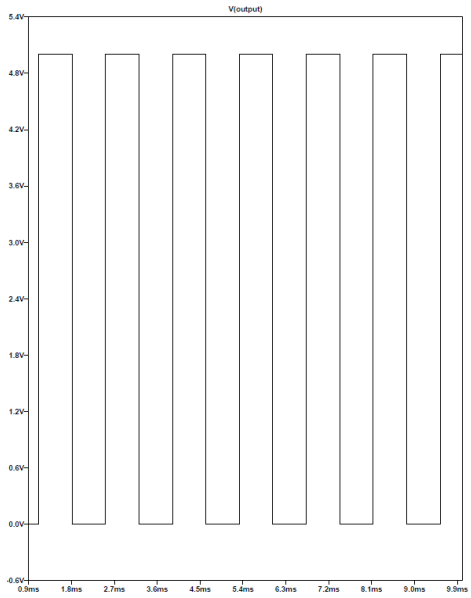

Fig. 7 R2 = 100Kohm

◊ Clock frequency:

- Expected: 1 / 0.693 * (201Kohm) * 10nF = 717.91Hz
- Simulated result: 1 / 1.40446ms = 712.01Hz

◊ Duty cycle:

- Expected: 101 / 201 = 50.24%%
- Simulated result: 49.92%

C. Schmitt Trigger Oscillator

1) Try Different Resistors: Related waveform for each resistor shown below.

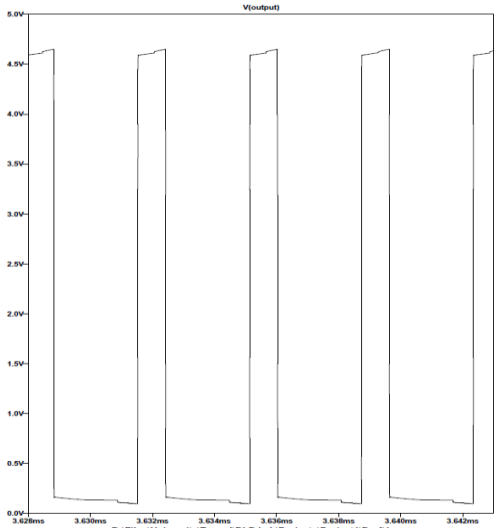

Fig. 8 R = 470ohm

◊ Clock frequency = 277.349KHz → α = 1.3

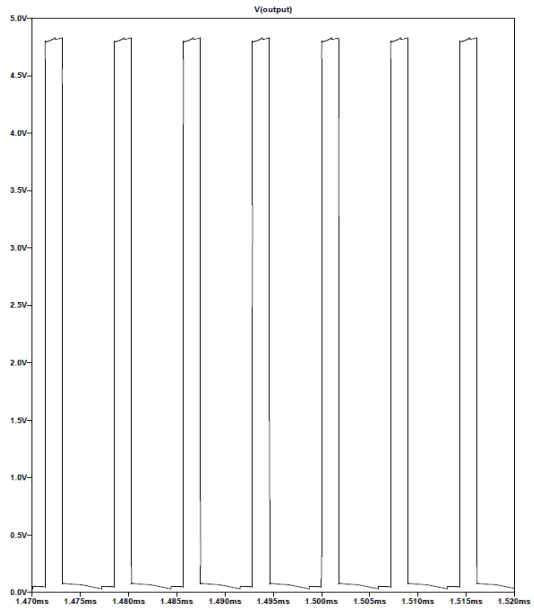

Fig. 9 R = 1Kohm

◊ Clock frequency = 139.532KHz → α = 1.3

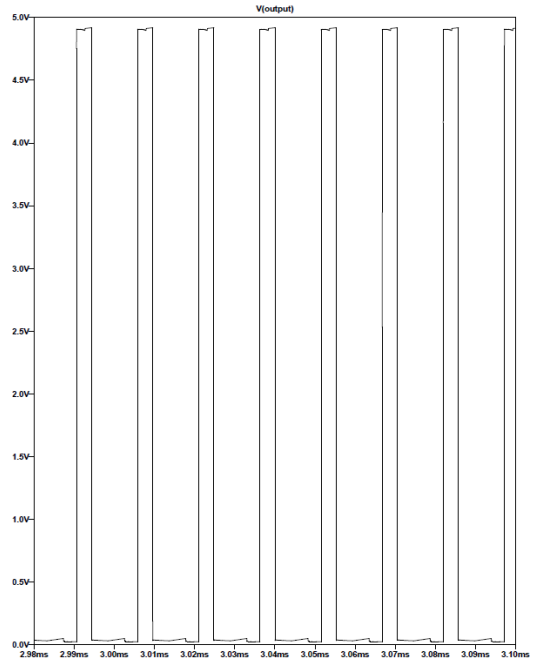

Fig. 10 R = 2.2Kohm

◊ Clock frequency = 65.643KHz → α = 1.4

2) α ~ 1.33

II. FPGA Design

A. Simulated Ring Oscillator Frequency = 53.56MHz

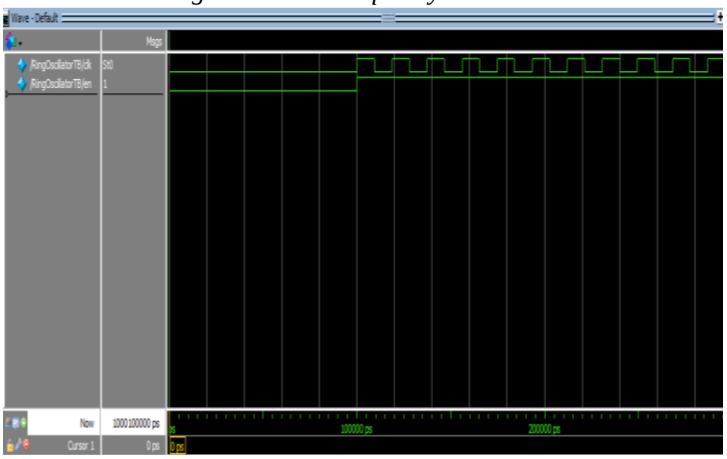

Fig. 11 Simulated waveform

B. New Frequency

New Frequency = 478.233KHz which is ring oscillator's frequency / 112

C. T Flip-Flop

We should add JK Flip-Flop like Fig. 14.

III. Baud Rate Generator for UART Serial Communication

A. Automatic Baud Rate Calculator

1) Controller state diagram has shown in Fig. 15

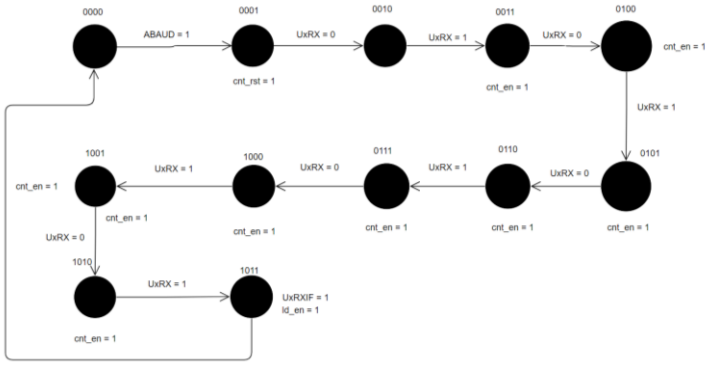

Fig. 15 State Diagram

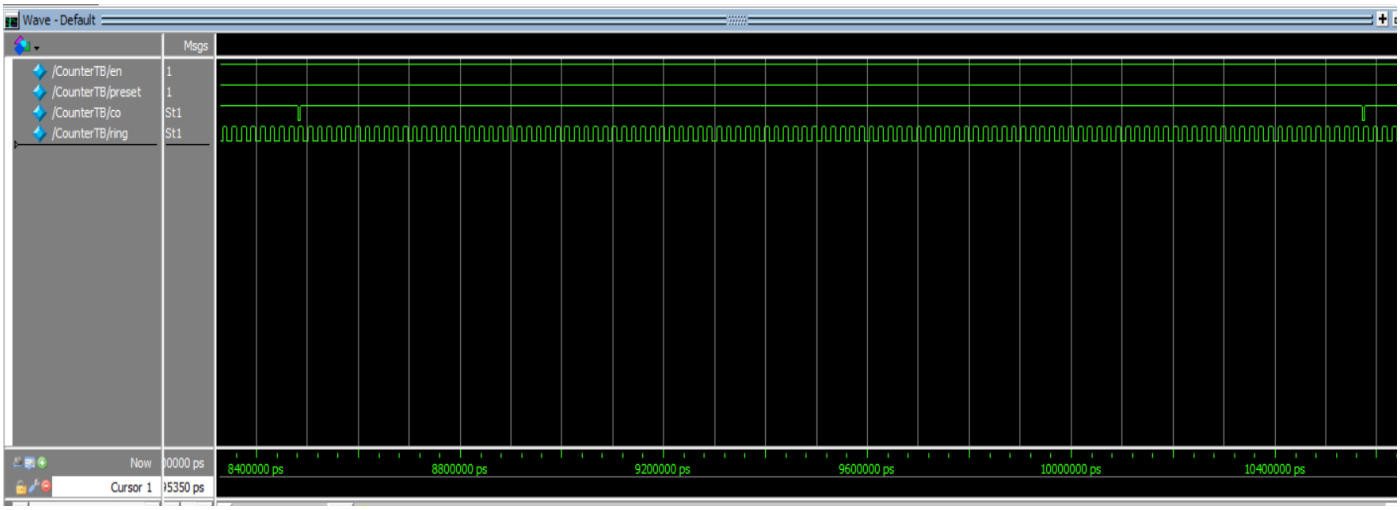

Fig. 12 MSB CO waveform

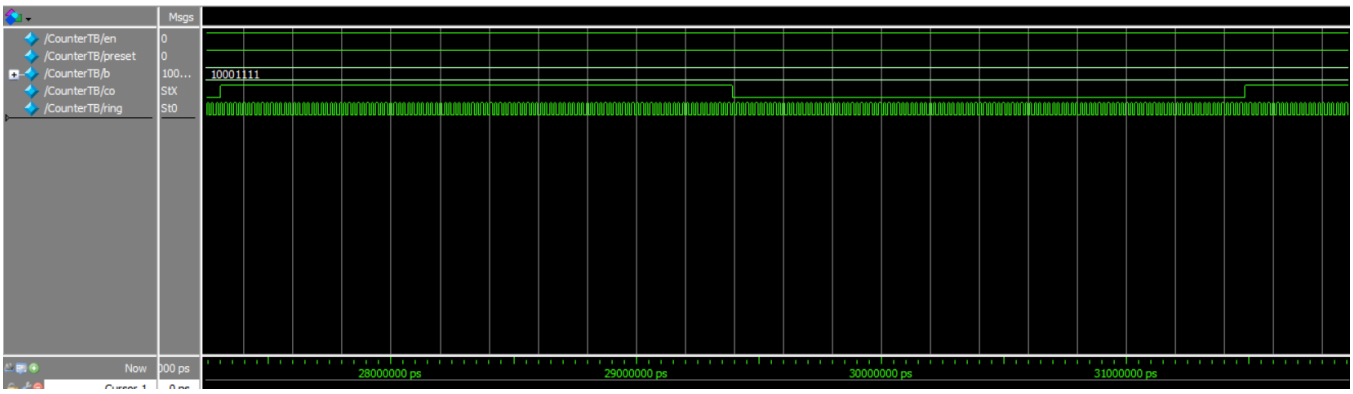

Fig. 13 New waveform after insert T Flip-Flop

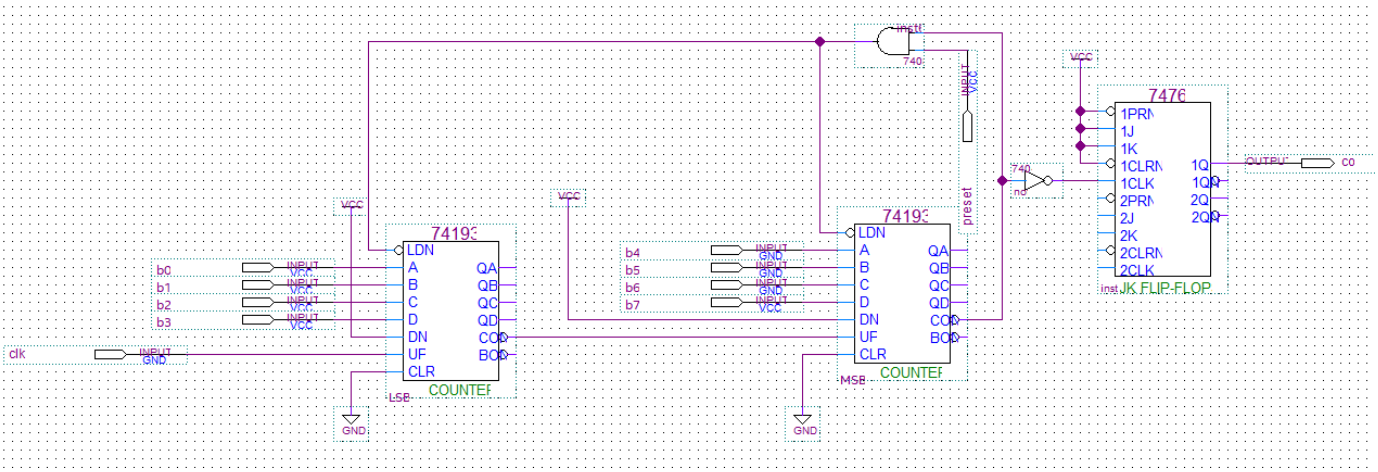

Fig. 14 Circuit after insert JK Flip-/flop

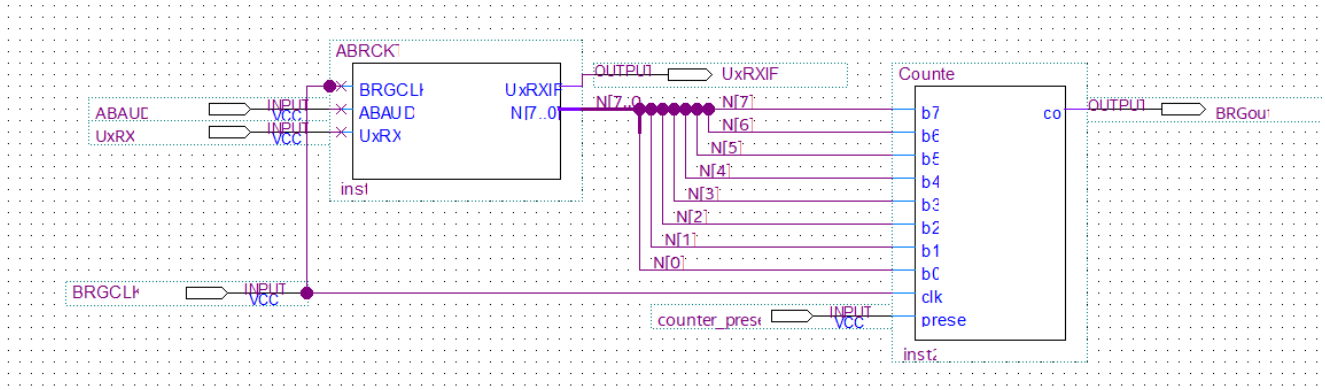

Fig. 15 Final BRGCKT schematic design

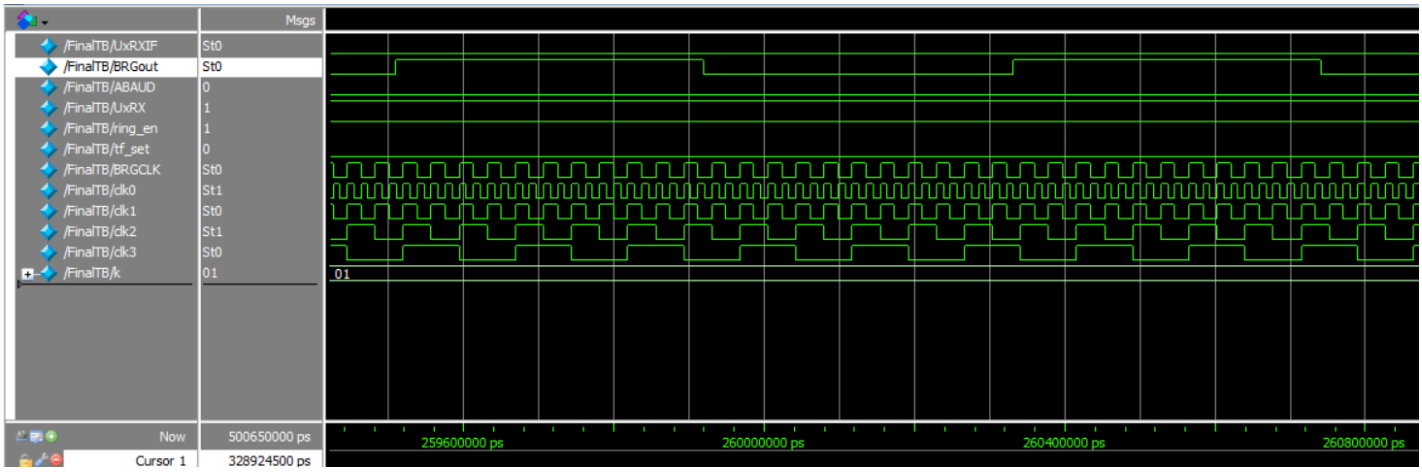

Fig. 16 BRGCKT test bench waveform

◊ BRGout frequency = 1.21 MHz

◊ BRGCLK = 53.56 MHz

Calculate expected fBaud frequency theoretically: k = 1, N = 11 → fBaud = $53.56 * 10^6 / (11 * 2^1 * 2) = 1.21$MHz which is equal to BRGout frequency.