Experiment #2 - Clock Adjusting and Monitoring

Moein Karami,

810198540

# Clock Adjusting Unit

## *Look at tables and figs 1 and 2*

Table1. Scenario1 With Fixed Setperiod Value

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Ring Oscillator Frequency** | **Desired Frequency** | **Final Parallel Loads** | **Initial Parallel Loads** | **Setperiod** |
| 20 MHz | 400KHz | 205 | 1 | 125 |

Table2. Scenario2 With Fixed Setperiod Value

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Ring Oscillator Frequency** | **Desired Frequency** | **Final Parallel Loads** | **Initial Parallel Loads** | **Setperiod** |
| 18 MHz | 400KHz | 214 | 205 | 125 |

1. Clock Monitoring Unit

## *Look at tables and figs 3, 4 and 5*

Table3. Scenario1 with Different PSIset Values

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Internal FRO** | **Desired Frequency** | **Final Parallel Loads** | **Final frequency** | **PSIset** |
| 20 MHz | 554KHz | 219 | 548KHz | 70 |

Table4. Scenario1 with Different PSIset Values

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Internal FRO** | **Desired Frequency** | **Final Parallel Loads** | **Final frequency** | **PSIset** |
| 20 MHz | 400KHz | 205 | 396KHz | 125 |

Table5. Scenario1 with Different PSIset Values

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Internal FRO** | **Desired Frequency** | **Final Parallel Loads** | **Final frequency** | **PSIset** |
| 20 MHz | 312KHz | 192 | 312KHz | 180 |

* 1. *Fro\_min = 30, Duration of external oscillator = 50, 100, 5000 and 6000 ns.(look at Fig6)*

1. Noise Eliminator unit
   1. *As you can see in figure 7, noise eliminator works correctly.*
   2. *As you can see in figure 8, when we issue power mode flag our main clock will be external ring oscillator output*

*otherwise it will be PSI(noise eliminated and adjusted internal oscillator).*

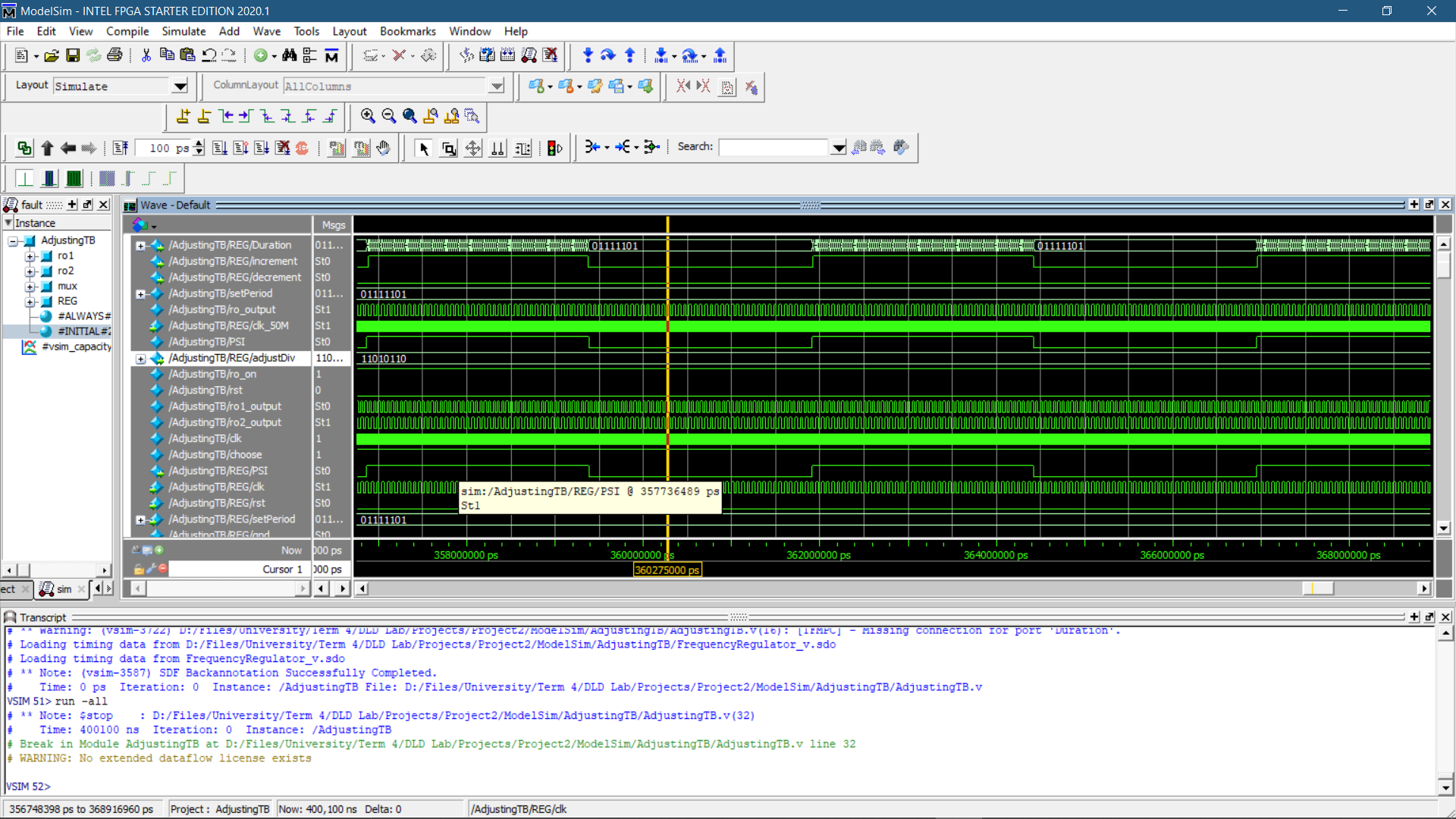
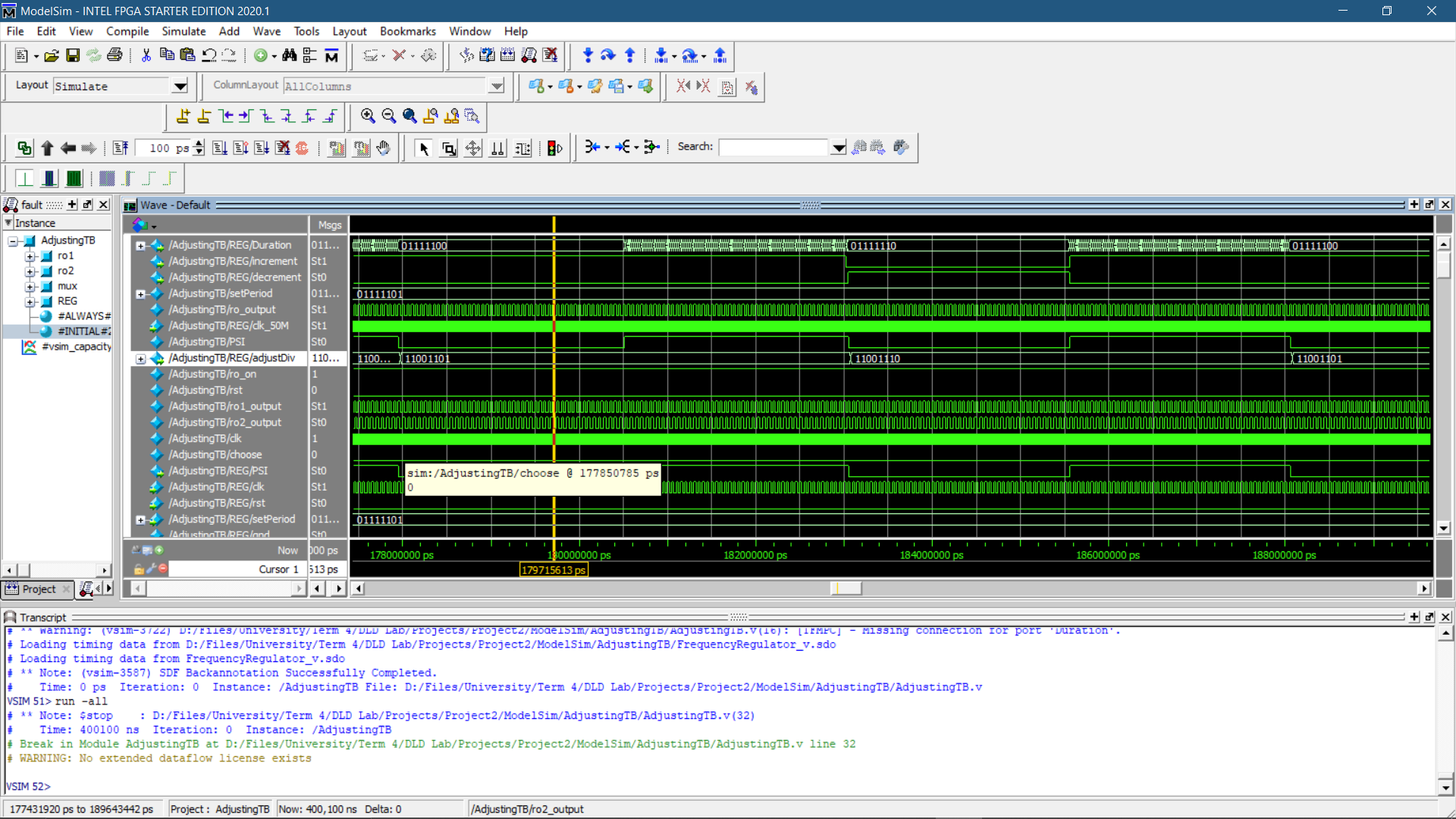
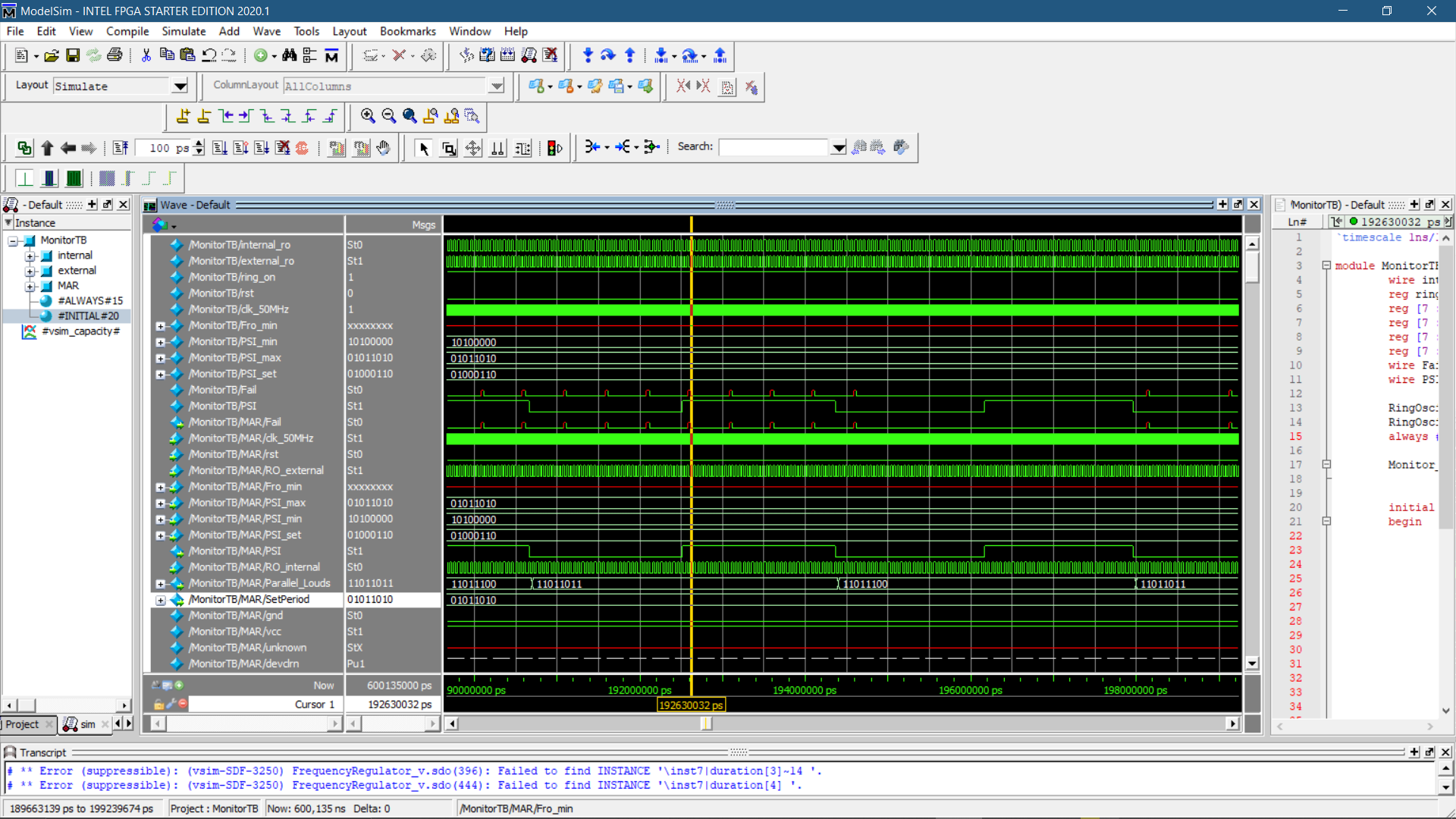


Fig. 3 Scenario 1

Fig. 1 Scenario 1

Fig. 2 Scenario 2

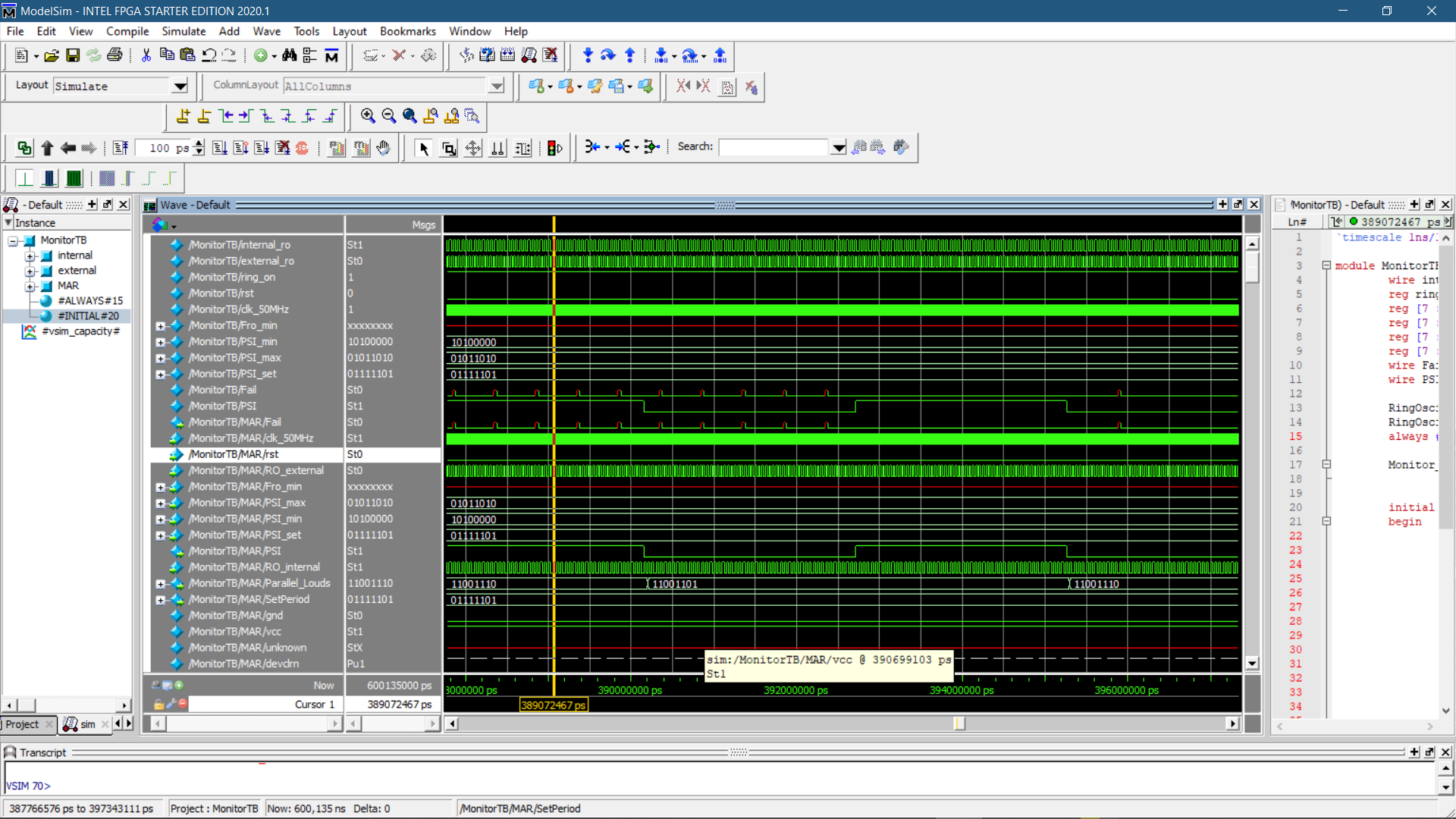
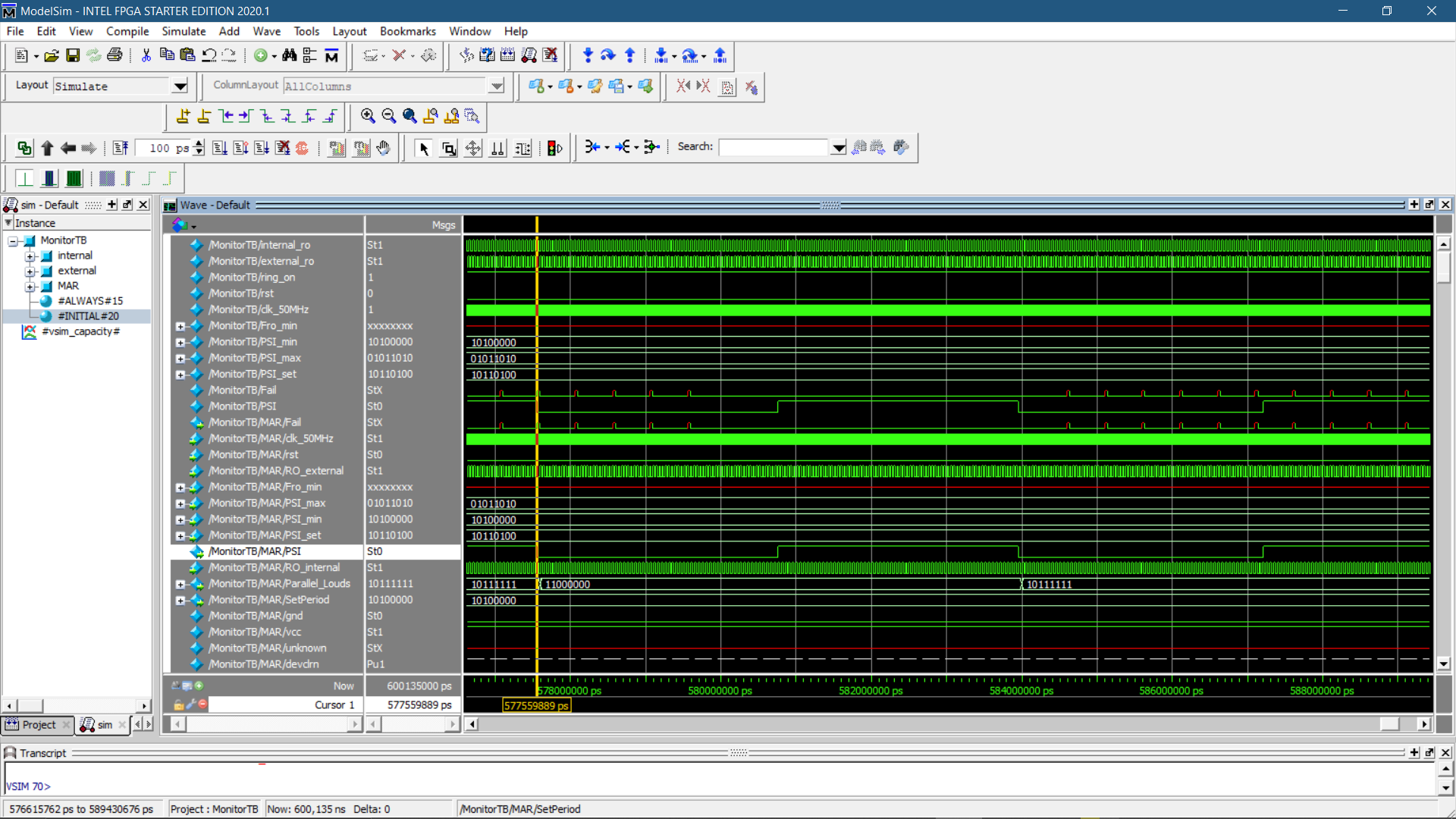


Fig. 5 Scenario 1

Fig. 4 Scenario 1

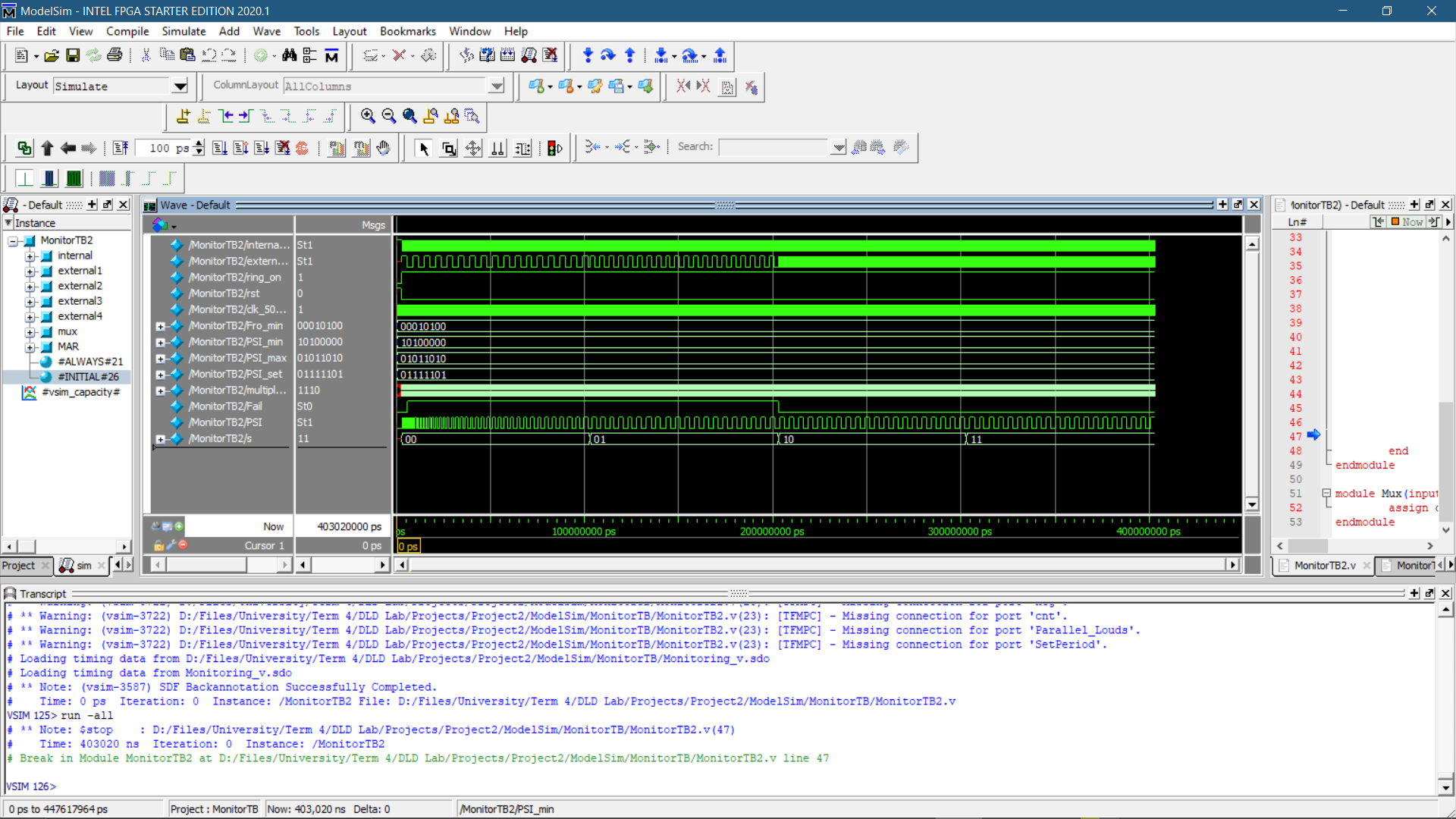
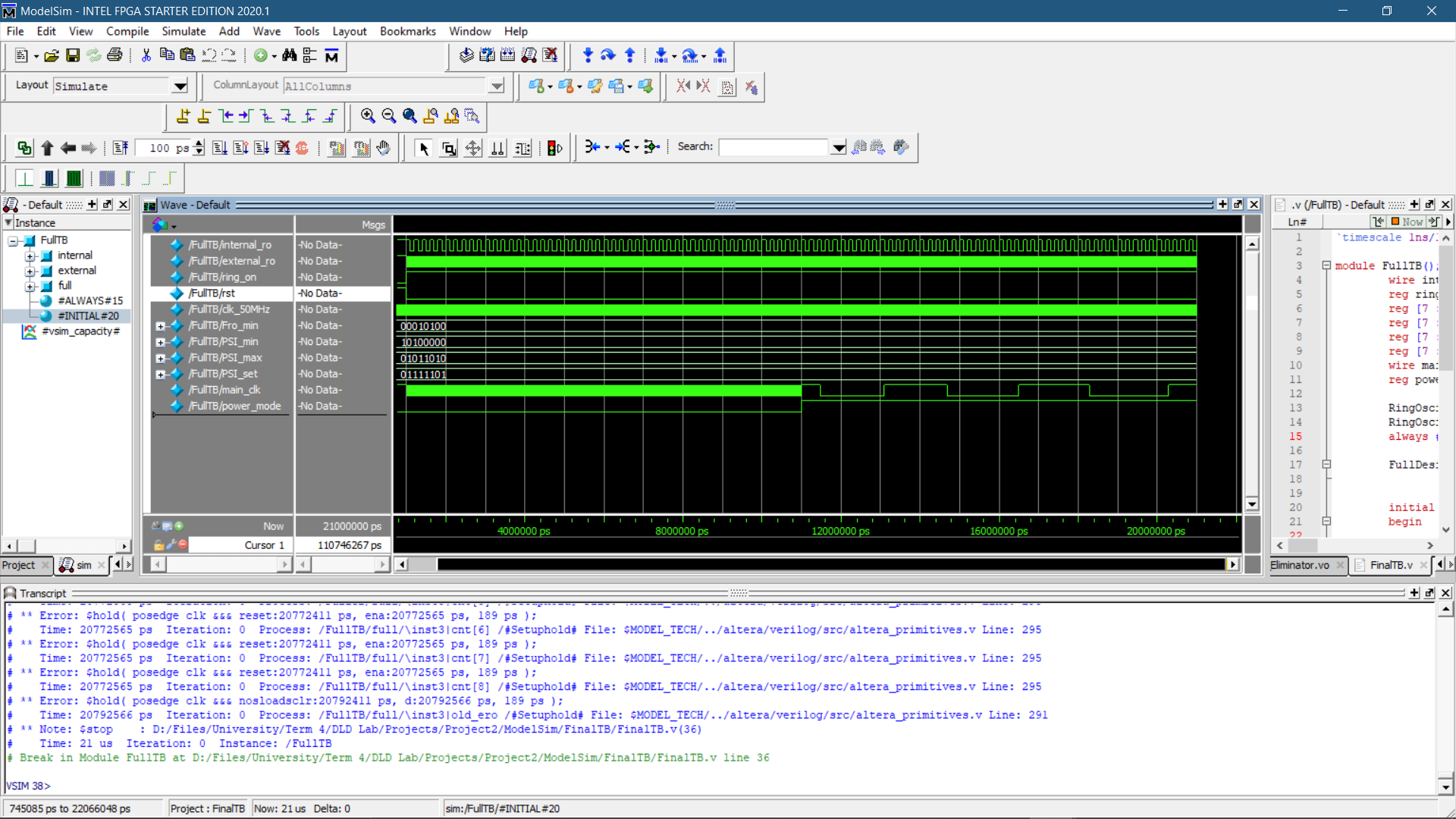
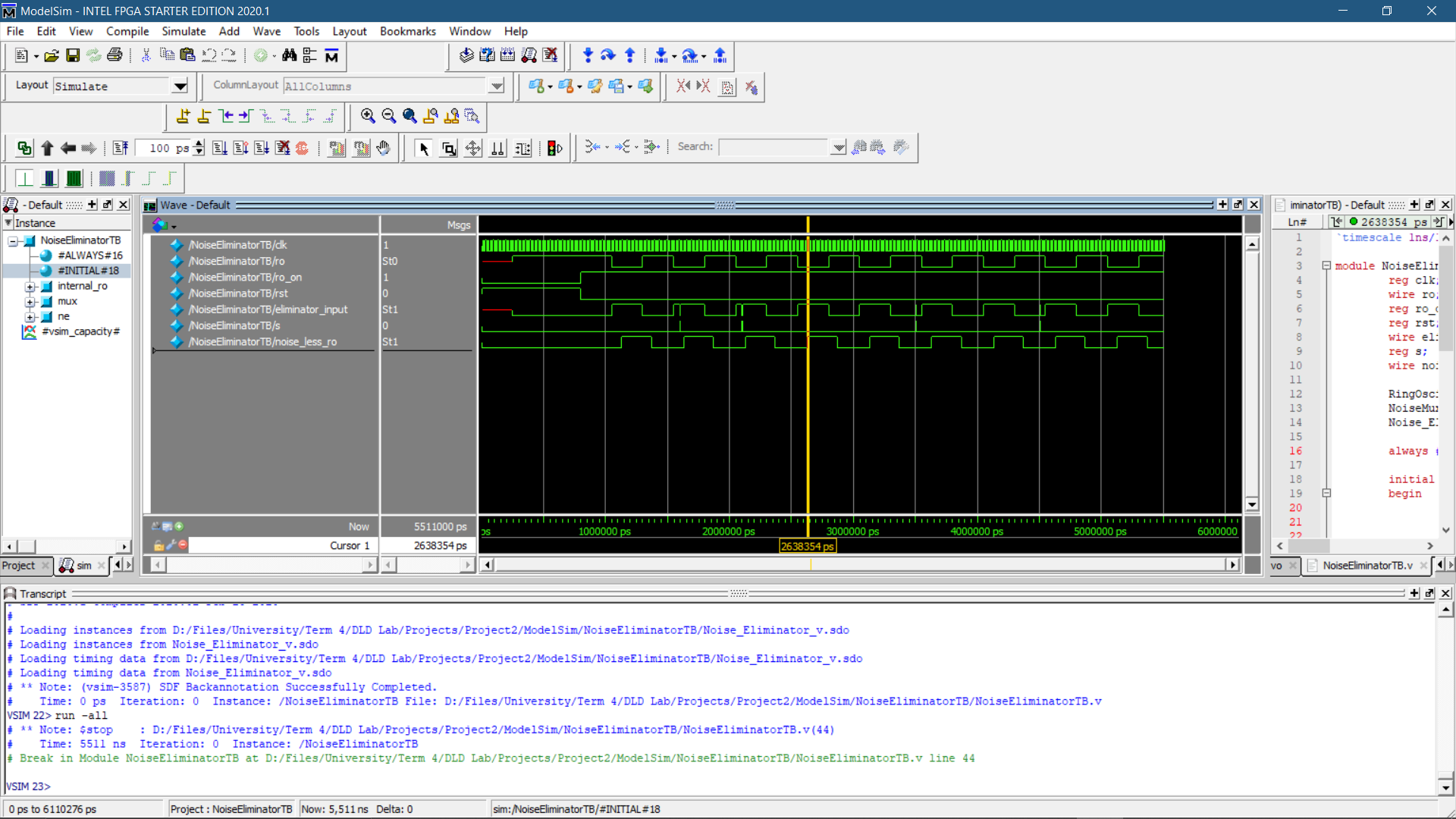


Fig. 8 Full Design waveform

Fig. 7 Noise Eliminator waveform

Fig. 6 Verify second task of clock monitoring unit