Maein Karami

8102985 40

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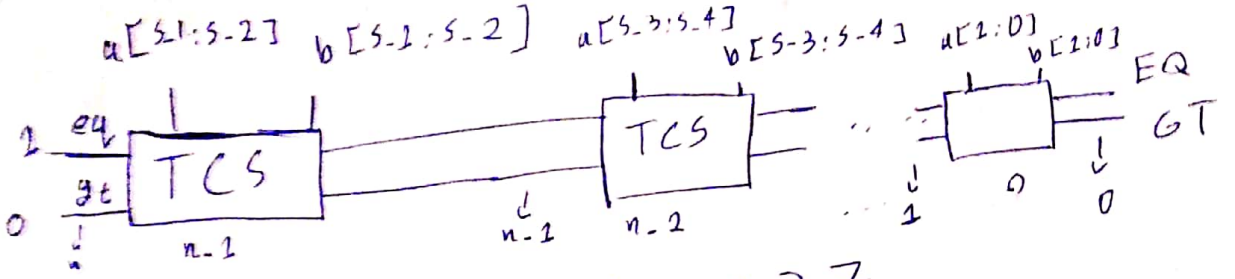
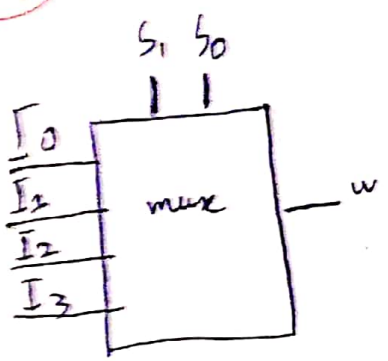
②



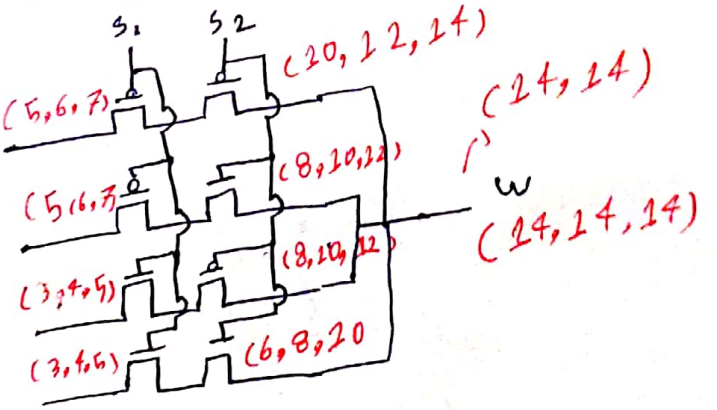
$n = 5/2$

worst case delay = 237

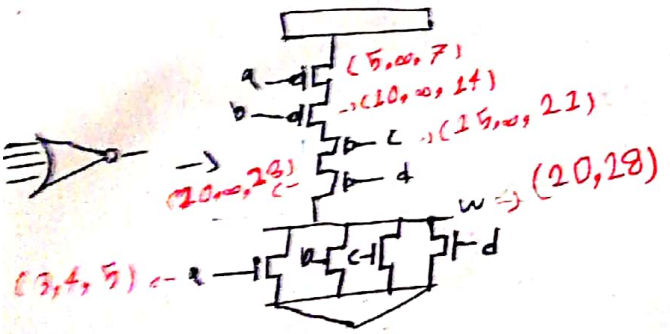
④ Nmos = (3,4,5) Pmos = (5,6,7)

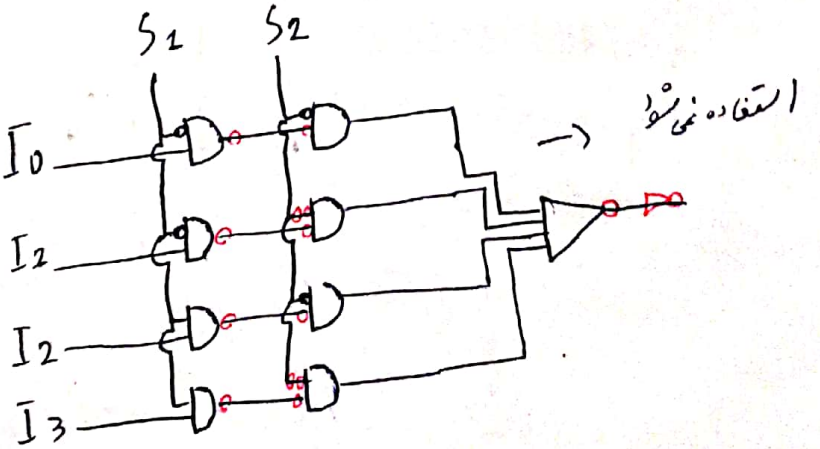


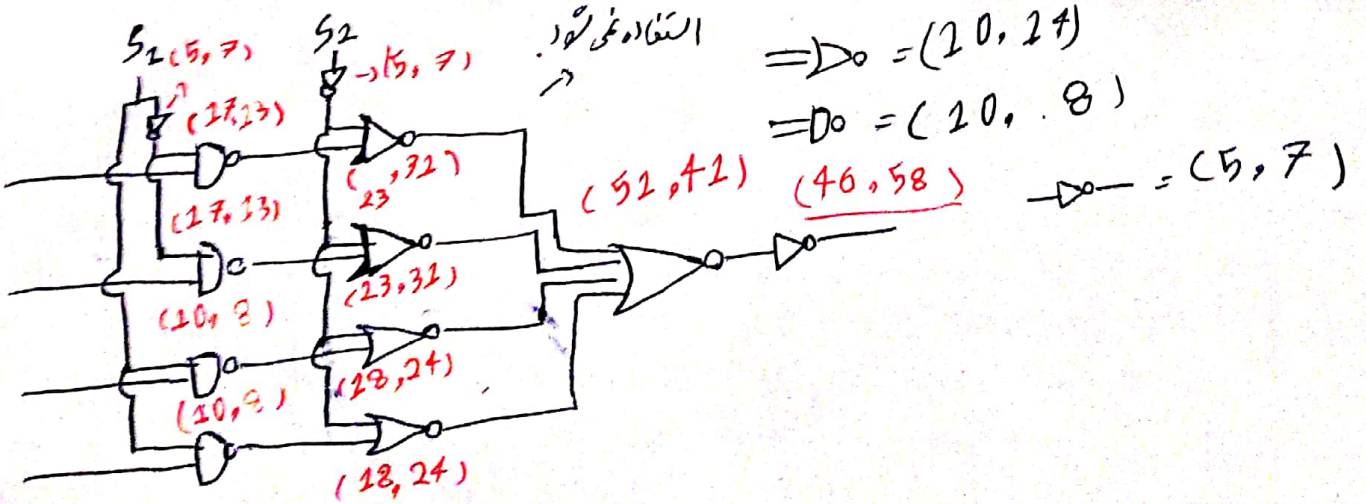
use pass transistor →



use CMOS structures →







Moein Kavami

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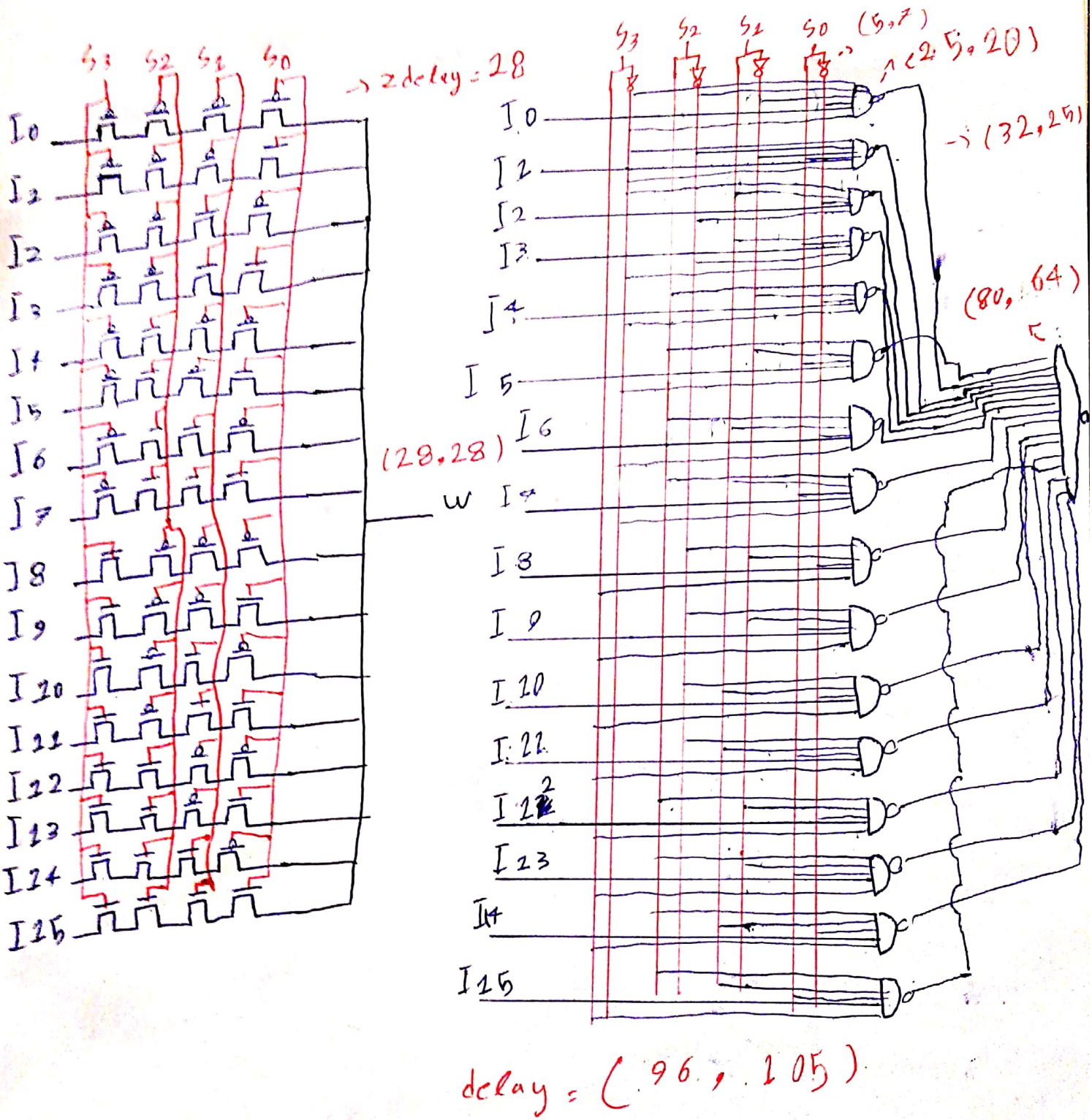


delay = (96, 105)

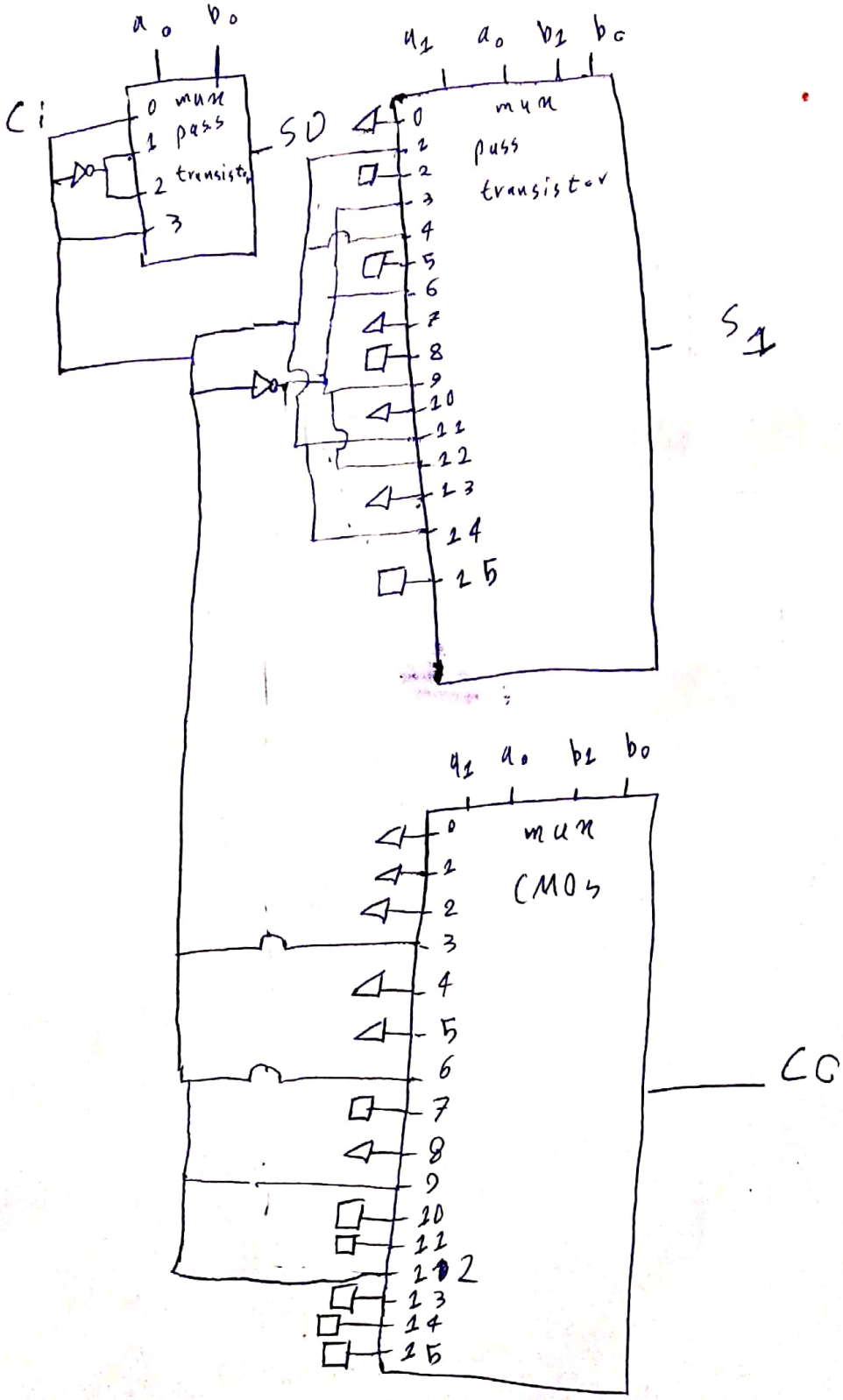
Moein Karami

8 1 0 1 9 8 5 4 0

Ci	a_1	a_0	b_1	b_0	Co	S_1	S_0	
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	1	0	2
0	0	0	1	1	0	1	1	3
0	0	1	0	0	0	0	1	4
0	0	1	0	1	0	1	0	5
0	0	1	1	0	0	1	1	6
0	0	1	1	1	1	0	0	7
0	1	0	0	0	0	1	0	8
0	1	0	0	1	0	1	1	9
0	1	0	1	0	1	0	0	10
0	1	0	1	1	1	0	1	11
0	1	1	0	0	0	1	1	12
0	1	1	0	1	1	0	0	13
0	1	1	1	0	1	0	1	14
0	1	1	1	1	1	1	0	15
1	0	0	0	0	0	0	1	16
1	0	0	0	1	0	1	0	17
1	0	0	1	0	0	1	1	18
1	0	0	1	1	1	0	0	19
1	0	1	0	0	0	1	0	20
1	0	1	0	1	0	1	1	21
1	0	1	1	0	1	0	0	22
1	0	1	1	1	1	0	1	23
1	1	0	0	0	0	1	1	24
1	1	0	0	1	1	0	0	25
1	1	0	1	0	1	0	1	26
1	1	0	1	1	1	1	0	27
1	1	1	0	0	1	0	0	28
1	1	1	0	1	1	0	1	29
1	1	1	1	0	1	1	0	30
1	1	1	1	1	1	1	1	31

Mocin Karami

8102985540



CO delay: to 1 = 384

to 0 = 420

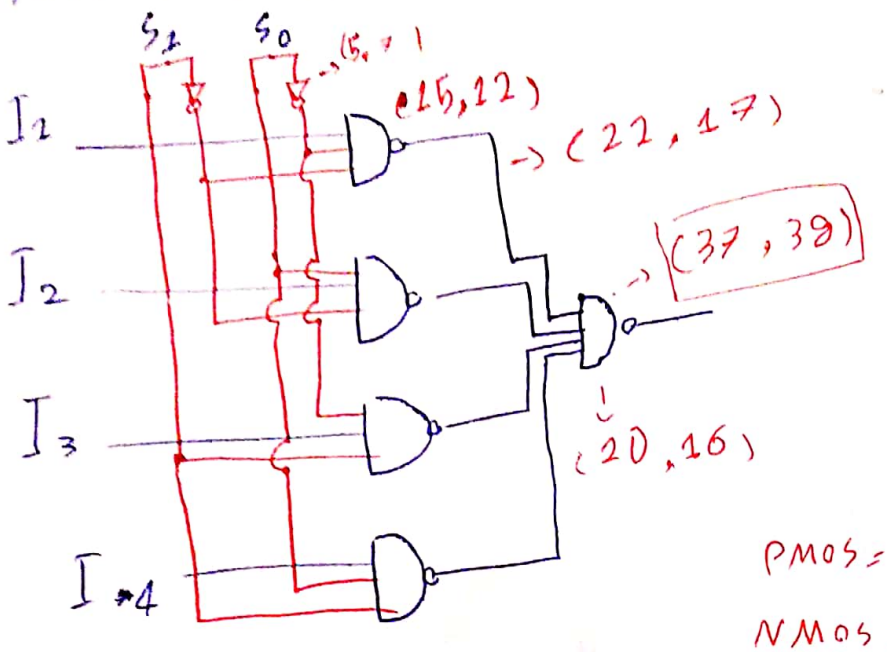
S delay = 348

Mosin Karami

810198540

7

CMOS mux 4_1



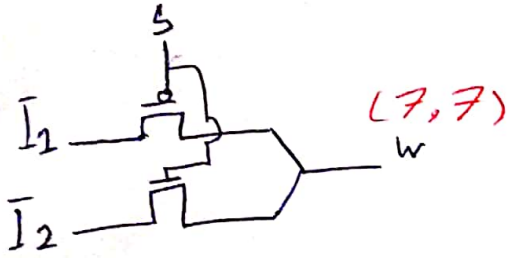
carry out worst case delay: to 1: 37
to 0: 76

worst case delay: 128

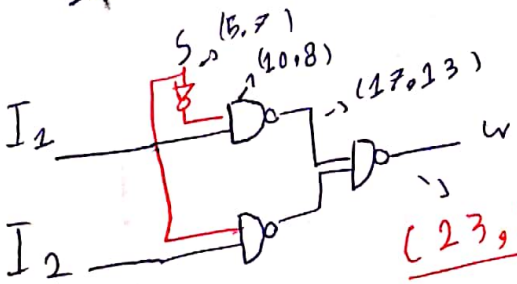
PMOS = (5, 6, 7)

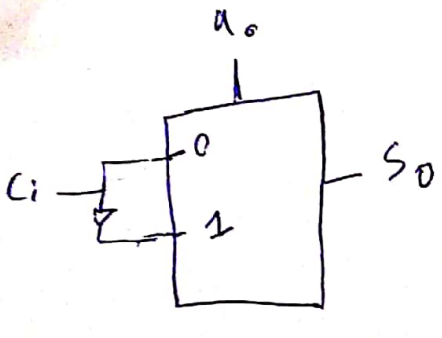
NMOS = (3, 4, 5)

2_1 mux pass transistor

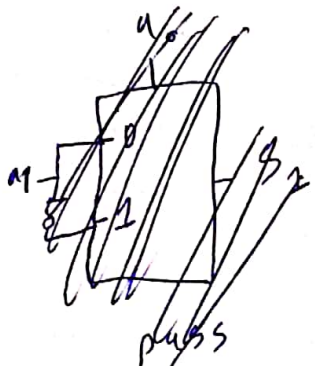


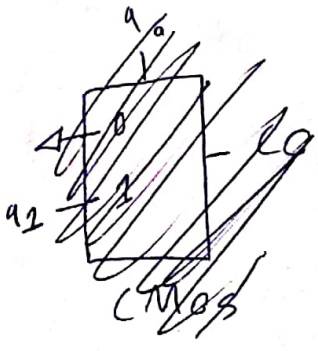
2_1 mux CMOS





pass

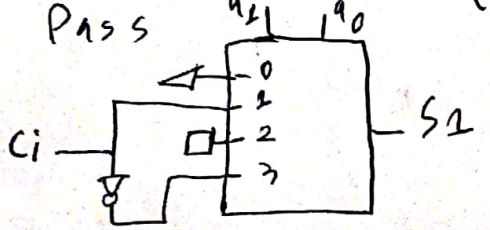




CMOS

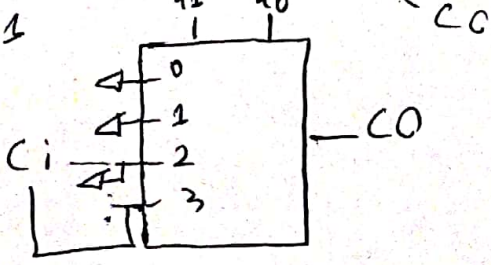
Ci \ a1a0	00	01	11	10
0	0	0	1	1
1	0	1	0	1

Pass



Ci \ a1a0	00	01	11	10
0	0	0	0	0
1	0	0	1	0

CMOS



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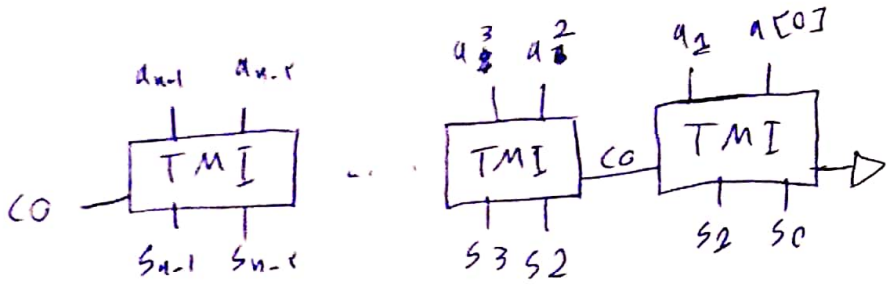
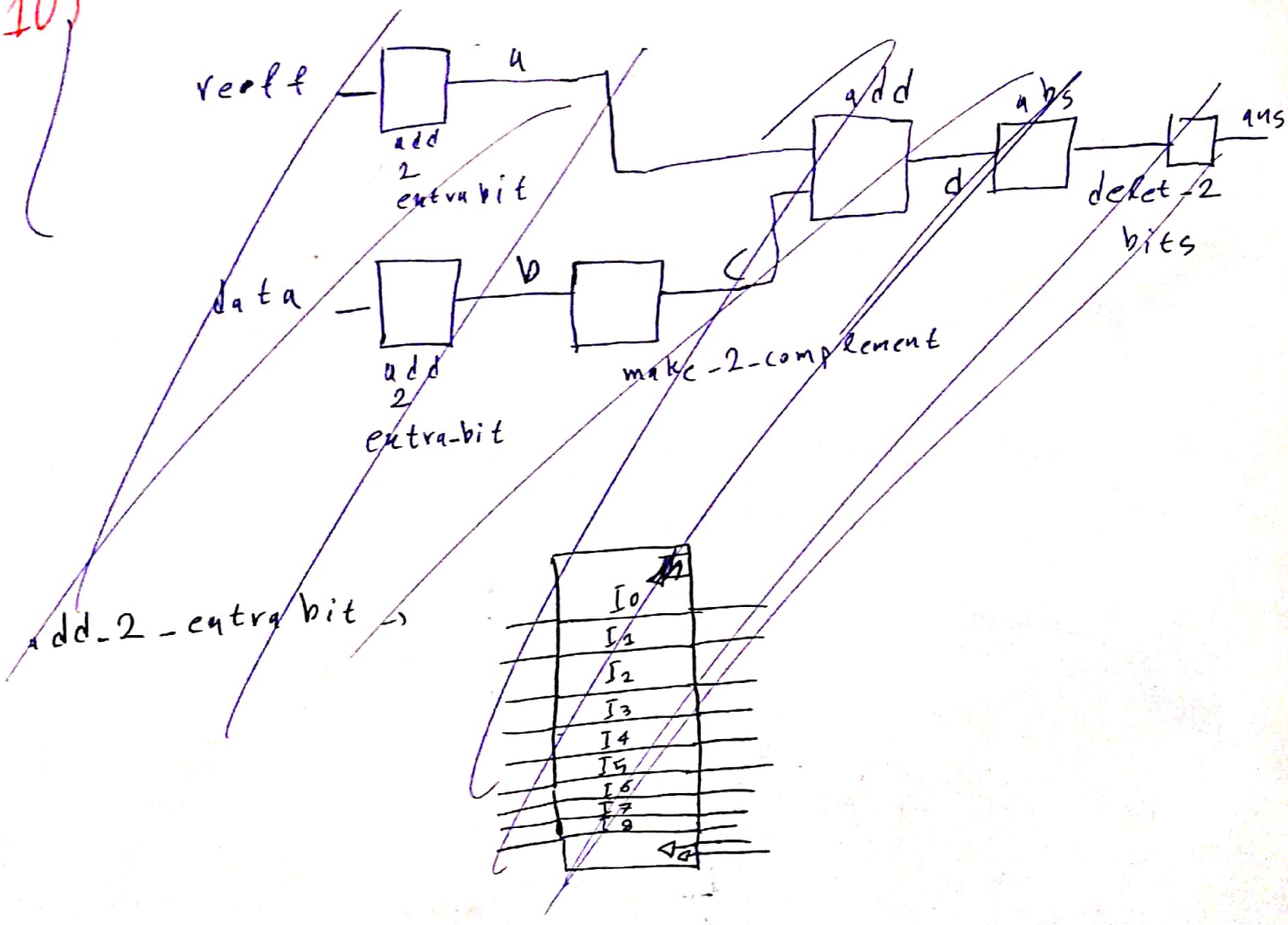


10)



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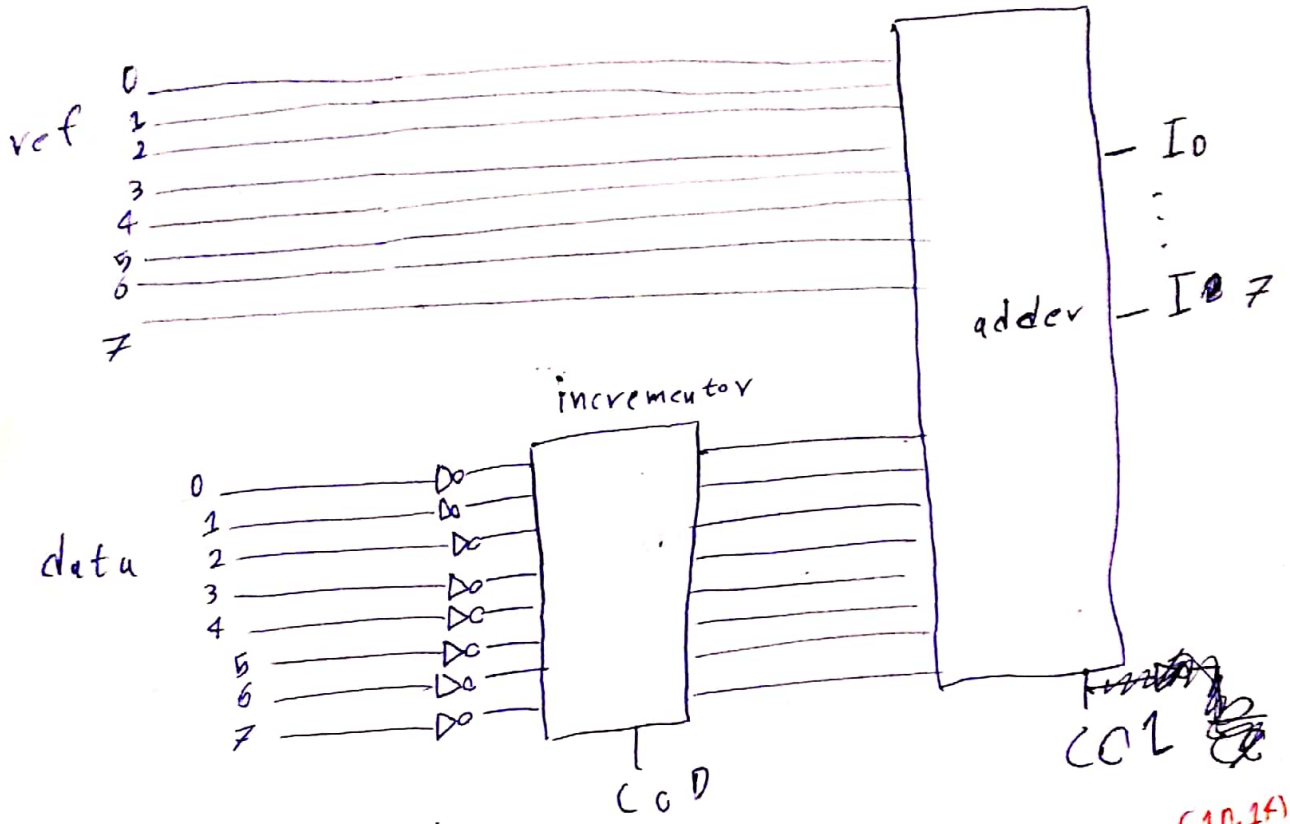
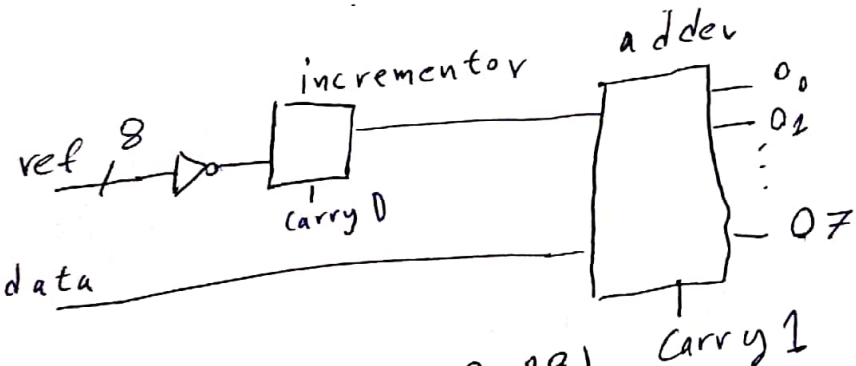
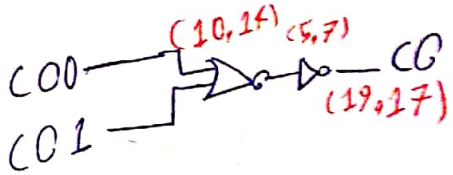
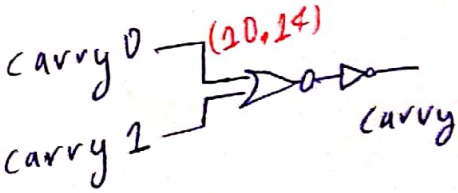
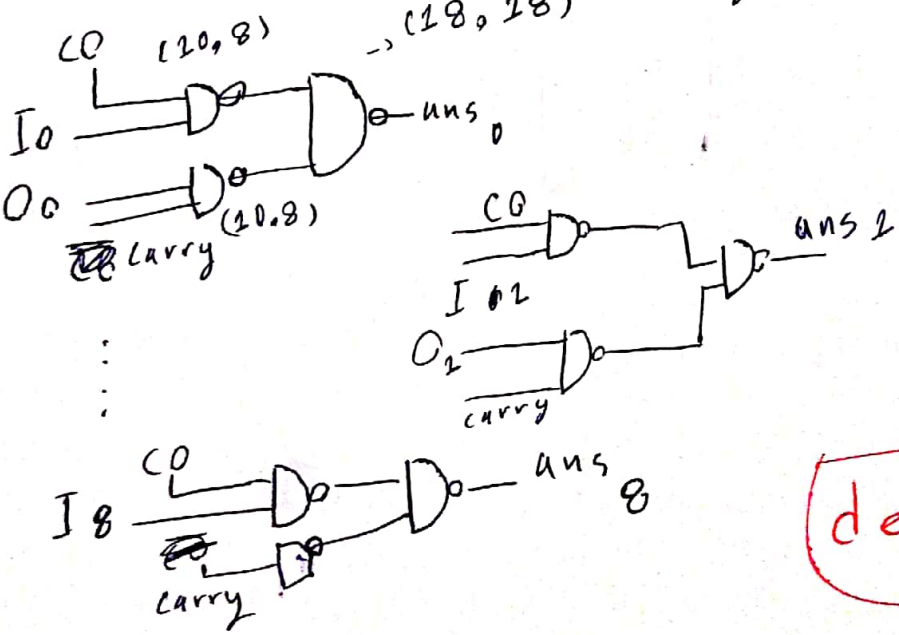






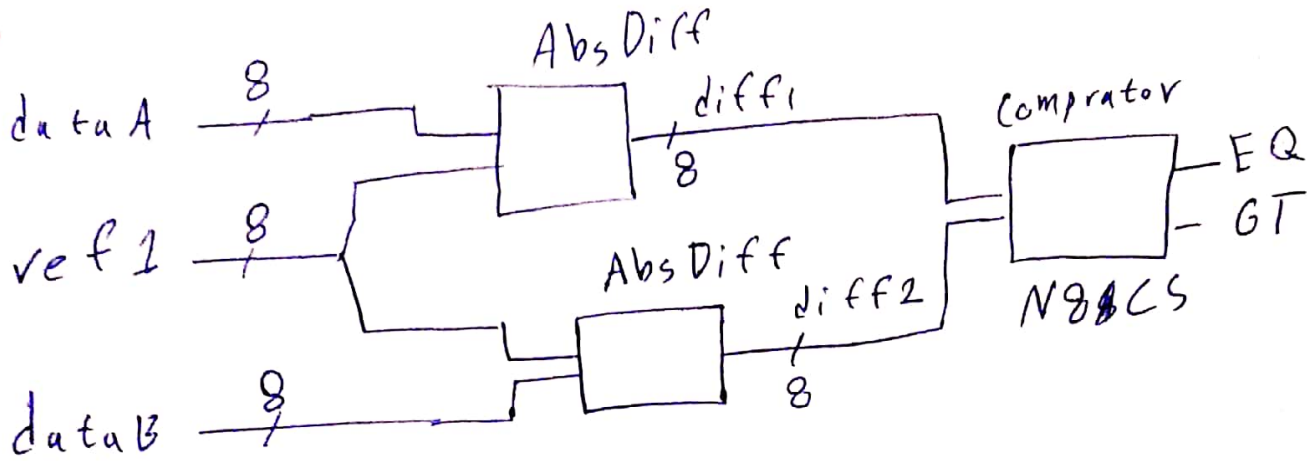


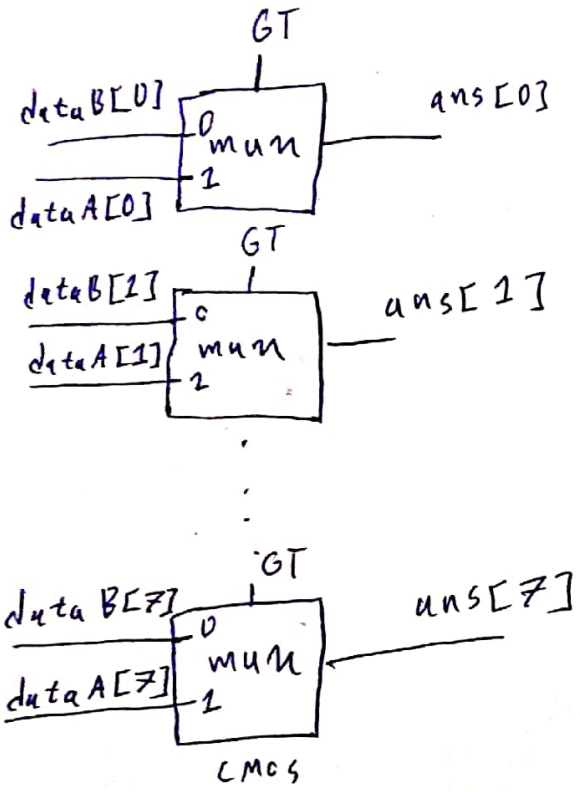


delay 459

Moein Karami 810198540

1.





delay = 737