Moein Ghaniyoun

Curriculum Vitæ

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Summary

I am fourth year Computer Science PhD student at OSU Computer Architecture Research Lab working on Computer Architecture, Performance Modeling, Hardware Security, and Trusted Execution Environments. Currently, I am more focused on pre-silicon validation of hardware designs using fuzzing techniques.

Education

2019–Present **Ph.D**, *The Ohio State University*, Columbus, OH, United States, Computer Science and Engineering,
GPA: 3.95 The Computer Architecture Research Lab.
Coursework: Advanced Computer Architecture, Machine Learning, Neural Networks, Network Security, Network Programming, System Security, Software Security, Hardware Security
Advisor: Radu Teodorescu

2014–2019 **B.Sc.**, *Shahid Beheshti University*, Tehran, Iran
Computer Science and Engineering (Computer Systems Architecture)

2007–2014 **Physics and Mathematics Diploma**, *Shahid Beheshti High School (Administered by National Organization for Development of Exceptional Talents (NODET))*

Publications

Jun-2023 **TEESec: Pre-Silicon Vulnerability Discovery for Trusted Execution Environments**,
50th IEEE/ACM International Symposium on Computer Architecture (**ISCA**)
Moein Ghaniyoun, Kristin Barber, Yuan Xiao , Yinqian Zhang, Radu Teodorescu

Jan-2022 **A Pre-Silicon Approach to Discovering Microarchitectural Vulnerabilities in Security Critical Applications**, IEEE Computer Architecture Letters (**CAL**)
Kristin Barber, **Moein Ghaniyoun**, Yinqian Zhang, Radu Teodorescu

Jun-2021 **IntroSpectre: A Pre-Silicon Framework for Discovery and Analysis of Transient Execution Vulnerabilities**, 48th IEEE/ACM International Symposium on Computer Architecture (**ISCA**),
Acceptance Rate: %18
Moein Ghaniyoun, Kristin Barber, Yinqian Zhang, Radu Teodorescu

Professional Experiences

Summer 2023 **Hardware Verification Intern (Security Team)** at **Rivos Inc.** Mountain View, CA

Summer 2022 **Research Intern (SW Group)** at **Rivos Inc.** Mountain View, CA
- Performance modeling of defenses against transient execution attacks on gem5 model and Chisel HDL
- Research on comprehensive mitigations to fully address all Spectre attacks

2019-Present **Graduate Researcher** at **The Computer Architecture Research Lab** Columbus, OH
- Developed a novel guided fuzzing approach to identify speculative execution vulnerabilities
- Developed a framework to analyze security implications of microarchitectural performance optimizations
- Designed a hardware verification framework to verify security guarantees of the TEE using fuzz testing and RTL profiling

Sep 2018-19 **Hardware Design Team Senior Member** at **Shahid Beheshti University** Tehran, Iran
- Founded and organized a High Level Synthesis Workshop (LegUp and intelHLS)
- Implemented an arrhythmia detector algorithm by ECG signal processing on MAX10 FPGA

Aug 2017-18 **FPGA Engineer Intern** at **Novin Tarasheh Alborz** Tehran, Iran

- Designed and implemented a sound source localization system using a microphone array on MAX10 NEEK FPGA using intelHLS and LegUp

Projects

Selected Academic Projects

OSU-SpecShield

Implemented a defense scheme to mitigate all current and future transient execution attacks on RISCV BOOM RTL (Chisel, Verilog)

OSU-RISC Fuzzer

Develop a RISC-V assembly instruction fuzzer with a novel feedback driven mechanism to target transient execution vulnerabilites (Python)

OSU-Quandary Interpreter, *Programming Languages*

Develop an interpreter for Quandary language with the support of garbage collection, memory management and deadlock-free multi-threading (Java)

OSU-Constant-time Code Breaker, *Network Security*

Investigate micro-architectural optimizations that may break constant-time crypto algorithms (RISC-V, Cryptography)

SBU-Encoder, *Hardware Modeling using VHDL*

An encoder system based on AES-128 bit algorithm to cipher flash memory data
(FPGA, VHDL, Cryptography, C)

SBU-Vowel Detector, *Digital Signal Processing*

Designing and implementing a system that detects vowels in a voice and prints the results on a LCD
(Arduino, AVR, Signal Processing)

SBU-Processor, *Computer Architecture Lab*

An 8 bit, 5 stage pipelined micro-processor
(Verilog)

Selected Projects

Real-Time Edge Detector

Performing Sobel Filter on a camera that is connected to a FPGA
(Verilog, LegUP HLS)

ECG Arrhythmia Detector

Designing and implementing a bio medical signal processing system which can diagnose heart arrhythmia
(Verilog)

Ball tachometer, *Cyrus Small Size Robotic Team*

Measuring speed of the incoming ball using ultra sonic sensors
(ARM, Sensor Fusion)

Computer skills

Programming Languages, x86/ARM/RISC-V Assembly, C/C++, Java, Scala, Python, Rust, Bash Scripting

Hardware Design, Chisel, SystemVerilog/Verilog, VHDL

Security Analysis (CTF Tools), GDB, RE/VR Tools, Ghidra, Angr, PIN, Valgrind, pwntools, Binary Ninja, Wireshark

Fuzzing and Taint Analysis, AFL, libdft, Z3

Simulation and Design Software, Verilator, gem5, MATLAB Simulink, Proteus, Quartus, ISE Modelsim, Atmel Studio, Keil MicroVision IDE, Mars

High Level Synthesis, *LegUP*, intelHLS

Parallel Programming, *OpenCL*, CUDA