Moein Ghaniyoun

Curriculum Vitæ

Baker Systems Engineering, 1971 Neil Ave, Columbus, OH 43210
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Education

2019–Present **Ph.D**, *The Ohio State University*, Columbus, OH, United States, Computer Science and Engineering, GPA: 3.90.
Advisor: Radu Teodorescu

2014–2019 **B.Sc.**, *Shahid Beheshti University*, Tehran, Iran.
Computer Engineering (Computer Systems Architecture), Last two years GPA: 17.49/20 (3.78 out of 4)

2007–2014 **Physics and mathematics Diploma**, *Shahid Beheshti High School (Administered by National Organization for Development of Exceptional Talents (NODET))*.
Overall GPA of: 19.37/20

Publications

2021 **IntroSpectre: A Pre-Silicon Framework for Discovery and Analysis of Transient Execution Vulnerabilities**, 48th IEEE/ACM International Symposium on Computer Architecture (**ISCA**), Acceptance Rate: %18.
Moein Ghaniyoun, Kristin Barber, Yinqian Zhang, Radu Teodorescu

2021 **A Pre-Silicon Approach to Discovering Microarchitectural Vulnerabilities in Security Critical Applications**, Submitted to IEEE Computer Architecture Letters (**CAL**).
Kristin Barber, **Moein Ghaniyoun**, Yinqian Zhang, Radu Teodorescu

Research Interests

Computer Architecture

System Security

Cloud Security

Trusted Execution Environments

FPGAs and Reconfigurable Computing

Fuzz Testing Software/Hardware

Professional Experiences

Fall 2019-Present Graduate Research Assistant at The Architecture Research Lab, *The Ohio State University, Columbus, OH*

Fall 2018 Established High Level Synthesis Workshop (LegUp and intelHLS), *Shahid Beheshti University, Tehran, Iran*

2018-2019 Hardware Design Team senior member, *Shahid Beheshti University, Tehran, Iran*

2017 Hardware Design Intern, on the project of ECG signal processing, *Novin Tarasheh Alborz,Tehran, Iran*

B.Sc. thesis

Design and implement a sound source localization system using a microphone array on MAX10 FPGA

Description Designing a sound source localization system using 4 microphones which are placed in a square shape panel. Signal processing part is done by MAX10 NEEK platform using LegUP High Level Synthesis (HLS) tool and intelHLS. All microphones are sampled at 100KHz using MAX10 ADC and this data is processed to determine difference among Time of Arrivals (ToA) that comes handy to calculate exact position of the sound source.

Projects

Selected Academic Projects

OSU-RISC Fuzzer.
Develop a RISC-V assembly instruction fuzzer with a novel feedback driven mechanism to target transient execution vulnerabilites
(Python)

OSU-Quandary Interpreter, *Programming Languages*.
Develop an interpreter for Quandary language with the support of garbage collection, memory management and deadlock-free multi-threading
(Java)

SBU-Home Management System, *Embedded Real-Time Systems*.
Design and implement master and slave nodes based on Arduino Uno boards using RS485 bus to control home appliances. C code was generated by MATLAB Simulink model-based design
(Simulink, AVR)

SBU-Wireless Network Player, *Computer Networks*.
A Network based music player which up to 10 devices can connect and play the same song
(Java, Multi threaded)

SBU-Encoder, *Hardware Modeling using VHDL*.
An encoder system based on AES-128 bit algorithm to cipher flash memory data
(FPGA, VHDL, Cryptography, C)

SBU-Vowel Detector, *Digital Signal Processing*.
Designing and implementing a system that detects vowels in a voice and prints the results on a LCD
(Arduino, AVR, Signal Processing)

SBU-Processor, *Computer Architecture Lab*.
An 8 bit, 5 stage pipelined micro-processor
(Verilog)

Selected Projects

Real-Time Edge Detector.
Performing Sobel Filter on a camera that is connected to a FPGA
(Verilog, LegUP HLS)

ECG Arrhythmia Detector.
Designing and implementing a bio medical signal processing system which can diagnose heart arrhythmia
(Verilog)

Ball tachometer, *Cyrus Small Size Robotic Team*.
Measuring speed of the incoming ball using ultra sonic sensors
(ARM, Sensor Fusion)

Computer skills

Programming Languages, x86/ARM/MIPS & RISCV64 Assembly, C/C++, Java, Scala, Python, Bash Scripting.

Hardware Design, Chisel, Verilog, VHDL.

Security Analysis, GDB, Ghidra, Angr, PIN, Valgrind, pwntools, IDA Pro.

Fuzzing and Taint Analysis, AFL, libdft, Z3.

Simulation and Design Software, Verilator, MATLAB Simulink, Proteus, Quartus, ISE Modelsim, Atmel Studio, Keil MicroVision IDE, Mars.

High Level Synthesis, *LegUP*, intelHLS.

Parallel Programming, *OpenCL*, CUDA.