

[nRF52 Series](#) > [nRF52832](#) > [nRF52832 Product Specification](#)

Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from [Reference layout nRF52 Series](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html) [<http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html>](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html).

Schematic QFAA and QFAB QFN48 with internal LDO setup

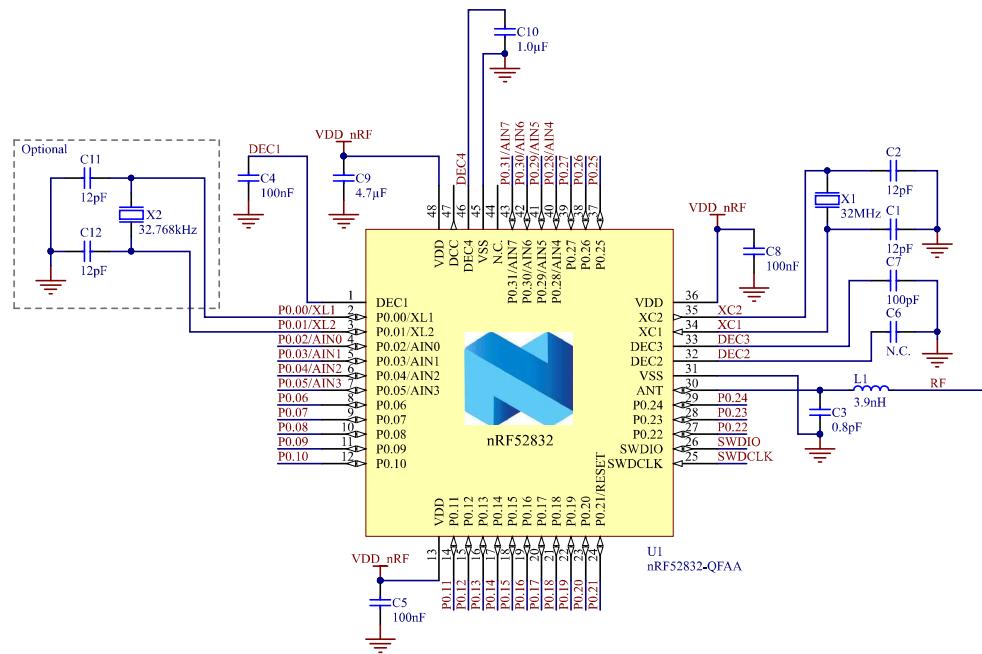


Figure 1. QFAA and QFAB QFN48 with internal LDO setup

For PCB reference layouts, see [Reference layout nRF52 Series](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html) [<http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html>](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html).

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, $\pm 2\%$	0402
C3	0.8 pF	Capacitor, NPO, $\pm 5\%$	0402
C4, C5, C8	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, $\pm 5\%$	0402
C9	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C10	1.0 μ F	Capacitor, X7R, $\pm 10\%$	0603
L1	3.9 nH	High frequency chip inductor $\pm 5\%$	0402
U1	nRF52832-QFAA and nRF52832-QFAB	Multi-protocol <i>Bluetooth</i> low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, Cl=9 pF, total tol. ± 50 ppm	XTAL_3215

Table 1. Bill of material for QFAA and QFAB QFN48 with internal LDO setup

Schematic QFAA and QFAB QFN48 with DC/DC regulator setup

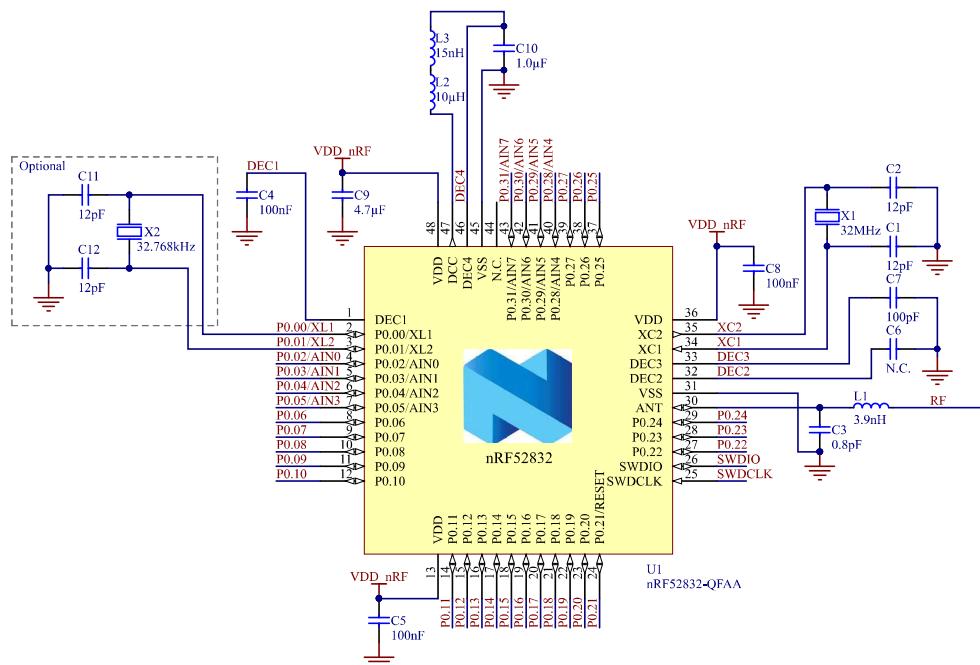


Figure 2. QFAA and QFAB QFN48 with DC/DC regulator setup

For PCB reference layouts, see **Reference layout nRF52 Series**

http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html.

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, $\pm 2\%$	0402
C3	0.8 pF	Capacitor, NPO, $\pm 5\%$	0402
C4, C5, C8	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, $\pm 5\%$	0402
C9	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C10	1.0 μ F	Capacitor, X7R, $\pm 10\%$	0603
L1	3.9 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 μ H	Chip inductor, IDC,min = 50 mA, $\pm 20\%$	0603
L3	15 nH	High frequency chip inductor $\pm 10\%$	0402
U1	nRF52832-QFAA and nRF52832-QFAB	Multi-protocol <i>Bluetooth</i> low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, Cl=9 pF, total tol. ± 50 ppm	XTAL_3215

Table 2. Bill of material for QFAA and QFAB QFN48 with DC/DC regulator setup

Schematic QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

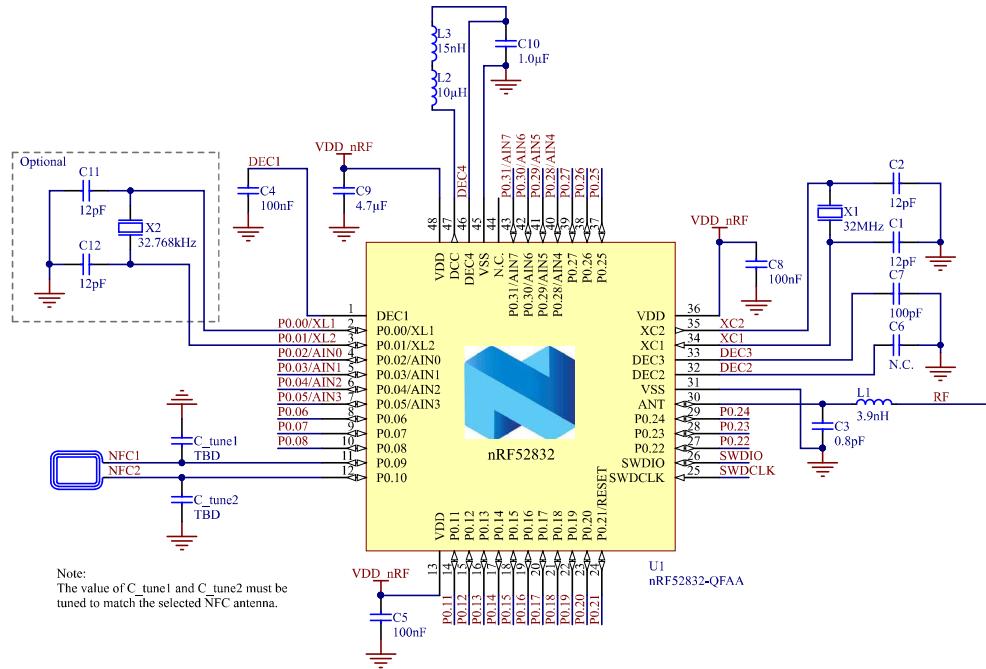


Figure 3. QFAA and QFAB QFN48 with DC/DC regulator and NFC setup

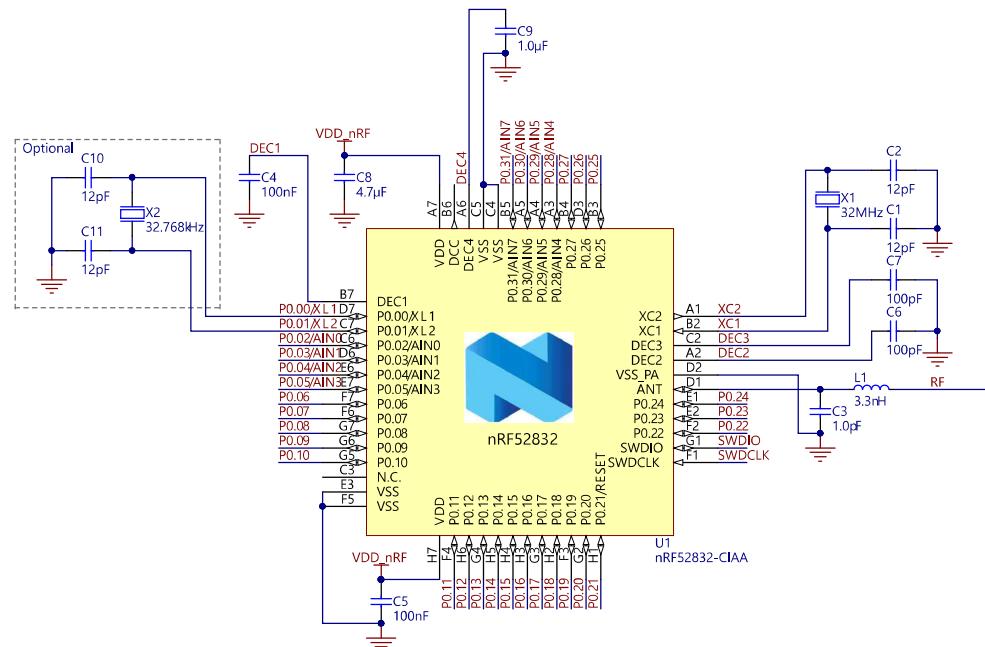
For PCB reference layouts, see [Reference layout nRF52 Series](#)

http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html

Designator	Value	Description	Footprint
C1, C2, C11, C12	12 pF	Capacitor, NPO, $\pm 2\%$	0402
C3	0.8 pF	Capacitor, NPO, $\pm 5\%$	0402
C4, C5, C8	100 nF	Capacitor, X7R, $\pm 10\%$	0402
C6	N.C.	Not mounted	0402
C7	100 pF	Capacitor, NPO, $\pm 5\%$	0402
C9	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C10	1.0 μ F	Capacitor, X7R, $\pm 10\%$	0603
C _{tune1} , C _{tune2}	TBD pF	Capacitor, NPO, $\pm 5\%$	0402
L1	3.9 nH	High frequency chip inductor $\pm 5\%$	0402
L2	10 μ H	Chip inductor, IDC,min = 50 mA, $\pm 20\%$	0603
L3	15 nH	High frequency chip inductor $\pm 10\%$	0402
U1	nRF52832-QFAA and nRF52832-QFAB	Multi-protocol <i>Bluetooth</i> low energy, ANT, and 2.4 GHz proprietary system on chip	QFN-48
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 3215, 32.768 kHz, Cl=9 pF, ± 50 ppm	XTAL_3215

Table 3. Bill of material for QFAA and QFAB QFN48 with DC/DC converter and NFC setup

Schematic CIAA WLCSP with internal LDO setup



For PCB reference layouts, see **Reference layout nRF52 Series**
http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html.

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4, C5	100 nF	Capacitor, X7R, $\pm 10\%$	0201
C6, C7	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C8	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C9	1.0 μ F	Capacitor, X5R, $\pm 5\%$	0402
L1	3.3 nH	High frequency chip inductor $\pm 5\%$	0201
U1	nRF52832-CIAA	Multi-protocol Bluetooth low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, total tol. ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, Cl=9 pF, ± 50 ppm	XTAL_2012

Table 4. Bill of material for CIAA WLCSP with internal LDO setup

Schematic CIAA WLCSP with DC/DC regulator setup

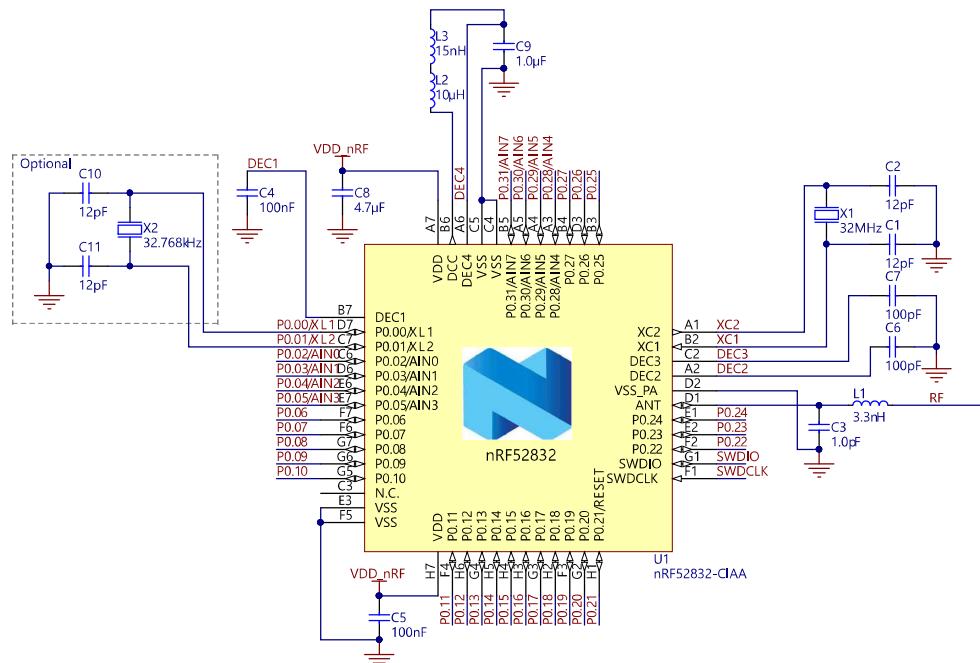


Figure 5. CIAA WLCSP with DC/DC regulator setup

For PCB reference layouts, see [Reference layout nRF52 Series](#)
http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html.

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4, C5	100 nF	Capacitor, X7R, $\pm 10\%$	0201
C6, C7	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C8	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C9	1.0 μ F	Capacitor, X5R, $\pm 5\%$	0402
L1	3.3 nH	High frequency chip inductor $\pm 5\%$	0201
L2	10 μ H	Chip inductor, IDC,min = 50 mA, $\pm 20\%$	0603
L3	15 nH	High frequency chip inductor $\pm 10\%$	0402
U1	nRF52832-CIAA	Multi-protocol <i>Bluetooth</i> low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, Cl=9 pF, ± 50 ppm	XTAL_2012

Table 5. Bill of material for CIAA WLCSP with DC/DC regulator setup

Schematic CIAA WLCSP with DC/DC regulator and NFC setup

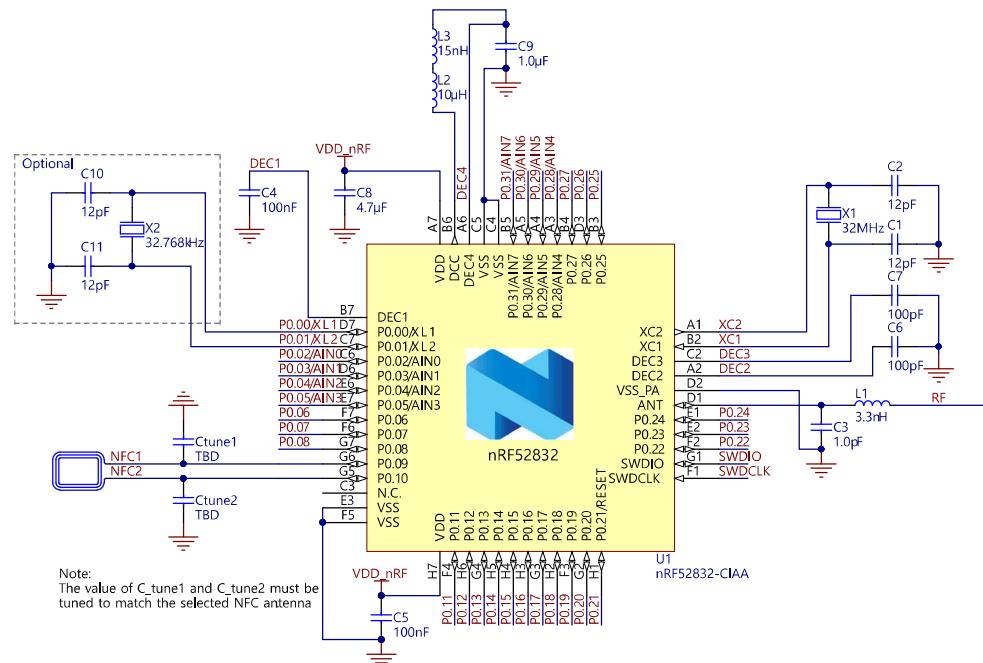


Figure 6. CIAA WLCSP with DC/DC regulator and NFC setup

For PCB reference layouts, see [Reference layout nRF52 Series](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html)
[<http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html>](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html).

Designator	Value	Description	Footprint
C1, C2, C10, C11	12 pF	Capacitor, NPO, $\pm 2\%$	0201
C3	1.0 pF	Capacitor, NPO, $\pm 5\%$	0201
C4, C5	100 nF	Capacitor, X7R, $\pm 10\%$	0201
C6, C7	100 pF	Capacitor, NPO, $\pm 5\%$	0201
C8	4.7 μ F	Capacitor, X5R, $\pm 10\%$	0603
C9	1.0 μ F	Capacitor, X5R, $\pm 5\%$	0402
C_{tune1}, C_{tune2}	TBD pF	Capacitor, NPO, $\pm 5\%$	0201
L1	3.3 nH	High frequency chip inductor $\pm 5\%$	0201
L2	10 μ H	Chip inductor, IDC,min = 50 mA, $\pm 20\%$	0603
L3	15 nH	High frequency chip inductor $\pm 10\%$	0402
U1	nRF52832-CIAA	Multi-protocol <i>Bluetooth</i> low energy, ANT, and 2.4 GHz proprietary system on chip	WLCSP_C50
X1	32 MHz	XTAL SMD 2016, 32 MHz, Cl=8 pF, Total Tol: ± 40 ppm	XTAL_2016
X2	32.768 kHz	XTAL SMD 2012, 32.768 kHz, Cl=9 pF, ± 50 ppm	XTAL_2012

Table 6. Bill of material for CIAA WLCSP with DC/DC converter and NFC setup

PCB guidelines

A well-designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality.

A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from [Reference layout nRF52 Series](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html)
[<http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html>](http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html).

To ensure optimal performance, it is essential that you follow the schematics and layout references closely. Especially in the case of the antenna matching circuitry (components between device pin ANT and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pin ANT and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the RF pin ANT and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in the recommended package reference circuitry in [Reference circuitry](#) above.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Fast switching digital signals should not be routed close to the crystal or the power supply lines. Capacitive loading of fast switching digital output lines should be minimized in order to avoid radio interference.

PCB layout example

The PCB layout shown below is a reference layout for the QFN package with internal LDO setup.

Important: Pay attention to how the capacitor C3 is grounded. It is not directly connected to the ground plane, but grounded via VSS pin 31. This is done to create additional filtering of harmonic components.

For all available reference layouts, see [Reference layout nRF52 Series](#)
http://infocenter.nordicsemi.com/topic/com.nordic.infocenter.nrf52/dita/nrf52/pdflinks/ref_layout.html.

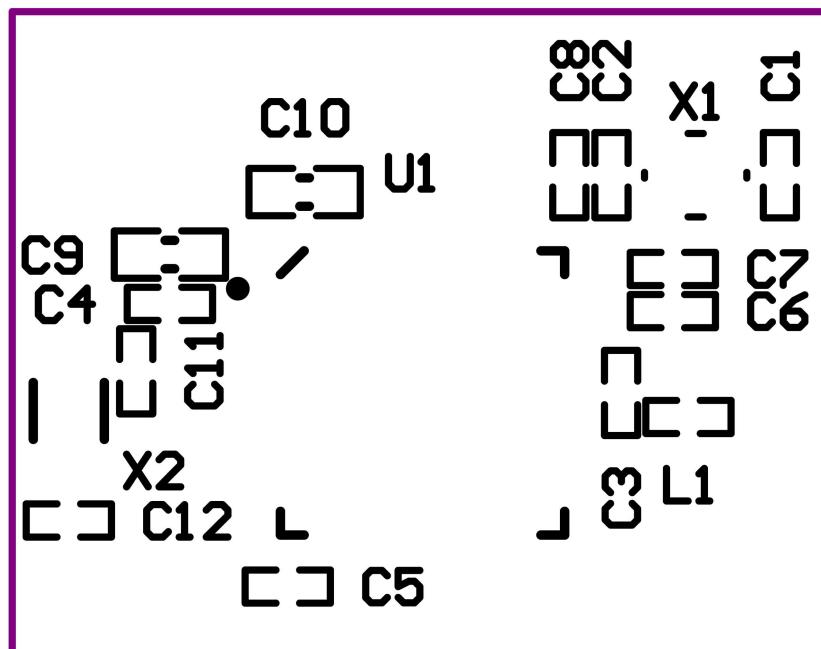


Figure 7. Top silk layer

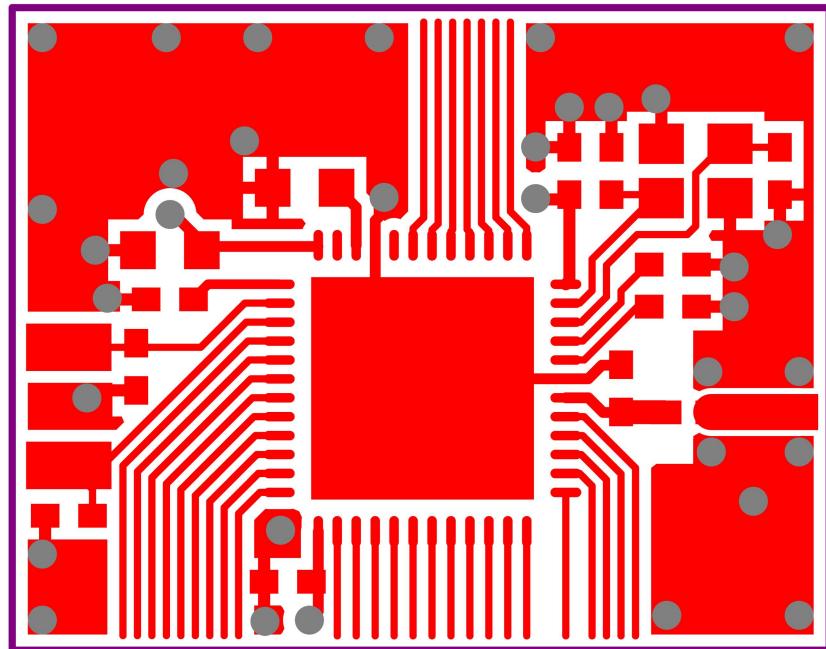


Figure 8. Top layer

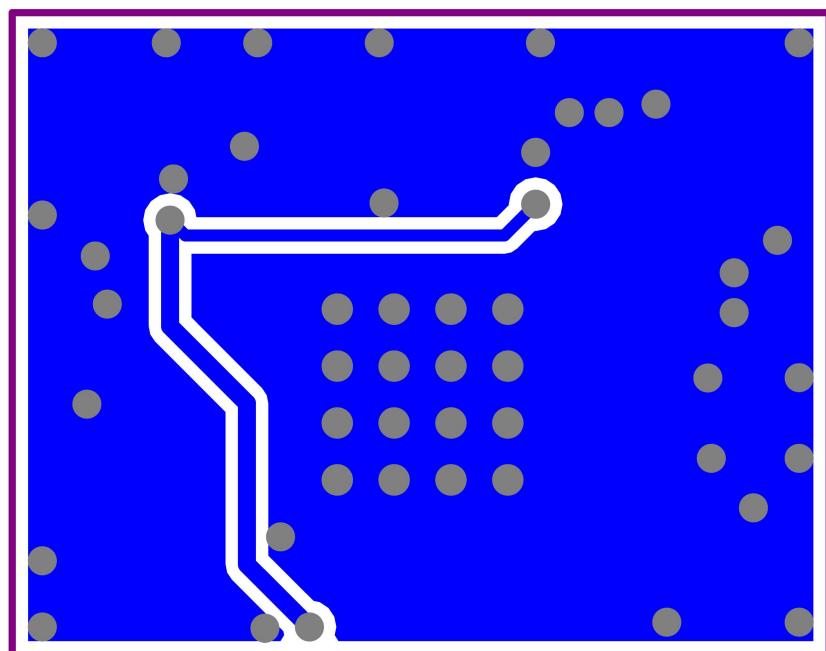


Figure 9. Bottom layer

Important: No components in bottom layer.

[Documentation feedback](#) | [Developer Zone <https://devzone.nordicsemi.com/questions/>](#) | Updated 2021-11-08