VLN1MxxS Series

Up to 30-min Voice IC in SOP-8 / SOP-16

Version 1.40

Nov. 9, 2018

1. GENERAL DESCRIPTION

The VLN1M series is a 32-bit MCU based high-quality speech/MIDI processor, which is specially designed in a SOP-8 / SOP-16 package with SPI Flash stacked inside the MCP. It is embedded with OTP (One Time PROM) for mass production, such that no mask is required while MOQ / Lead Time are kept minimized.

With Instruction / Data Local Memory bus (ILM/DLM) built in CPU, the VLN1M can run 1.57 DMIPS per MHz and up to 50+ DMIPS @ 32MHz. In addition, the dual clock design let customers switch between fast / slow clocks for achieving the best power consumption and performance ratio.

The VLN1M series consists of several derivatives with respect to the memory size of stacked SPI Flash, I/O and package type. With memory-mapped architecture, the VLN1M can address up to 16MB space that includes memory, register files, peripheral and SPI Flash storage (including instruction / data modes). SBC (Sub-Band Coding) is achieved with greatly enhanced quality & much less memory size compared against traditional ADPCM coding due to the incorporation of efficient DSP algorithms as well as the upgrade of H/W spec. Via the high performance of 32-bit MCU, the S/W-based MIDI synthesizer can reach more than 16-ch polyphonic channels. All data including SBC / MIDI files, wavetable timbres, XIP codes and general user data, can be accessed from the SPI Flash stacked inside the MCP.

There are various useful features inside the VLN1M series: Two sets of 16-bit Timers; 14-bit DAC + 1.3-watt Push-Pull power amplifier to drive speaker directly; independently configurable GPIO per pin with alternate functions; IR TX that supports 38KHz / 57KHz / 125KHz / 500KHz carrier for Infrared or QFID applications; SPI0 for the control of the stacked SPI Flash, powered by embedded 3.3V LDO, which supports single/dual/quad I/O mode with XIP (e**X**ecute **I**n **P**lace) capability.

The VLN1M series adopts stacked MCP technology, which integrates SPI Flash into the small SOP-8 / SOP-16 package, to meet various kinds of long-duration synthesis applications.

2. FEATURES

- Wide Operating Voltage: 2.4V ~ 5.5V
  - SPI Flash @ SPI0 powered by embedded 3.3V LDO.
  - Min. operating voltage is 3.0V @ 32MHz maximum CPU clock, and 2.2V @ 12MHz minimum CPU clock.
- 32-bit CPU core
  - Like ARM Cortex-M0+.
  - Max. CPU clock: 32MHz, up to 50+ DMIPS cooperated with zero wait-state high speed OTP.
  - 1-cycle fast multiplier.
- There are bodies in the VLN1M series. The SPI Flash size ranges from 4Mb to 32Mb.

P/N	*RAM*	*OTP*	*I/O*	*Flash (Mb)*	*SPI0*	*16-bit Timer*	*Push-Pull*	*Package*
VLN1M04S8X	4KB	32KB	4	4	v	2	v	SOP-8, 150mil
VLN1M08S8X	4KB	32KB	4	8	v	2	v	SOP-8, 150mil
VLN1M08S16X	4KB	32KB	12	8	v	2	v	SOP-16, 150mil
VLN1M32S8X	4KB	32KB	4	32	v	2	v	SOP-8, 150mil
VLN1M32S16X	4KB	32KB	12	32	v	2	v	SOP-16, 150mil

Table 1 Product Line-Up of VLN1M Series

- Dual Clock Operation. Built-in oscillators for HI_CLK (32MHz) and LO_CLK (32.768KHz), accuracy trimmed to +/-0.5% for HI_CLK and +/-1.5% for LO_CLK.
- Power management to support 4 operating modes: Normal / Slow / Standby / Halt mode. At Halt mode, the consumption current is less than 1uA.
- LVD (Low Voltage Detection): Total 6-level options: 3.6V, 3.4V, 3.2V, 2.6V, 2.4V, 2.2V.
- LVR (Low Voltage Reset): User-configurable, default values are 2.7V @ 32MHz for VLN1, 2.4V @ 24MHz, 2.0V @ 16MHz, 1.8V @ 12MHz.
- Timers (Timer0 / Timer1): Each Timer consists of divider and 16-bit down-counter with various clock sources.
- Built-in 14-bit DAC + 1.3-Watt Push-Pull power amplifier
- Up to 12 pins GPIO. Bit configurability for every I/O pin by register control, except pull-up value by byte.
- SPI master supported to connect with the SPI Flash stacked inside MCP
  - Up to 32MHz clock speed.
  - Support Data mode and XIP mode (eXecute In Place).
  - Support Single / Dual / Quad I/O mode of SPI Flash.
- IR TX supported.
- RTC with 16KHz / 1KHz / 64Hz / 2Hz interrupts.

- WDT (Watch-Dog Timer) supported with optional 188ms / 750ms Reset.
- MCP (Multi-Chip Package)
  - SPI Flash stacked inside SOP-8 / SOP-16 packages
  - Support 4Mb / 8Mb / 16Mb / 32Mb SPI Flash density
  - SPI0 interface bonded inside the package, leaving more GPIO pins available
  - Built-in Push-Pull PA to drive speaker directly
  - Max. GPIO pins: 4 @ SOP-8, 12 @ SOP-16
  - Master or Slave operation
- Support OTP Security Lock to prevent OTP data from being read.
- S/W-based Speech/MIDI Codec & various algorithms
  - ADPCM Codec (Adaptive Differential PCM): 4-bit / 5-bit per sample.
  - SBC Codec (Sub-Band Coding): 7.2K ~ 32Kbps with maximum 16KHz bandwidth.
  - CELP Decoder (Code-Excitation Linear Prediction): 4.8Kbps @ 8KHz SR for human voice only.
  - MIDI: Up to 16-channel MIDI @ 32KHz Output Sample Rate.
- Noise filter @ 4x Up-Sampling.
- Shipping Form
  - Package: SOP-8 / SOP-16 MCP.

3. BLOCK DIAGRAM

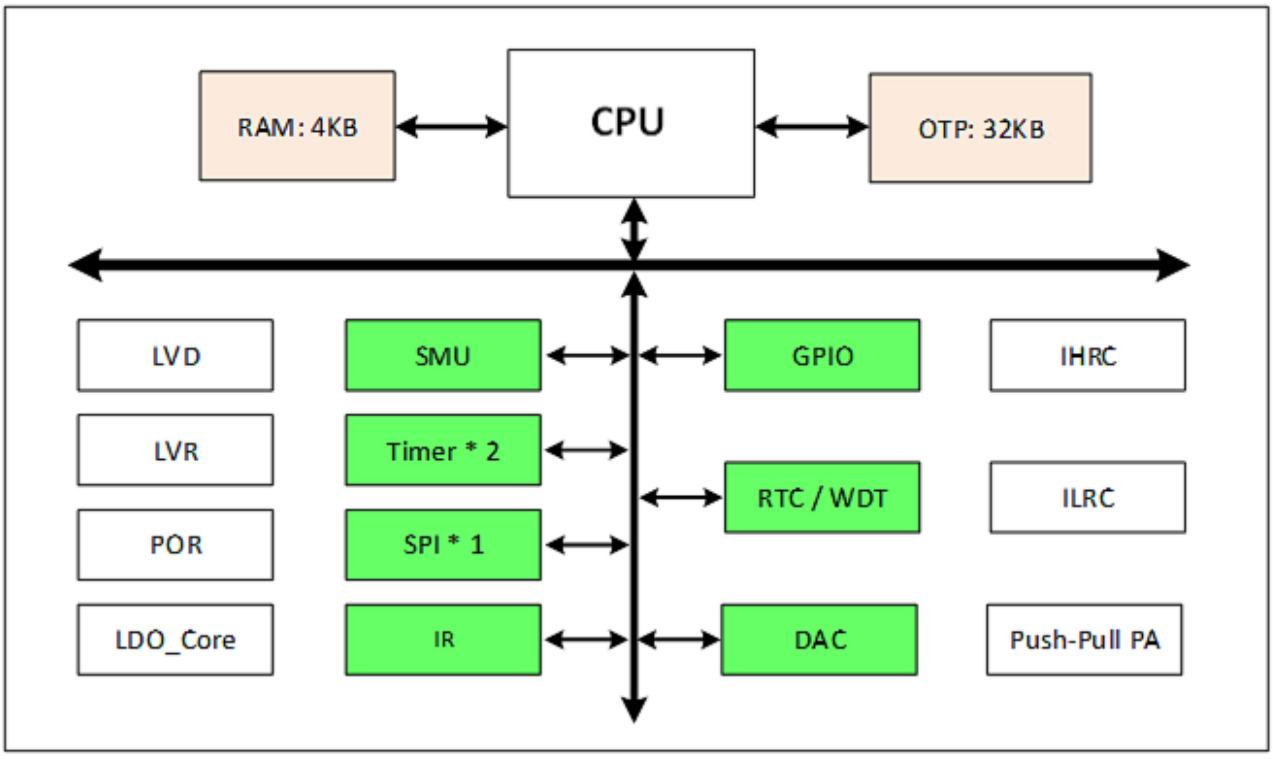


Figure 1 Block Diagram of VLN1M Series

4. PAD DESCRIPTION

Name	ALT 1	Type	Description
Power & Ground			
VDD	-	P, I	Power input
VSS	-	P, I	Ground
PP / DAC			
PP1	DAC0	AO	Push-Pull PA output 1 or DAC0
PP2	-	AO	Push-Pull PA output 2
Port A			
PA0	-	I/O	PA0 or Analog input 0
PA1	-	I/O	PA1 or Analog input 1
PA2		I/O I/P	PA2
PA3	-	I/O	PA3
PA4		I/O, I	PA4
PA5	IR	I/O, O	PA5
PA6	-	I/O, O	PA6
PA7	-	I/O, I	PA7
PA8	-	I/O	PA8
PA9	-	I/O	PA9
PA10	-	I/O	PA10
PA11	-	I/O	PA11

Pad Type: P = Digital Power, I = Digital Input, O = Digital Output, AI = Analog Input, AO = Analog output, AP=Analog Power.

5. CLOCK GENERATOR

The clock generator consists of 2 clock sources:

- Built-in high clock (I_HRC): Output frequency can be 32MHz, 24MHz, 16MHz, or 12MHz by option.
- Built-in low clock (I_LRC): Output frequency is 32,768Hz.

The internal oscillators, I_HRC and I_LRC, are trimmed to achieve +/-0.5% and +/-1.5% accuracy, respectively.

6. PERIPHERALS

6.1 I/O Port

Up to 12 * I/O pins are available, since PB0 ~ PB5 are dedicated to interface with the stacked SPI Flash. These are shared multiple function pins under control of the alternate multiple function registers. These 12 * I/O pins belong to Port A (PA0 ~ PA11).

Each pin can be configured as input or output, weak / strong pull-high resistor and can generate interrupt signal to CPU.

6.2 SPI0

The SPI0 that is dedicated for connecting with the stacked SPI Flash to store most of the data used for various applications like speech (ADPCM, SBC, or CELP), melody (including MIDI file and wavetable timbres), user's general data storage. With single/dual/quad I/O modes supported, the SPI Flash can run up to 32MHz clock. Together with the XIP capability (e**X**ecute **I**n **P**lace), users can extend the program code to the SPI Flash at a descent performance for many applications.

6.7 IR TX

The VLN1M provide a 5-bit IR carrier, it can generate different IR frequency by assign different counter value.

- Support output stop at 0 or 1.
- Support 5 bits reload data to adjust IR's frequency.

7. TIMER

The VLN1M has two 16-bit timers: TIMER0 / TIMER1, which can be used as a trigger source for or as a function of time delay, clock generation, etc.

- Programmable source of timer clock
- 16-bit counter for each timer

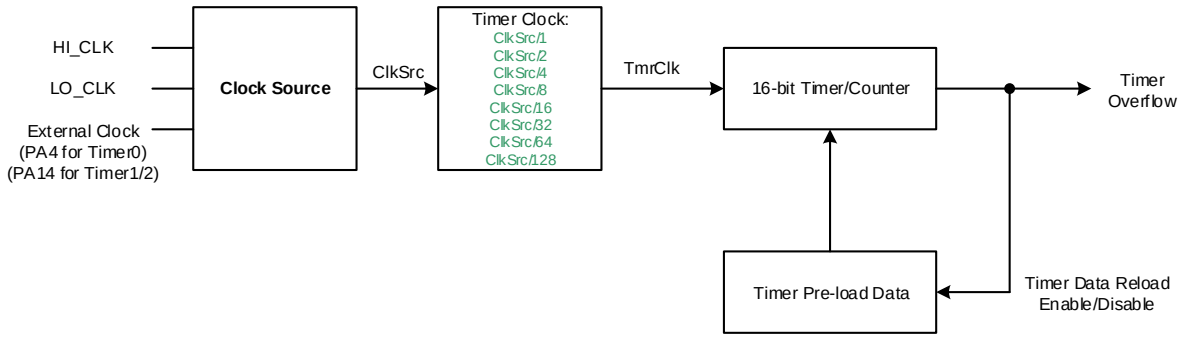


Figure 2 Timer Block Diagram

8. RTC

As the name implies, the RTC (Real-Time Clock) is generally used to keep the time, with the clock source from either an internal built-in I_LRC (trimmed to 32,768Hz with +/-1.5% accuracy), or an external crystal (32,768Hz). The RTC support periodic time tick interrupts with 4 options: 16KHz, 1KHz, 64Hz, 2Hz.

9. WDT

The Watchdog Timer (WDT) is used to perform a system reset when the system is not responding. There are two period options for the WDT to generate a reset: 188ms / 750ms.

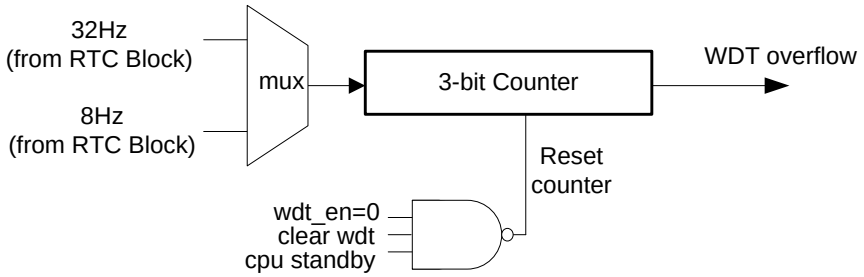


Figure 3 WDT Block Diagram

10. DAC & PP

The VLN1M provides two data buffers with 8-level FIFO each and up to two 14-bit Digital-to-Analog converters (optional) with interpolation function. It can be started by software or TIMER trigger.

- Provide 8-level FIFO per channel data buffer
- Provide hardware up-sampling (interpolation) function
- /Support mixing mode for two-channel data applications

11. LVD

The LVD (Low Voltage Detector) is trimmed to +/-0.1V accuracy for the user to detect the battery voltage @ VDD pin. When the VDD voltage falls below the specified LVD level, the LVD_Flag will be set as HIGH.

LVD_SEL[2:0]	Voltage
111	*Reserved*
110	*Reserved*
101	3.6V
100	3.4V
011	3.2V
010	2.6V
001	2.4V
000	2.2V

Table 2 LVD voltage select

12. OPTIONS

Users may select different options depending on the application requirement. There are several options that users may select for the VLN1M series, as shown in Table 3 User Options.

Item	Name	Options
1	High Oscillation Source	1. I_HRC 2. E_HXT
2	Low Oscillation Source	1. I_LRC 2. E_LXT
3	HI_CLK Frequency	1. 32MHz (Core LDO @ 3.3V) 2. 24MHz (Core LDO @ 2.8V) 3. 16MHz (Core LDO @ 2.5V) 4. 12MHz (Core LDO @ 2.5V)
4	VDD Voltage	1. 4.5V 2. 3.0V
5	SPI0_VDD Voltage	1. 3.3V (fixed for VLN1M series)
6	LVR Voltage	1. 2.9V / 2.8V / 2.7V / 2.6V / 2.5V (HI_CLK @ 32MHz) 2. 2.6V / 2.5V / 2.4V / 2.3V / 2.2V (HI_CLK @ 24MHz) 3. 2.2V / 2.1V / 2.0V / 1.9V / 1.8V (HI_CLK @ 16MHz) 4. 2.0V / 1.9V / 1.8V / 1.7V / 1.6V (HI_CLK @ 12MHz)

Table 3 User Options

13. ELECTRICAL CHARACTERISTICS

13.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
V_{DD} - V_{SS}	Supply voltage	-0.5 ~ +7.5	V
V_{IN}	Input voltage	V_{SS} - 0.3 ~ V_{DD} + 0.3	V
T_{OP}	Operating Temperature	0 ~ +70	°C
T_{ST}	Storage Temperature	-25 ~ +85	°C

13.2 DC Characteristics *(T_A=25ºC, unless otherwise specified)*

Symbol	Parameter		V_{DD}	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage		-	3.0	4.5	5.5	V	CPU_CLK=32MHz
				2.7	4.5	5.5		CPU_CLK=24MHz
				2.2	3.0	5.5		CPU_CLK=16MHz
				2.2	3.0	5.5		CPU_CLK=12MHz
				2.2	3.0	5.5		CPU_CLK=32.768KHz
I_{HALT}	Halt Current		3		0.1		uA	CPU stop, all functions off
			4.5		0.1			
I_{SB}	Standby Current		3		3.5		uA	CPU stop, all functions off, RTC on
			4.5		4.5			
I_{OP}	Operating Current	Slow Mode	3		58.3		uA	CPU_CLK=32.768KHz
			4.5		75			
		Normal Mode	3		6.1		mA	CPU_CLK = 12MHz, Core_LDO = 2.3V
			3		7.5		mA	CPU_CLK = 16MHz, Core_LDO = 2.3V
			4.5		12.0		mA	CPU_CLK = 24MHz, Core_LDO = 2.7V
			4.5		16.1		mA	CPU_CLK = 32MHz, Core_LDO = 3.3V
I_{IL}	Input current (Internal pull-high)	Weak (1MΩ)	3		-2.7		uA	V_{IL} = 0V
			4.5		-7.2			
		Strong (100KΩ)	3		-30			
			4.5		-78			
		SDC pad (20KΩ)	3		-144			
			4.5		-215			

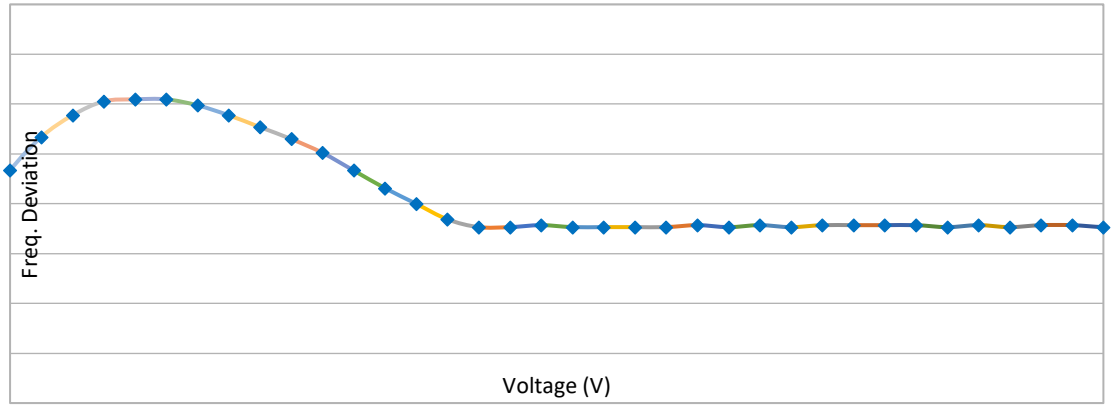
Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Unit	Condition
I_{OH}	Normal drive current (PA)	3		-8.7		mA	V_{OH} = 2.0V
		4.5		-13.7			V_{OH} = 3.5V
	Normal drive current (PB for SPI0)	3		-12.9			V_{OH} = 2.0V
		4.5		-20.2			V_{OH} = 3.5V
	Large drive current (PB for SPI0)	3		-24.8			V_{OH} = 2.0V
		4.5		-38.0			V_{OH} = 3.5V
I_{OL}	Normal sink current	3		12.4		mA	V_{OL} = 1.0V
		4.5		16.2			
	Large sink current	3		24.3			
		4.5		37.1			
ΔF/F	Frequency deviation by voltage drop (I_HRC=32MHz/24MHz)	4.5		-0.5		%	$\frac{Fosc(4.5v) - Fosc(3.3v)}{Fosc(4.5v)}$
	Frequency deviation by voltage drop (I_HRC=16MHz/12MHz)	3		-0.5			$\frac{Fosc(3.0v) - Fosc(2.4v)}{Fosc(3.0v)}$
		4.5		-0.5			$\frac{Fosc(4.5v) - Fosc(3.0v)}{Fosc(4.5v)}$
ΔF/F	Frequency deviation by lot	3	-0.5		0.5	%	$\frac{Fosc(3.0v) - Ftyp(3.0v)}{Ftyp(3.0v)}$

13.3 DAC Characteristics

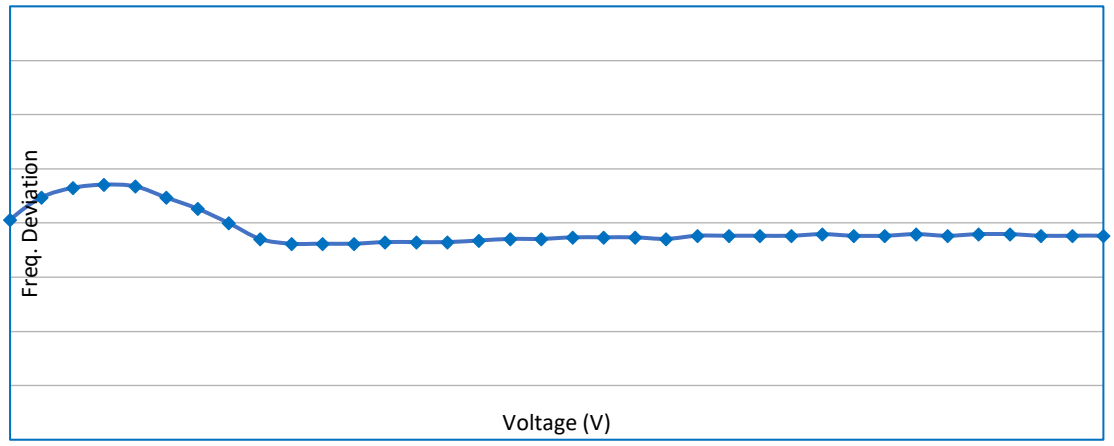
Symbol	Characteristics	Min.	Typ.	Max.	Unit	Condition
B_{RES}	Resolution of DAC			14	Bit	-
DR	Dynamic Range (Vin = -60 dBFS)		-73		dBr A	No Load
SNR	Noise at No Signal (Vin = -90 dBFS)		-97		dBr A	
P_O	THD+N 1%		0.7		W	4Ω Load
	THD+N 10%		1.3		W	

13.4 Voltage vs. Frequency

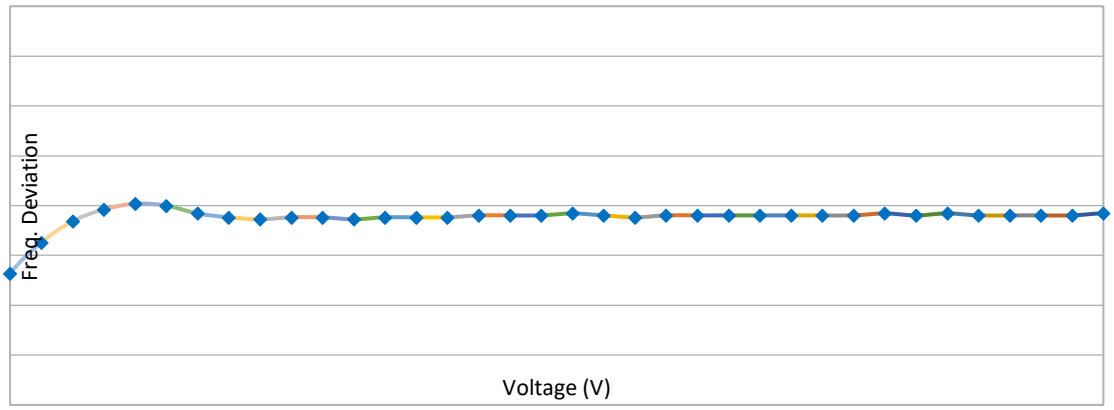
13.4.1 I_HRC @ 32 MHz



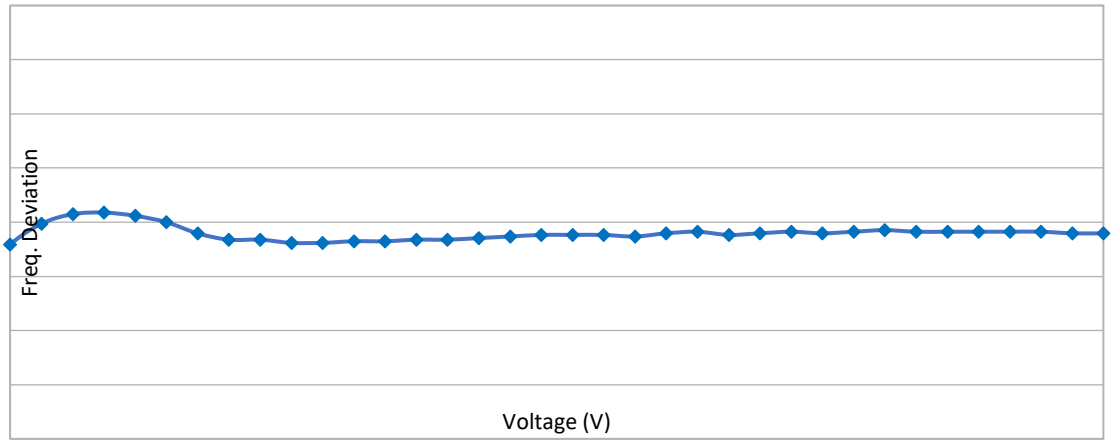
13.4.2 I_HRC @ 24 MHz



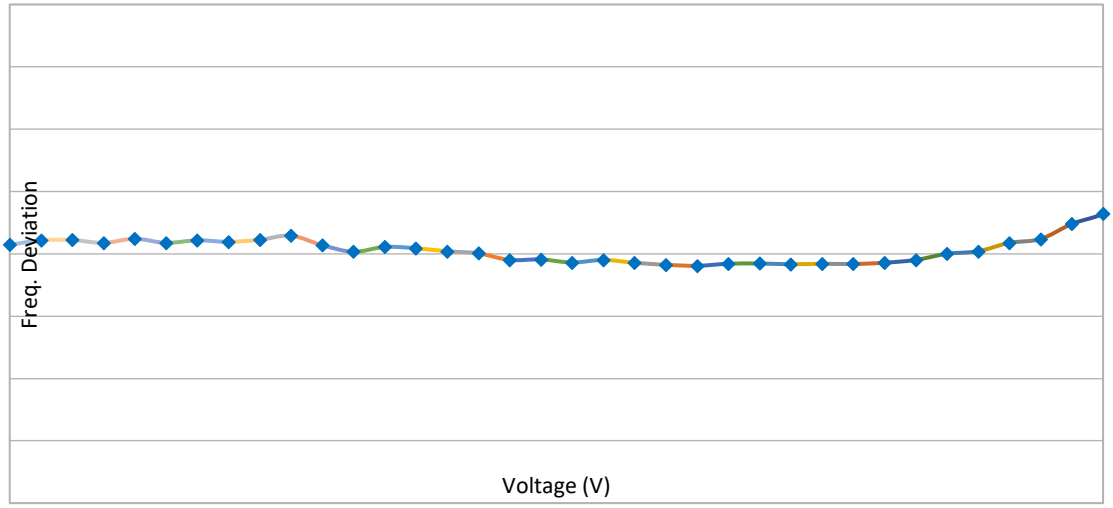
13.4.3 I_HRC @ 16 MHz



13.4.4 I_HRC @ 12 MHz



13.4.5 I_LRC @ 32 KHz



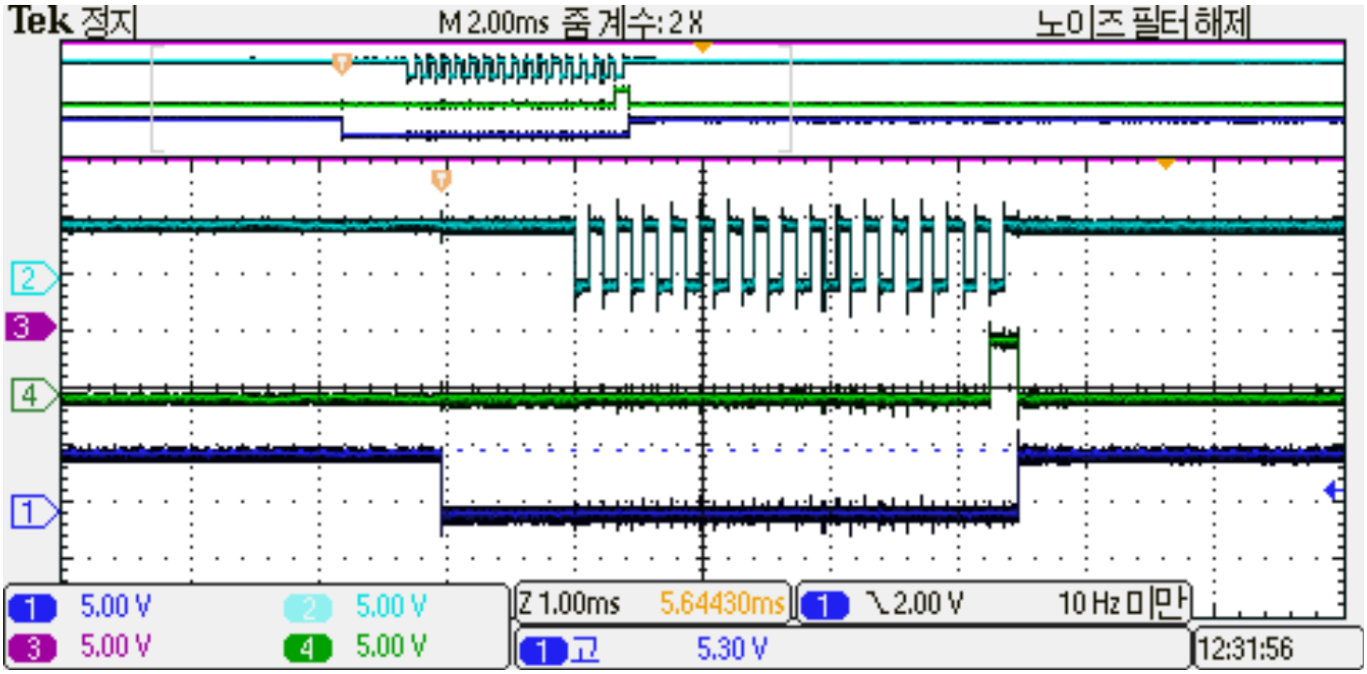
14. SPI Timing Chart

2 Sky color line : Clock PA2 (pin 3 of SOP 8pins type)

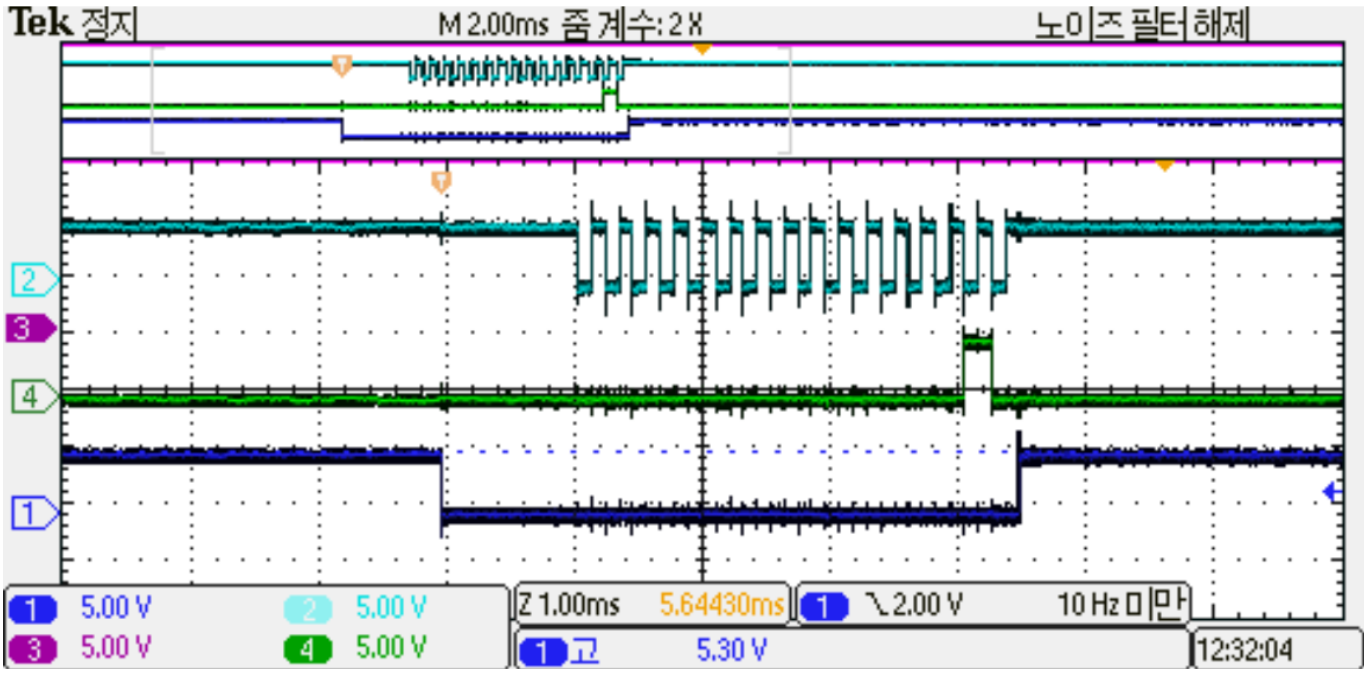
4 Green color line : Data PA3 (pin 4 of SOP 8pins type)

1 Blue color line : Enable PA4 (pin 5 of SOP 8pins type)

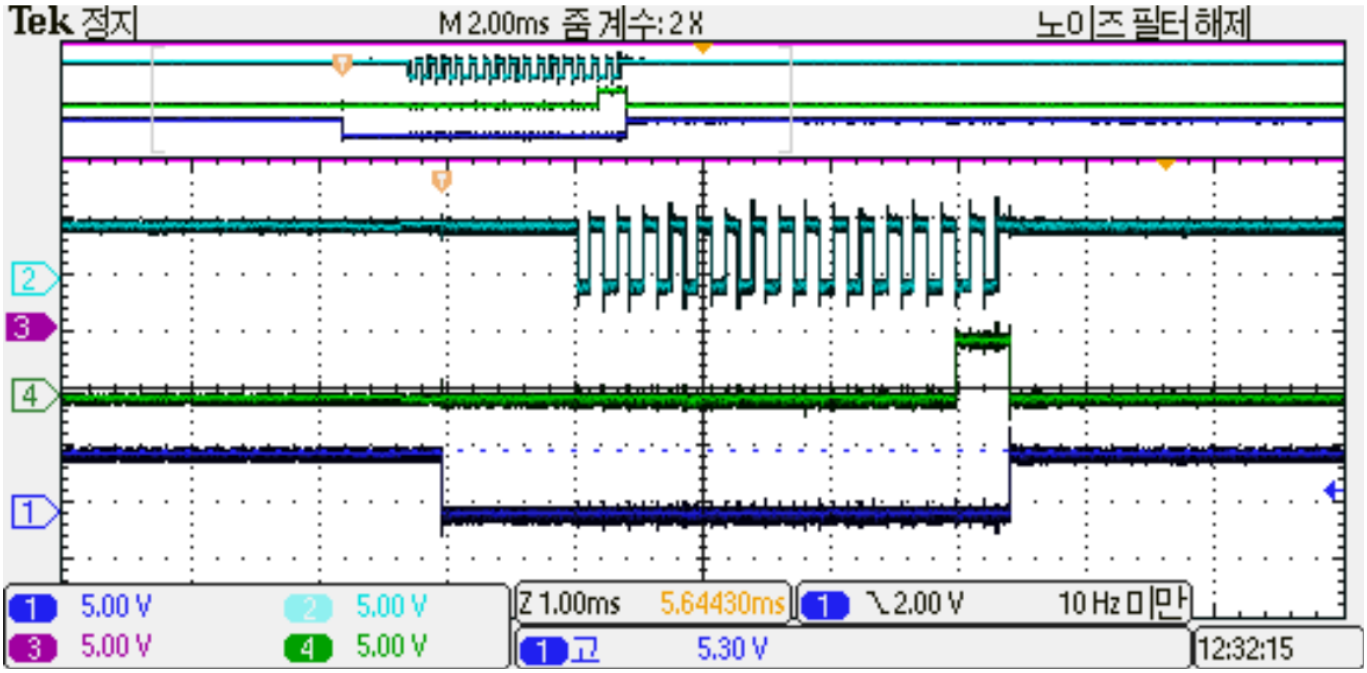
Code 1:



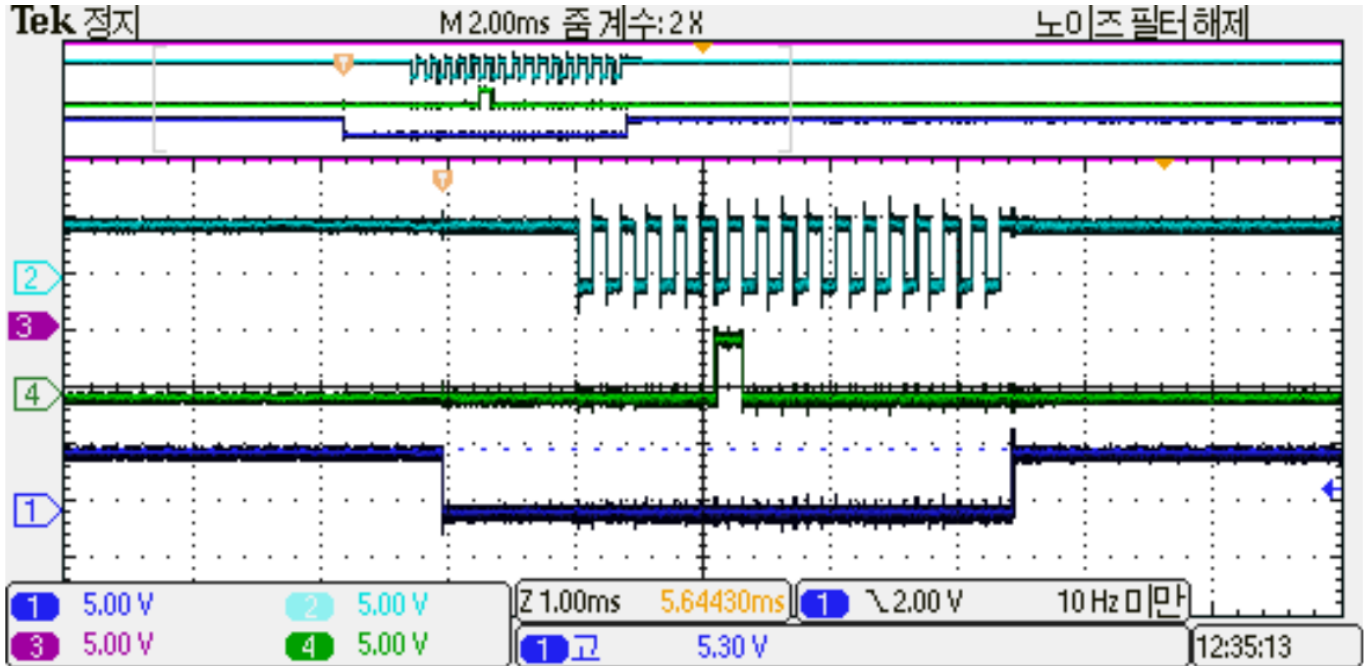
Code 2:



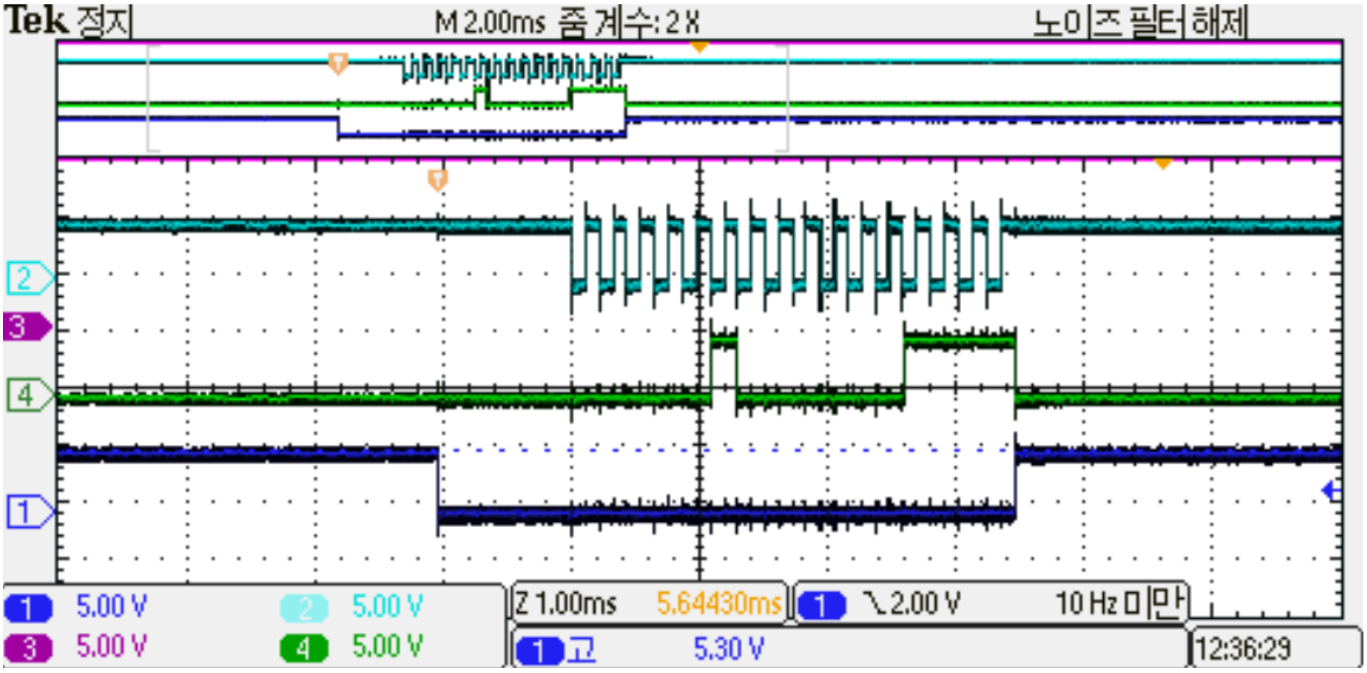
Code 3:



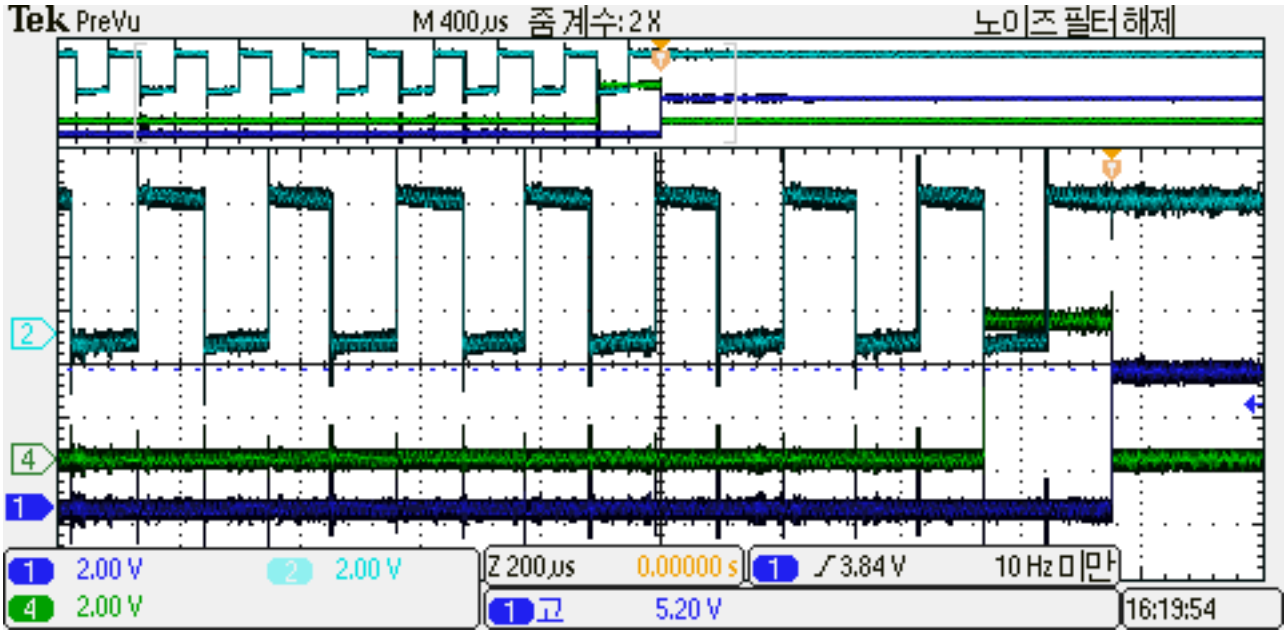
Code 1024 = Volume 1 (Min.):



Code 1039 = Volume 16 (Max.):



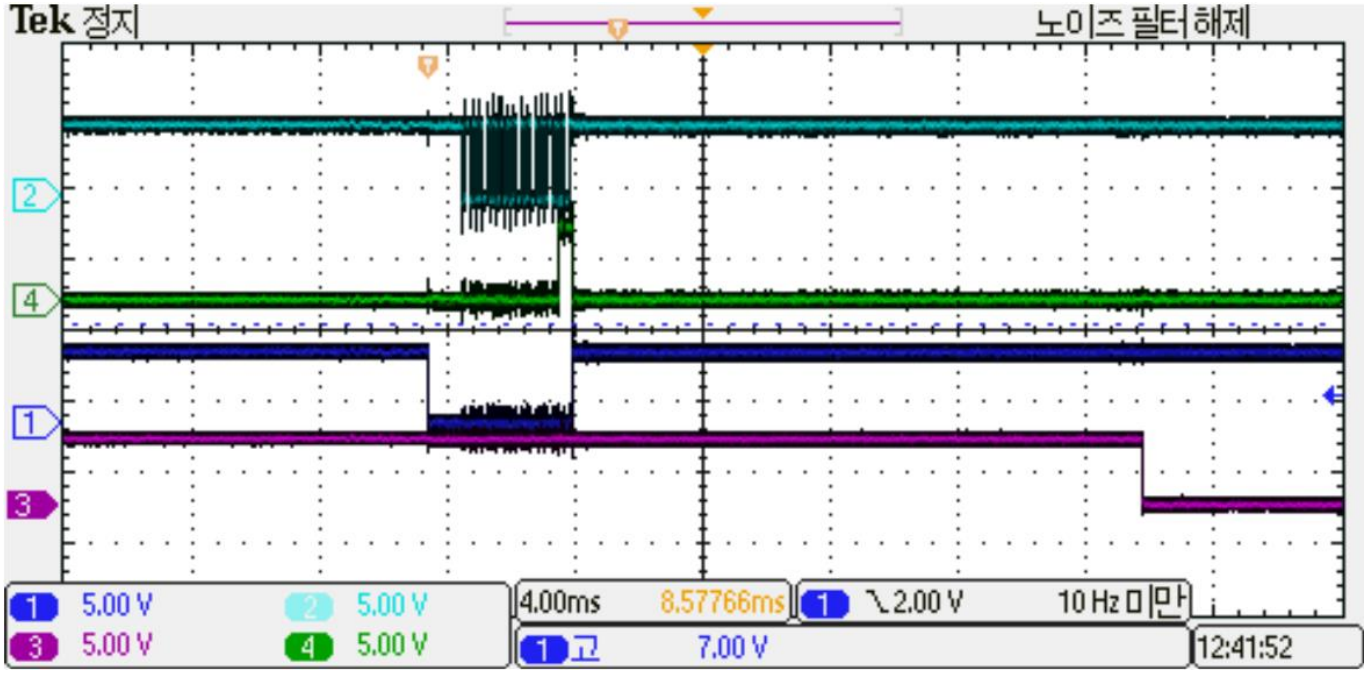
Pulse width timing:



1 Blue color line : Enable PA4 (pin 5 of SOP 8pins type)

3 Red color line : Busy PA5 (pin 6 of SOP 8pins type)

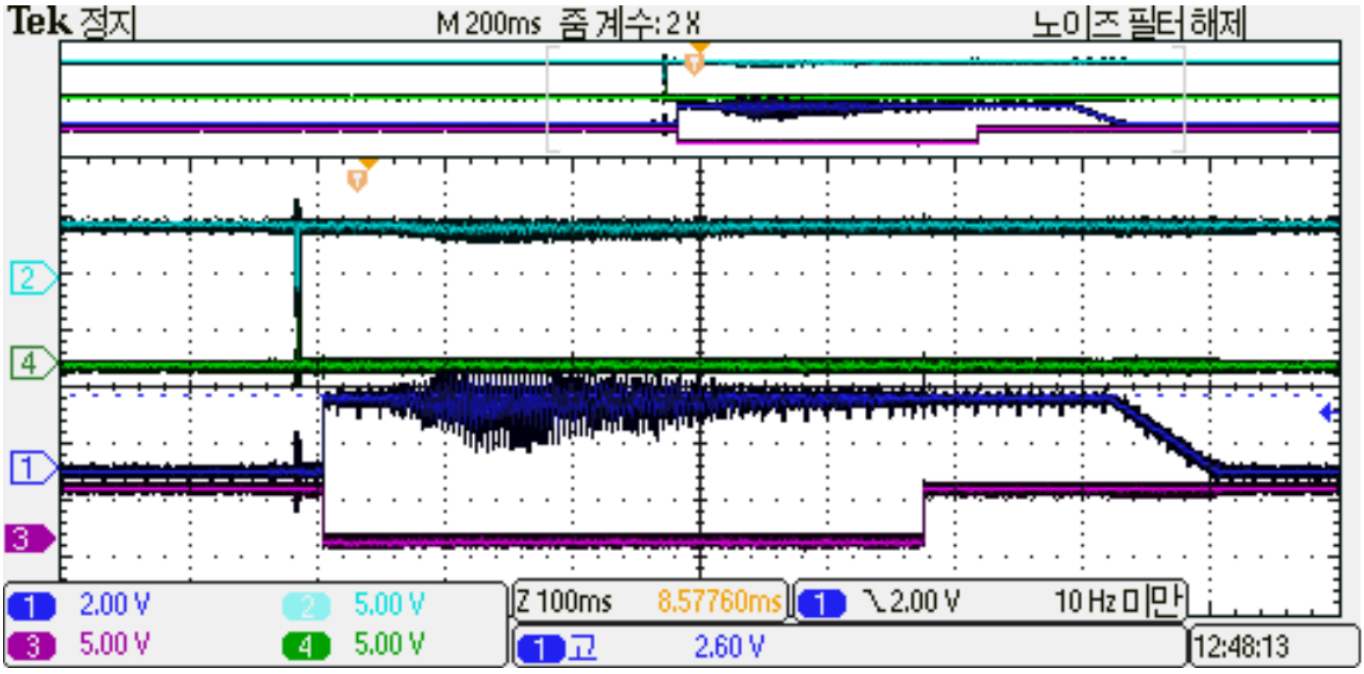
Enable & Busy :



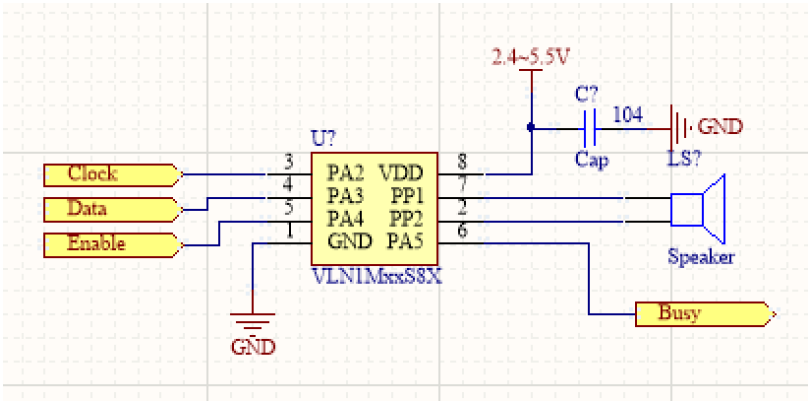
1 Blue color line : Sound PP1 (pin 7 of SOP 8pins type)

3 Red color line : Busy PA5 (pin 6 of SOP 8pins type)

Busy & Sound End :



15. APPLICATION

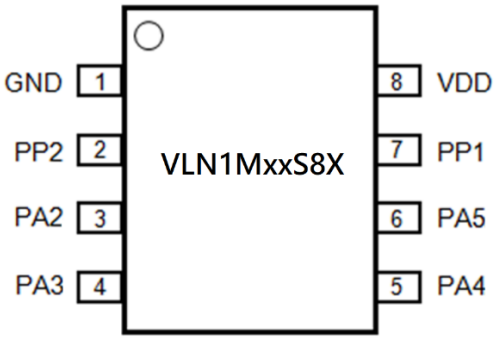


* PP1 (DAC) – When user want to use AMP, it can PP1(DAC) port connect with AMP

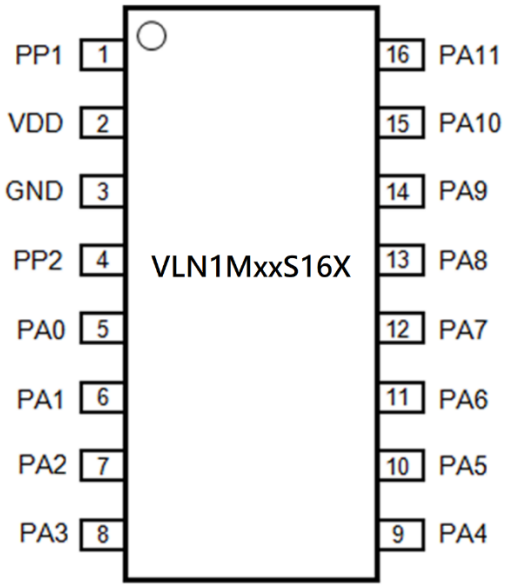
* Power voltage select when program – 3V or 5V

16. PACKAGE PIN ASSIGNMENT

8-pin SOP (150mil)

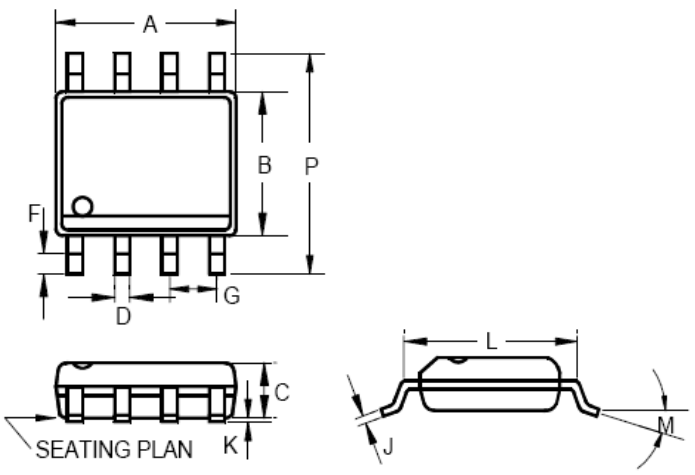


16-pin SOP (150mil)



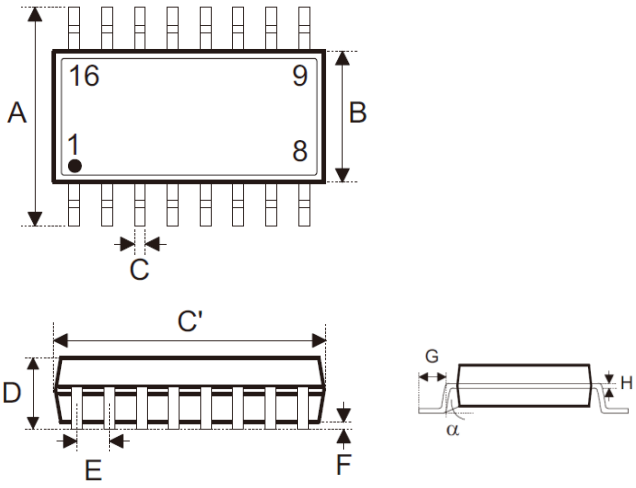
17. PACKAGE DIMENSION

17.1 8-Pin Plastic SOP (150 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.183	-	0.202	4.65	-	5.13
B	0.144	0.150	0.163	3.66	3.81	4.14
C	0.068	-	0.074	1.35	-	1.88
D	0.010	-	0.020	0.25	-	0.51
F	0.015	-	0.035	0.38	-	0.89
G	0.050 BSC			1.27 BSC		
J	0.007	-	0.010	0.19	-	0.25
K	0.005	-	0.010	0.13	-	0.25
L	0.189	-	0.205	4.80	-	5.21
M	-	-	8°	-	-	8°
P	0.228	-	0.244	5.79	-	6.20

17.2 SOP-16 (150mil, 1.27mm pin pitch)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.236 BSC			6.00 BSC		
B	0.154 BSC			3.90 BSC		
C	0.012	-	0.020	0.31	-	0.51
C'	0.390 BSC			9.90 BSC		
D	0.065	-	0.069	1.64	-	1.75
E	0.050 BSC			1.27 BSC		
F	0.004	-	0.010	0.10	-	0.25
G	0.016	-	0.050	0.40	-	1.27
H	0.004	-	0.010	0.10	-	0.25
α	-	-	8°	-	-	8°

18. ORDERING INFORMATION

P/N	*Shipping Type*	*Remark*
VLN1M04S8X	SOP-8 (MCP)	Width 150 mil, pitch 1.27mm
VLN1M08S8X	SOP-8 (MCP)	Width 150 mil, pitch 1.27mm
VLN1M08S16X	SOP-16 (MCP)	Width 150 mil, pitch 1.27mm
VLN1M32S8X	SOP-8 (MCP)	Width 150 mil, pitch 1.27mm
VLN1M32S16X	SOP-16 (MCP)	Width 150 mil, pitch 1.27mm