**7.4. Why are there two different registers (MAR and MDR) associated with memory? What are the equivalents in the Little Man Computer?**

Answer:

MAR which stands for memory address register, and MDR which stands for memory data register are both located between the CPU and the main memory and they store a binary number temporarily while an instruction is being processed. The MAR can hold the address which will be executed next, the address which should be loaded from, or stored on. In the Little Man Computer this is called the counter. Two registers, the memory address register and the memory data register, act as an interface

between the CPU and memory. The memory data register is called the memory buffer register

by some computer manufacturers.

Figure 7.4 is a simplified representation of the relationship between the MAR, the MDR,

and memory. Each cell in the memory unit holds 1 bit of data. The cells in Figure 7.4 are

organized in rows. Each row consists of a group of one or more bytes. Each row represents the

data cells for one or more consecutive memory addresses, shown in the figure as addresses 000,

001, . . . , 2n − 1.

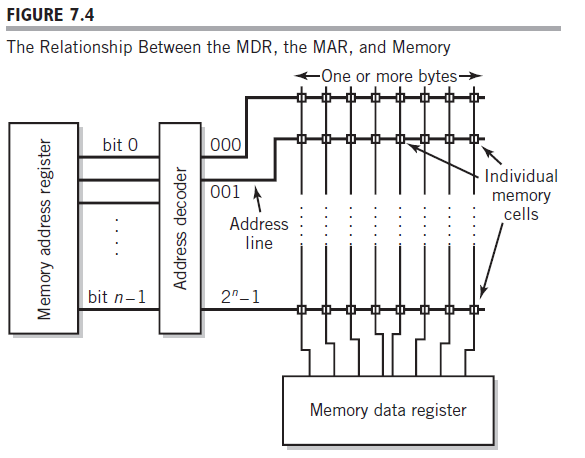
The memory address register holds the address in the memory that is to be “opened” for

data. The MAR is connected to a decoder that interprets the address and activates a single

address line into the memory. There is a separate address line for each row of cells in the

memory; thus, if there are n bits of addressing, there will be 2n address lines. These are the

horizontal lines in the figure.



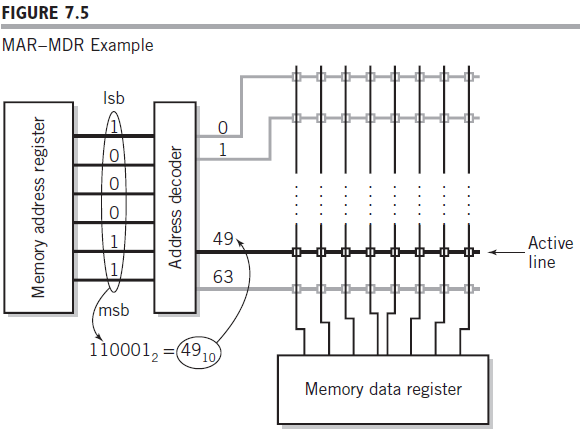
The memory data register is designed such that it is effectively connected to every cell in

the memory unit. Each bit of the MDR is connected in a column to the corresponding bit of

every location in memory (the vertical lines). However, the addressing method assures that

only a single row of cells is activated at any given time. Thus, the MDR only has access to the

values in that single row. A specific example of this is shown in Figure 7.5.



These are two registers with different functions to be performed, one of them stores the address and the other one stores the data. We cannot unify them into a single unit as a result there are two registers being used for memory inside the CPU.

**7.11 Suppose that the instruction format for a modified Little Man Computer requires two**

**consecutive locations for each instruction. The high-order digits of the instruction are**

**located in the first mail slot, followed by the low-order digits. The IR is large enough**

**to hold the entire instruction and can be addressed as IR [high] and IR [low] to load**

**it. You may assume that the op code part of the instruction uses IR [high] and that the**

**address is found in IR [low]. Write the fetch–execute cycle for an ADD instruction on**

**this machine.**

**Answer:**

PC → MAR

MDR → IR [High]

PC + 1 → PC

PC → MAR

MDR → IR [Low]

IR [Low] → MAR

MRD → A

PC + 1 → PC