V-14 Digital Design diploma

(Ninja Turtles group)

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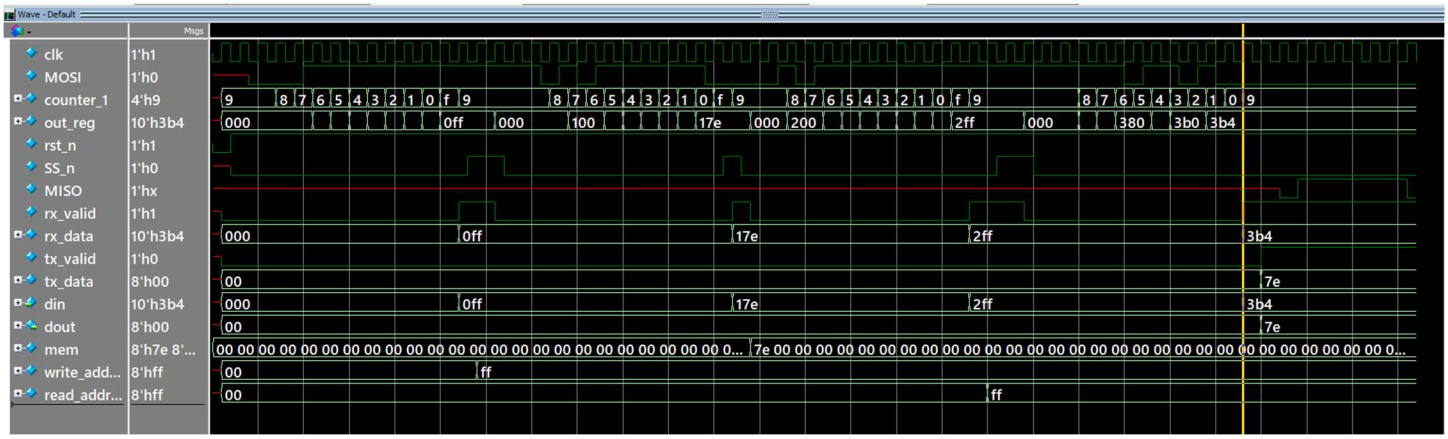
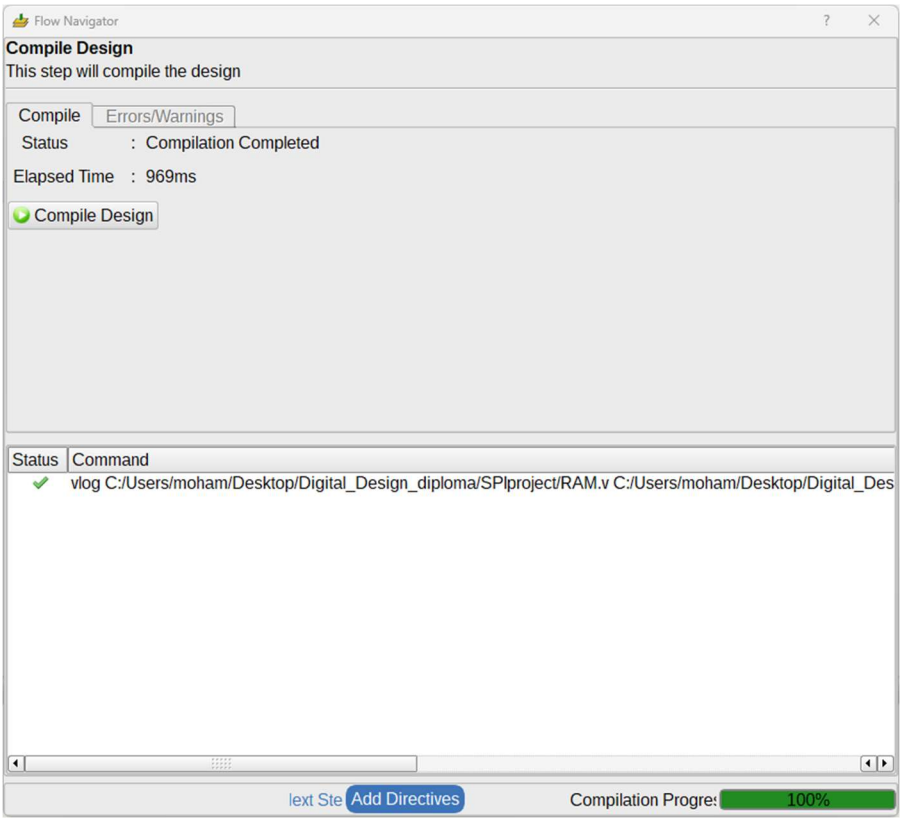
SPI Slave with Single Port RAM

1) Questasim snippets :



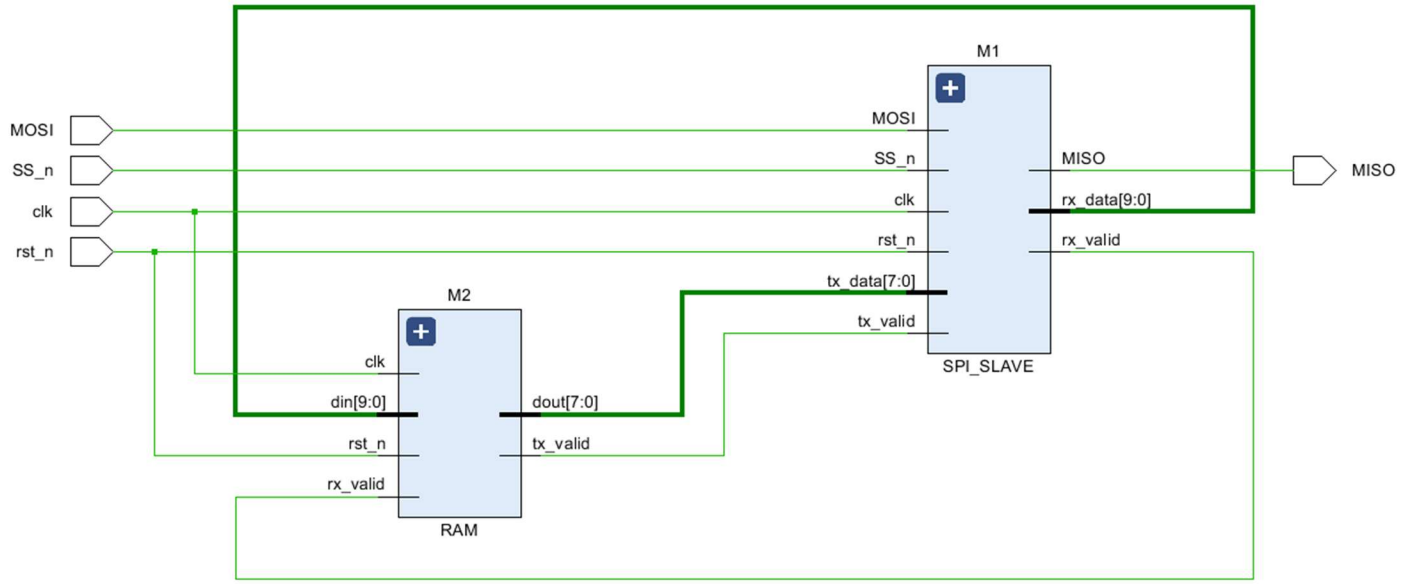
2) Questalint snippets :

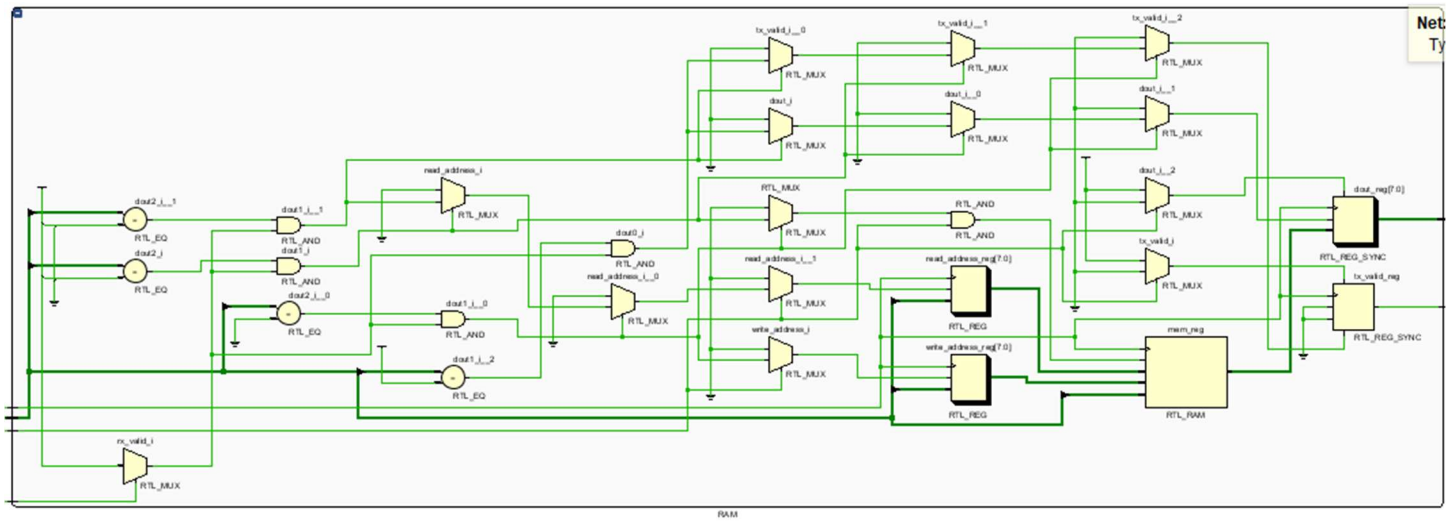


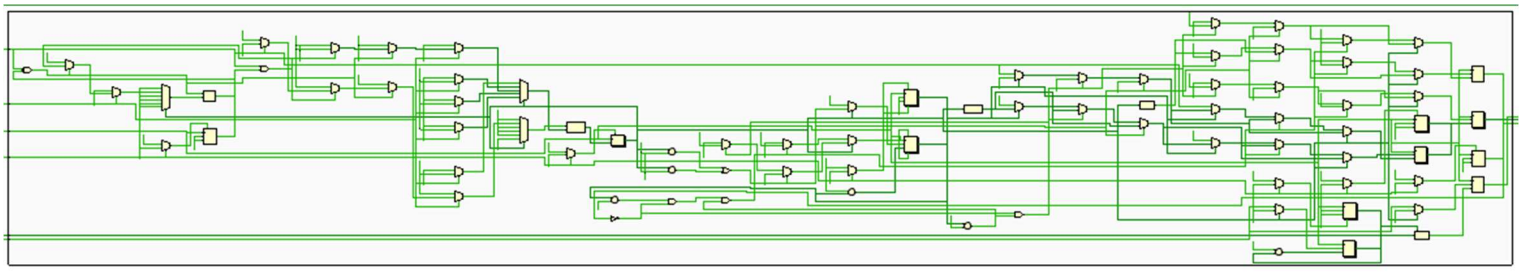
3) Synthesis Tool :

a) Elaboration :

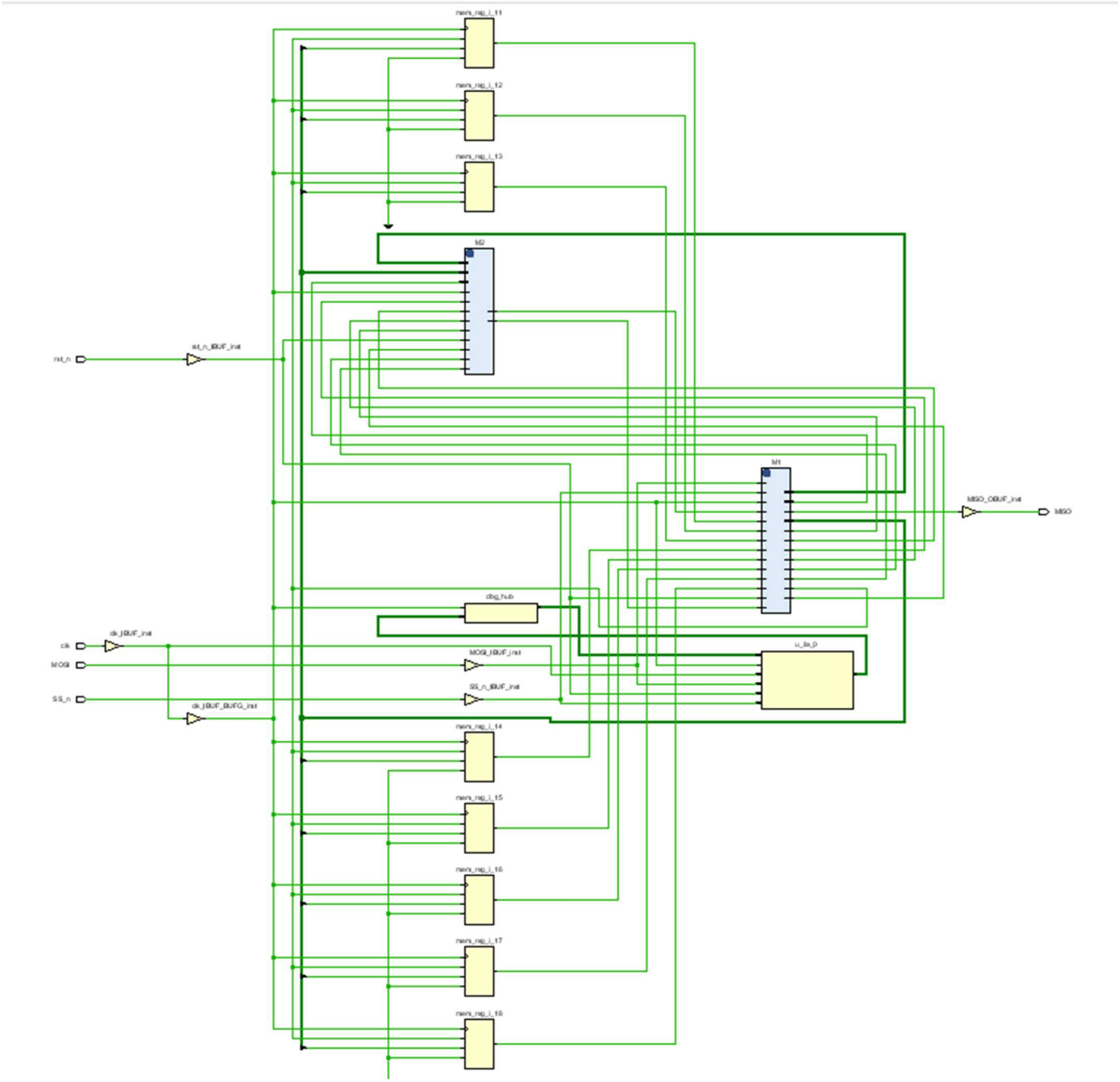
- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/Vivado/2018.2/data/ip'.
- Elaborated Design (11 infos)
  - General Messages (11 infos)
    - [Synth 8-6157] synthesizing module 'SPI' [SPI.v:1] (2 more like this)
    - [Synth 8-155] case statement is not full and has no default [SPI_SLAVE.v:41]
    - [Synth 8-6155] done synthesizing module 'SPI_SLAVE' (1#1) [SPI_SLAVE.v:1] (2 more like this)
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    - [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.







b) synthesis :



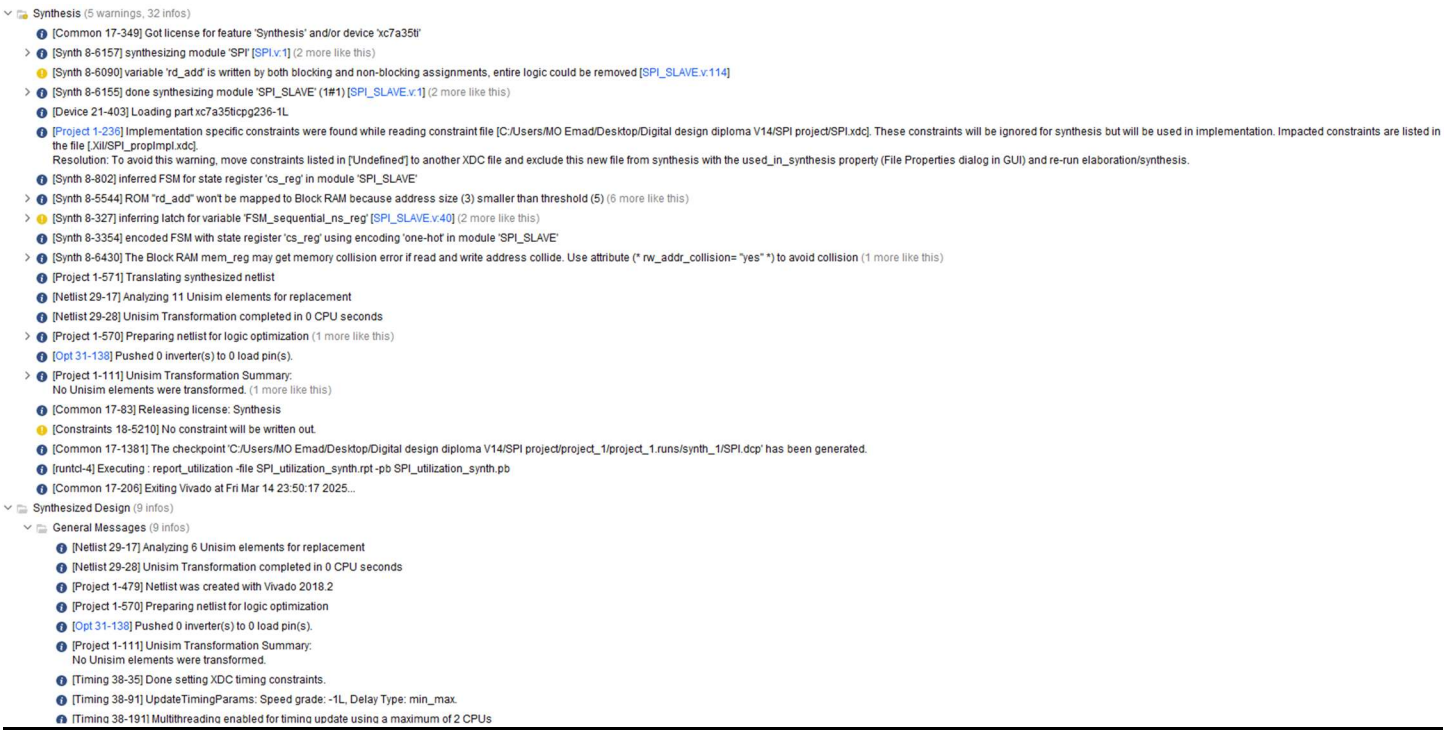


Figure 1

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI	67	57	1	0.5	5	1
dbg_hub (dbg_hub_CV)	0	0	0	0	0	0
M1 (SPI_SLAVE)	65	40	0	0	0	0
M2 (RAM)	2	9	1	0.5	0	0
u_ila_0 (u_ila_0_CV)	0	0	0	0	0	0

i – gray-FSM-encoding :

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.182 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	108	Total Number of Endpoints:	108	Total Number of Endpoints:	55

All user specified timing constraints are met.

ii – one-hot-FSM-encoding :

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.182 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	108	Total Number of Endpoints:	108	Total Number of Endpoints:	55

All user specified timing constraints are met.

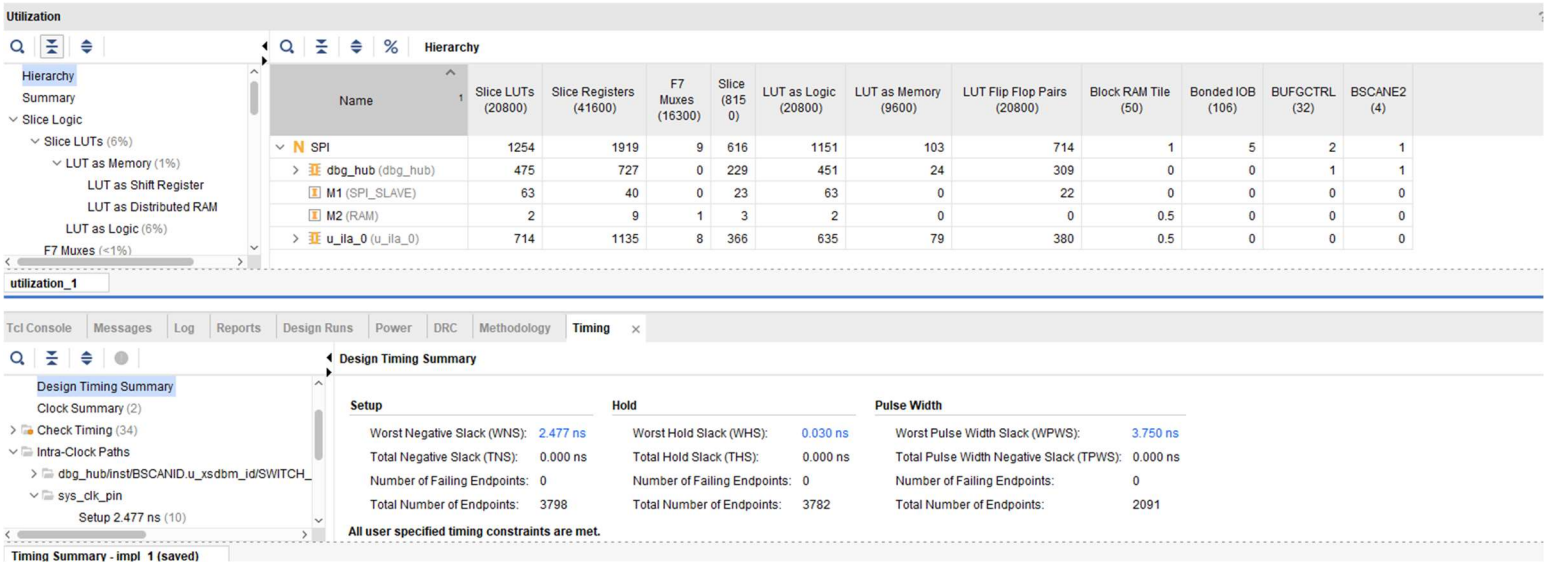
iii – seq-FSM-encoding :

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.182 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	108	Total Number of Endpoints:	108	Total Number of Endpoints:	55

All user specified timing constraints are met.

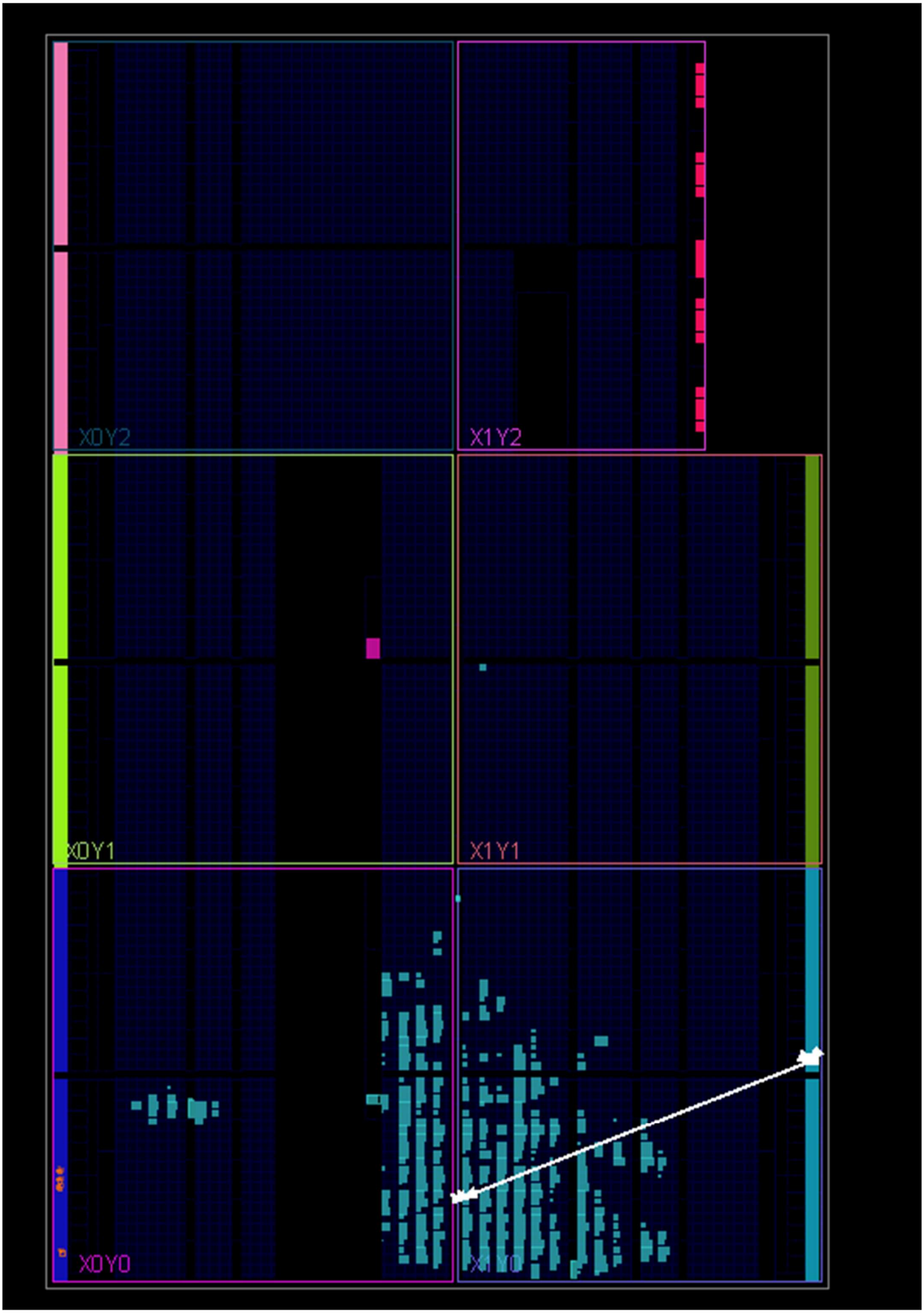
c) Implementation :



Implemented Design (1 warning, 10 infos)

General Messages (1 warning, 10 infos)

- [Netlist 29-17] Analyzing 96 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
  A total of 50 instances were transformed.
  CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 44 instances
  RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances


X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0

d) Generation of bitstream file :