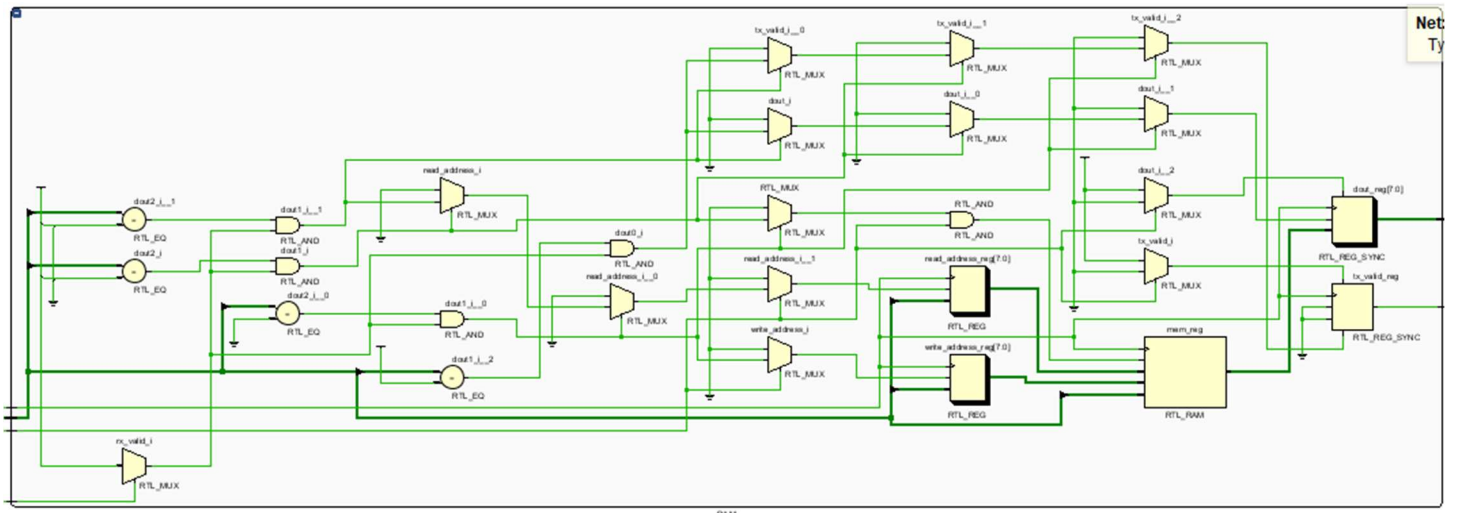
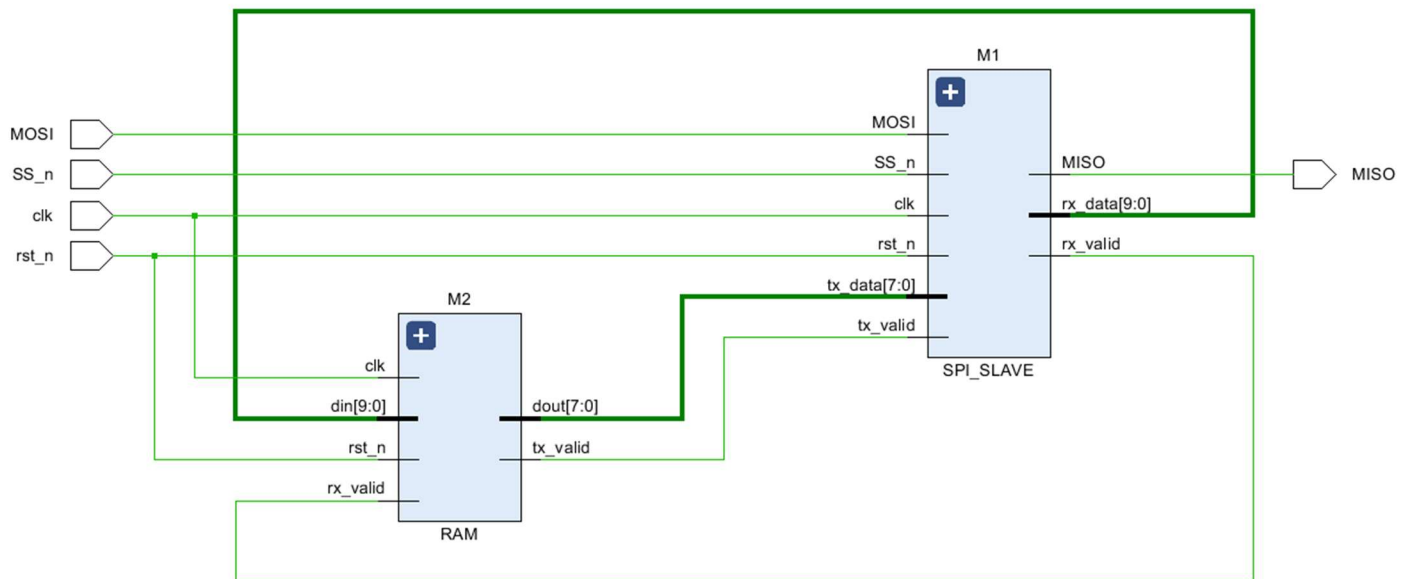
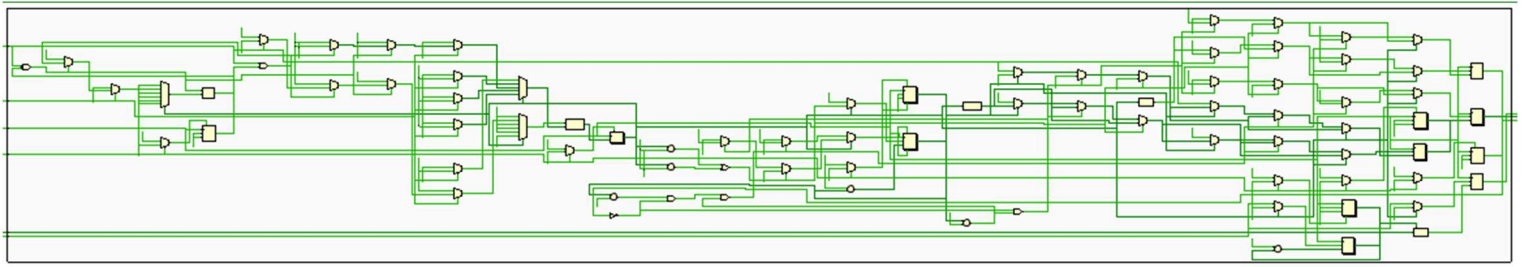


3) Synthesis Tool :

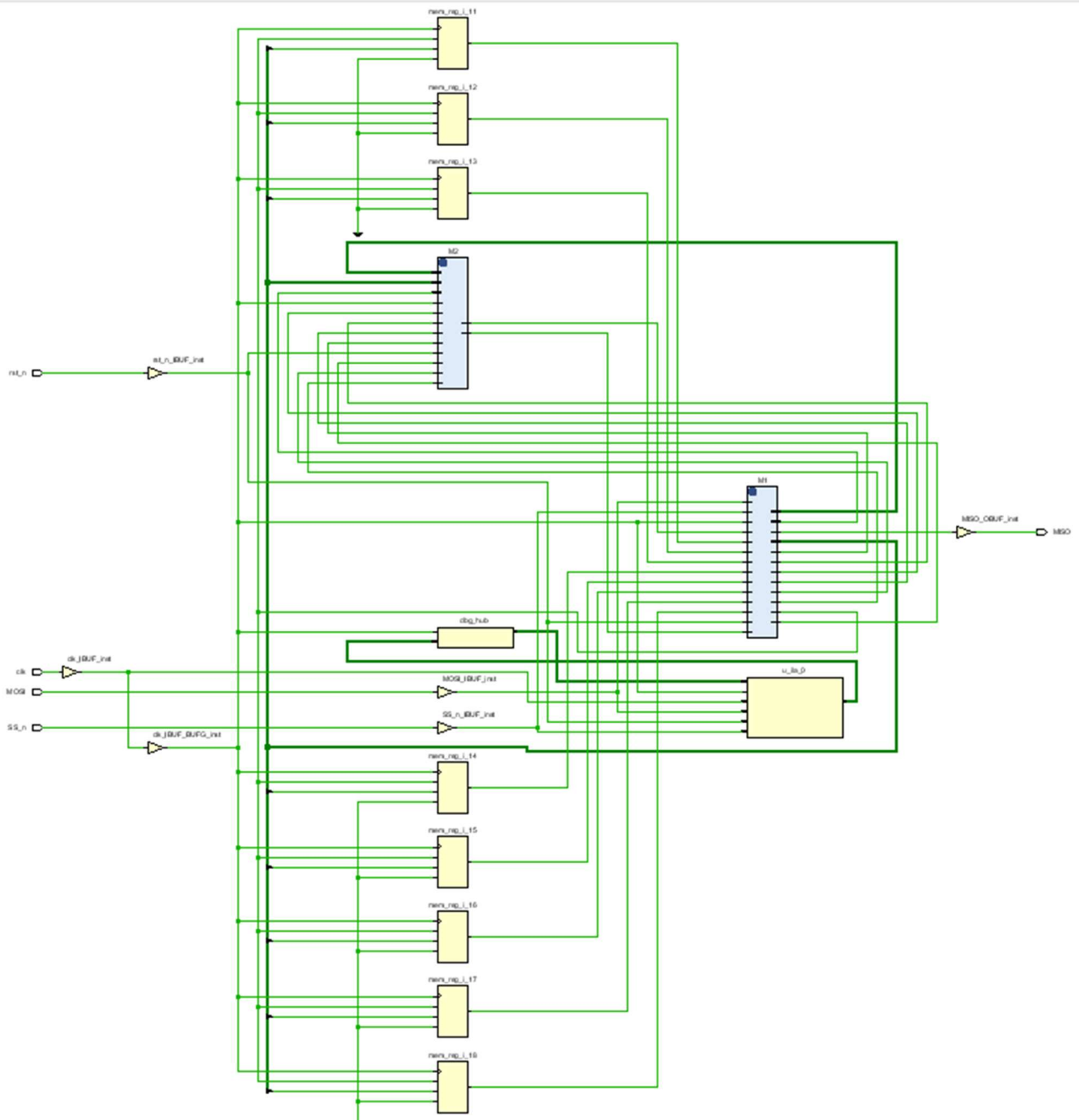
a) Elaboration :

- ▼ Vivado Commands (3 infos)
 - ▼ General Messages (3 infos)
 - ❗ [IP_Flow 19-234] Refreshing IP repositories
 - ❗ [IP_Flow 19-1704] No user IP repositories specified
 - ❗ [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/Vivado/2018.2/data/ip'.
 - ▼ Elaborated Design (11 infos)
 - ▼ General Messages (11 infos)
 - > ❗ [Synth 8-6157] synthesizing module 'SPI' [SPI.v:1] (2 more like this)
 - ❗ [Synth 8-155] case statement is not full and has no default [SPI_SLAVE.v:41]
 - > ❗ [Synth 8-6155] done synthesizing module 'SPI_SLAVE' (1#1) [SPI_SLAVE.v:1] (2 more like this)
 - ❗ [Device 21-403] Loading part xc7a35ticpg236-1L
 - ❗ [Project 1-570] Preparing netlist for logic optimization
 - ❗ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - ❗ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.





b) synthesis :



Synthesis (5 warnings, 32 infos)

[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

[Synth 8-6157] synthesizing module 'SPI' [SPI.v:1] (2 more like this)

[Synth 8-6090] variable 'rd_add' is written by both blocking and non-blocking assignments, entire logic could be removed [SPI_SLAVE.v:114]

[Synth 8-6155] done synthesizing module 'SPI_SLAVE' (1#1) [SPI_SLAVE.v:1] (2 more like this)

[Device 21-403] Loading part xc7a35tcpq236-1L

[Project 1-235] Implementation specific constraints were found while reading constraint file [C:/Users/MO Emad/Desktop/Digital design diploma V14/SPI project/SPI.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [XII/SPI_propmimpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

[Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_SLAVE'

[Synth 8-5544] ROM 'rd_add' won't be mapped to Block RAM because address size (3) smaller than threshold (5) (5 more like this)

[Synth 8-327] inferring latch for variable 'FSM_sequential_ns_reg' [SPI_SLAVE.v:40] (2 more like this)

[Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_SLAVE'

[Synth 8-6430] The Block RAM mem_reg may get memory collision error if read and write address collide. Use attribute ("rw_addr_collision="yes") to avoid collision (1 more like this)

[Project 1-571] Translating synthesized netlist

[Netlist 29-17] Analyzing 11 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

[Project 1-570] Preparing netlist for logic optimization (1 more like this)

[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)

[Common 17-83] Releasing license: Synthesis

[Constraints 18-5210] No constraint will be written out.

[Common 17-1381] The checkpoint 'C:/Users/MO Emad/Desktop/Digital design diploma V14/SPI project/project_1/project_1_runs/synth_1/SPI.dcp' has been generated.

[runtcl-4] Executing : report_utilization -file SPI_utilization_synth.rpt -pb SPI_utilization_synth.pb

[Common 17-206] Exiting Vivado at Fri Mar 14 23:50:17 2025...

Synthesized Design (9 infos)

General Messages (9 infos)

[Netlist 29-17] Analyzing 6 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

[Project 1-479] Netlist was created with Vivado 2018.2

[Project 1-570] Preparing netlist for logic optimization

[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).






[Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.

[Timing 38-35] Done setting XDC timing constraints.

[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max.

[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

Figure 1

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
 SPI	67	57	1	0.5	5	1
 dbg_hub (dbg_hub_CV)	0	0	0	0	0	0
 M1 (SPI_SLAVE)	65	40	0	0	0	0
 M2 (RAM)	2	9	1	0.5	0	0
 u_ila_0 (u_ila_0_CV)	0	0	0	0	0	0

i – gray-FSM-encoding :

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.182 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 108	Total Number of Endpoints: 108	Total Number of Endpoints: 55

All user specified timing constraints are met.

ii – one-hot-FSM-encoding :

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.182 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 108	Total Number of Endpoints: 108	Total Number of Endpoints: 55

All user specified timing constraints are met.

iii – seq-FSM-encoding :

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 6.182 ns	Worst Hold Slack (WHS): 0.139 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 108	Total Number of Endpoints: 108	Total Number of Endpoints: 55

All user specified timing constraints are met.

c) Implementation :

Utilization

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)	BSCAN2 (4)
N SPI	1254	1919	9	616	1151	103	714	1	5	2	1
dbg_hub (dbg_hub)	475	727	0	229	451	24	309	0	0	1	1
M1 (SPI_SLAVE)	63	40	0	23	63	0	22	0	0	0	0
M2 (RAM)	2	9	1	3	2	0	0	0.5	0	0	0
u_ila_0 (u_ila_0)	714	1135	8	366	635	79	380	0.5	0	0	0

utilization_1

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.477 ns	Worst Hold Slack (WHS): 0.030 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 3798	Total Number of Endpoints: 3782	Total Number of Endpoints: 2091

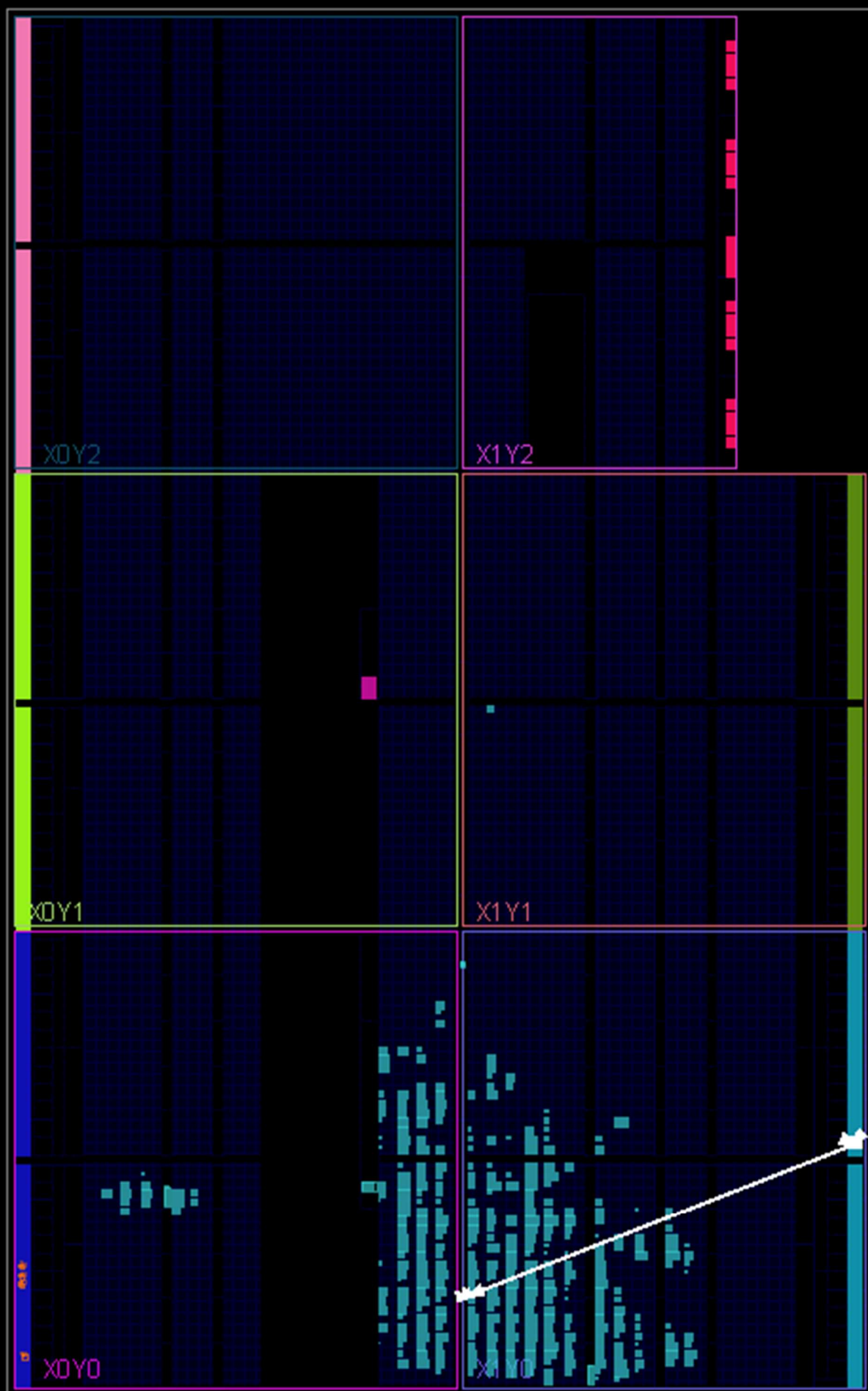
All user specified timing constraints are met.

Timing Summary - impl 1 (saved)

Implemented Design (1 warning, 10 infos)

General Messages (1 warning, 10 infos)

- [Netlist 29-17] Analyzing 96 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
A total of 50 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 44 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances



d) Generation of bitstream file :

