

DSP48A1 project

1. RTL code :

```
1  module REG_MUX #(
2      parameter RSTTYPE = "SYNC" ,
3      parameter reg_SIZE = 18 )(
4          input [reg_SIZE-1:0] IN ,
5          input clk , rst , CE ,PIPELINE_EN ,
6          output [reg_SIZE-1:0] out );
7 // INSTANTIATION TEMPLATE:
8 // REG_MUX #(.RSTTYPE("SYNC"),.reg_SIZE()) YOUR_INSTANCE_NAME (.IN(),.clk(),.rst(),.CE(),.PIPELINE_EN(),.out()) ;
9
10 reg [reg_SIZE-1:0] REG ;
11
12 generate
13     if (RSTTYPE == "SYNC") begin
14         always @ (posedge clk ) begin
15             if (rst) REG <= {reg_SIZE{1'b0}} ;
16             else if (CE) REG <= IN ;
17         end
18     end
19     else if (RSTTYPE == "ASYNC") begin
20         always @ (posedge clk or posedge rst) begin
21             if (rst) REG <= {reg_SIZE{1'b0}} ;
22             else if (CE) REG <= IN ;
23         end
24     end
25 endgenerate
26
27 assign out = (PIPELINE_EN)? REG : IN ;
28
29 endmodule
```

```
1  module DSP48A1 #(
2      parameter A0REG = 1'b0 ,
3      parameter A1REG = 1'b1 ,
4      parameter B0REG = 1'b0 ,
5      parameter B1REG = 1'b1 ,
6      parameter CREG = 1'b1 ,
7      parameter DREG = 1'b1 ,
8      parameter MREG = 1'b1 ,
9      parameter PREG = 1'b1 ,
10     parameter CARRYINREG = 1'b1 ,
11     parameter CARRYOUTREG = 1'b1 ,
12     parameter OPMODEREG = 1'b1 ,
13     parameter CARRYINSEL = "OPMODES" ,
14     parameter B_INPUT = "DIRECT" ,
15     parameter RSTTYPE = "SYNC" )(

16     input [17:0] A , B , D ,
17     input [47:0] C ,
18     input [17:0] BCIN ,
19     input [47:0] PCIN ,
20     input CARRYIN ,
21     input clk ,
22     input [7:0] OPMODE ,
23     input CEA , CEB , CEC , CECARRYIN , CED , CEM , CEOPMODE , CEP ,
24     input RSTA , RSTB , RSTC , RSTCARRYIN , RSTD , RSTM , RSTOPMODE , RSTP ,
25     output CARRYOUT , CARRYOUTF ,
26     output [47:0] P ,
27     output [35:0] M ,
28     output [17:0] BCOUT ,
29     output [47:0] PCOUT );
```

```

30
31 wire [7:0] opmode ;
32 wire [17:0] W0 , W1 , W2 , W3 , W5 , W6 , W7 , W8;
33 wire [47:0] W4 , W13 , W14 , DAB , W15 ;
34 wire [35:0] W9 , W10;
35 wire W11 , W12 , W16 ;
36 assign W0 = (B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? BCIN : 18'b0 ;
37 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(8)) OPMODE_REG (.IN(OPMODE),.PIPELINE_EN(OPMODEREG),.clk(clk),.rst(RSTOPMODE),.CE(CEOPMODE),.out(opmode)) ;
38 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(18)) D_REG (.IN(D),.PIPELINE_EN(DREG),.clk(clk),.rst(RSTD),.CE(CED),.out(W1)) ;
39 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(18)) B0_REG (.IN(W0),.PIPELINE_EN(B0REG),.clk(clk),.rst(RSTB),.CE(CEB),.out(W2)) ;
40 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(18)) A0_REG (.IN(A),.PIPELINE_EN(A0REG),.clk(clk),.rst(RSTA),.CE(CEA),.out(W3)) ;
41 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(48)) C_REG (.IN(C),.PIPELINE_EN(CREG),.clk(clk),.rst(RSTC),.CE(CEC),.out(W4)) ;
42 assign W5 = (opmode[6])? W1-W2 : W1+W2 ;
43 assign W6 = (opmode[4])? W5 : W2 ;
44 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(18)) B1_REG (.IN(W6),.PIPELINE_EN(B1REG),.clk(clk),.rst(RSTB),.CE(CEB),.out(W7)) ;
45 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(18)) A1_REG (.IN(W3),.PIPELINE_EN(A1REG),.clk(clk),.rst(RSTA),.CE(CEA),.out(W8)) ;
46 assign BCOUT = W7 ;
47 assign DAB = {W1[11:0] , W8[17:0] , W7[17:0]} ;
48 assign W9 = W7 * W8 ;
49 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(36)) M_REG (.IN(W9),.PIPELINE_EN(MREG),.clk(clk),.rst(RSTM),.CE(CEM),.out(W10)) ;
50 assign M = W10 ;
51 assign W11 = (CARRYINSEL == "OPMODE5")? opmode[5] : (CARRYINSEL == "CARRYIN")? CARRYIN : 1'b0 ;
52 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(1)) CYI (.IN(W11),.PIPELINE_EN(CARRYINREG),.clk(clk),.rst(RSTCARRYIN),.CE(CECARRYIN),.out(W12)) ;
53 assign W13 = (opmode[1:0] == 2'b00) ? 48'b0 :
54 (opmode[1:0] == 2'b01) ? {12'b0,W10} :
55 (opmode[1:0] == 2'b10) ? P :
56 (opmode[1:0] == 2'b11) ? DAB : 48'b0 ;
57 assign W14 = (opmode[3:2] == 2'b00) ? 48'b0 :
58 (opmode[3:2] == 2'b01) ? PCIN :
59 (opmode[3:2] == 2'b10) ? P :
60 (opmode[3:2] == 2'b11) ? W4 : 48'b0 ;
61 assign {W16,W15} = (opmode[7])? (W14 - (W13 + W12)) : (W14 + (W13 + W12)) ;
62 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(1)) CYO_REG (.IN(W16),.PIPELINE_EN(CARRYOUTREG),.clk(clk),.rst(RSTCARRYIN),.CE(CECARRYIN),.out(CARRYOUT)) ;
63 assign CARRYOUTF = CARRYOUT ;
64 REG_MUX #(.RSTTYPE(RSTTYPE),.reg_SIZE(48)) P_REG (.IN(W15),.PIPELINE_EN(PREG),.clk(clk),.rst(RSTP),.CE(CEP),.out(P)) ;
65 assign PCOUT = P ;
66
67 endmodule

```

2. Testbench code :

```

● ● ●
1 module DSP48A1_tb ();
2   parameter A0REG = 0 ;
3   parameter A1REG = 1 ;
4   parameter B0REG = 0 ;
5   parameter B1REG = 1 ;
6   parameter CREG = 1 ;
7   parameter DREG = 1 ;
8   parameter MREG = 1 ;
9   parameter PREG = 1 ;
10  parameter CARRYINREG = 1 ;
11  parameter CARRYOUTREG = 1 ;
12  parameter OPMODEREG = 1 ;
13  parameter CARRYINSEL = "OPMODE5" ;
14  parameter B_UNPUT = "DIRECT" ;
15  parameter RSTTYPE = "SYNC" ;
16  reg [17:0] A , B , D ;
17  reg [47:0] C ;
18  reg [17:0] BCIN ;
19  reg [47:0] PCIN ;
20  reg CARRYIN ;
21  reg clk ;
22  reg [7:0] OPMODE ;
23  reg CEA , CEB , CEC , CECARRYIN , CED , CEM , CEOPMODE , CEP ;
24  reg RSTA , RSTB , RSTC , RSTCARRYIN , RSTD , RSTM , RSTOPMODE , RSTP ;
25  reg [47:0] P_expected ;
26  reg CARRYOUT_expected ;
27  wire CARRYOUT , CARRYOUTF ;
28  wire [47:0] P ;
29  wire [35:0] M ;
30  wire [17:0] BCOUT ;
31  wire [47:0] PCOUT ;
32
33  DSP48A1 DUT(.*) ;
34

```

```

initial begin
  clk = 0 ;
  forever begin
    #1 clk = ~clk ;
  end
end
initial begin
  RSTA = 1 ; RSTB = 1 ; RSTC = 1 ; RSTD = 1 ;
  RSTCARRYIN = 1 ;
  RSTM = 1 ;

  RSTP = 1 ;
  @(negedge clk) ;
  RSTA = 0 ;
  RSTB = 0 ;
  RSTC = 0 ;
  RSTCARRYIN = 0 ;
  RSTD = 0 ;
  RSTM = 0 ;
  RSTOPMODE = 0 ;
  RSTP = 0 ;
  CEA = 1'b1 ;
  CEB = 1'b1 ;
  CEC = 1'b1 ;
  CECARRYIN = 1'b1 ;
  CED = 1'b1 ;
  CEM = 1'b1;
  CEOPMODE = 1'b1 ;
  CEP = 1'b1 ;
  //////////////
  OPMODE = 8'b000100000 ;
  {CARRYOUT_expected,P_expected} = 1 ;
  repeat(4) @ (negedge clk) ;
  $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
  $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b", P, P_expected, CARRYOUT);
  $display("_____");

  if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;

  //////////////
  OPMODE = 8'b10100000 ;
  {CARRYOUT_expected,P_expected} = -1 ;
  repeat(4) @ (negedge clk) ;
  $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
  $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b", P, P_expected, CARRYOUT);
  $display("_____");

  if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;

  //////////////
  3
  4
  5
  6
  7
  8
  9
  0
  {CARRYOUT_expected,P_expected} = {D[11:0] , A[17:0] , B[17:0]} + OPMODE[5] ;
  1
  repeat(4) @ (negedge clk) ;
  2
  $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
  3
  $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b", P, P_expected, CARRYOUT);
  4
  $display("_____");

  5
  if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
  6
  7

```

```

97
98 //////////////
99 OPMODE = 8'b00110011 ;
100 A = $random ;
101 B = $random ;
102 C = $random ;
103 D = $random ;
104 {CARRYOUT_expected,P_expected} = {D[11:0] , A[17:0] , (D+B)} + OPMODE[5] ;
105 repeat(4) @ (negedge clk) ;
106 $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
107 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
108 $display("_____");
109
110 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
111
112 //////////////
113 OPMODE = 8'b00100001 ;
114 A = $random ;
115 B = $random ;
116 C = $random ;
117 D = $random ;
118 {CARRYOUT_expected,P_expected} = (A*B) + OPMODE[5] ;
119 repeat(4) @ (negedge clk) ;
120 $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
121 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
122 $display("_____");
123
124 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
125
126 //////////////
127 OPMODE = 8'b01010001 ;
128 A = $random ;
129 B = $random ;
130 C = $random ;
131 D = $random ;
132 {CARRYOUT_expected,P_expected} = (A*(D-B)) + OPMODE[5] ;
133 repeat(4) @ (negedge clk) ;
134 $display("Inputs: A=%h, B=%h, D=%h, C=%h, OPMODE=%b, CARRYIN=%b", A, B, D, C, OPMODE, CARRYIN);
135 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
136 $display("_____");
137
138 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
139
140 //////////////
141 OPMODE = 8'b00000111 ;
142 A = $random ;
143 B = $random ;
144 C = $random ;
145 D = $random ;
146 PCIN = $random ;
147 {CARRYOUT_expected,P_expected} = PCIN + ({D[11:0] , A[17:0] , B[17:0]} + OPMODE[5]) ;
148 repeat(4) @ (negedge clk) ;
149 $display("Inputs: A=%h, B=%h, D=%h, C=%h, PCIN=%h OPMODE=%b, CARRYIN=%b", A, B, D, C, PCIN , OPMODE, CARRYIN);
150 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
151 $display("_____");
152
153 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
154

```

```

154 //////////////
155 OPMODE = 8'b00110111 ;
156 A = $random ;
157 B = $random ;
158 C = $random ;
159 D = $random ;
160 PCIN = $random ;
161 {CARRYOUT_expected,P_expected} = PCIN + ({D[11:0] , A[17:0] , (D+B)} + OPMODE[5]) ;
162 repeat(4) @ (negedge clk) ;
163 $display("Inputs: A=%h, B=%h, D=%h, PCIN=%h OPMODE=%b, CARRYIN=%b", A, B, D, PCIN , OPMODE, CARRYIN);
164 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
165 $display("_____");
166
167 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
168
169 //////////////
170 OPMODE = 8'b00100101 ;
171 A = $random ;
172 B = $random ;
173 C = $random ;
174 D = $random ;
175 PCIN = $random ;
176 {CARRYOUT_expected,P_expected} = PCIN + ((A*B)+ OPMODE[5]) ;
177 repeat(4) @ (negedge clk) ;
178 $display("Inputs: A=%h, B=%h, D=%h, C=%h, PCIN=%h OPMODE=%b, CARRYIN=%b", A, B, D, C, PCIN , OPMODE, CARRYIN);
179 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
180 $display("_____");
181
182 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
183
184 //////////////
185 OPMODE = 8'b00111111 ;
186 A = $random ;
187 B = $random ;
188 C = $random ;
189 D = $random ;
190 PCIN = $random ;
191 {CARRYOUT_expected,P_expected} = C + ({D[11:0] , A[17:0] , (D+B)}) + OPMODE[5] ;
192 repeat(4) @ (negedge clk) ;
193 $display("Inputs: A=%h, B=%h, D=%h, C=%h, PCIN=%h OPMODE=%b, CARRYIN=%b", A, B, D, C, PCIN , OPMODE, CARRYIN);
194 $display("Outputs: P=%h, Expected P=%h, CARRYOUT=%b ,CARRYOUT_expected=%b", P, P_expected, CARRYOUT,CARRYOUT_expected);
195 $display("_____");
196
197 if ((P != P_expected)|| (CARRYOUT!=CARRYOUT_expected)) $display ("%t : ERROR ",$time) ;
198
199
200 $stop;
201
202 end
203
204
205 endmodule

```



3. Do file :

```

1 vlib work
2 vlog REG_MUX.v DSP48A1_tb.v DSP48A1.v
3 vsim -voptargs=+acc work.DSP48A1_tb
4 add wave *
5 run -all
6

```

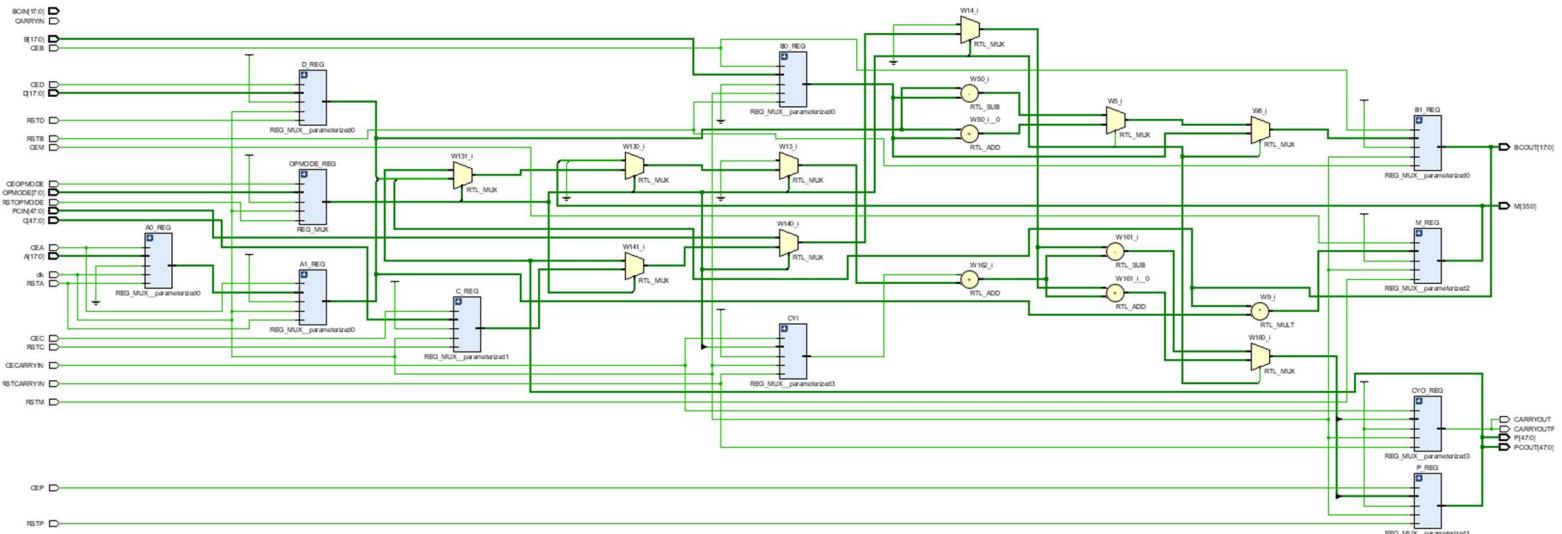
4. QuestaSim Snippets :



5. Constraint File :

```
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMS3 } [get_ports clk]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11
```

6. Elaboration :



Elaborated Design (20 warnings, 16 infos)

General Messages (20 warnings, 16 infos)

- ⚠ [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
- > ⓘ [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (5 more like this)
- > ⓘ [Synth 8-6155] done synthesizing module 'REG_MUX' (1#1) [REG_MUX.v:1] (5 more like this)
- > ⓘ [Synth 8-3331] design DSP48A1 has unconnected port BCIN[17] (18 more like this)
- ⓘ [Device 21-403] Loading part xc7a200tffg1156-3
- ⓘ [Project 1-570] Preparing netlist for logic optimization
- ⓘ [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ⓘ [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

7. Synthesis :

Name	1	Slice LUTs (134600)	Slice Registers (269200)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)	
N DSP48A1	182	160	1	327	1		
A1_REG (REG_MUX_...	0	18	0	0	0	0	
B1_REG (REG_MUX_...	0	18	0	0	0	0	
C_REG (REG_MUX_...	0	48	0	0	0	0	
CYI (REG_MUX_para...	1	1	0	0	0	0	
CYO_REG (REG_MUX...	0	1	0	0	0	0	
D_REG (REG_MUX_...	0	18	0	0	0	0	
OPMODE_REG (REG_...	180	8	0	0	0	0	
P_REG (REG_MUX_...	0	48	0	0	0	0	

Synthesis (58 warnings, 48 infos)

- ① [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- ① [Synth 8-2490] Overwriting previous definition of module DSP48A1 [DSP48A1.v1]
- > ① [Synth 8-1657] synthesizing module 'DSP48A1' [DSP48A1.v1] (5 more like this)
- > ① [Synth 8-1655] done synthesizing module 'REG_MUX (#1)' [REG_MUX.v1] (5 more like this)
- > ① [Synth 8-3331] design DSP48A1 has unconnected port BCIN[17] (37 more like this)
- ① [Device 21-403] Loading part xc7a200tfg1156-3
- ① [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/MO Emad/Desktop/Digital design diploma V14/DSP48A1 project/DSP.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xilf/DSP48A1_propimpl.xdc]. Resolution: To avoid this warning, move constraints listed in 'Undefined' to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
- > ① [Synth 8-5818] HDL ADVISOR - The operator resource <addr> is shared. To prevent sharing consider applying a KEEP on the output of the operator [DSP48A1.v42] (1 more like this)
- > ① [Synth 8-3886] merging instance 'A0_REG/REG_reg[0]' (FDRE) to 'A1_REG/REG_reg[0]' (17 more like this)
- > ① [Synth 8-3332] Sequential element (B0_REG/REG_reg[17]) is unused and will be removed from module DSP48A1. (17 more like this)
- ① [Synth 8-5842] Cannot pack DSP OPMODE registers because of constant '1' value. Packing the registers will cause simulation mismatch at initial cycle [DSP48A1.v48]
- ① [Project 1-571] Translating synthesized netlist
- ① [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- > ① [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- > ① [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)
- ① [Common 17-83] Releasing license: Synthesis
- ① [Constraints 18-5210] No constraint will be written out.
- ① [Common 17-1381] The checkpoint 'C:/Users/MO Emad/Desktop/Digital design diploma V14/DSP48A1 project/project_3/project_3/runs/synth_1/DSP48A1.dcp' has been generated.
- ① [runcl-4] Executing : report_utilization -file DSP48A1_utilization.rpt -pb DSP48A1_utilization_synth.pb
- ① [Common 17-206] Exiting Vivado at Tue Mar 11 01:14:19 2025...

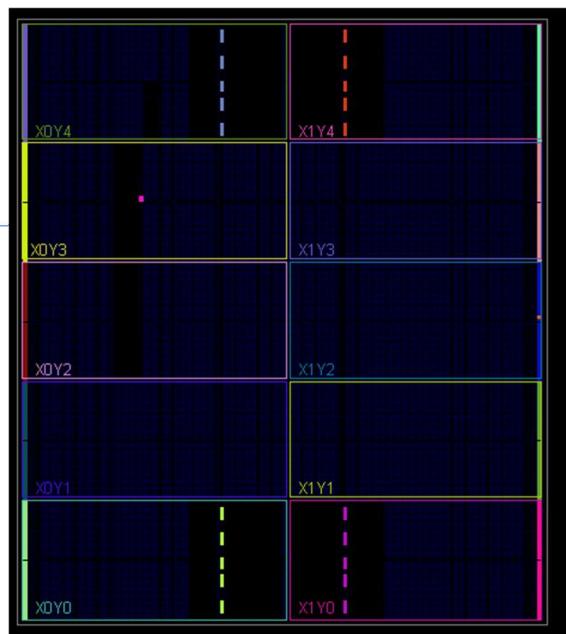
Synthesized Design (9 infos)

- ① [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- ① [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- ① [Project 1-479] Netlist was created with Vivado 2018.2
- ① [Project 1-570] Preparing netlist for logic optimization
- ① [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- ① [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed.
- ① [Timing 38-35] Done setting XDC timing constraints.
- ① [Timing 38-91] UpdateTimingParams: Speed grade: -3, Delay Type: min_max.
- ① [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

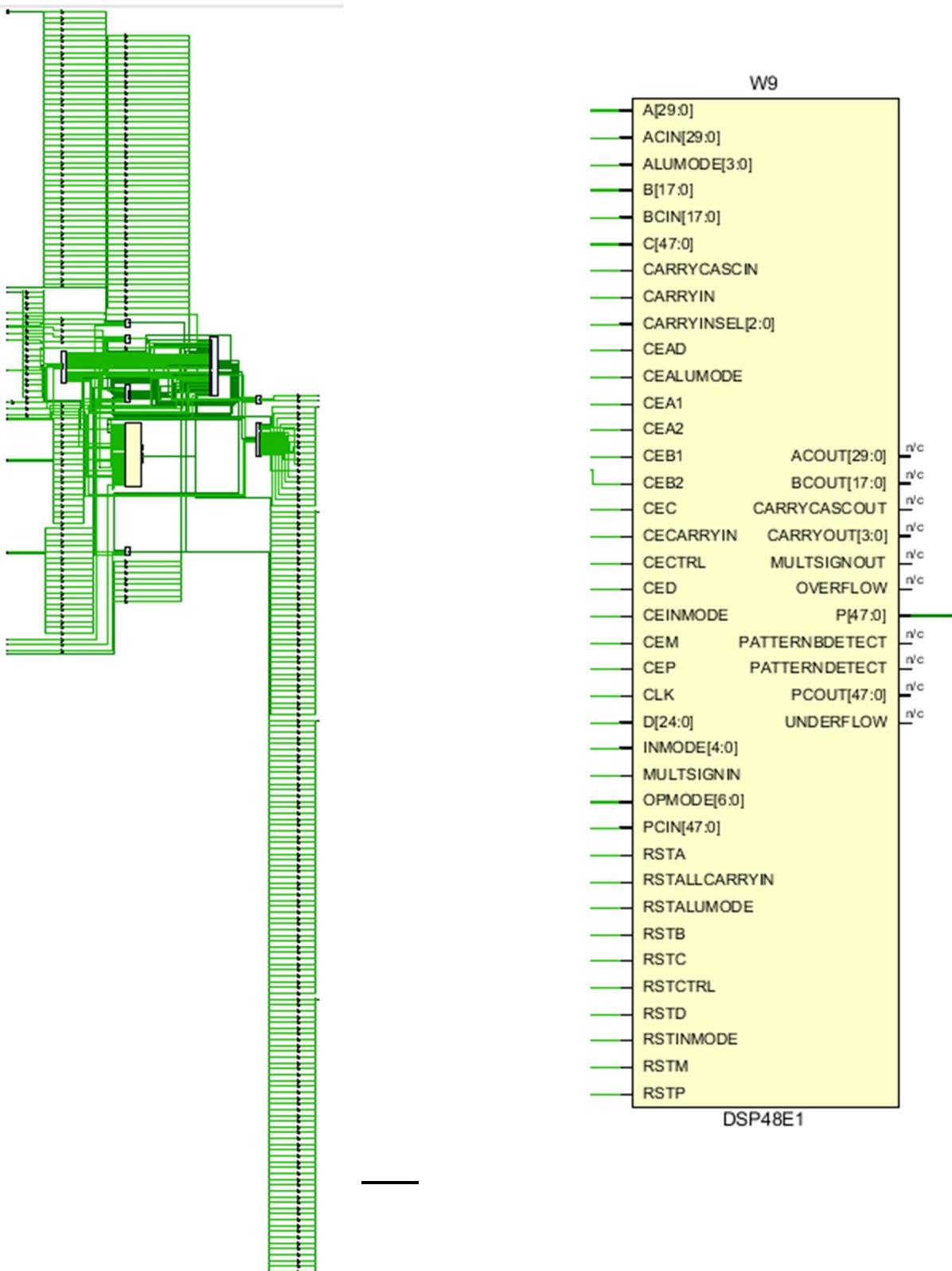
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.172 ns	Worst Hold Slack (WHS): 0.182 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWNS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 106	Total Number of Endpoints: 106	Total Number of Endpoints: 162

All user specified timing constraints are met.



8. Implementation :



Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.980 ns	Worst Hold Slack (WHS): 0.273 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 125	Total Number of Endpoints: 125	Total Number of Endpoints: 181

All user specified timing constraints are met.

Name	1	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
N DSP48A1	181		179	83	181		50	1	327	1
A1_REG (REG_MUX_...	0		18	5	0		0	0	0	0
B1_REG (REG_MUX_...	0		36	11	0		0	0	0	0
C_REG (REG_MUX_...	0		48	14	0		0	0	0	0
CYI (REG_MUX_para...	1		1	1	1		1	0	0	0
CYO_REG (REG_MUX...	0		2	2	0		0	0	0	0
D_REG (REG_MUX_...	0		18	9	0		0	0	0	0
OPMODE_REG (REG_...	180		8	58	180		0	0	0	0
P_REG (REG_MUX_...	0		48	12	0		0	0	0	0

Implementation (91 infos)

Design Initialization (11 infos)

- [Netlist 29-17]* Analyzing 207 Unisim elements for replacement
- [Netlist 29-28]* Unisim Transformation completed in 0 CPU seconds
- [Project 1-479]* Netlist was created with Vivado 2018.2
- [Device 21-403]* Loading part xc7a200tffg1156-3
- [Project 1-570]* Preparing netlist for logic optimization
- [Timing 38-478]* Restoring timing data from binary archive.
- [Timing 38-479]* Binary timing data restore complete.
- [Project 1-856]* Restoring constraints from binary archive.
- [Project 1-853]* Binary constraint restore complete.
- [Project 1-111]* Unisim Transformation Summary:
 No Unisim elements were transformed.
- [Project 1-604]* Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646