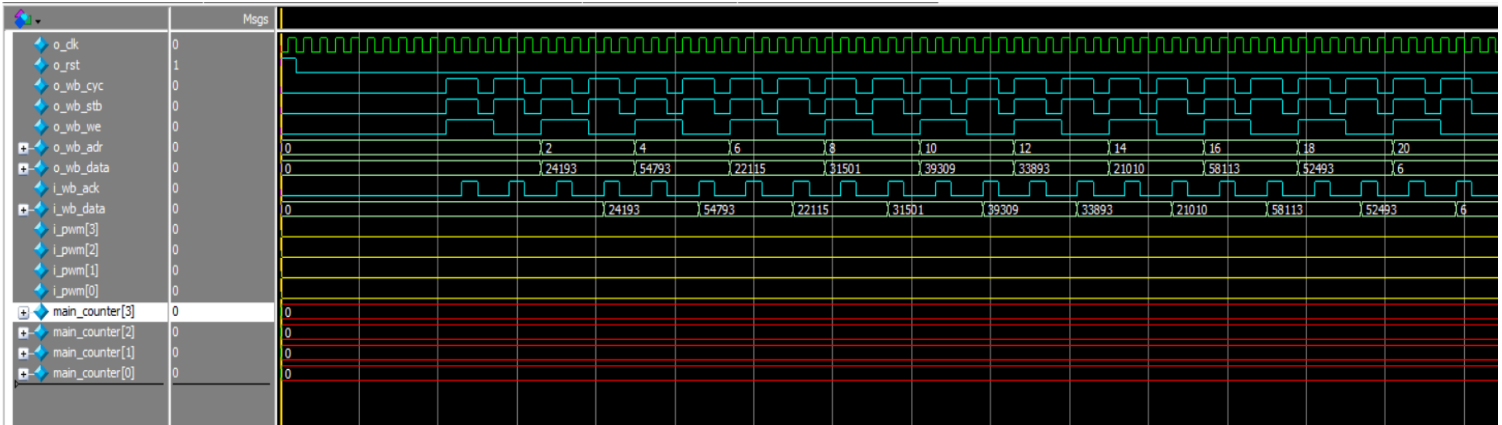


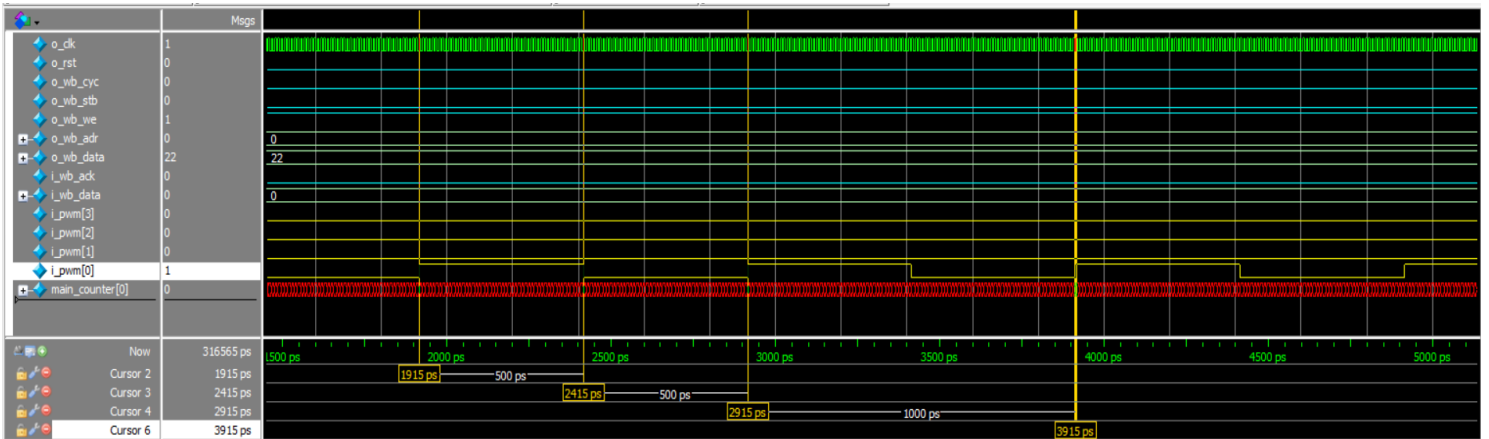
Simulation Results

Clk Cycle = 10 ps .

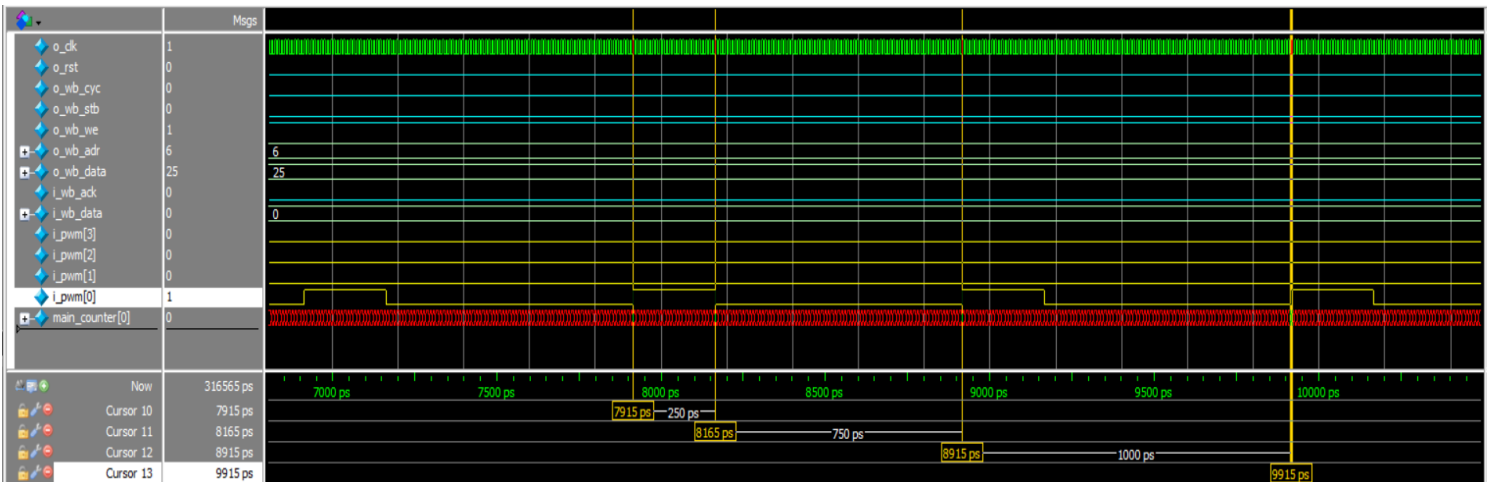
Wishbone read/write operations:



PWM output for DC=50%:



PWM output for DC=25%:



One shot:

The timing diagram displays the following signals and their values over time:

- o_clk**: 1
- o_rst**: 0
- o_wb_cyc**: 0
- o_wb_stb**: 0
- o_wb_we**: 1
- o_wb_addr**: 20
- o_wb_data**: 1
- i_wb_ack**: 0
- i_wb_data**: 0
- i_pwm[3]**: 0
- i_pwm[2]**: 0
- i_pwm[1]**: 0
- i_pwm[0]**: 0
- main_counter[0]**: 1

The diagram also shows a sequence of events where the counter increments and the PWM signal changes state. A yellow vertical line marks a specific time point.

Signal	Value
o_clk	1
o_rst	0
o_wb_cyc	0
o_wb_stb	0
o_wb_we	1
o_wb_addr	20
o_wb_data	1
i_wb_ack	0
i_wb_data	0
i_pwm[3]	0
i_pwm[2]	0
i_pwm[1]	0
i_pwm[0]	0
main_counter[0]	1

Continuous:

The timing diagram displays the following signals and their values over time:

- q_clk**: 1 (Clock signal)
- q_rst**: 0 (Reset signal)
- q_wb_cyc**: 0 (Write cycle signal)
- q_wb_stb**: 0 (Write strobe signal)
- q_wb_we**: 1 (Write enable signal)
- q_wb_adr**: 0 (Write address signal)
- q_wb_data**: 12 (Write data signal)
- l_wb_ack**: 0 (Write acknowledge signal)
- l_wb_data**: 0 (Write data signal)
- l_pwm[3]**: 0 (PWM signal 3)
- l_pwm[2]**: 0 (PWM signal 2)
- l_pwm[1]**: 0 (PWM signal 1)
- l_pwm[0]**: 1 (PWM signal 0)
- main_counter[0]**: 0 (Main counter signal)

The diagram includes a legend on the left, a main signal area with waveforms, and a bottom section with time markers and cursor positions:

- Now**: 316565 ps
- Cursor 3**: 69495 ps
- Cursor 11**: 70815 ps
- Cursor 12**: 71895 ps

Time markers and intervals are also shown:

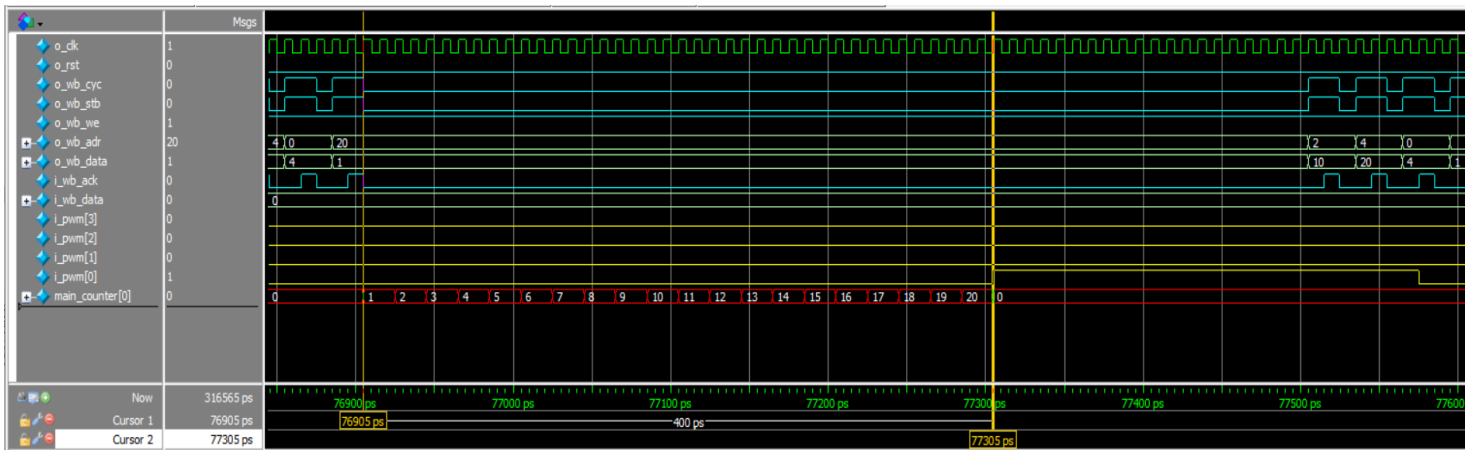
- 69540 ps
- 70000 ps
- 70500 ps
- 71000 ps
- 71500 ps
- 72000 ps
- 1320 ps (interval between 69495 ps and 70815 ps)
- 1080 ps (interval between 70815 ps and 71895 ps)

Down Clocking with Divisor=2:

Testing Down Clocking

Testing Down Clocking with Divisor = 2 , timer mode

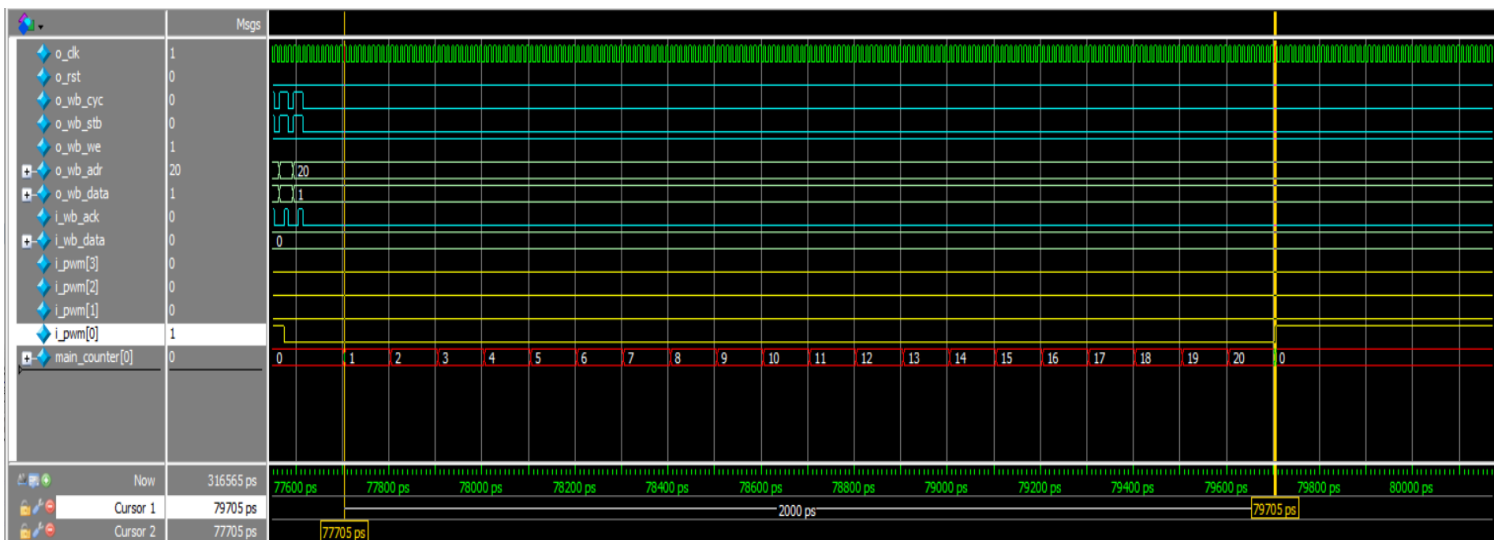
? INTERRUPT GENERATED! Period: 20 , divisor: 2



Down Clocking with Divisor=10:

Testing Down Clocking with Divisor = 10 , timer mode

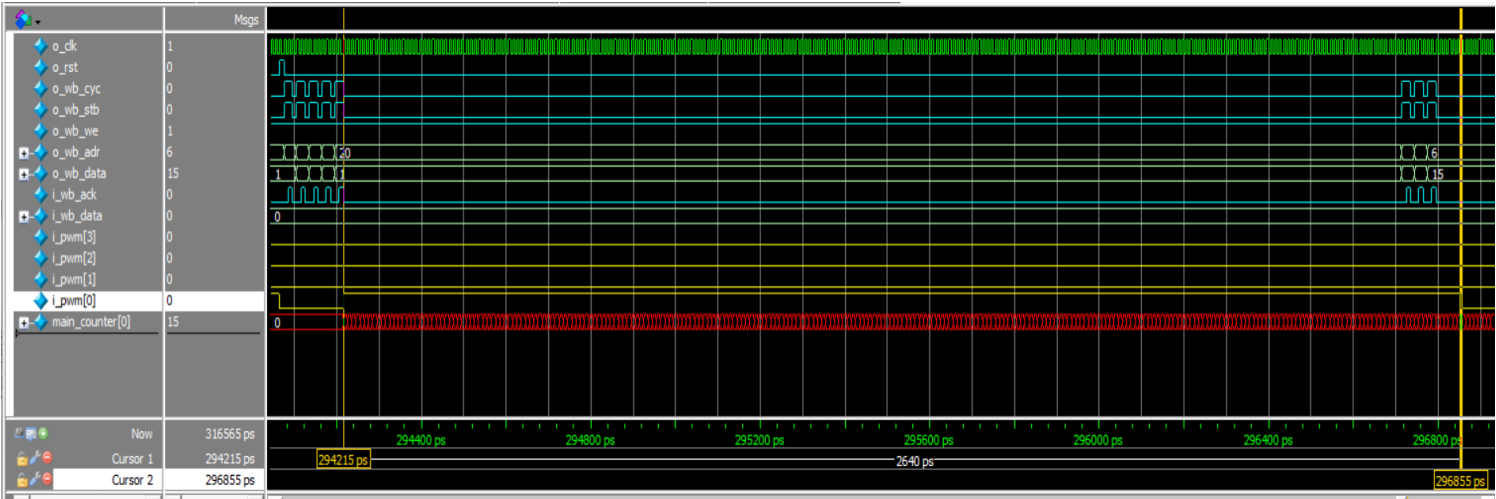
? INTERRUPT GENERATED! Period: 20 , divisor: 10



Additional Features :

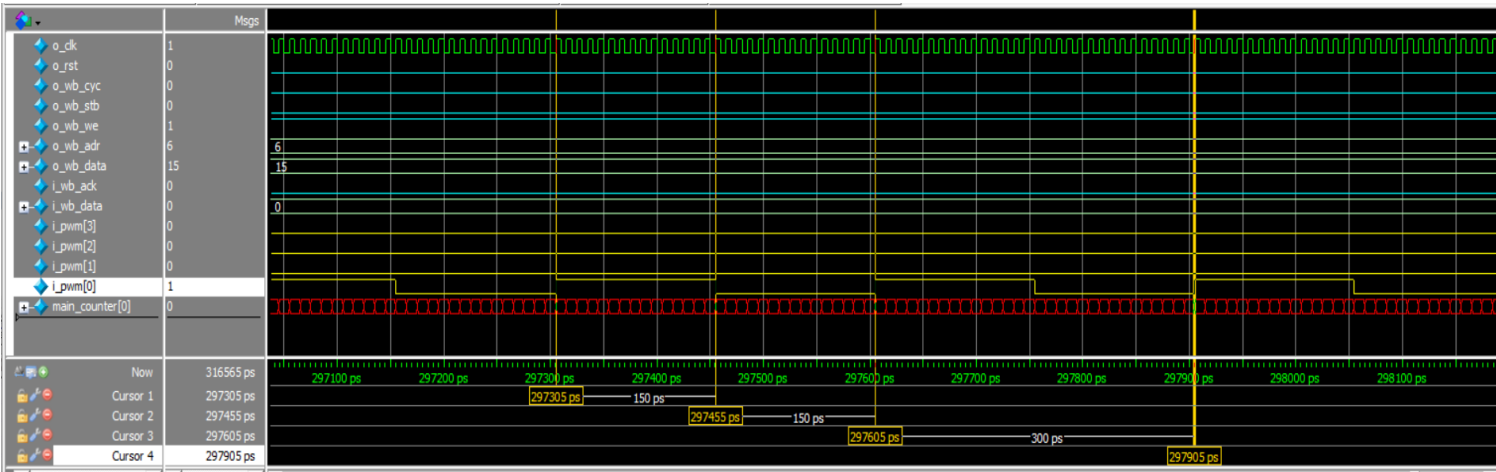
DC > Period:

Testing Edge Cases
Sub-test: Duty Cycle > Period
Expected: PWM should be always HIGH



invalid Divisor:

Sub-test: Divisor = 0
Expected: Should work as Divisor = 1



Multi-Channel PWM:

- $i_pw[0]$ & $i_pw[1]$ has the same period = 200 but different duty cycle $DC[0]=100$ & $DC[1]=50$, as shown by purple cursor.
- $i_pw[2]$ has period = 100 & $DC[2]=25$, $i_pw[3]$ has period = 50 & $DC[3]=20$.

