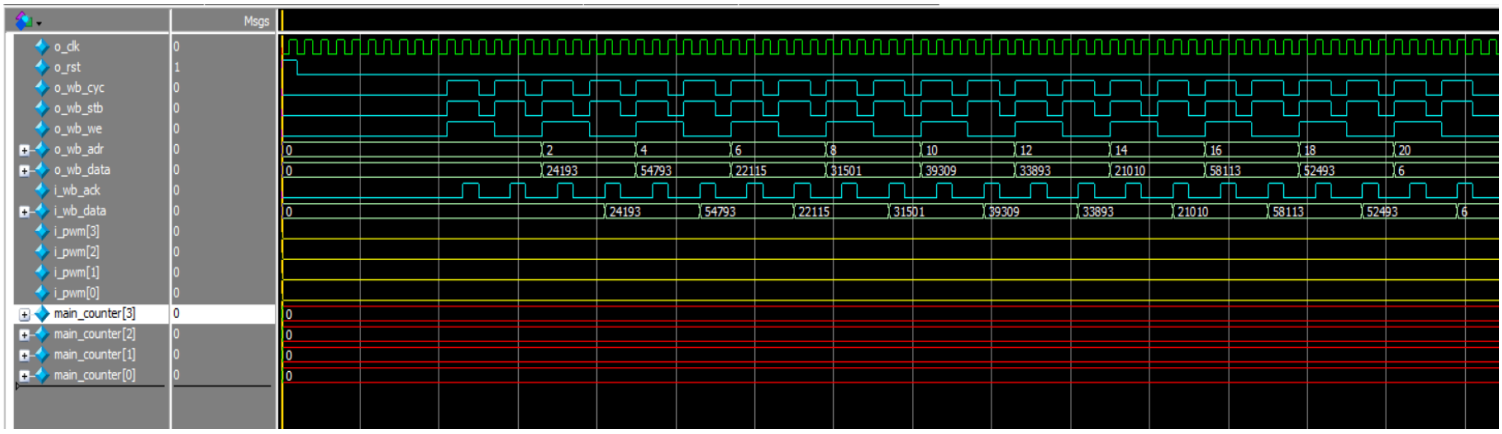
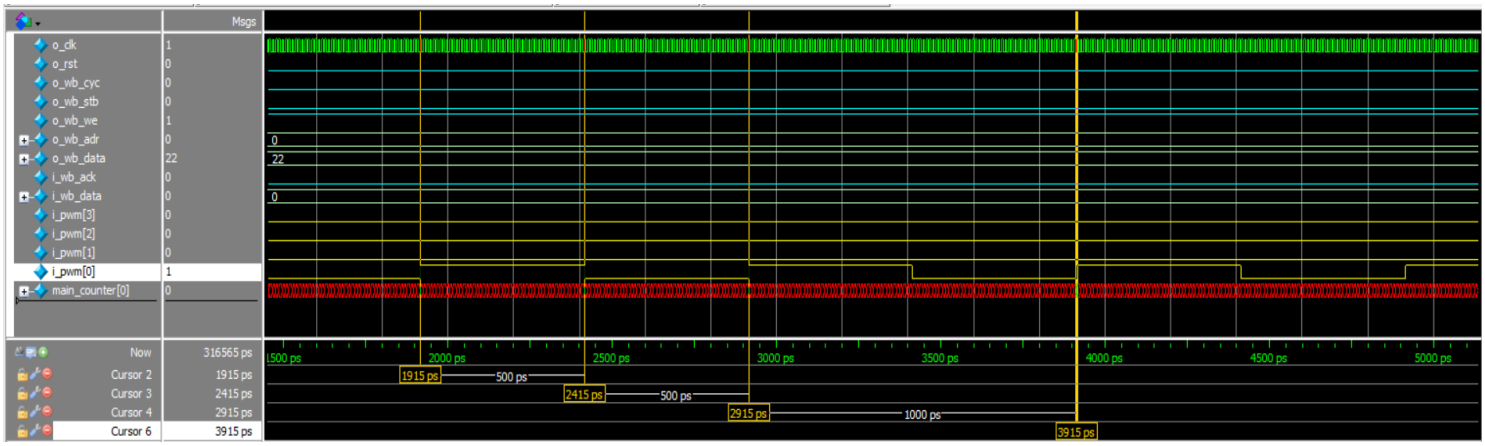
Simulation Results

Clk Cycle = 10 ps .

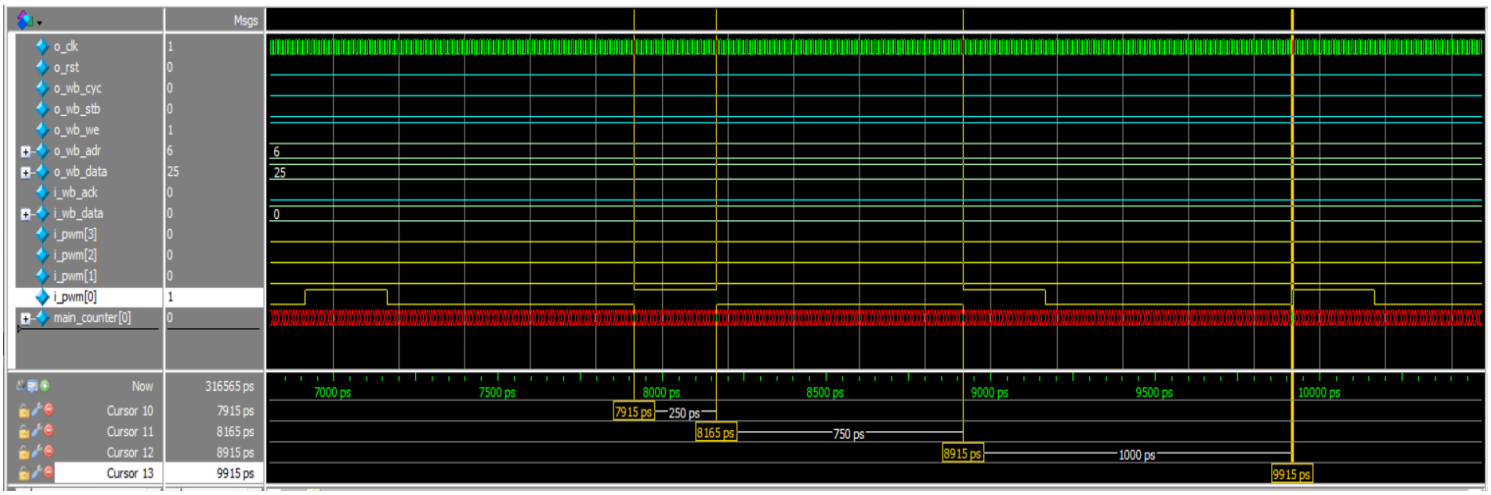
Wishbone read/write operations:



PWM output for DC=50%:



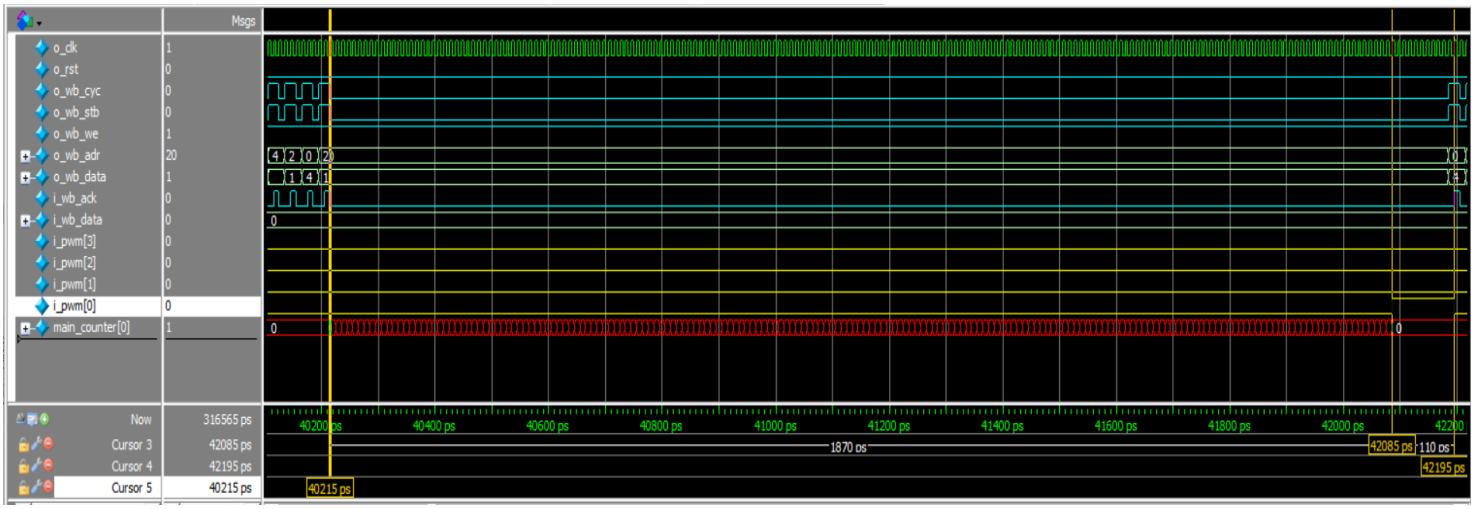
PWM output for DC=25%:



Timer Mode interrupt generation and clearing:

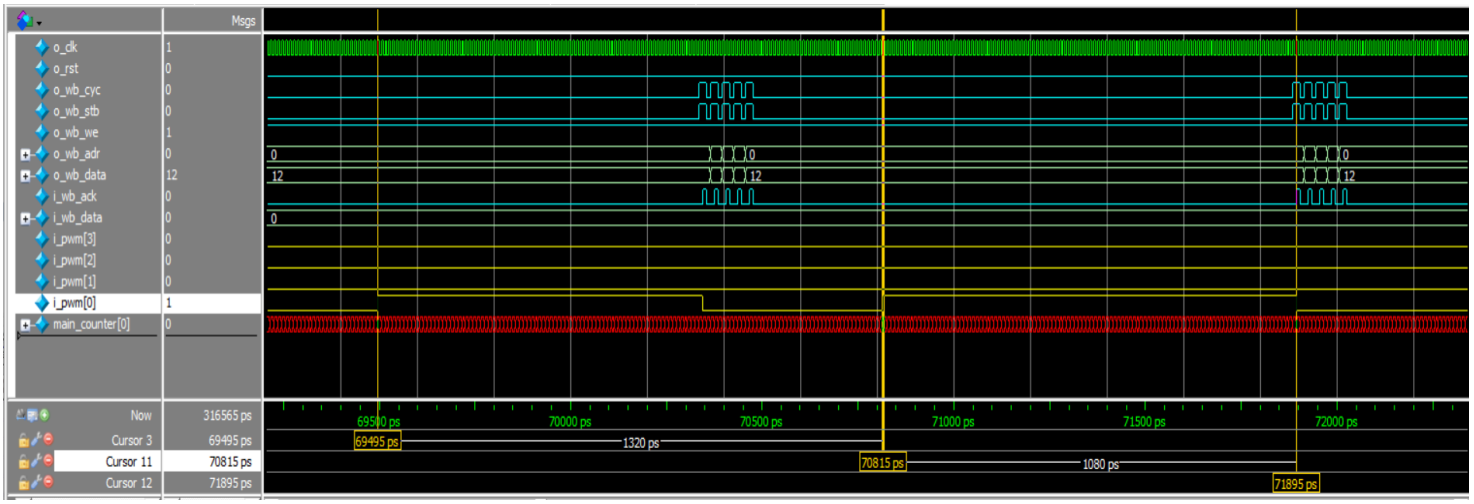
One shot:

```
? INTERRUPT GENERATED! Period:    187
? INTERRUPT CLEARED!   Period:    187
```



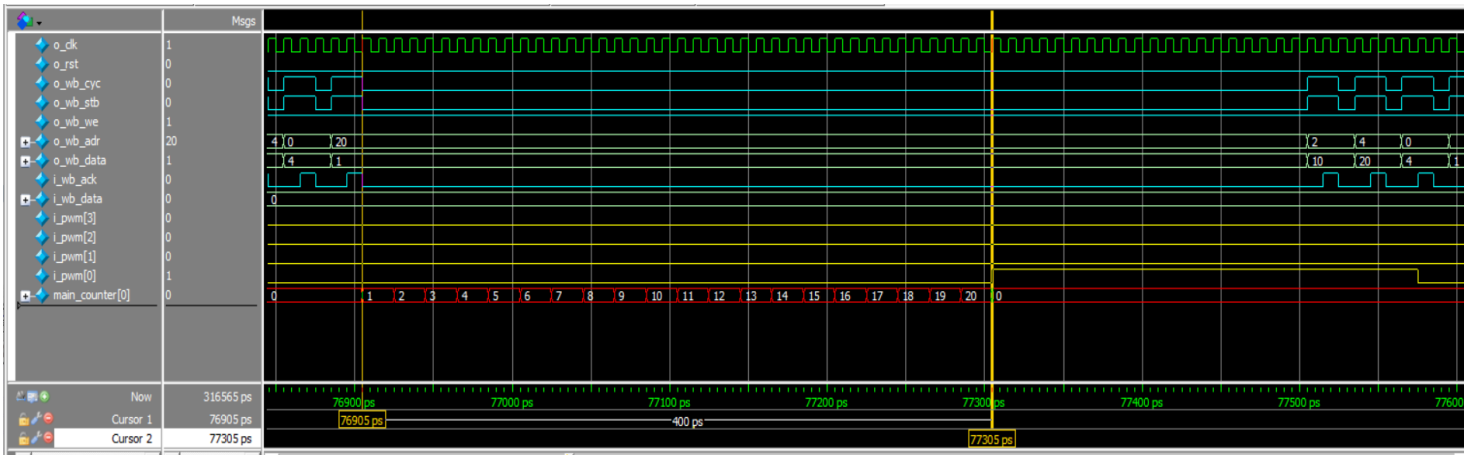
Continuous:

```
? INTERRUPT GENERATED! Period:    131
? INTERRUPT CLEARED!   Period:    131
```



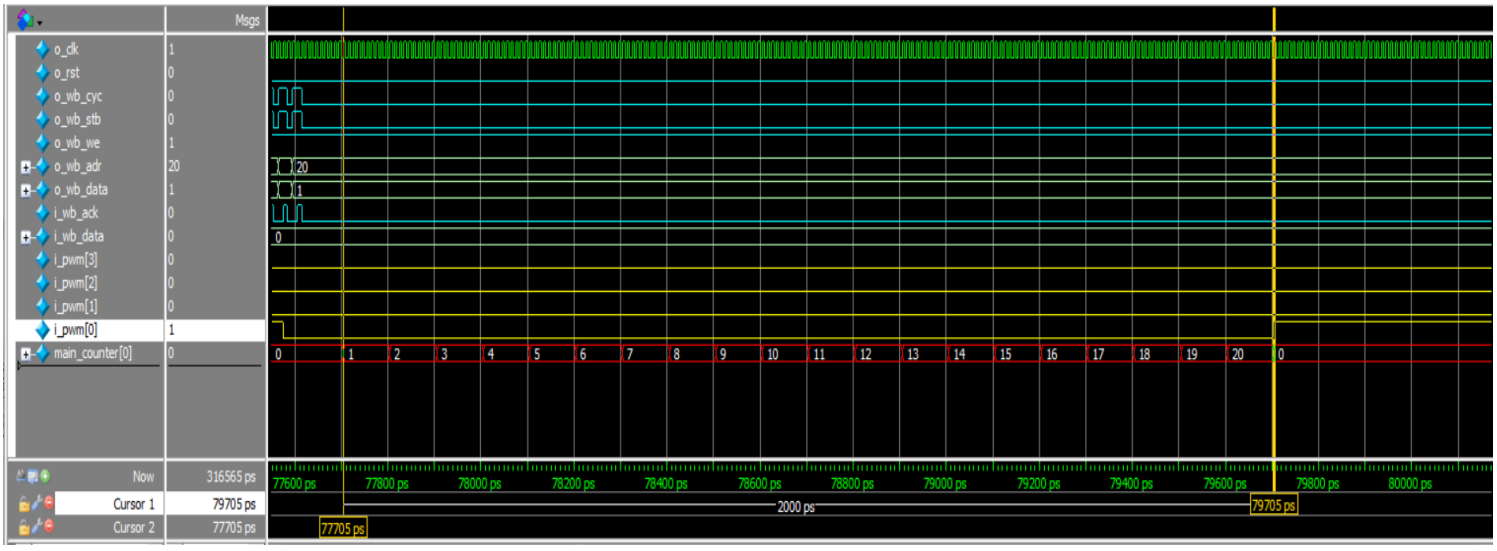
Down Clocking with Divisor=2:

```
Testing Down Clocking
Testing Down Clocking with Divisor = 2 , timer mode
? INTERRUPT GENERATED! Period:    20 , divisor:     2
```



Down Clocking with Divisor=10:

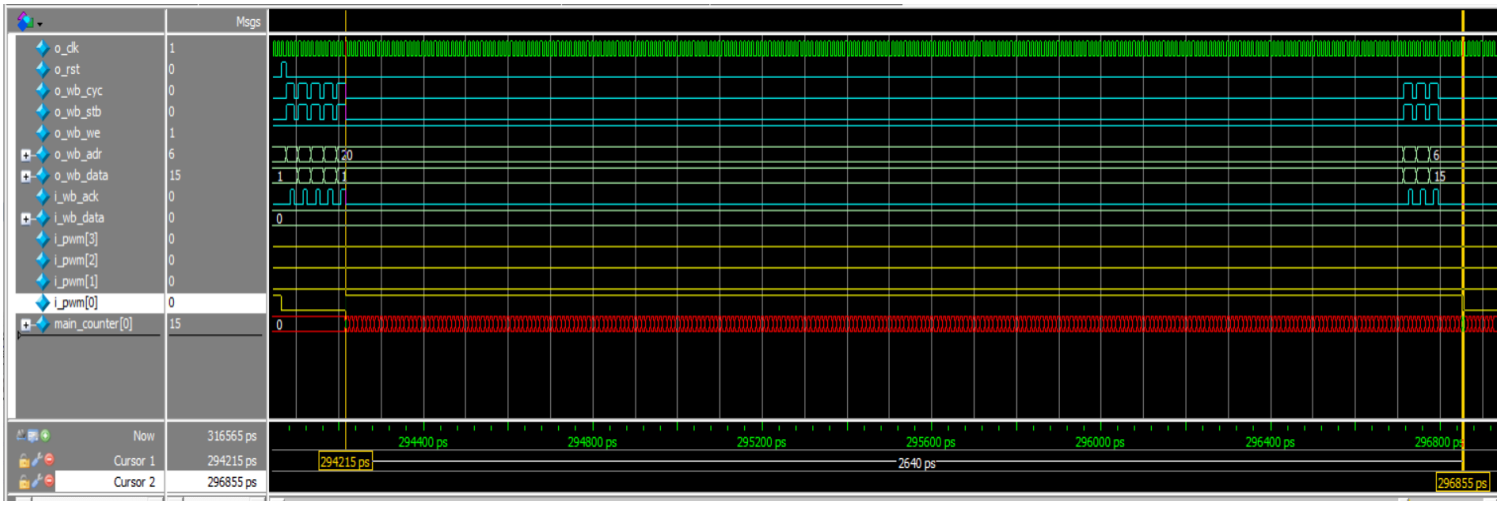
```
Testing Down Clocking with Divisor = 10 , timer mode
? INTERRUPT GENERATED! Period:    20 , divisor:    10
```



Additional Features :

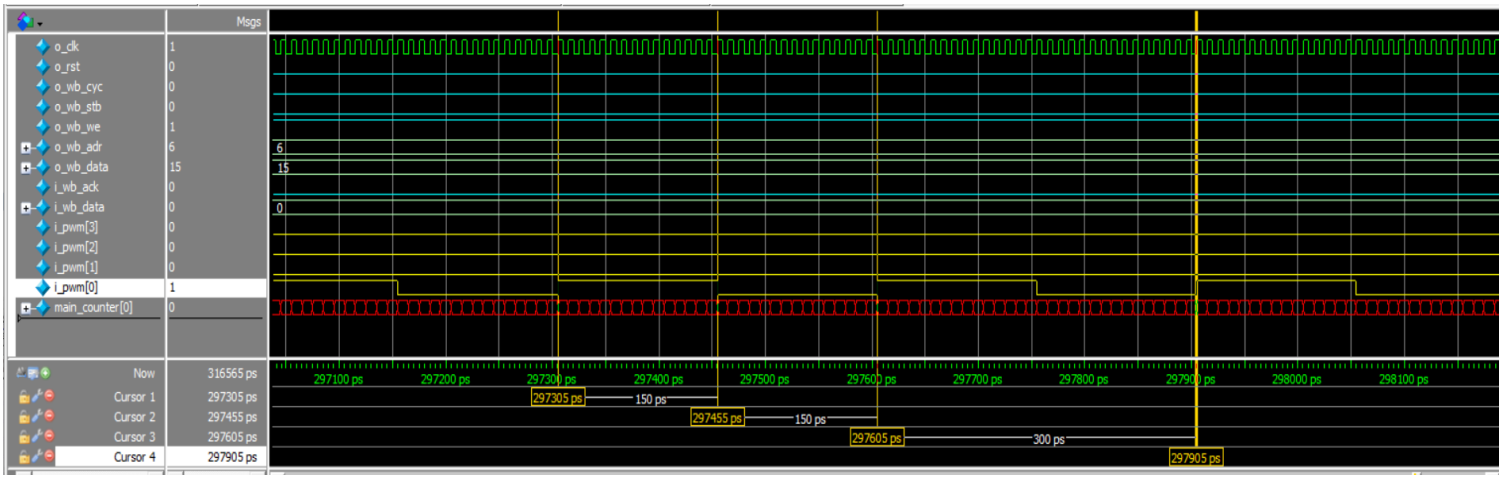
DC > Period:

```
Testing Edge Cases
Sub-test: Duty Cycle > Period
Expected: PWM should be always HIGH
```



invalid Divisor:

```
Sub-test: Divisor = 0
Expected: Should work as Divisor = 1
```



Multi-Channel PWM:

- i_pw[0] & i_pw[1] has the same period = 200 but different duty cycle DC[0]=100 & DC[1]=50, as shown by purple cursor.
- i_pw[2] has period = 100 & DC[2]=25 , i_pw[3] has period = 50 & DC[3]=20.