Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

Digital Electronics and Computer Organization Lab

Report 2

Sequential Logic Circuits

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I. Abstract

The aim of this experiment is to understand the differences between combinational and sequential Logic circuits, and the applications of various memory units. Learn about the operating principles and applications of various flip-flops, constructing counters with JK flip-flops, and understand the concepts of synchronous and asynchronous counters.

II. Tables

A. Table of Content

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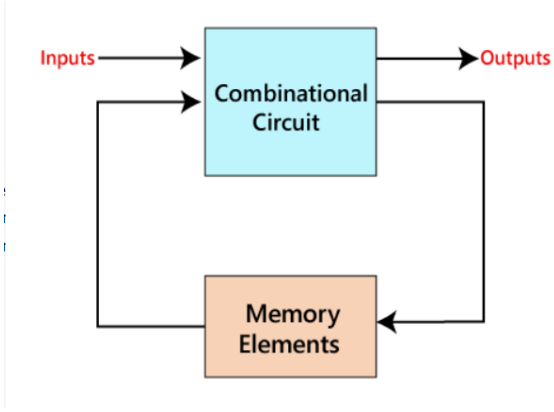
III. Theory

A. Sequential Circuits

Sequential circuits Output is a function of Inputs and internal Memory, there is an internal memory that stores the state of the circuit, Time is very important because memory changes with time, there are Two Types of Sequential Circuits: 1. Synchronous Sequential Circuit: Uses a clock signal as an additional input, Changes in the memory elements are controlled by the clock, Changes happen at discrete instances of time. 2. Asynchronous Sequential Circuit: No clock signal, Changes in the memory elements can happen at any instance of time[1].



[2]

Figure 1:block diagram of a sequential circuit

B. Latches

1. The SR (Set-Reset) Latch

a) SR latch with NOR gates

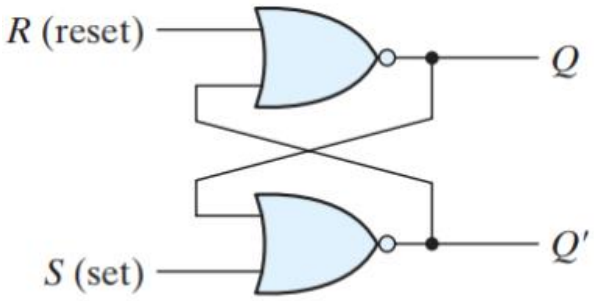
An SR Latch can be built using two cross-coupled NOR gates, with two inputs: S (Set) and R (Reset), and two outputs: Q and ~Q.

If S = 1 and R = 0 then Set (Q = 1, ~Q = 0)

If S = 0 and R = 1 then Reset (Q = 0, ~Q = 1)

When S = R = 0, Q and ~Q are unchanged

When S = R = 1, Q and ~Q are undefined (should never be used)[3].



[3]

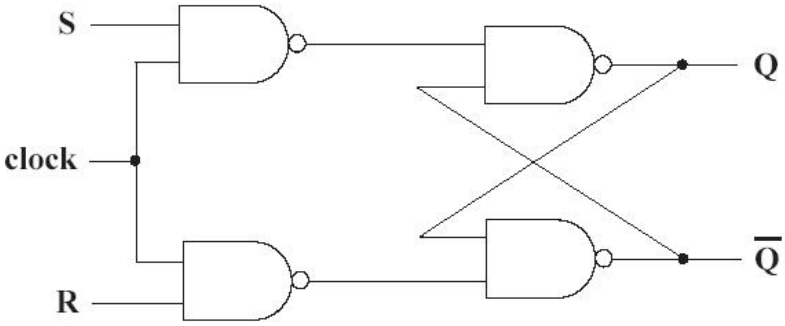
Figure 2:SR latch with NOR gate

S	R	Q	~Q	state
1	0	1	0	Set
0	0	1	0	
0	1	0	1	
0	0	0	1	Reset
1	1	0	0	Undefined

Table 1: SR latch with NOR gate Truth table.

b) RS latch with control input

In this latch an additional Clock (enable) input signal C is used it controls when the state of the latch can be changed, When C=0, the S and R inputs have no effect on the latch The latch will remain in the same state, regardless of S and R when C=1, then normal SR latch operation[3].



[4]

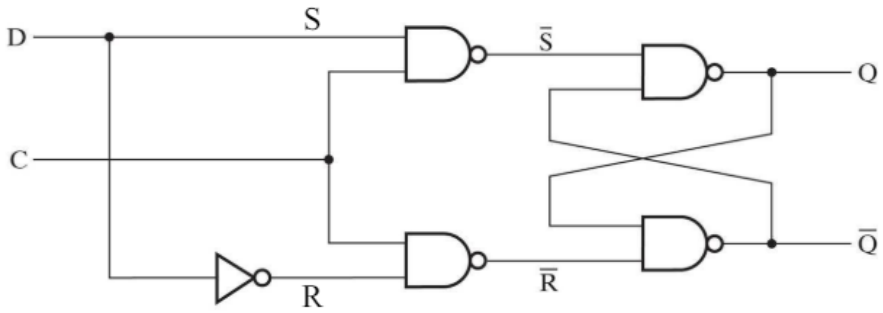
Figure 3: RS latch with control input.

INPUT			OUTPUT		State
C	S	R	Qn+1	$\bar{Q}$	
0	X	X	Qn	$\bar{Q}$	No Change/ Memory
1	0	0	Qn	$\bar{Q}$	No Change/Memory
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	0	0	Indeterminate

Table 2:RS latch with control truth table.

2. The D Latch

In D Latch there is one data input D, where $S = D$ and $R = D$, and eliminate the undefined condition of the indeterminate state in the RS latch. When $C = 1$, $R = S = D$



[4]

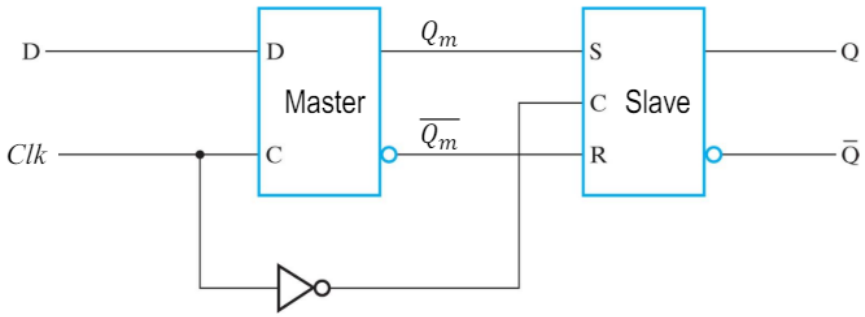
Figure 4: D-Latch.

C	D	Next State Of Q
0	X	No change
1	0	Q=0; Reset
1	1	Q=1; Set

Table 3:D latch truth table.

C. Flip-Flops

A Flip-Flop is a better memory element for synchronous circuits, it solves the problem of latches in synchronous sequential circuits, A latch is sensitive to the level of the clock, but flip-flop is sensitive to the edge of the clock, it called an edge-triggered memory element, because it changes it output value at the edge of the clock[3].

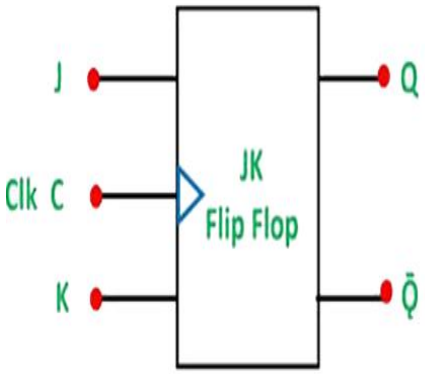


[3]

Figure 5:D flip flop implemented with two D latches

Input	Output		State
D	Qn+1	~Q	
0	0	1	Reset
1	1	0	Set

Table 4:D flip flop truth table

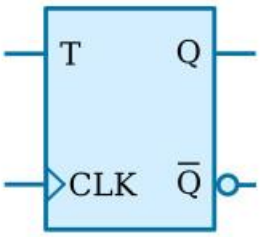


[5]

Figure 6:JK flip flop

Input		Output	State
J	K	Qn	
0	0	Qn	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}$	Complement

Table 5:JK flip flop truth table



[6]

Figure 7:T flip flop

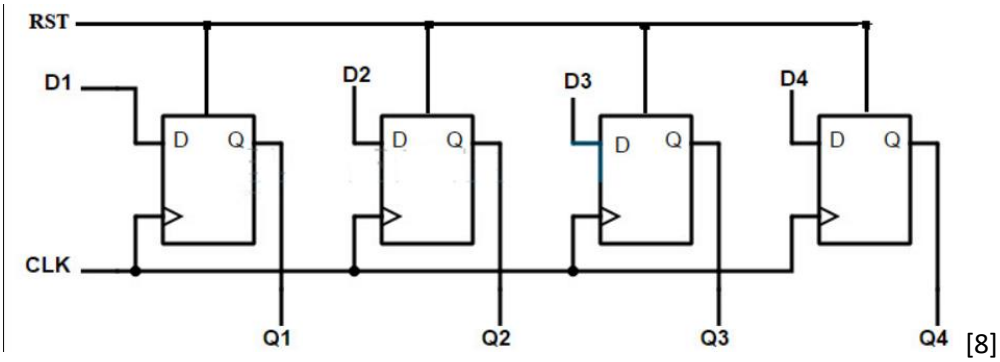
Input	Output	State
T	Qn+1	
0	Qn	No Change
1	$\overline{Q}$	Complement

Table 6: T flip flop truth table

D. Registers

1. Simple Register

A Register is a collection of flip flops, the storage capacity increased by grouping more than one flip flops. If we want to store an n-bit word, we have to use an n-bit register containing n number of flip flops[7].

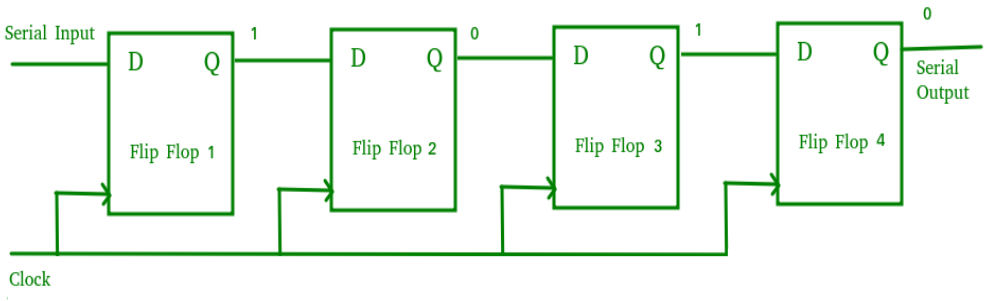


[8]

Figure 8:4-bit Register

2. Shift Register

Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops in a chain so that the output from one flipflop becomes the input of the next flip-flop[9].

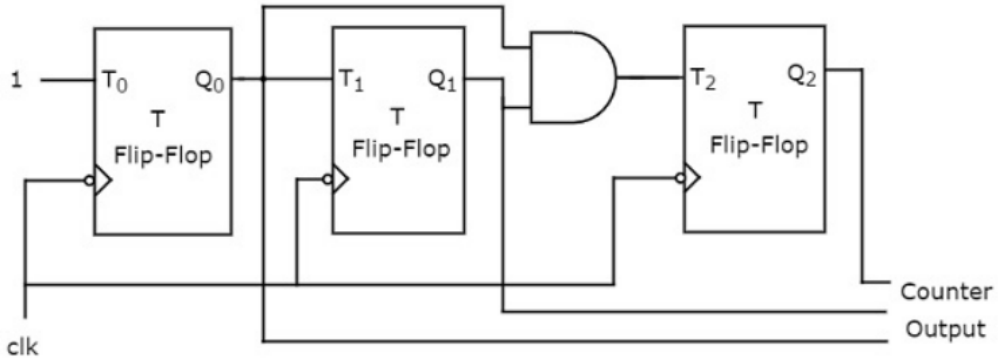


[9]

Figure 9: 4-bit shift- right register.

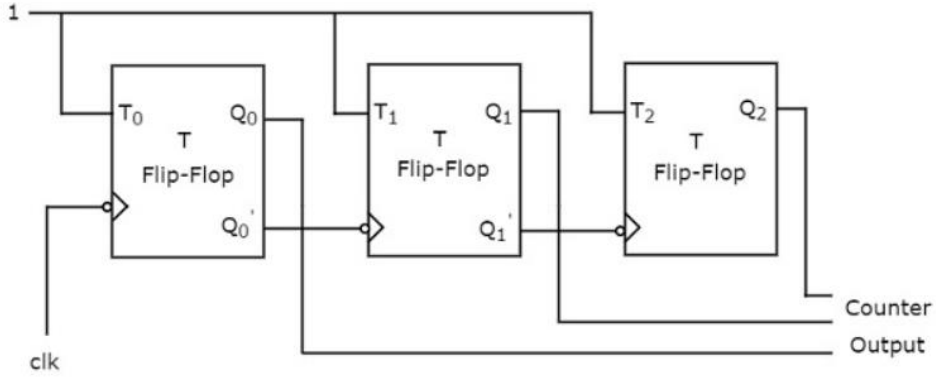
E. Counters

Counter is a special-purpose register, it is a register that goes through a prescribed sequence of states, there are two types of counters based on the flip-flops that are connected in: Ripple and Synchronous counters. In ripple flip-flops do not receive the same clock signal, but in Synchronous flip-flops receive the same clock signal[10].



[10]

Figure 10: 3-bit synchronous counter



[10]

Figure 11: 3-bit ripple counters

IV. Procedure

A. Encoder Circuit

1. Constructing RS latch with Basic Logic Gates

The circuit can be constructed using the Module IT-3008 block flip flop circuit. From the RS latch circuit, it will have 2 inputs and 2 outputs. The first input A3 connected to Switch 1, and input A4 connected to Switch 2, and the outputs F6 and F7 to Logic Indicator L1 and L2. Also, we Connect +5V of module IT-3008 to the +5V output of fixed power supply section of IT-3000. The figure below shows it clearly.

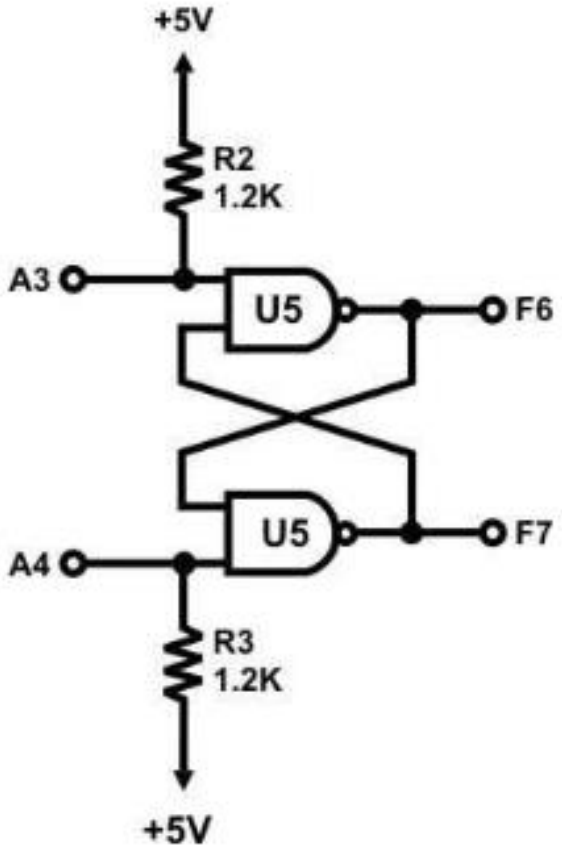


Figure 12:wiring diagram RS latch.

Below we find figure for the circuit connection RS latch in the lab.

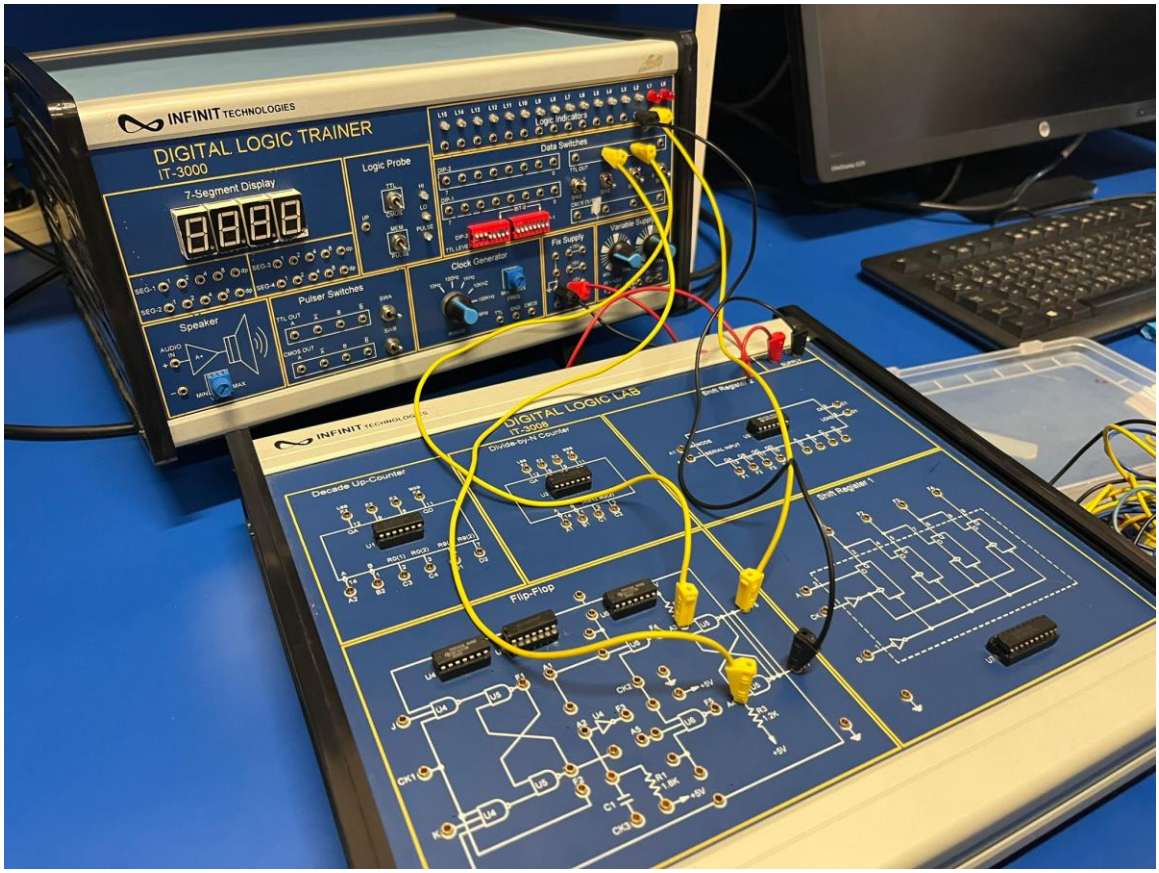


Figure 13:wiring connection RS latch

Inputs		Outputs	
A3	A4	F6	F7
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1

Table 7:Data for RS latch

After testing the RS latch, and collect this data we verify that if both inputs put 0, the latch produce undefined outputs, Otherwise, the output is correct. and same as RS latch truth table.

2. Constructing RS latch with control input

In this part the same block used. First, +5V of the module connected to the +5V output of the fixed power supply, then the inputs A1 and A2 to SW1, SW2. after that outputs F6 and F7 connected to Logic indicators L1 and L2.

Below figure of the RS latch with control input diagram.

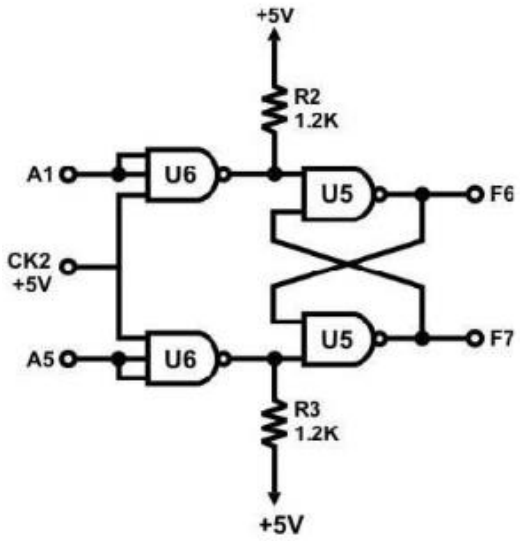


Figure 14: RS Latch with control input.

Here we find figure for the circuit connection in the lab.

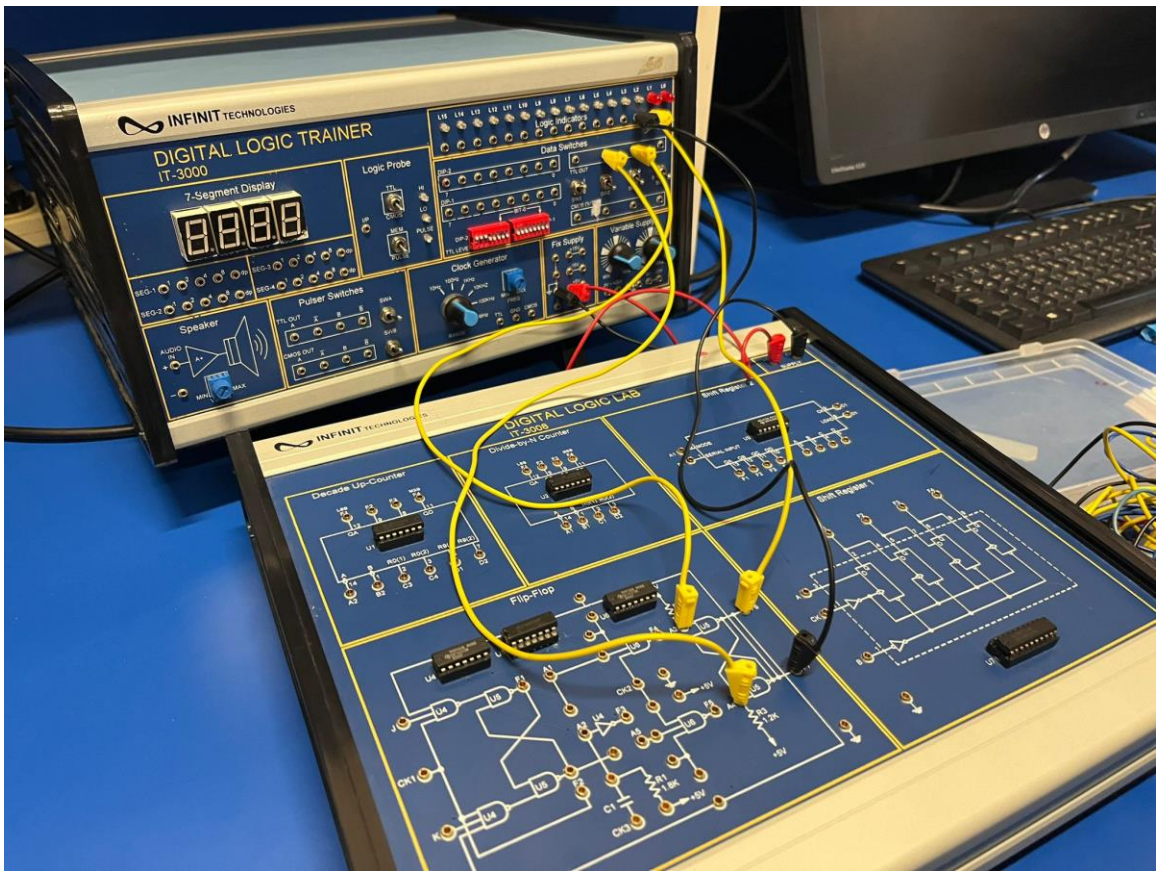


Figure 15:wiring connection of RS Latch with control input.

Inputs		Outputs	
A1	A5	F6	F7
0	0	0	1
0	1	0	1
1	0	1	0
1	1	1	1

Table 8:Data for of RS Latch with control input.

The table lists various combinations of inputs, In the operation of the latch, when both inputs are active, it gives undefined outputs, Otherwise, the output is correct. And the data were collected equals to the latch truth data, so that's mean the circuit done correctly.

3. Constructing D latch with RS latch

In this section of the experiment, also same Block of module IT-3008 used. So, first +5V of the module connected to the +5V output of the fixed power supply, input A1 to Data Switch SW1, and CK2 to SWA A second, we connect outputs F6 to Logic Indicators L1. Finally, the input sequences for A1 followed and output states recorded. Below figure of the circuit diagram inputs and outputs.

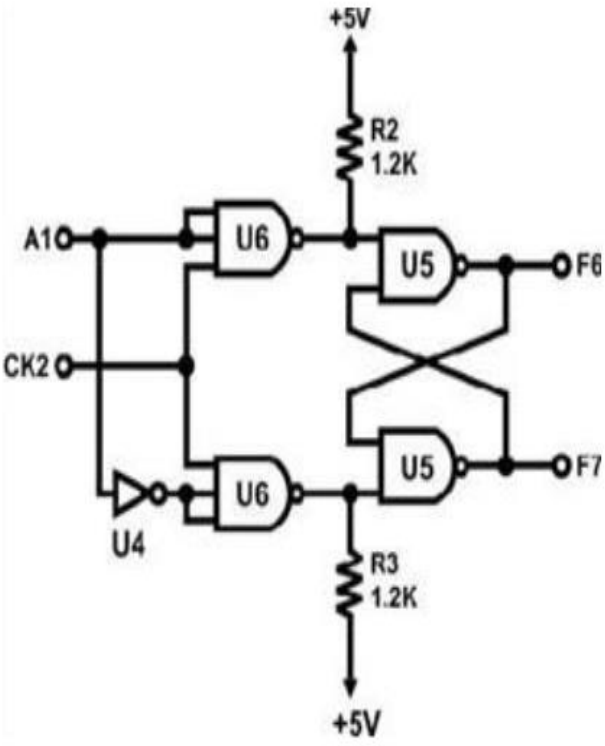


Figure 16: D latch.

Here we find figure for the circuit connection in the lab.

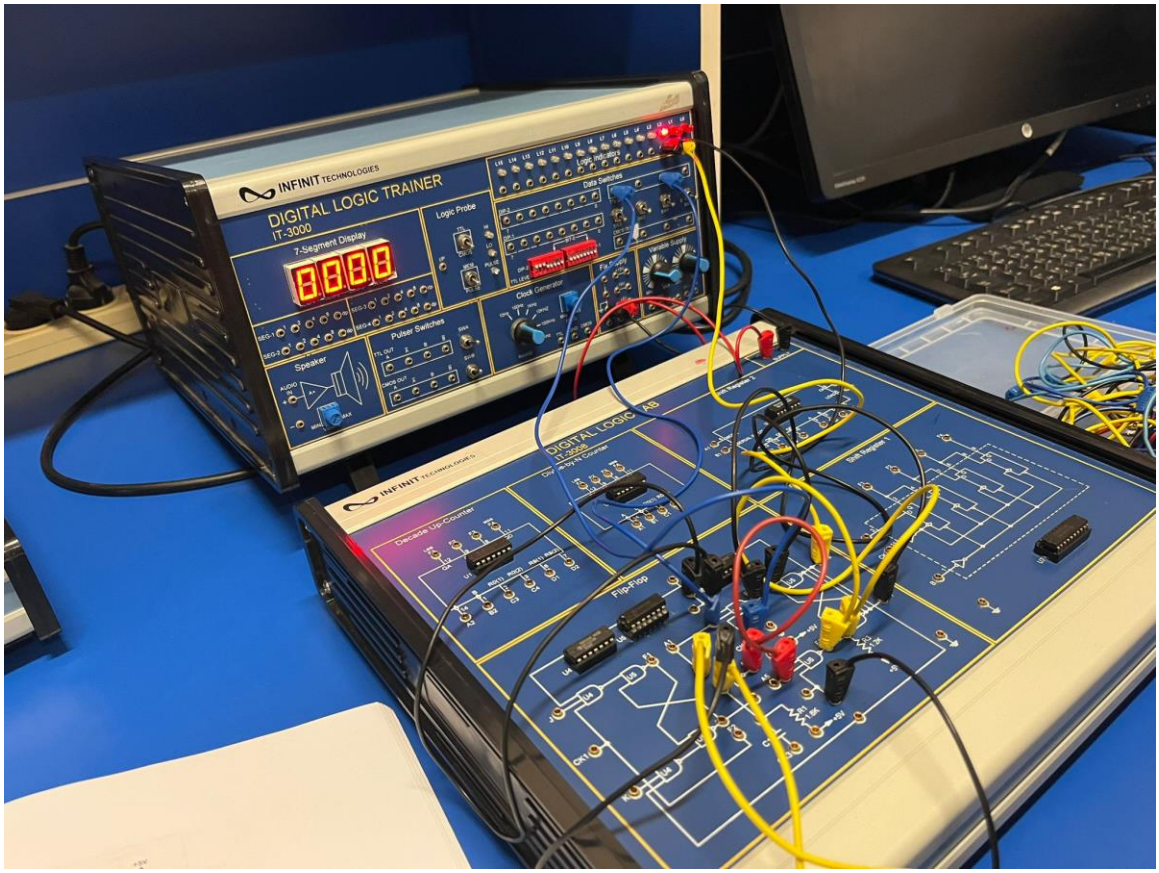


Figure 17:wiring connection of D latch

Inputs		Outputs
CK2	A1	F6
0	0	No change
0	1	No change
⎍	0	0
⎍	1	1

Table 9:Data for D latch.

From the collected table the D latch activates only CK2 input is active, and when it active it ensures that no undefined state. And actually, this is the D latch job.

4. Constructing JK latch with RS latch

Also, same block of module IT-3008 will be uses in this part, so first, CK2 connected to SWB B output, A1 to SW0, A5 to SW1, F6 to L1 and the feedback as shown in the figure bellow. Finally, the input sequences followed and output states recorded.

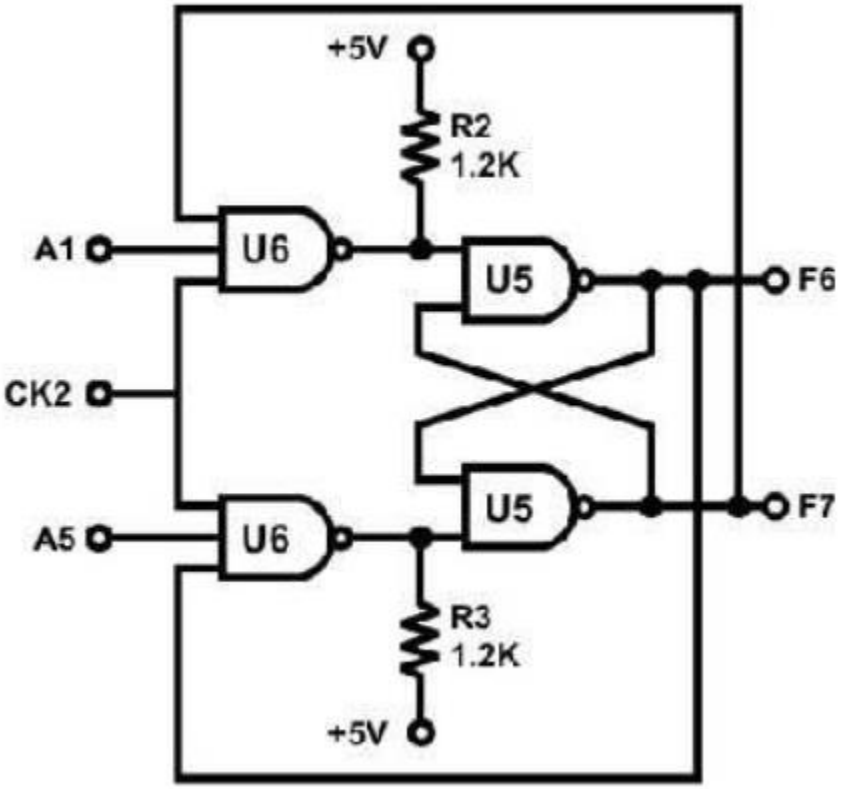


Figure 18: JK Latch.

Here we find figure for the circuit connection in the lab.

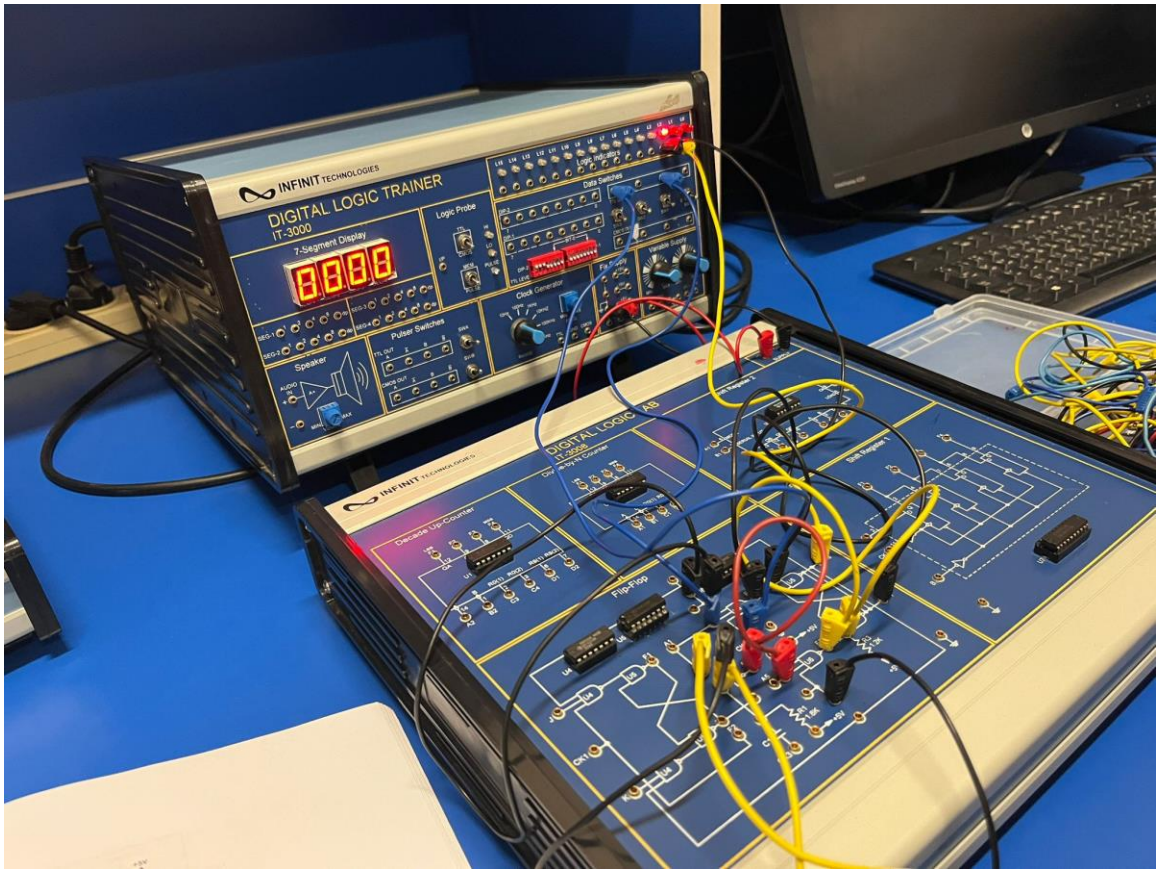


Figure 19:wiring connection of JK latch

Inputs			Output	Status
CK2	A1	A5	F6	
⎍	1	0	1	Set
⎍	0	0	1	No Change
⎍	1	1	0	Complement
⎍	1	0	1	Set
⎍	0	0	1	No Change
⎍	0	1	0	Reset
⎍	1	1	1	Complement

Table 10:Data for JK latch.

From the collected table, when both J and K inputs are 0, the latch holds its state (Qn+1 = Qn). When J is 0 and K is 1, the latch resets (Qn+1 = 0). When J is 1 and K is 0, the latch sets (Qn+1 = 1). When both J and K are 1, the latch toggles (Qn+1 = Qn).

5. Constructing JK Flip-flop with master- slave RS latches

Also, same block of module IT-3008 will be uses in this part, so first, CK1 connected to SWA A output, J to SW1, K to SW0 F1, F2, F6, F7 to L3, L2, L1 and L0, respectively. Finally, the input sequences followed and output states recorded.

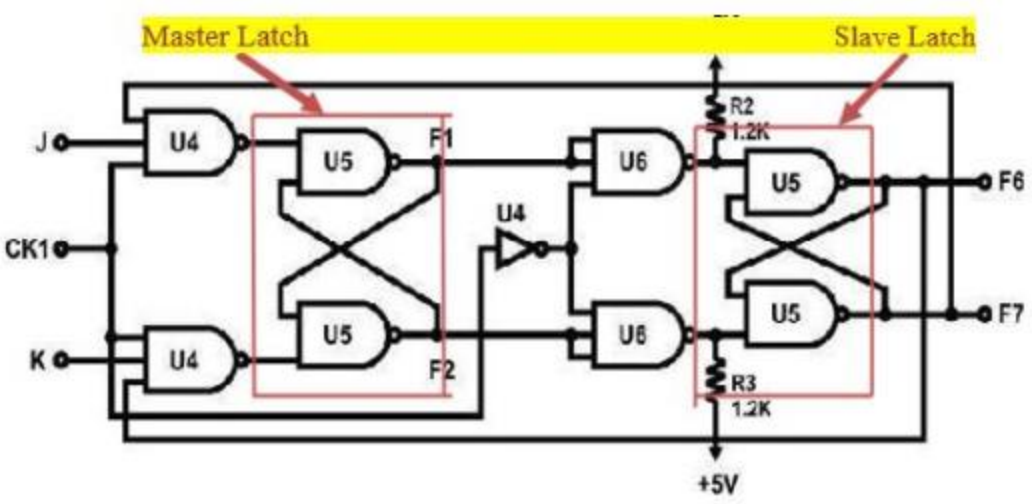


Figure 20:JK Flip-Flop.

Here we find figure for the circuit connection in the lab.

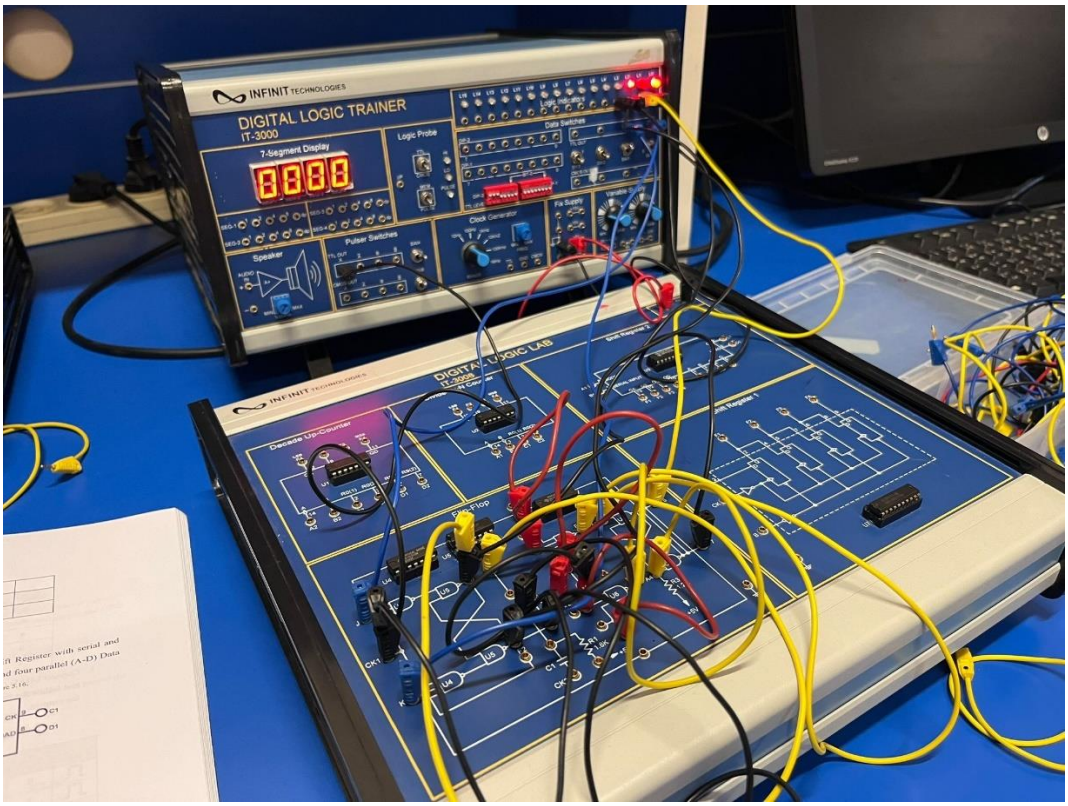


Figure 21:wiring connection of JK flip flop

Inputs			Outputs			
CK1	K	J	F1	F2	F6	F7
⎍	0	0	1	0	1	0
⎍	0	1	1	0	1	0
⎍	1	0	0	1	0	1
⎍	1	1	1	0	1	0
⎍	1	1	0	1	0	1

Table 11:Data for JK flip flop

From the collected table, when CK1 = 1, master latch is activated while slave latch is deactivated. This means that J and K signals can now change the state of the latch-1, however, the internal state of the latch-2 cannot be changed. If J = 1, K = 0 the output of the latch-1 is 1 (Q=1). And if CK1 = 0, latch-1 deactivates and latch-2 is activated. The latch-2 captures the output of latch-1 while latch-1 RETAIN the state it had when CK1 = 1. The output of latch-1 was Q=1 (and Q = 0) so, the input to latch 2 is again S = 1 and R = 0. Hence the output of latch-2 is again Q = 1. Since the latch-1 is disabled, nothing can enter this flip-flop. When CLK = 1 again, the latch-1 is enabled while latch-2 is disabled again. Since the latch-2 is disabled, the latch-2's state is unchanged while latch-1 can change its state.

B. Registers.

1. Constructing Shift Register with D Flip-Flops

In this section of the experiment, Block Shift Register 1 of module IT-3008 will be used. So, first +5V of the module will be connected to the +5V output of the fixed power supply, and B (clear) to SW0, A (I/P) to SW1, CK to SWA A output, F1, F2, F3, F4 to L1, L2, L3, L4, respectively. Finally, SW0 turned to 0 to clear B and then SW0 to 1, then the input sequence for A(I/P) followed and output states recorded. Below figure of the Shift Right Register diagram inputs and outputs.

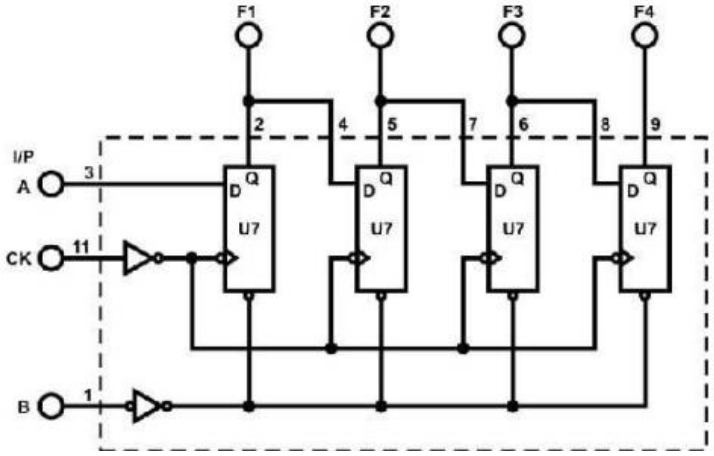


Figure 22: Shift Right Register.

Here we find figure for the circuit connection in the lab.

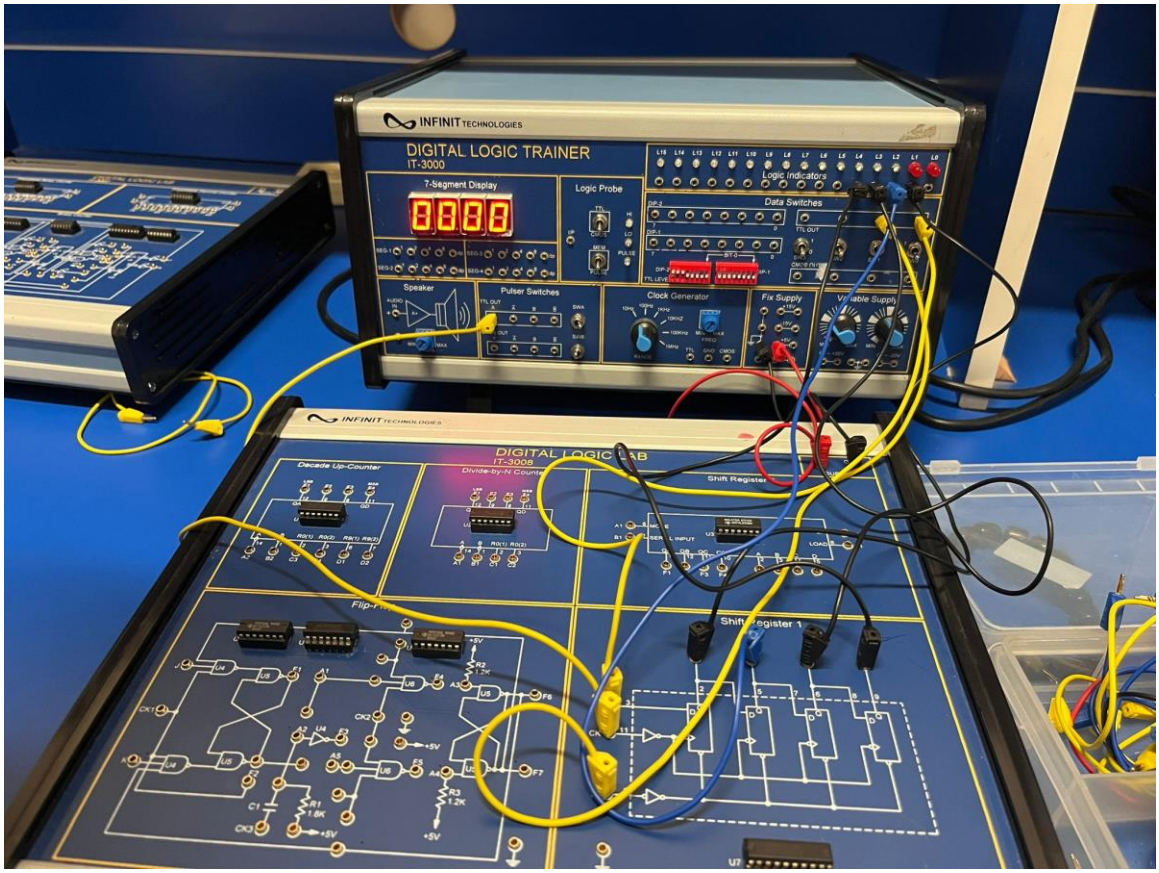


Figure 23:wiring connection of Shift Right Register.

INPUT		OUTPUT			
A	CK	F1	F2	F3	F4
1	⎍	1	1	0	0
0	⎍	0	1	1	0
0	⎍	0	0	1	1
1	⎍	1	1	1	0

Table 12:Data for Shift Right Register

From the collected table, the circuit acts exactly as its job and hold 4-bit binary digits.

2. 4-Bit Shift Register with serial and parallel load

In this section of the experiment, Block Shift Register 2 of module IT-3008 will be used. So, first +5V of the module will be connected to the +5V output of the fixed power supply, and Inputs A, B, C, D to SW0, SW1, SW2, SW3 Outputs F1, F2, F3, F4 to L0, L1, L2, L3, respectively, B1 (I/P) to DIP2.0, A1 (MODE) to DIP2.1, CK (C1) to the clock generator TTL level output at 1Hz and data at B1 with DIP2.0 changed. Finally, the input sequence for A1 followed and outputs recorded. Below figure of the Shift Right Register diagram inputs and outputs.

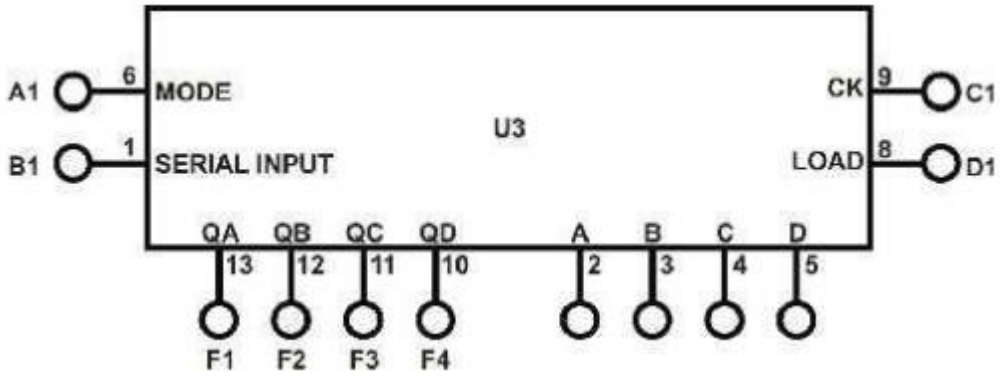


Figure 24:4-Bit Shift Register with serial and parallel load

Here we find figure for the circuit connection in the lab.

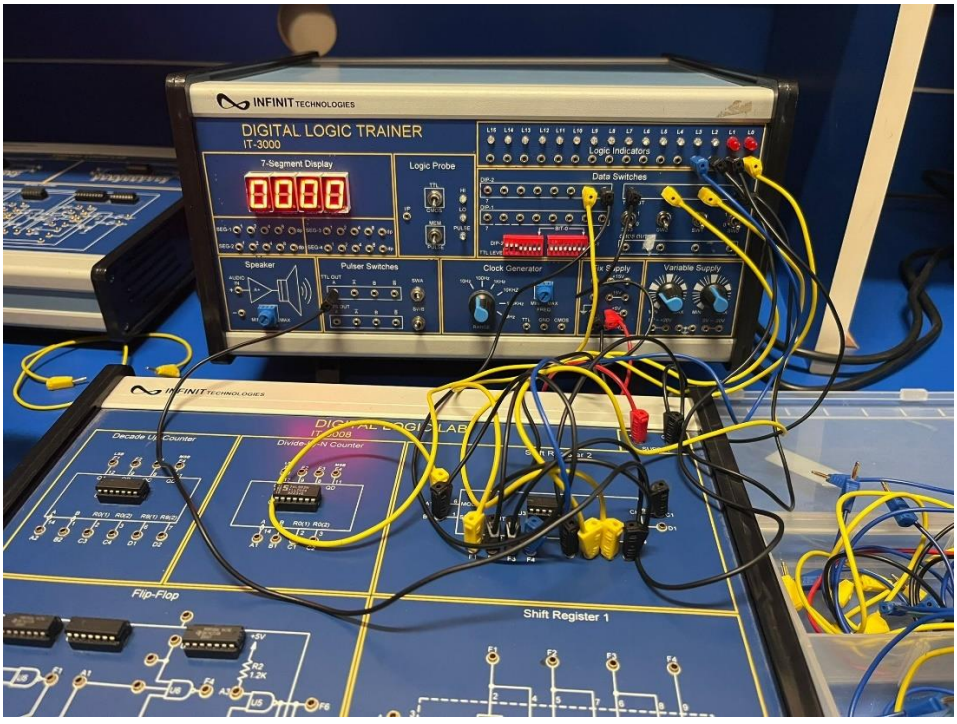


Figure 25:wiring connection of 4-Bit Shift Register with serial and parallel load

INPUT		OUTPUT			
A1	C1	L3	L2	L1	L0
0	⎍	0	0	0	1
0	⎍	0	0	1	0
0	⎍	0	1	0	0
1	⎍	1	0	0	1

D1	D	C	B	A	L3	L2	L1	L0
⎍	0	0	1	0	0	0	1	0
⎍	1	0	1	0	1	0	1	0
⎍	1	1	1	0	1	1	1	0
⎍	0	1	1	1	0	1	1	1
⎍	0	1	1	0	0	1	1	0

Table 13:Data for 4-Bit Shift Register with serial and parallel load

The tables list various combinations of inputs for two modes, In the operation of the 4-Bit Shift Register with serial and parallel load IC, And the data we collect equal to the IC truth data, so that's mean the circuit done correctly.

C. Counters

1. 2-bit Synchronous Counter

In this section of the experiment, binary counter Block of module IT-3007 will be used. So, first +5V of the module will be connected to the +5V output of the fixed power supply, CLK to pulser switch SWA, Q1 and Q0 to indication lamps L1, L2, respectively. Finally, the clock pulses to CLK input applied and outputs recorded in binary and decimal. Below figure of the 2-bit Synchronous Counter diagram inputs and outputs.

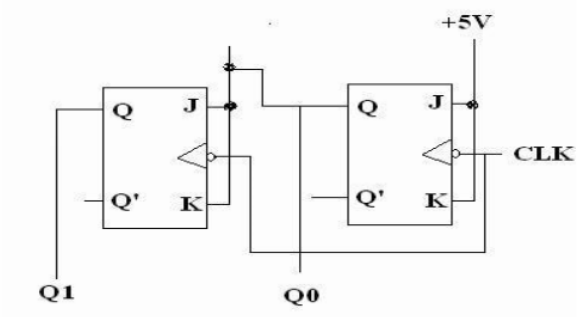


Figure 26: 2-bit Synchronous Counter

Here we find figure for the circuit connection in the lab.

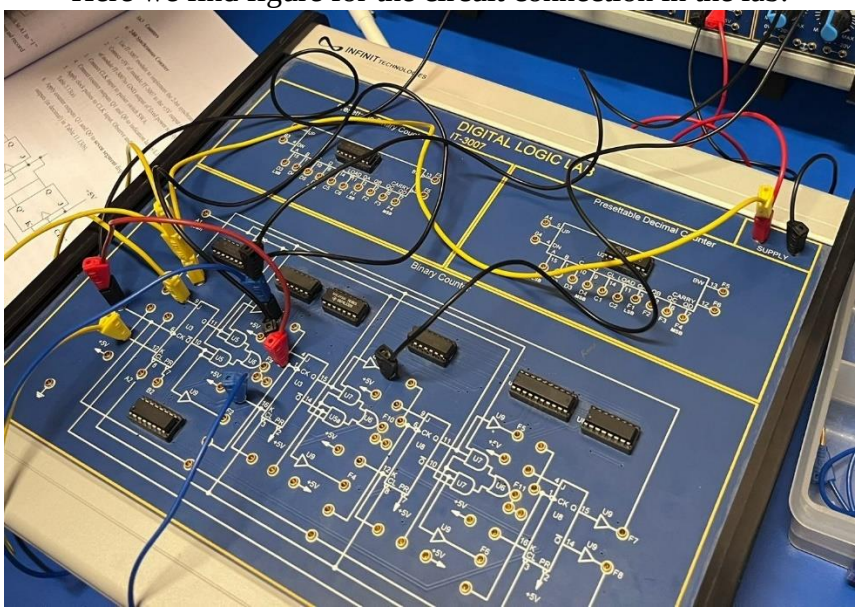


Figure 27:wiring connection of 1-to-2 Demultiplexer

input	Output	
CLK	Q1	Q2
⎍	0	0
⎍	0	1
⎍	1	0
⎍	1	1
⎍	0	0
⎍	0	1
⎍	1	0
⎍	1	1

input	Output
CLK	D
⎍	0
⎍	1
⎍	2
⎍	3
⎍	0
⎍	1
⎍	2
⎍	3

Table 14:Data for 2-bit Synchronous Counter

From the collected tables, the circuit acts as 2-bit Synchronous Counter.

2. 3-bit (divide-by-eight) Ripple Counter

In this section of the experiment, binary counter Block of module IT-3007 will be used. So, first +5V of the module will be connected to the +5V output of the fixed power supply, CLK to pulser switch SWA, Q2, Q1 and Q0 to indication lamps. Finally, the clock pulses to CLK input applied and outputs recorded in binary and decimal. Below figure of the 3-bit (divide-by-eight) Ripple Counter diagram inputs and outputs.

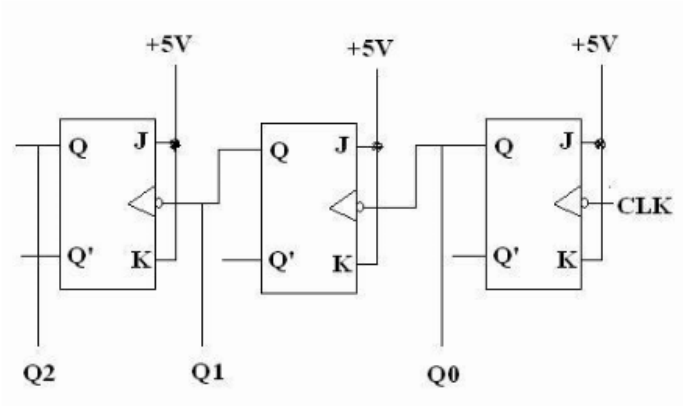


Figure 28: 3-bit (divide-by-eight) Ripple Counter

Here we find figure for the circuit connection in the lab.

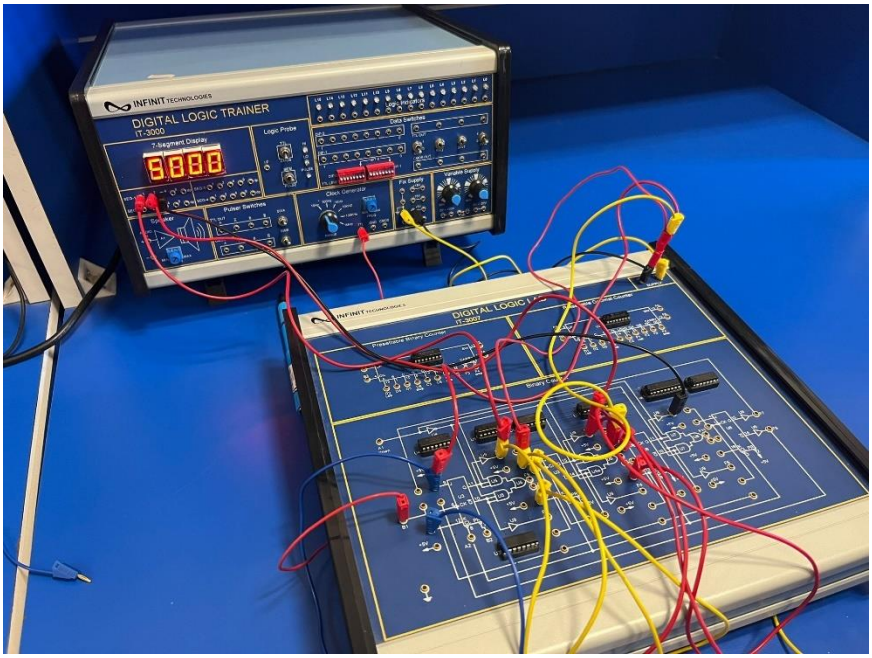


Figure 29:wiring connection of 3-bit (divide-by-eight) Ripple Counter

Inputs	Outputs		
CLK	Q2	Q1	Q0
⎍	0	0	0
⎍	0	0	1
⎍	0	1	0
⎍	0	1	1
⎍	1	0	0
⎍	1	0	1
⎍	1	1	0
⎍	1	1	1
⎍	0	0	0
⎍	0	0	1

input	Output
CLK	D
⎍	0
⎍	1
⎍	2
⎍	3
⎍	4
⎍	5
⎍	6
⎍	7
⎍	0
⎍	1

Table 15:Data for 3- bit (divide-by-eight) Ripple Counter.

The tables list pulse to CLK, In the operation of the 3- bit (divide-by-eight) Ripple Counter, And the data we collect equal to the counter truth data, so that's mean the circuit done correctly.

3. BCD Counter

In this section of the experiment, BCD counter Block of module IT-3008 will be used. So, first +5V of the module will be connected to the +5V output of the fixed power supply, C3, C4 to SW0 and SW1, D1, D2 to SW2 and SW3, F1~F4 to L1~L4, A2 to SWA A output. 3. Connect F1 to B2, and C3, C4, D1 and D2 applied to ground and A2 to SWA A pulse. Finally, the clock pulses to CLK input applied and outputs recorded. Below figure of the BCD Counter diagram inputs and outputs.

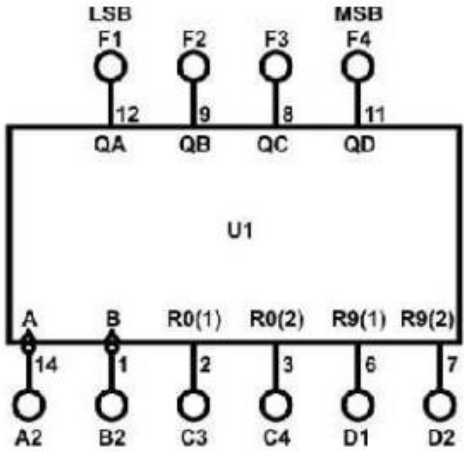


Figure 30: IC 7490 BCD Counter.

Here we find figure for the circuit connection in the lab.

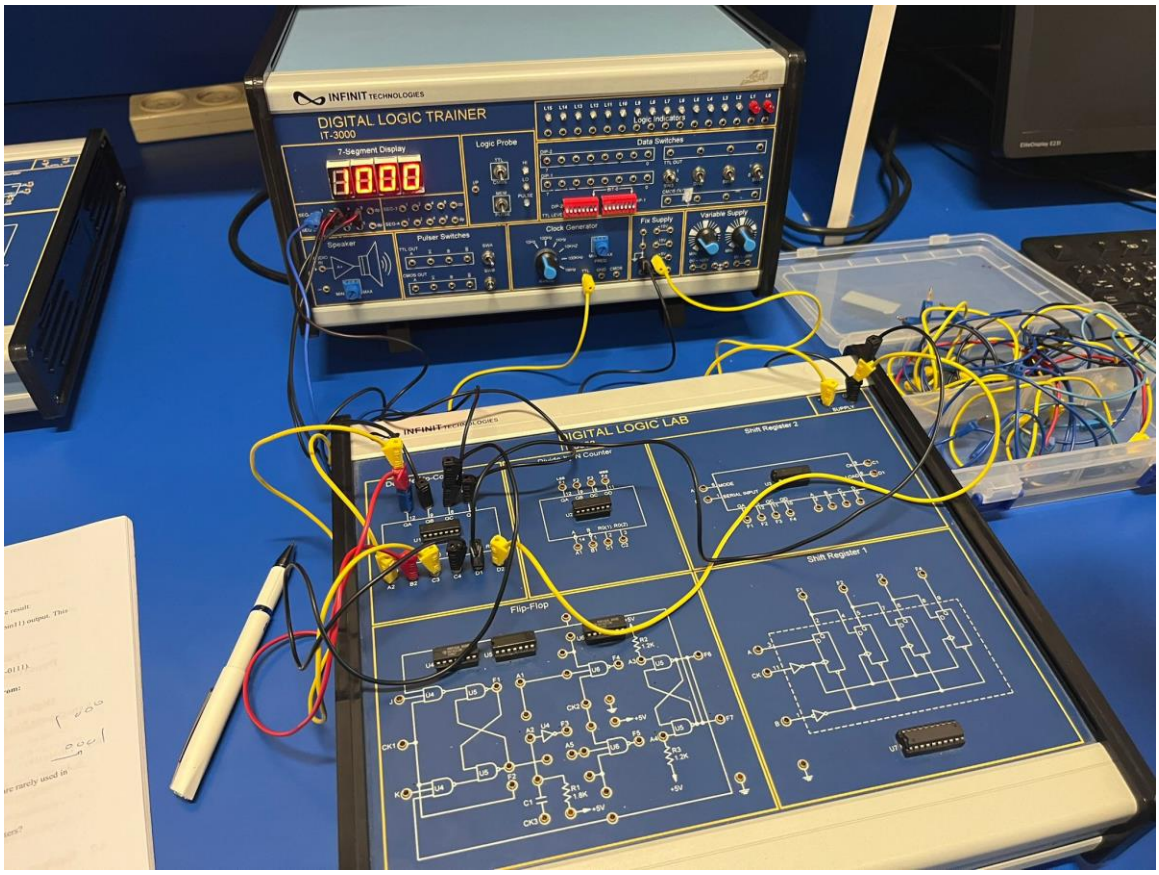


Figure 31:wiring connection of BCD Counter

From the data collected this counter counts from 0 to 9 then resets to 0, the circuit resets when R0(1) & R0(2) are both ones.

4. Divide-by-8 counter using BCD chip counter

To implement this circuit, BCD Counter circuit will be modified. R0(2) (pin3) Changed to +5V, and R0(1) (pin2) connected to QD (pin11) output. clock A2 (pin14) connected to pulser switch. outputs A, B, C, and D connected to indication lamps, Finally, the clock pulses to CLK input applied to A2 and outputs recorded.

note:

If we need to make the counter count 0-5 we need to connect QB and QC to R0(1) and R0(2).

V. Conclusion

In conclusion the experiment went smoothly with no complications, everything was giving the same answers as the theoretical datasheets. This proved that everything was correct. This experiment was simply to understand how latches, flip flops, registers, and counters work and how to implement each one. The construction of each design was done through basic gates and IC's. Furthermore, it appears that the counter can be designed to reach a desired numerical value.

VI. References

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