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# **Education**

* + **Shahid-Chamran University…….**Ahvaz, Iran

Master of Science in Electrical and Electronic Engineering July 2011 **GPA: 16.66 out of 20**

**Thesis title**: *Digital Background Calibration of Timing and Gain Mismatch Errors in Time-Interleaved ADCs*

* + **Quchan University of Technology…….**Quchan, Iran

Bachelor of Science in Telecommunication Technology Engineering July 2009 **GPA: 16.16 out of 20**

**Project title**: *6-Channel High Frequency Remote Control*

* + **Shahid-Mohajer Isfahan Technical Higher Educational Center…….** Isfahan, Iran

Associate Degree in Electronics (The Forth Top Student)

September 2007 **GPA: 16.16 out of 20**

**Project title**: *Ultrasonic Distance Meter by Microcontroller*

* + **Shahid-Beheshti High School …….**Dezful, Iran

Diploma in Electronics (Top Student in High School) September 2005 **GPA: 18.29 out of 20**

# **Teaching Experience**

* + ***Applied Mathematics***• Undergraduate Students, Shahid-Mohajer Isfahan Technical Higher Educational Center **–** Recitation Classes
* ***Electronics 2***• Undergraduate Students, Quchan University of Technology **–** Recitation Classes

# **Industry Experience**

**Instrumentation & Control Engineer:** Engineering Department, National Iranian South Oil Company, Ahvaz, Iran……………..December 2019 – present

* I & C engineering in the most important EPC projects of Iran
* Assessing designing documents
* Evaluating design, engineering, and construction of projects in compliance with International Standards
* Corresponding with contractors in English

**Telecommunication Engineer:** Marun Oil & Gas Production Units, National Iranian South Oil Company, Ahvaz, Iran ……………..June 2010 – November 2019

* Electronic Supervisor
* Design of Self-Powered Electronic Boards for Telephones
* Transforming the analog telecom. links into the digital

***CEO & Founder: Fannavari Sotudeh Kardan Co., Ahvaz, Iran, 2024***………..present

* Offering engineering services
* Maintenance and installation of technical devices and systems

# **Publications**

Journal publications:

* ["](https://www.techrxiv.org/articles/preprint/A_New_Technique_for_Gain_and_Timing_Calibration_in_Time-Interleaved_ADCs_Using_an_Estimation_Signal/21938294)[*[A New Adaptive Blind Background Calibration of Gain and Timing Mismatch for a Two-Channel Time-Interleaved ADC](https://www.techrxiv.org/articles/preprint/A_New_Technique_for_Gain_and_Timing_Calibration_in_Time-Interleaved_ADCs_Using_an_Estimation_Signal/21938294)*[", Microelectronics Journal, 2018.](https://www.techrxiv.org/articles/preprint/A_New_Technique_for_Gain_and_Timing_Calibration_in_Time-Interleaved_ADCs_Using_an_Estimation_Signal/21938294)](https://www.sciencedirect.com/science/article/abs/pii/S0026269218300211)
* "*High-Speed Estimation-Based Calibration of Gain and Timing Mismatches in Multi-Channel Time-Interleaved ADCs*", submitted to Computers and Electrical Engineering, 2025. (July 18, 2025)

Conference publications:

* "*A Reduction in Mismatch Error Tones by Randomization of Errors in Time-Interleaved ADCs*", Engineering Sciences and Novel Ideas Conference, 2013.
* "*Digital Background Calibration in Time-Interleaved ADCs*", Engineering Sciences and Novel Ideas Conference, 2013.

# **Professional Membership**

* Iranian Society of Electrical Engineer
* Reviewer at Journal of Circuits, Systems, and Computers (JCSC)

# **Research Interests**

* Analog & Mixed-Signal Circuits and Data Converters
* Integrated Circuit Design
* Brain-Computer Interfaces
* Wearable Sensors

# **Programming Languages**

* Python
* C/C++ Code
* MATLAB
* Assembly & Visual Basic
* VHDL

# **TECHNICAL SKILLS**

* **Hardware Description & Scripting Languages:**
* **VHDL**, **Verilog**, Python, TCL, Visual Basic, Assembly
* **EDA & IC Design Tools:**
* **Commercial:** Cadence Virtuoso
* **Open-Source:** Magic VLSI, OpenROAD, Xschem, KLayout, Netgen
* **PDKs:** SKY130 (Efabless ecosystem)
* **Design Flow Expertise:**
* Schematic Entry • Analog/Digital Simulation • Layout • LVS/DRC • Post-Layout Simulation • GDSII
* Post-Layout Simulations • Custom Testbenching (Verilog/VHDL + Python)
* **Circuit Domains:**
* Mixed-Signal Interfaces • ADC Calibration • Energy-Efficient Logic Design
* **Simulation & Modeling:**
* HSpice, PSpice, OrCAD, MATLAB/Simulink, Proteus
* **PCB Design:**
* Proteus • Altium Designer
* **Additional Info.**
* TOEFL (Oct, 2, 2024): 91

# **References**

* Alimorad Mahmoudi, Professor of Electrical & Electronic Engineering,

Shahid Chamran University, Email address ([a.mahmoudi@scu.ac.ir](mailto:a.mahmoudi@scu.ac.ir)), Phone: +98-613-3330011 - Ext: 5734

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