Analog/Mixed-Signal Simulation and Modeling

Module 07
Introduction to Phase Locked Loops (PLL)

Dr. Hesham A. Omran

Integrated Circuits Laboratory (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

This lecture is mainly based on "T. Carusone, D. Johns, K. Martin, Analog integrated circuit design, Wiley, 2012", "B. Razavi, Design of analog CMOS integrated circuits, McGraw-Hill Ed., 2017 ", and "B. Razavi, RF Microelectronics, Prentice Hall, 2nd Edition, 2012"

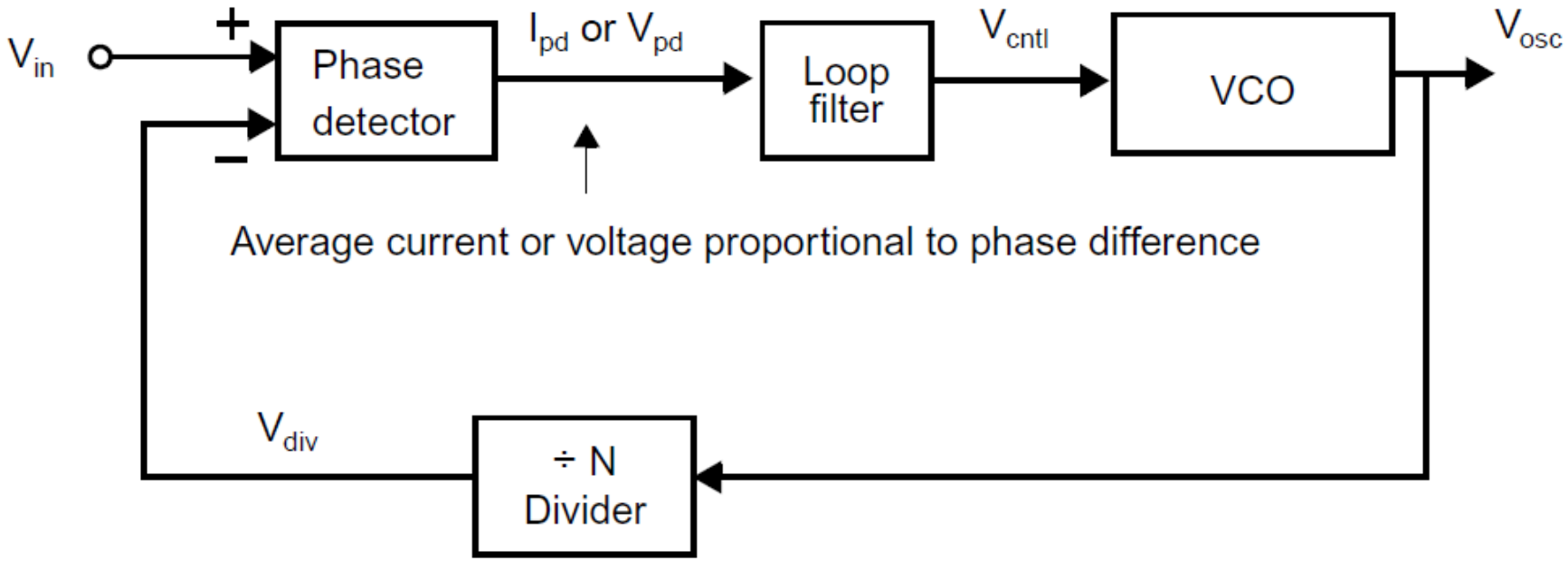
Why PLLs?

- Practically all digital and radio frequency circuits and most analog/mixed-signal circuits require a precision oscillator
- Integrated circuit oscillators are not, on their own, suitable for use as frequency- or time-references
  - PVT variations
  - Jitter
- Insert the oscillator into a phase locked loop where the operating frequency and phase is continuously compared against a precise external time-reference
- Precise external references are in the 1-200 MHz range
  - Use PLL for synthesizing higher and/or different output frequencies

    ➔ Clock/Frequency synthesis
  - Other applications exist

PLL Architecture

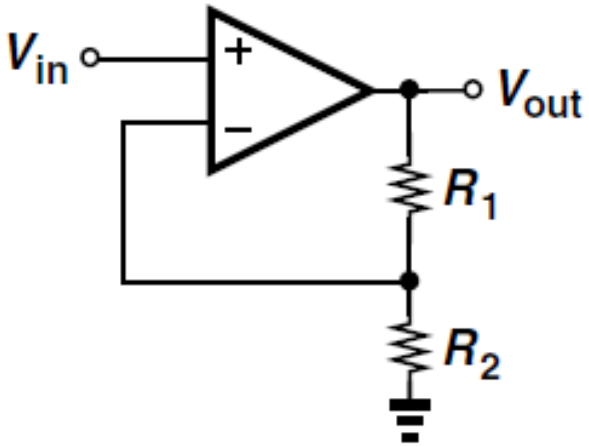
- Negative feedback loop
  - At steady state: Phase lock condition
    - $\phi_{in} - \phi_{fb} = \phi_{err} = constant \quad \rightarrow \quad \frac{d\phi_{in}}{dt} - \frac{d\phi_{fb}}{dt} = 0$
    - $f_{fb} = f_{in}$ (no error)
    - $f_{out} = N \times f_{in}$

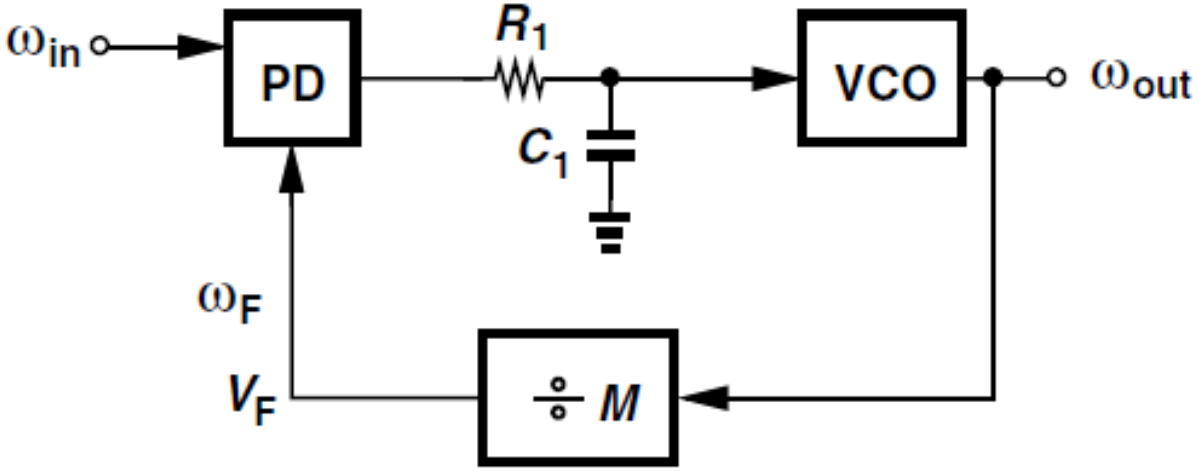


[Johns & Martin, 2012]

Amplifier vs PLL

- The op-amp circuit amplifies the input voltage by using voltage divider in the FB path
- The PLL amplifies the frequency by using frequency divider in the FB path
- The divide ratio M is called the “modulus”





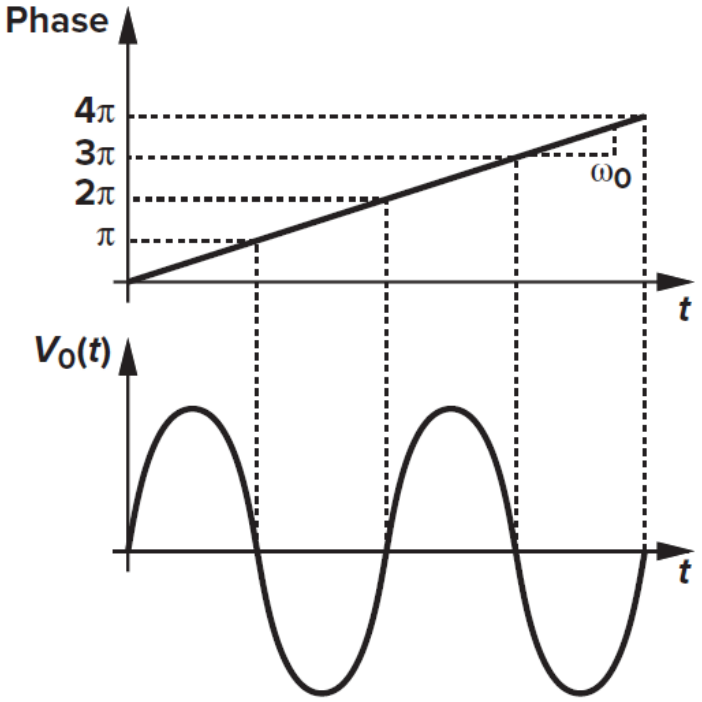
[Razavi, RF Microelectronics, 2012]

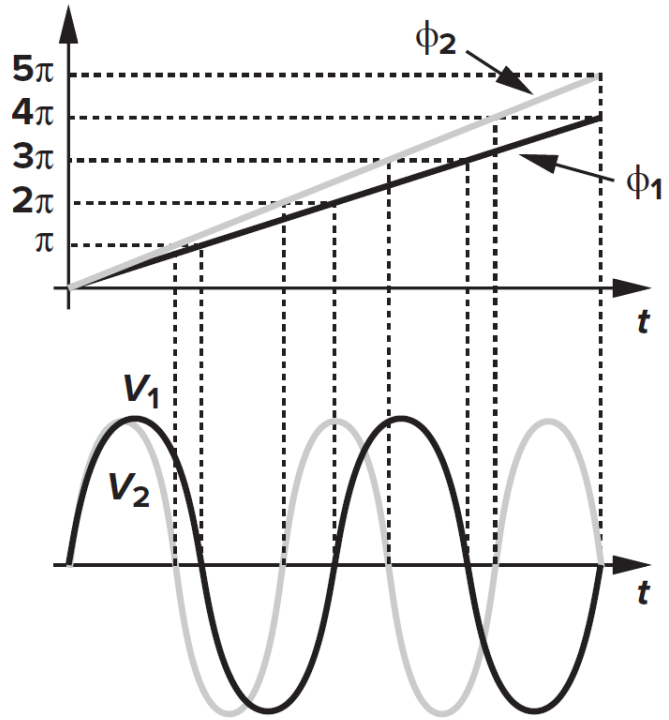
Voltage-Controlled Oscillator (VCO)

- $V_{out} = A\sin(\phi) = A\sin(\omega t) \rightarrow \omega = \frac{d\phi}{dt} = K_{VCO}V_{cntl}$

$$\frac{\phi}{V_{cntl}} = \frac{K_{VCO}}{s}$$

- Higher frequency means faster phase accumulation





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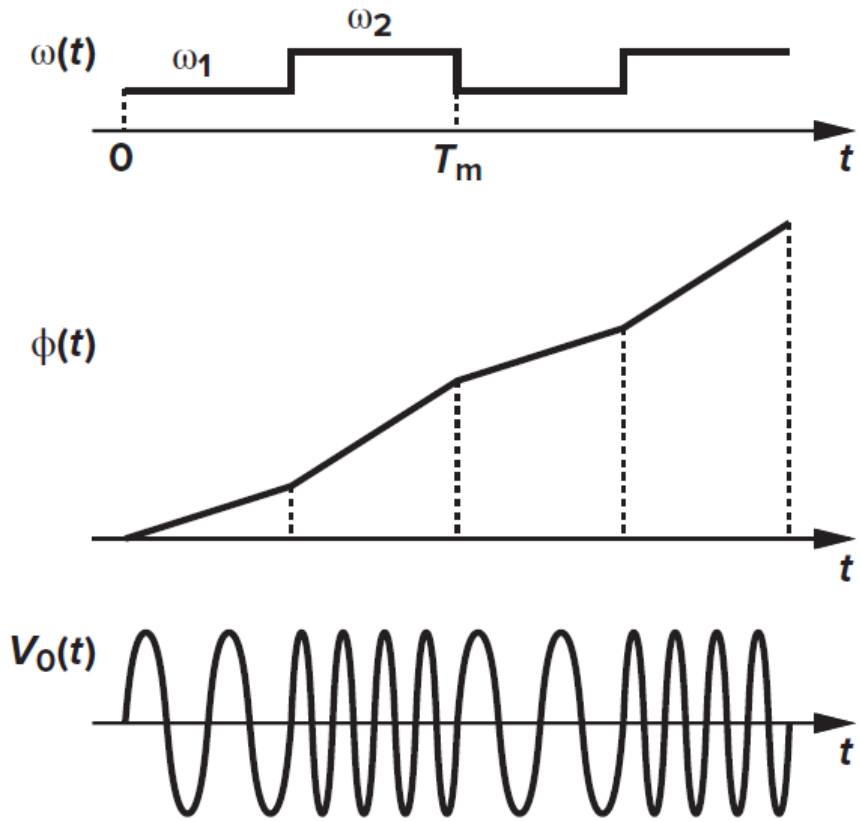


[Razavi, RF Microelectronics, 2012]

Voltage-Controlled Oscillator (VCO)

- ω_o: $free\ running\ freq$ $\omega(t) = K_{VCO}V_{cntl}$: $deviation\ from\ \omega_o$

$$V_{osc}(t) = E\ \sin[\omega_0 t + \phi(t)]$$

$$\omega_{inst}(t) = \frac{d[\omega_0 t + \phi(t)]}{dt} = \omega_0 + \frac{d\phi(t)}{dt}$$

$$\omega(t) = \omega_{inst}(t) - \omega_0$$

$$\omega(t) = \frac{d\phi(t)}{dt}$$

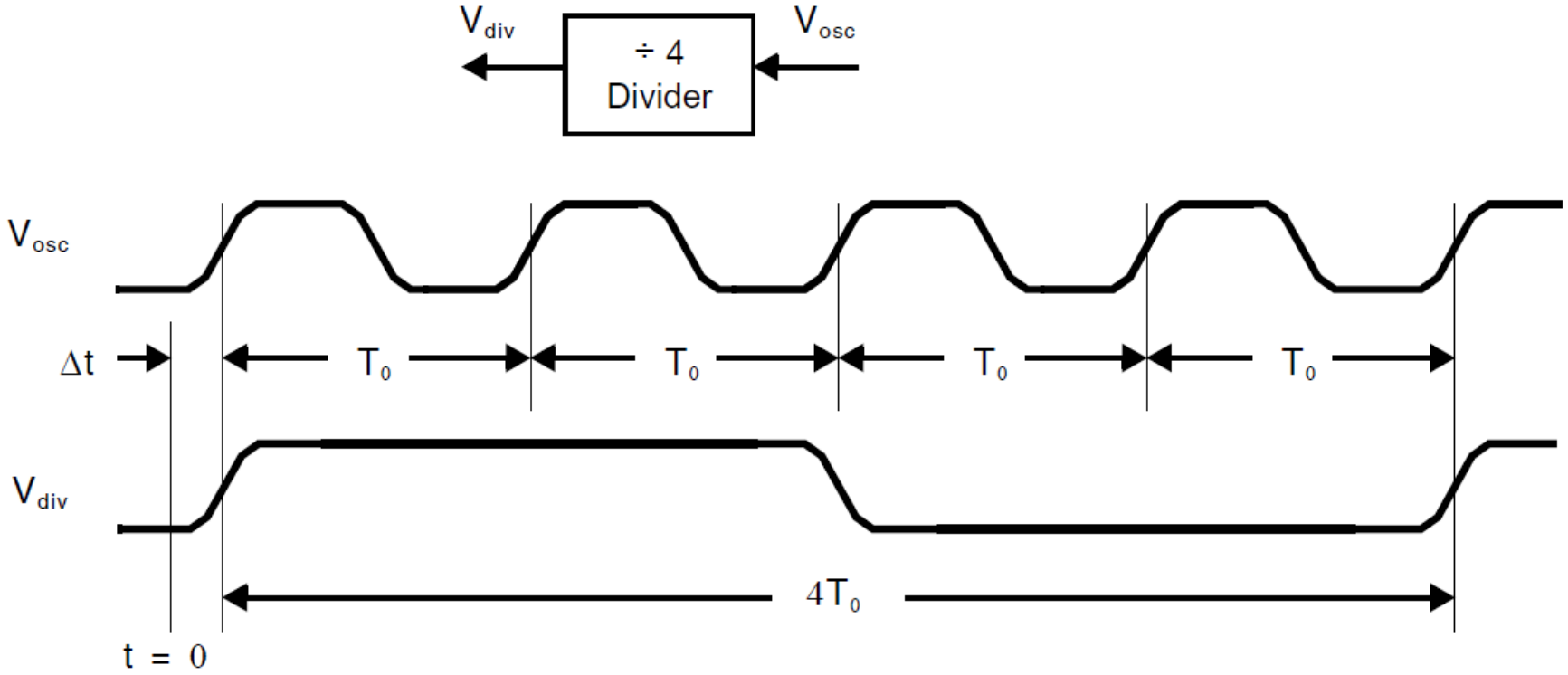
$$\phi(t) = \phi(0) + \int_0^t \omega(\tau)\, d\tau$$

$$\phi(s) = \frac{\omega(s)}{s}$$

$$\omega(t) = K_{osc}V_{cntl}(t)$$

[Johns & Martin, 2012]

Frequency Divider



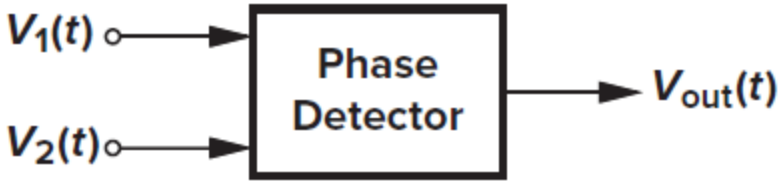
$$\phi = 2\pi \frac{\Delta t}{T_0}$$

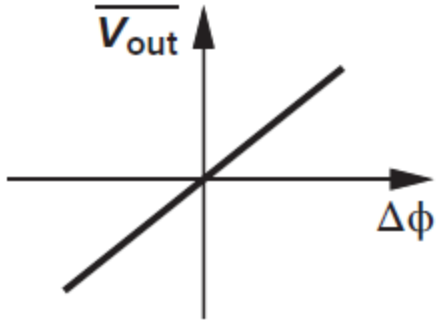
$$\phi_{div} = 2\pi \frac{\Delta t}{NT_0} = \frac{\phi}{N}$$

$$\phi_{div}(s) = \frac{\phi(s)}{N}$$

[Johns & Martin, 2012]

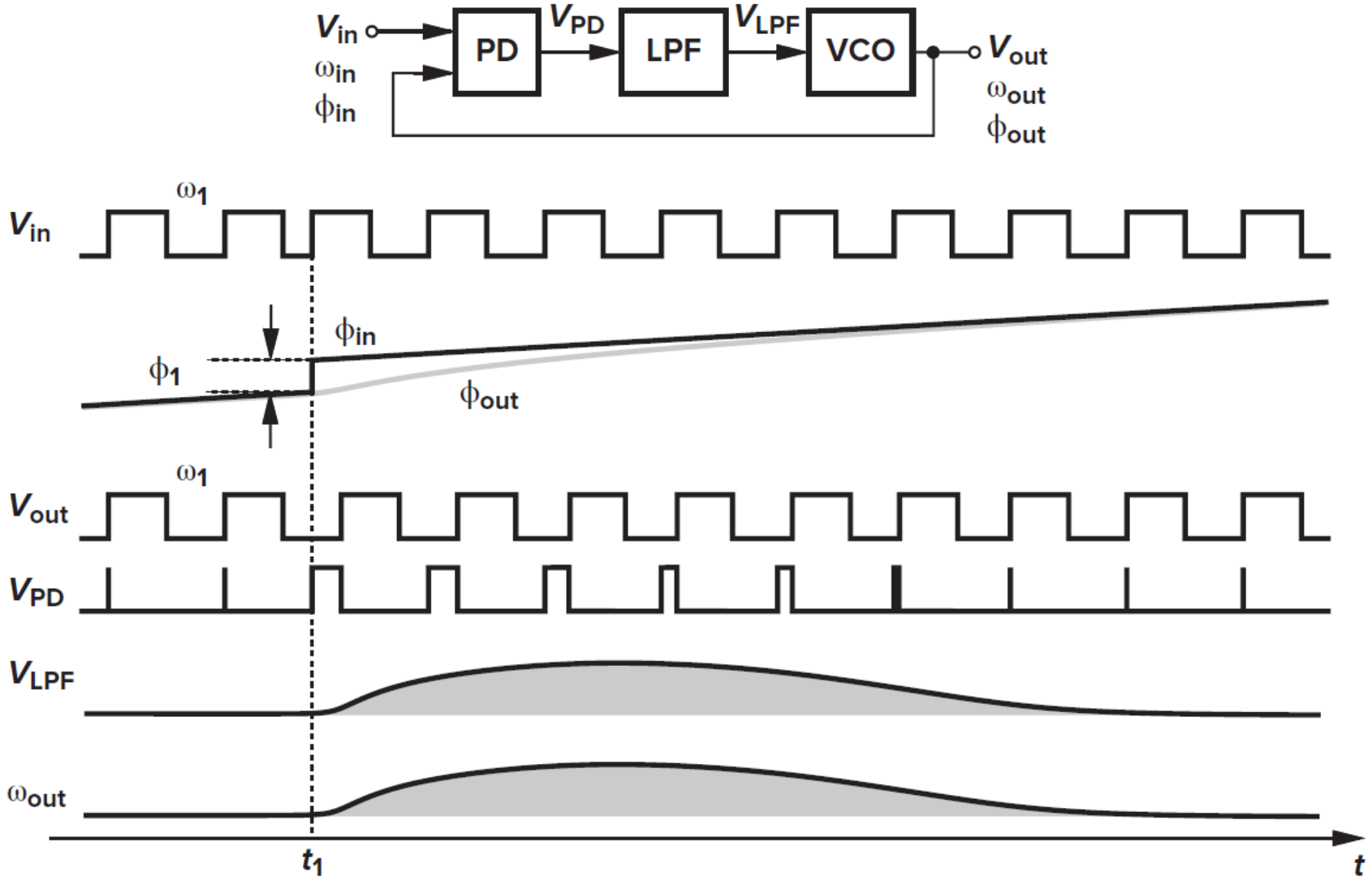
Ideal Phase Detector





[Razavi, RF Microelectronics, 2012]

PLL Response to Phase Step



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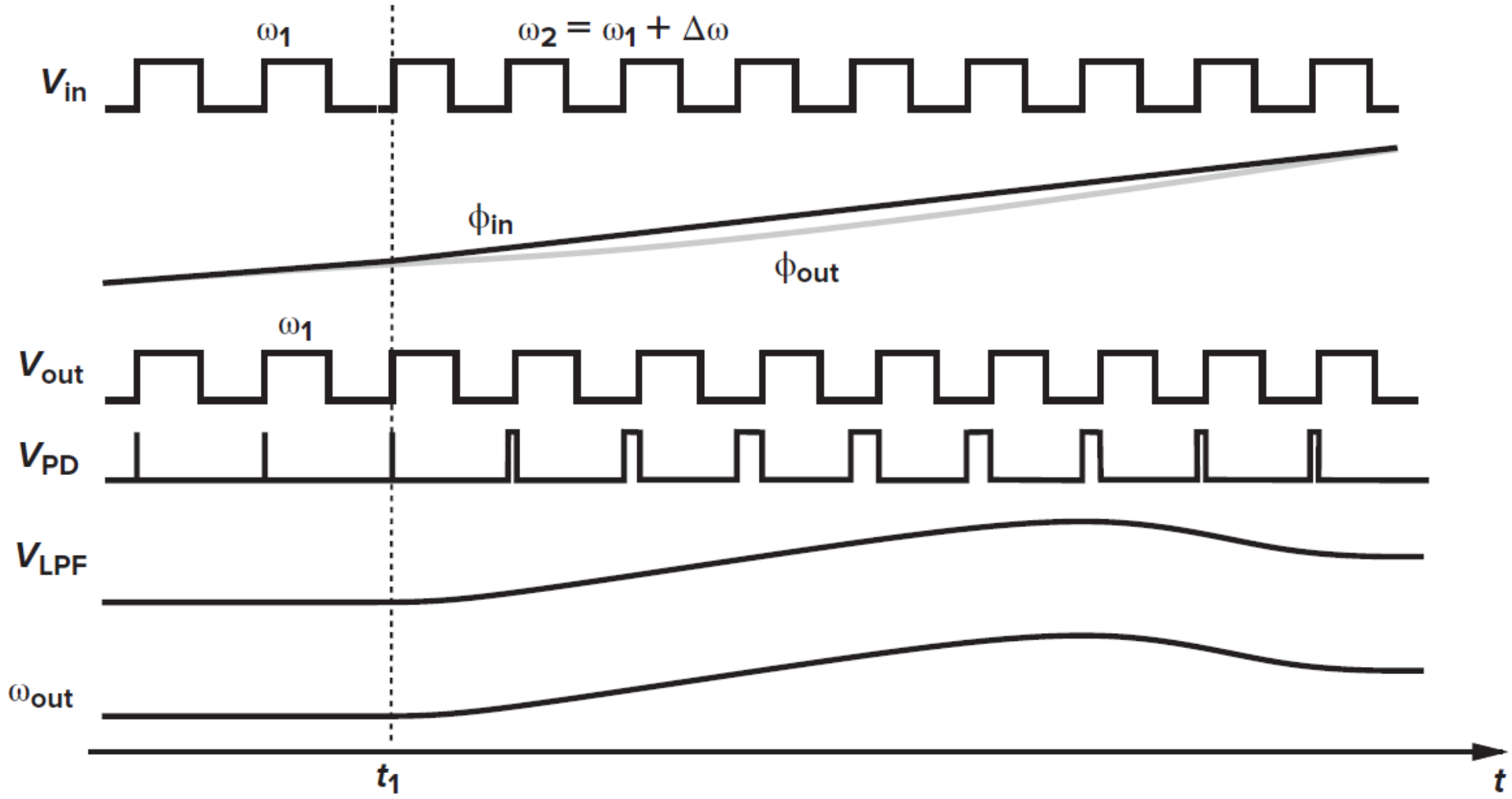
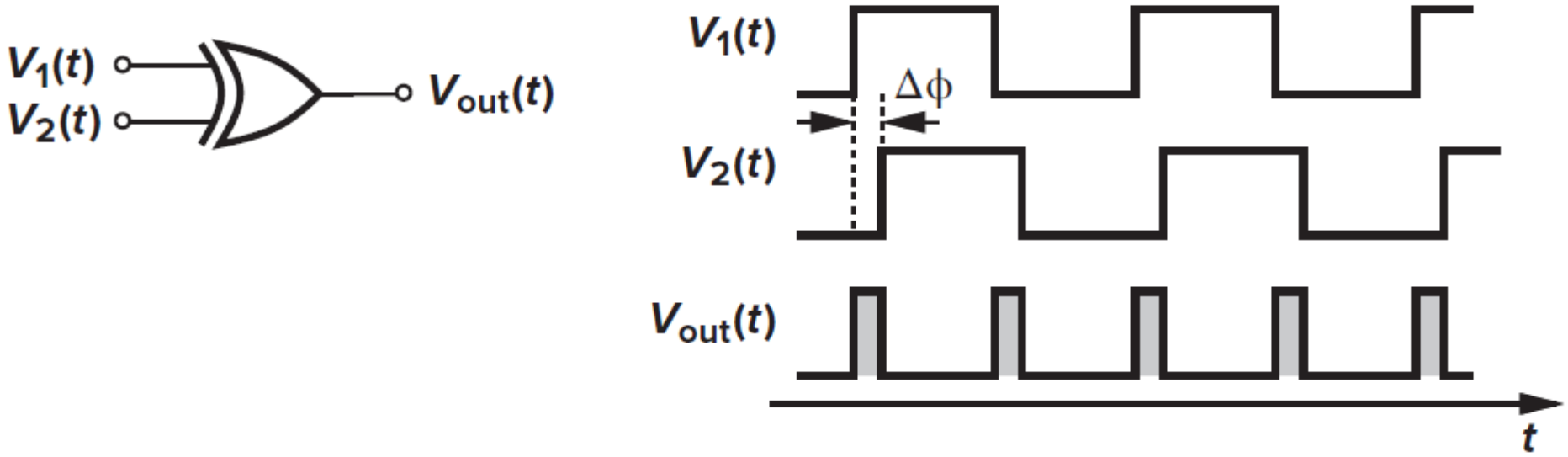
PLL Response to Frequency Step



[Razavi, RF Microelectronics, 2012]

XOR Phase Detector

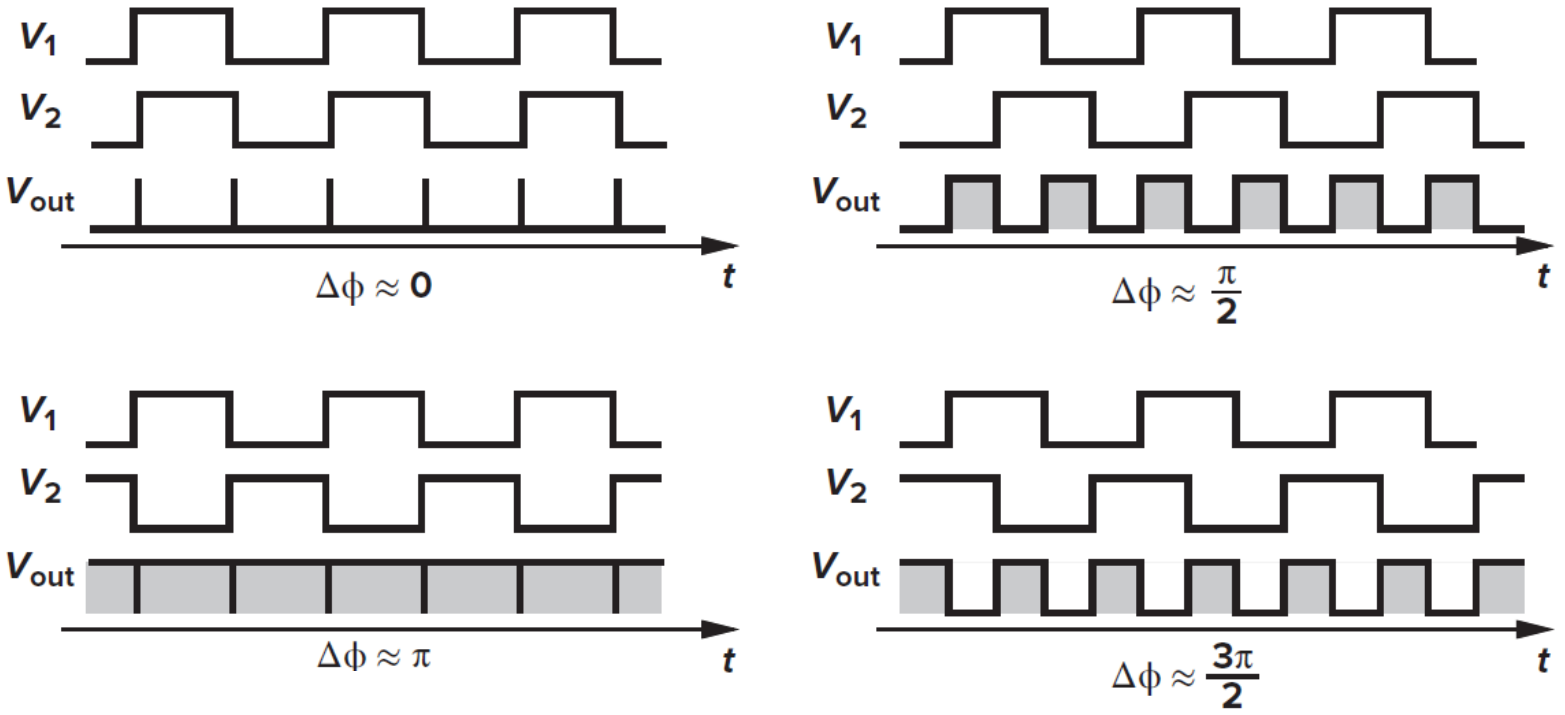
- VCO output and the reference input are both digital signals or have been converted to digital signals by a limiter

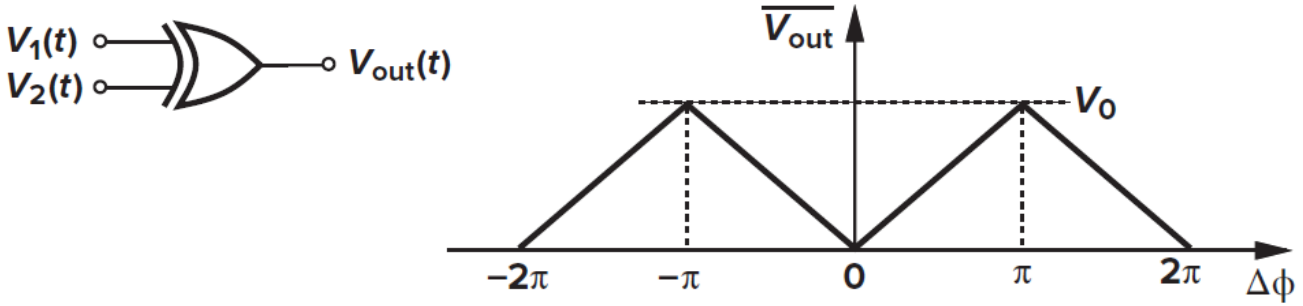


[Razavi, RF Microelectronics, 2012]

XOR Phase Detector

- $K_{PD} = \frac{\Delta V_{out}}{\Delta \phi} = \frac{V_o}{\pi}$

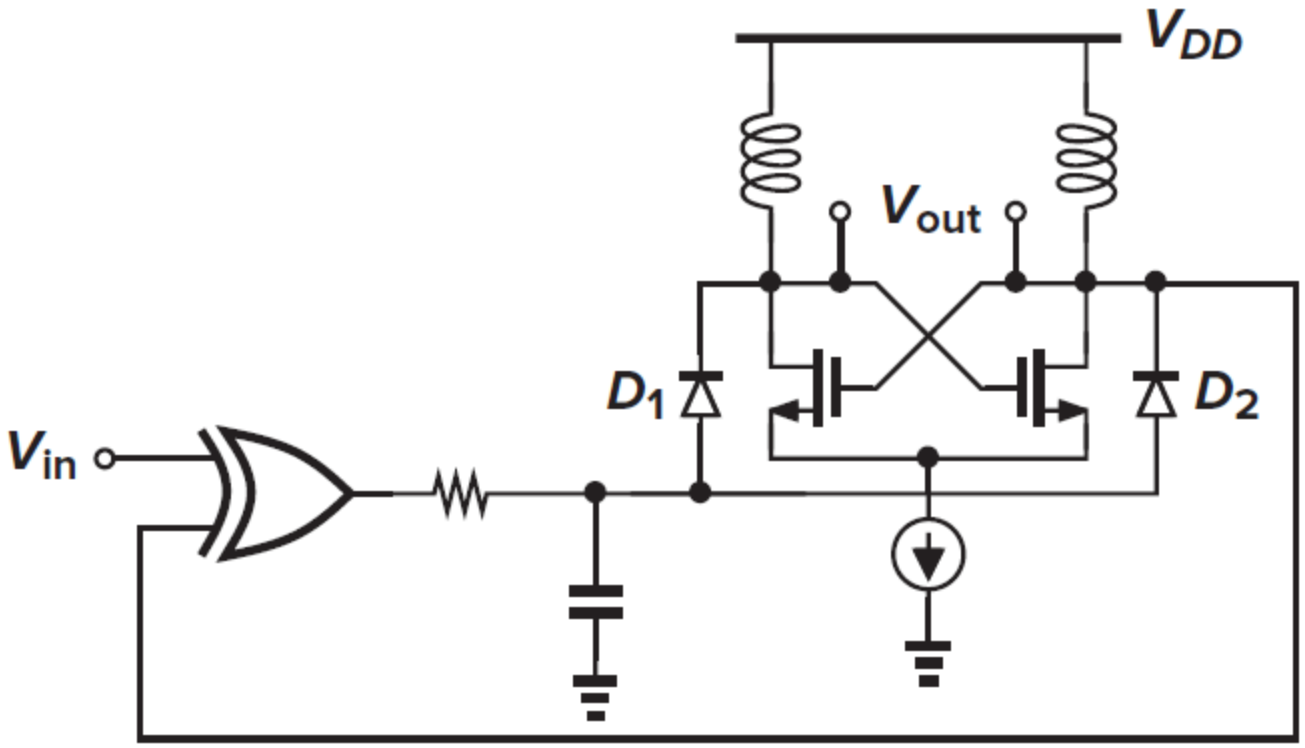




[Razavi, RF Microelectronics, 2012]

Simple PLL Example

- The VCO is a negative-Gm LC oscillator tuned by varactors
- PLL order (no. of poles) = loop filter (LF) order + 1 (VCO)
- PLL type = no. of ideal integrators (poles at origin)



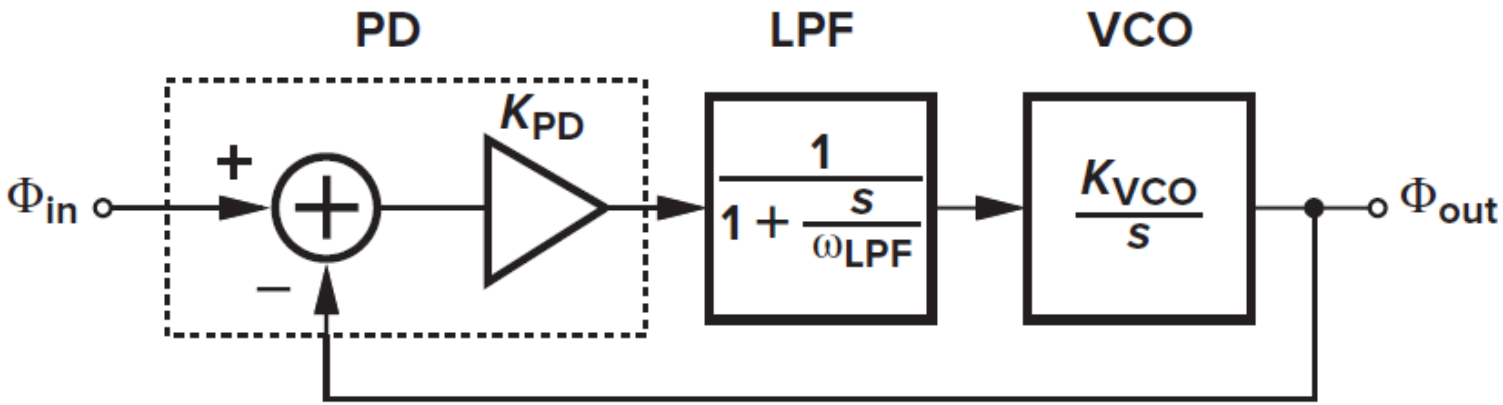
[Razavi, RF Microelectronics, 2012]

Steady State Error

- $\frac{v_{out}}{v_{in}} = \frac{A}{1+\beta A}$
- $\frac{v_{err}}{v_{in}} = \frac{1}{1+\beta A} \approx \frac{1}{LG}$
- Final value theorem: $\lim_{t\to\infty} f(t) = \lim_{s\to 0} sF(s)$
- Steady state error $= \epsilon_s = v_{err}(t \to \infty) = \lim_{s\to 0} \frac{sV_{in}(s)}{LG(s)}$
- No. of poles at s = 0 (at origin) = no. of ideal integrators
- How to get zero ϵ_s?
  - Step input: $V_{in}(s) = \frac{1}{s}$ → LG must have one ideal integrator
  - Ramp input: $V_{in}(s) = \frac{1}{s^2}$ → LG must have two ideal integrators

Type I PLL

- Type I → Loop gain has ONE pole at origin (ONE ideal integrator)



$$H(s)|_{\text{open}} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{\text{open}}$$

$$= K_{PD} \cdot \frac{1}{1+\frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s}$$

$$H(s)|_{\text{closed}} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

[Razavi, RF Microelectronics, 2012]

Type I PLL

- $\Phi_{in} = \int \omega_{in} dt \rightarrow$ the input phase is **ramp input**
  - Type I has only one integrator → suffer from static phase error
  - Need two ideal integrators for $\phi_{err} = 0$
  - Two poles at origin → Type II PLL
- Other drawbacks of Type I:
  - Trade-off between ω_{LPF} and stability (ζ)
  - Limited acquisition range (solved by using PFD)

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

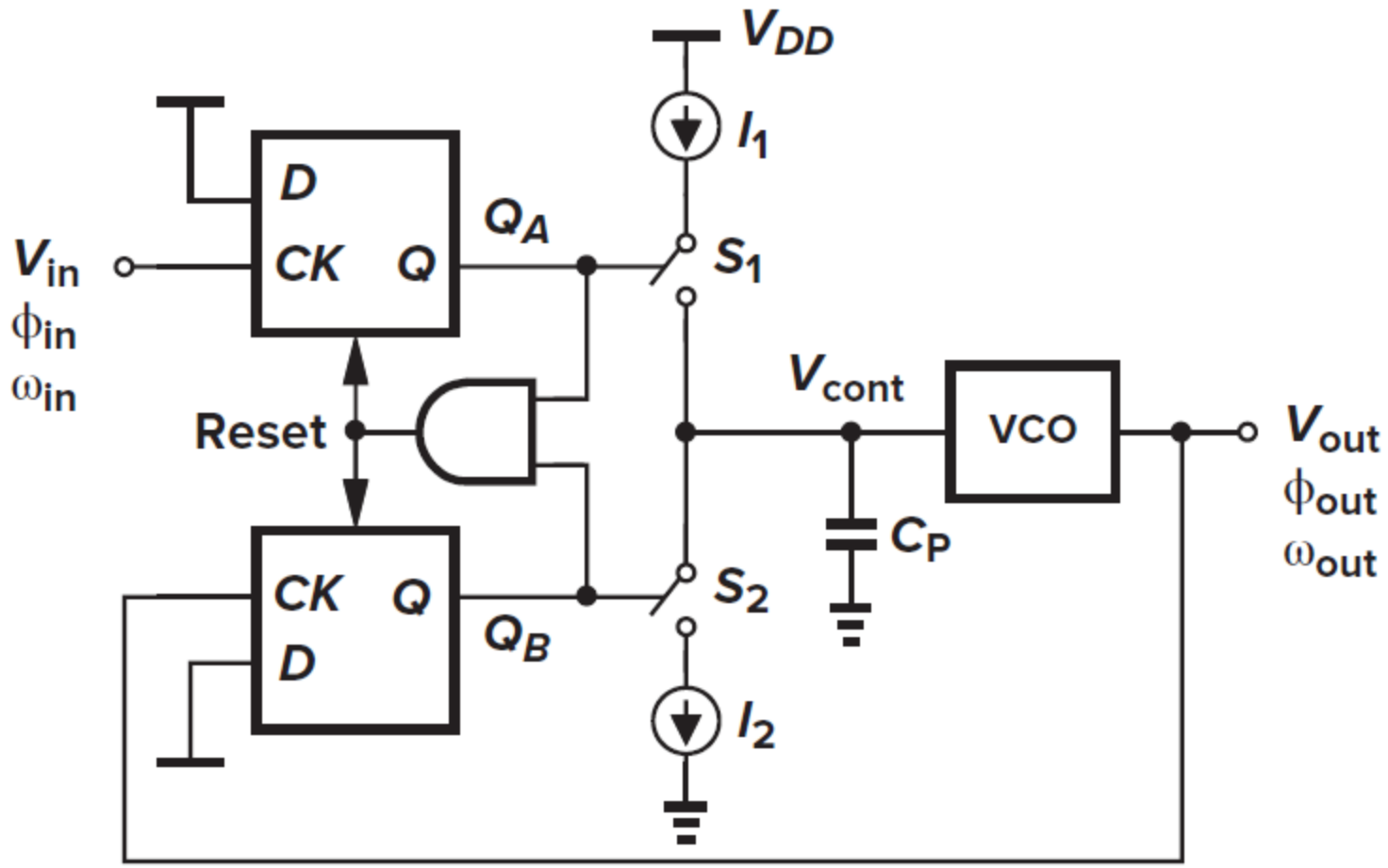
$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

[Razavi, RF Microelectronics, 2012]

Type II PLL: Charge Pump (CHP) PLL

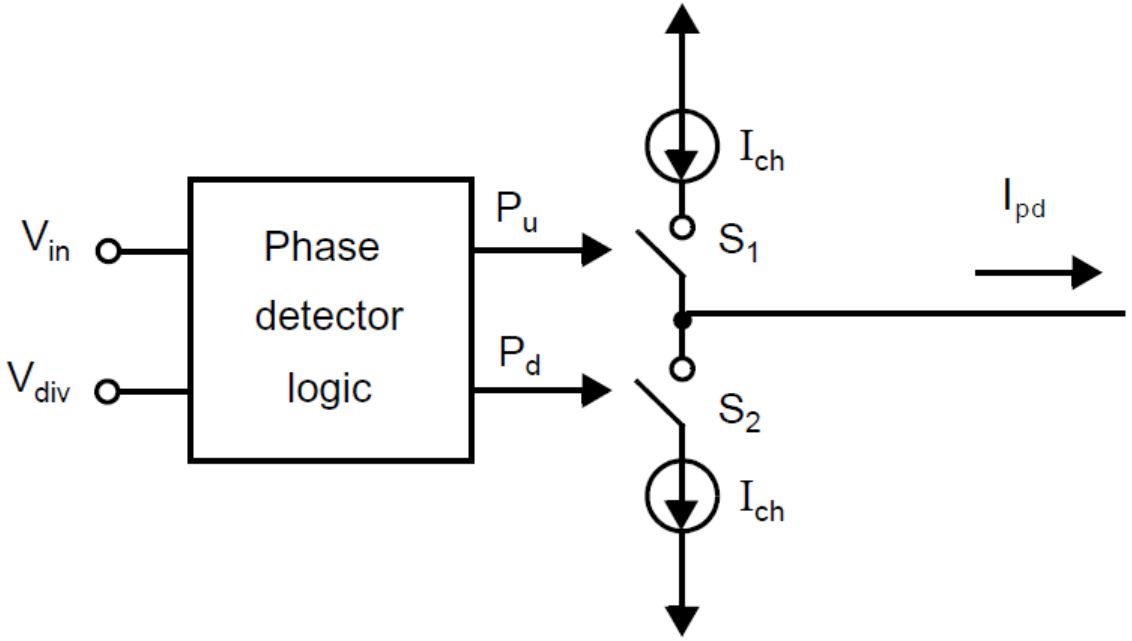
- One more ideal integrator in the PD + LF
  - Simply, current source charging a capacitor



[Razavi, RF Microelectronics, 2012]

CHP Phase/Frequency Detector (PFD)

- Type I has limited acquisition range: because phase detectors produce little information if they sense unequal frequencies
  - Acquisition range can be widened if a frequency detector is added to the loop
- Three-states: Pu = 1, Pd = 1, and Pu = Pd = 0
- The falling edges of both V_{in} and V_{div} have no effect on Pu and Pd

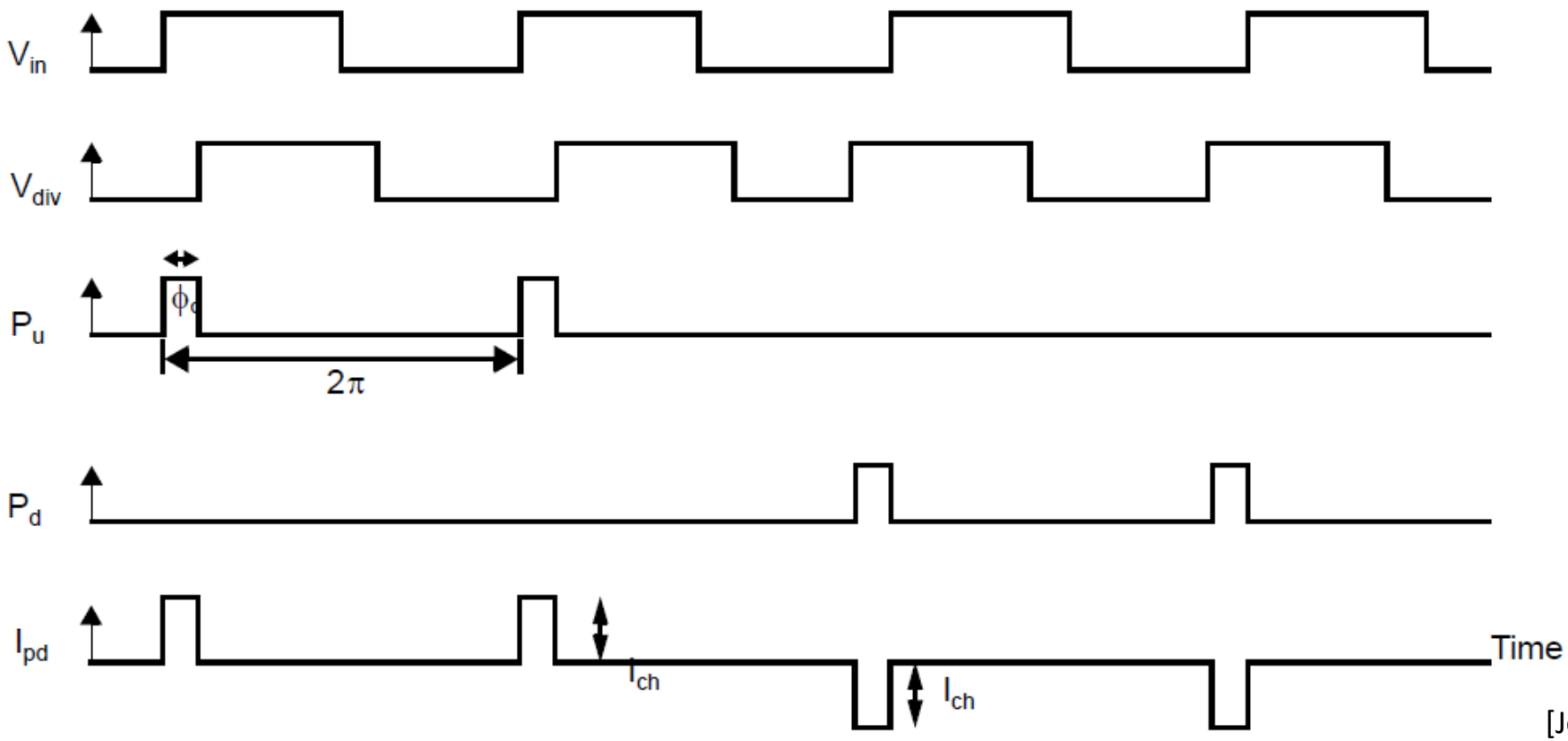


[Johns & Martin, 2012]

Charge Pump PFD

$$\overline{I_{pd}} = I_{ch}\frac{\phi_d}{2\pi}$$

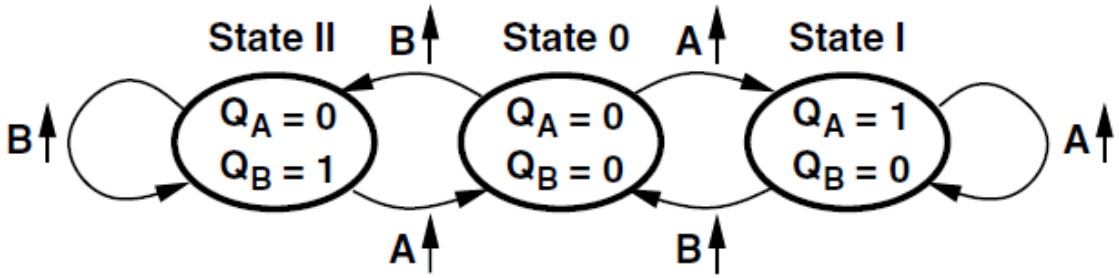
$$K_{pd} = \frac{I_{ch}}{2\pi}$$

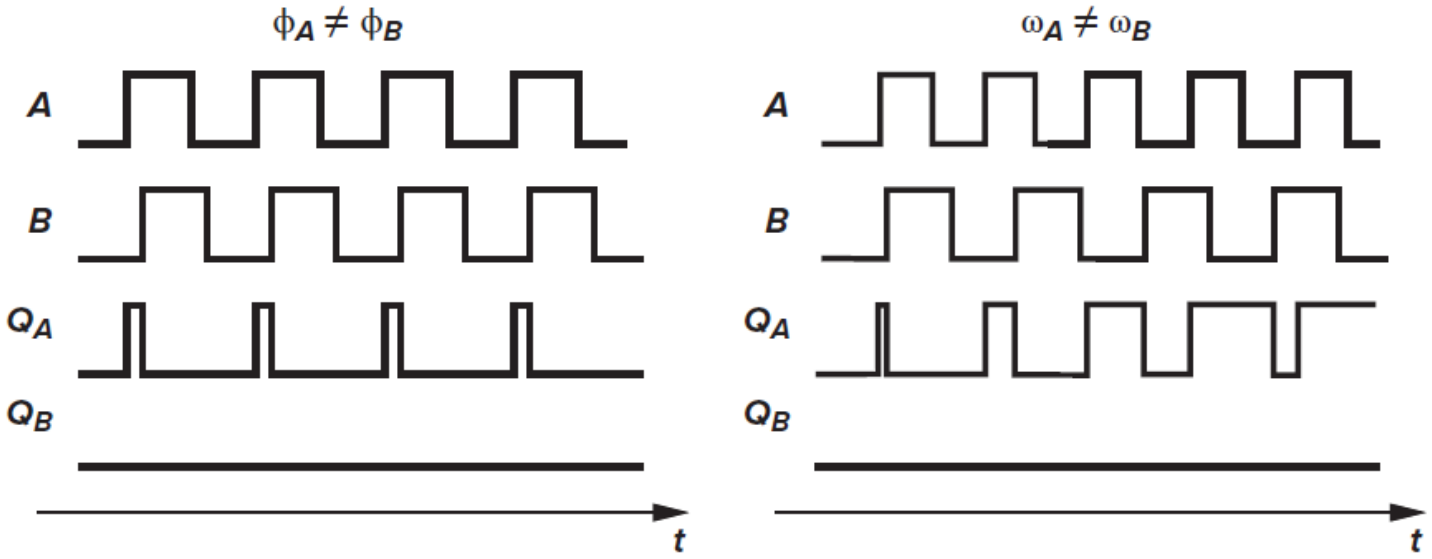


[Johns & Martin, 2012]

Charge Pump PFD

- QA: UP
- QB: DOWN (DN)

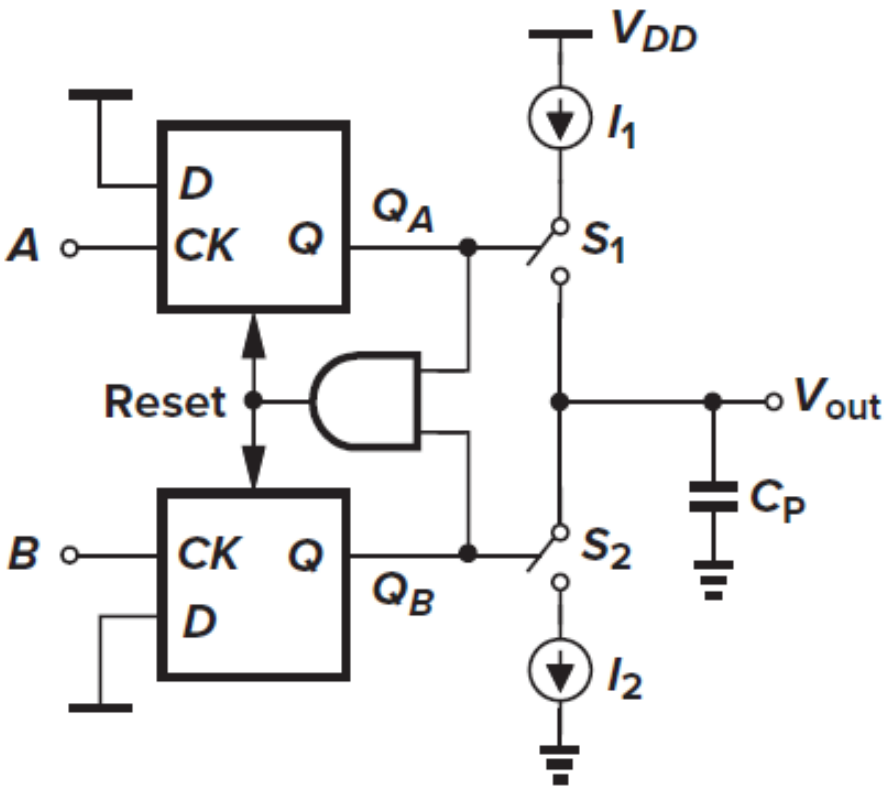


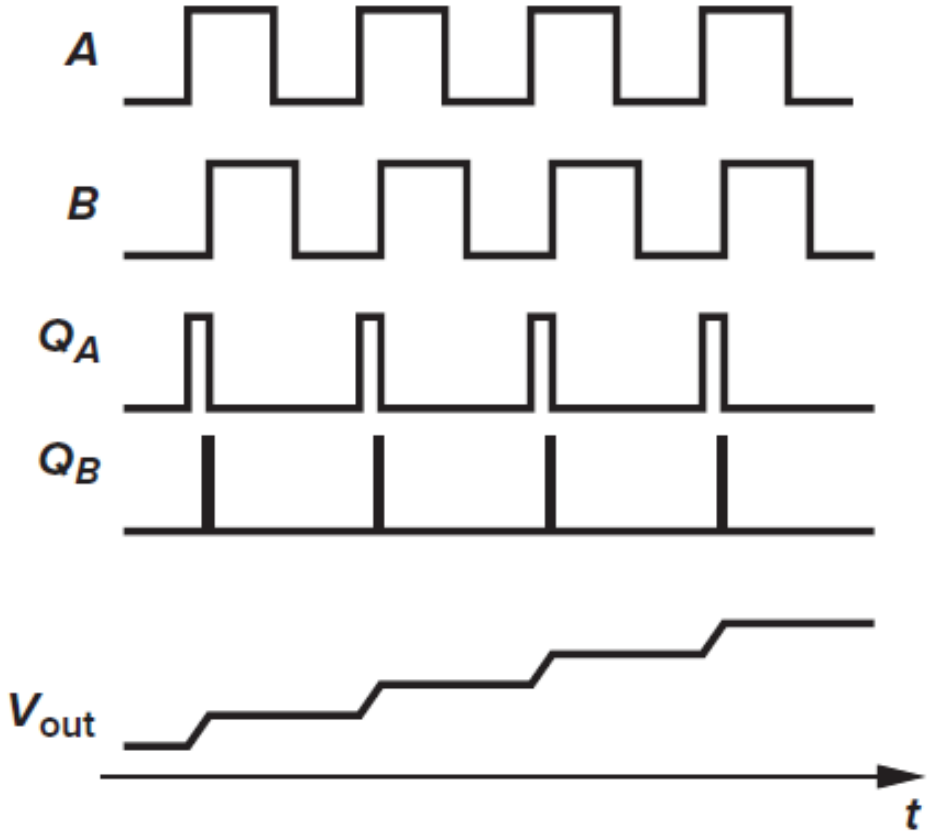


[Razavi, RF Microelectronics, 2012]

Charge Pump PFD

- A very small input phase error gives growing output
  - Infinite gain → Ideal integrator behavior

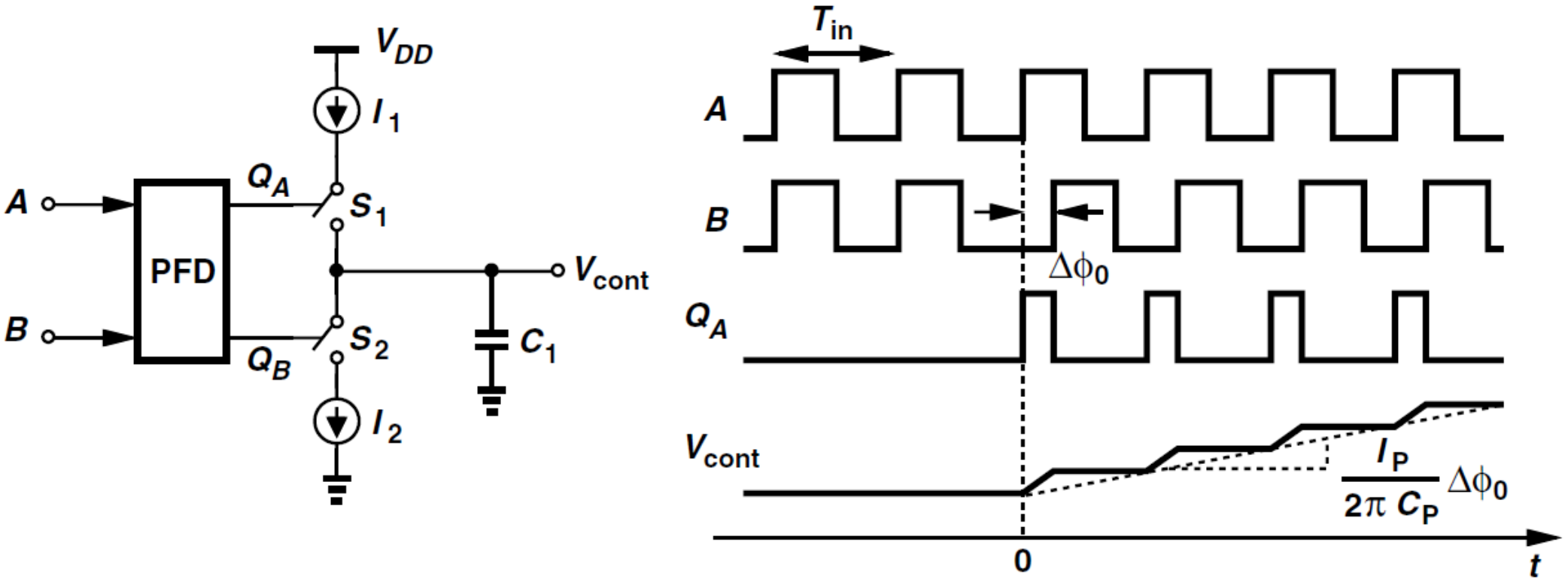




[Razavi, RF Microelectronics, 2012]

CHP PFD Continuous-time (CT) Approx

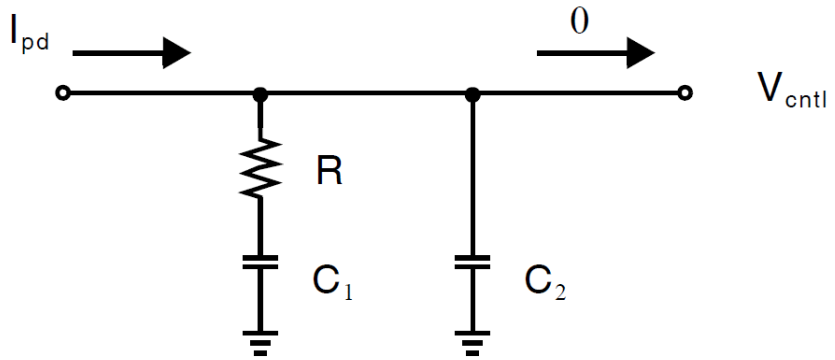
- CHP PFD is a non-linear system
  - But the waveform can be approximated as a ramp: CT approx



[Razavi, RF Microelectronics, 2012]

Loop Filter (LF)

- R introduces a zero necessary for stability
- C_2 introduces a high frequency pole to suppress voltage spikes
  - Current spikes passing through R will cause voltage spikes
- Usually $C_1 \gg C_2$



$$K_{lp}H_{lp}(s) = \frac{V_{cntl}(s)}{I_{pd}(s)} = \frac{1}{s(C_1 + C_2)} \cdot \frac{1 + sRC_1}{1 + sR\left(\frac{C_1C_2}{C_1 + C_2}\right)}$$

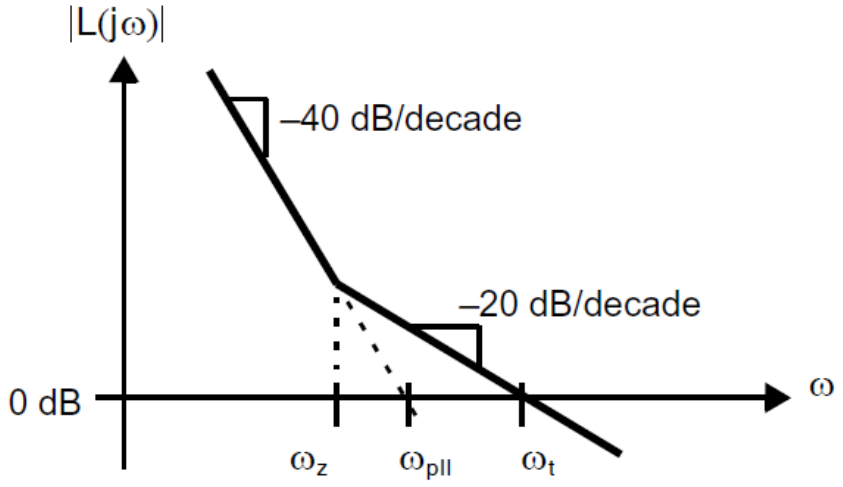
$$K_{lp}H_{lp}(s) = \frac{V_{cntl}(s)}{I_{pd}(s)} \cong \frac{1}{C_1}\left(\frac{1 + sRC_1}{s}\right)$$

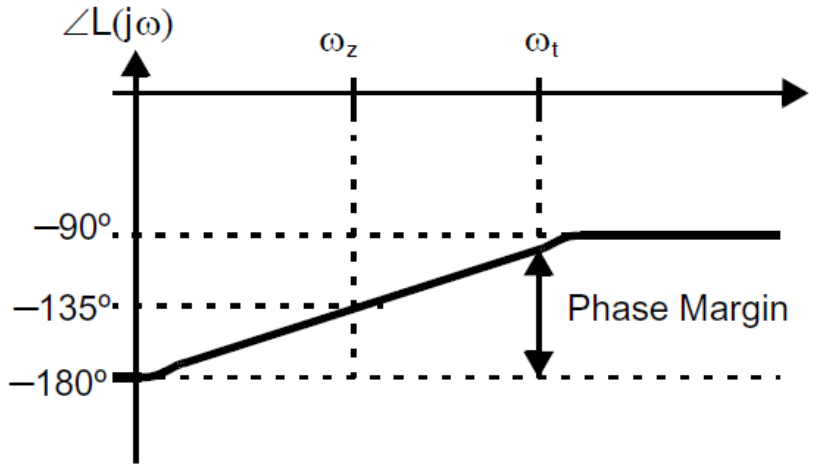
$$K_{lp} = 1/C_1 \qquad \omega_z = 1/(RC_1)$$

[Johns & Martin, 2012]

Bode Plot

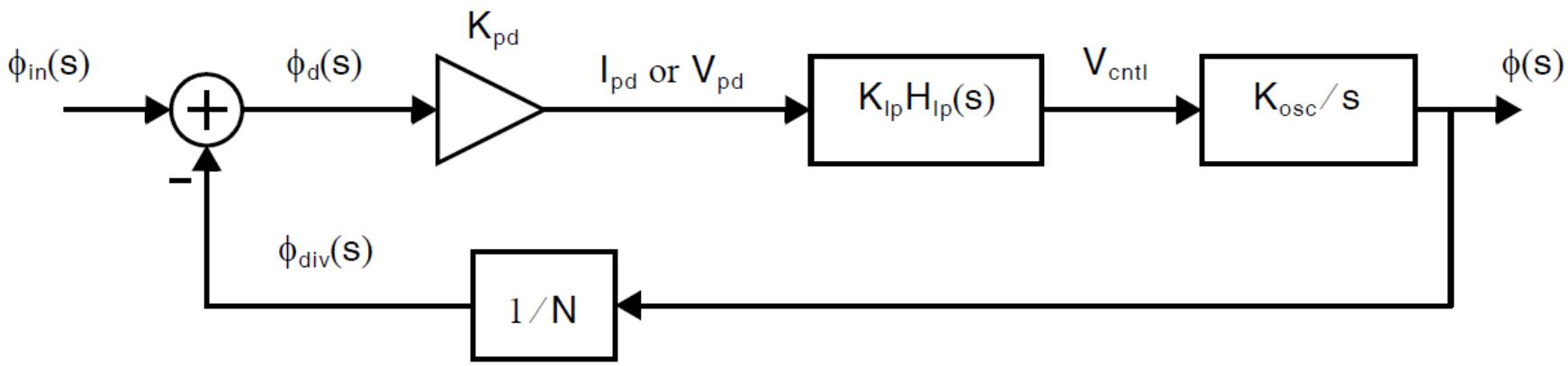
- Two poles at origin
- The zero is necessary to achieve stability
- The non-dominant pole due to C_2 reduces the PM
  - But necessary to filter out voltage spikes





[Johns & Martin, 2012]

Linearized Small-Signal Model



$$\frac{\phi_d(s)}{\phi_{in}(s)} = \frac{1}{1 + L(s)}$$

$$L(s) = \frac{K_{pd} K_{lp} K_{osc} H_{lp}(s)}{Ns}$$

$$\frac{\phi_d(s)}{\phi_{in}(s)} = \frac{s}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)/N}$$

[Johns & Martin, 2012]

PLL Model

- Loop constant (loop resonance frequency)

$$\omega_{pll} = \sqrt{\frac{K_{pd}K_{lp}K_{osc}}{N}}$$

- Loop gain

$$L(s) = \frac{\omega_{pll}^2}{s^2} \cdot \left(1 + \frac{s}{\omega_z}\right)$$

- Error TF

$$\frac{\phi_d(s)}{\phi_{in}(s)} = \frac{1}{\omega_{pll}^2} \cdot \frac{s^2}{\left(1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{pll}^2}\right)}$$

- Phase TF

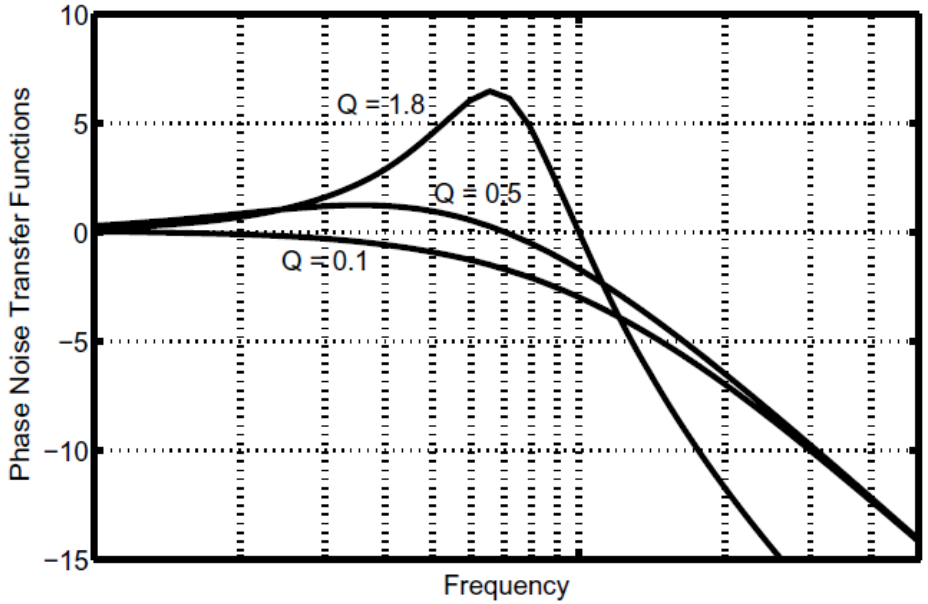
$$H(s) = \frac{\phi(s)}{\phi_{in}(s)} = \frac{N(1 + s/\omega_z)}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{pll}^2}}$$

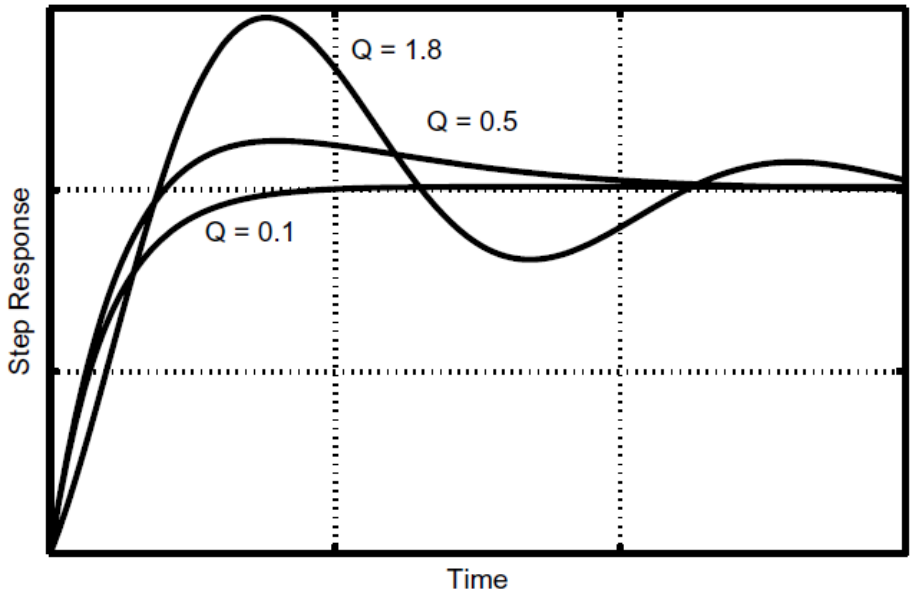
[Johns & Martin, 2012]

Closed Loop Response

$$H(s) = \frac{\phi(s)}{\phi_{in}(s)} = \frac{N(1 + s/\omega_z)}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{pll}^2}}$$

$$\omega_{pll} = \sqrt{\frac{K_{pd}K_{lp}K_{osc}}{N}} \qquad Q = \frac{\omega_z}{\omega_{pll}} \qquad \zeta = 1/2Q$$





[Johns & Martin, 2012]

Q = 0.5

- An all-pole system with Q = 0.5 will have no overshoot or peaking
  - But the PLL has a zero which introduces both slight overshoot and peaking (jitter peaking) even when Q = 0.5
- Q = 0.5 gives reasonable LF time constant → can be implemented on-chip

$$\omega_z = \omega_{pll}/2$$

$$H(s) = \frac{N(1 + s/\omega_z)}{(1 + s/\omega_{pll})^2}$$

$$\omega_{3dB} = 2.5\omega_{pll}$$

- Q = 0.1 offers even better tracking behavior, but generally demands a larger loop-filter time constant for the same loop bandwidth

Resolution-Bandwidth Trade-off

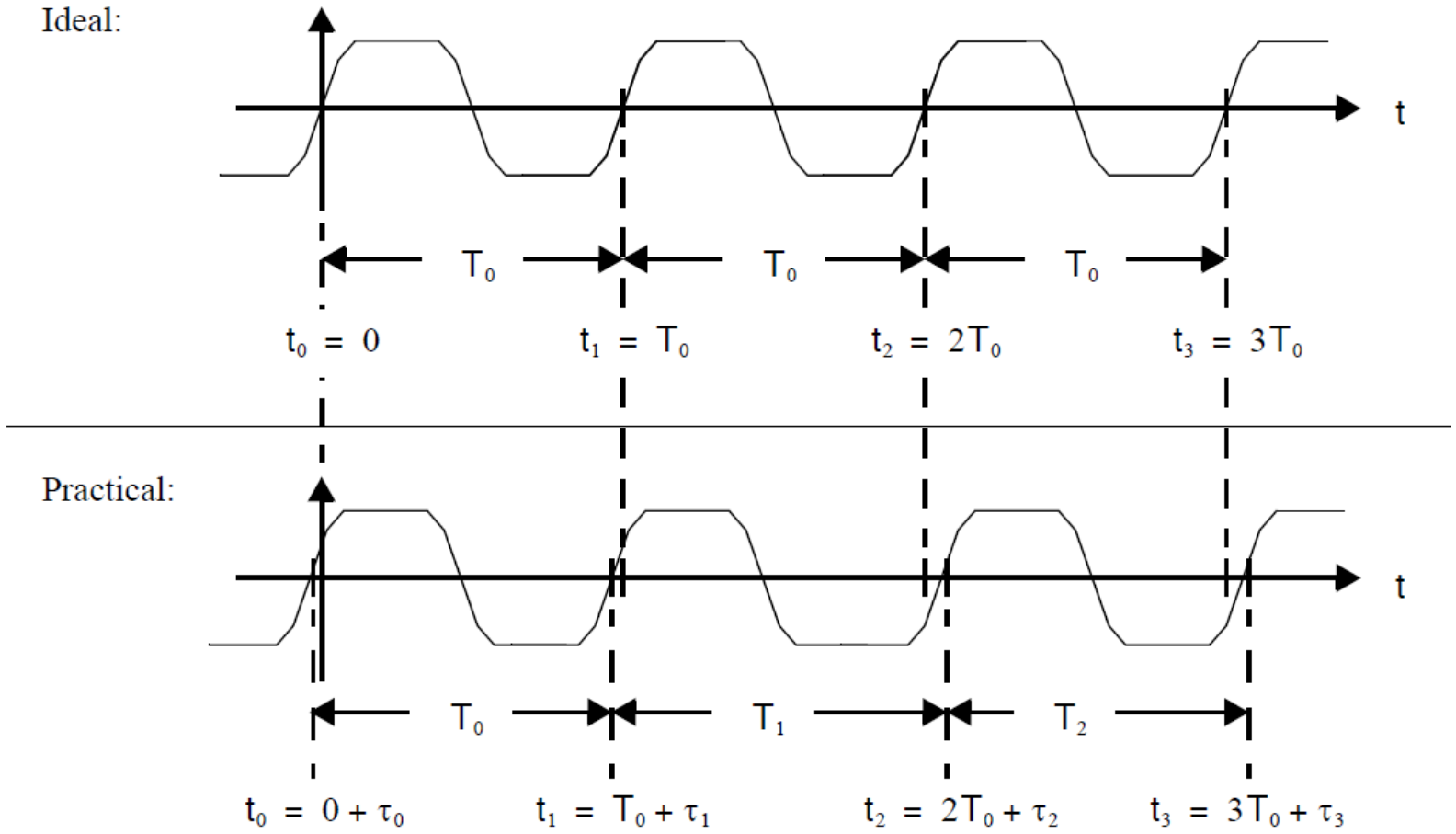
- For integer-N PLL, the tuning resolution is determined by ω_{in}
  - The smaller ω_{in}, the finer the resolution
  - If finer resolution is required, use fractional-N PLL
- PLL is a discrete time system
  - ω_{in} is the sampling frequency
  - For the PLL CT linear model approximation to be valid

$$\omega_{3dB} \ll \omega_{in}$$
$$\omega_{3dB} < 0.1\omega_{in}$$

  - Moreover, we need $\omega_{3dB} \ll \omega_{in}$ to filter out the reference spurs (reference transients modulate the VCO)
  - The smaller ω_{in}, the slower the loop (longer settling time)
  - Also higher loop bandwidths permit the use of smaller components in the loop filter

Jitter

- Jitter is the random variation in clock transition instants



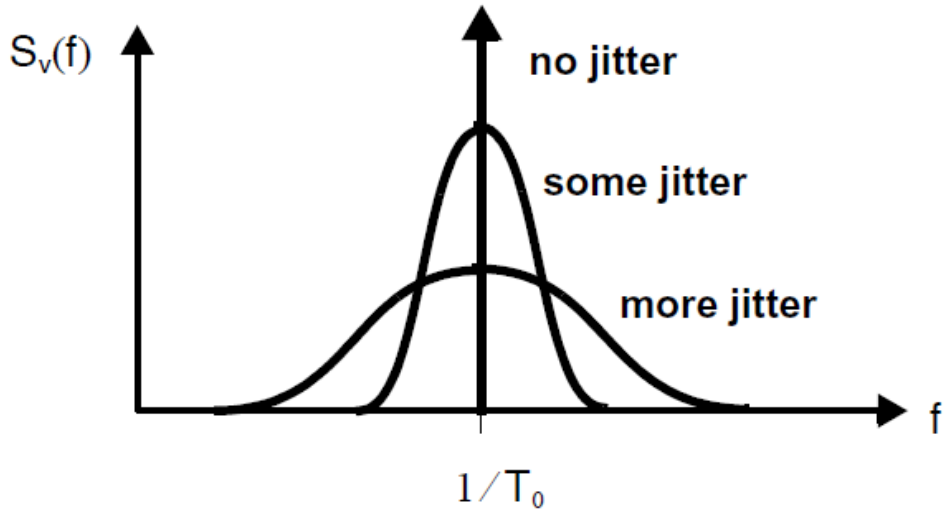
[Johns & Martin, 2012]

Phase Noise

- Phase noise is the frequency-domain representation of jitter
- Jitter (τ_k) to phase noise (ϕ_k):

$$t_k = kT_o + \tau_k \qquad \phi_k = \tau_k \cdot \frac{2\pi}{T_o}$$

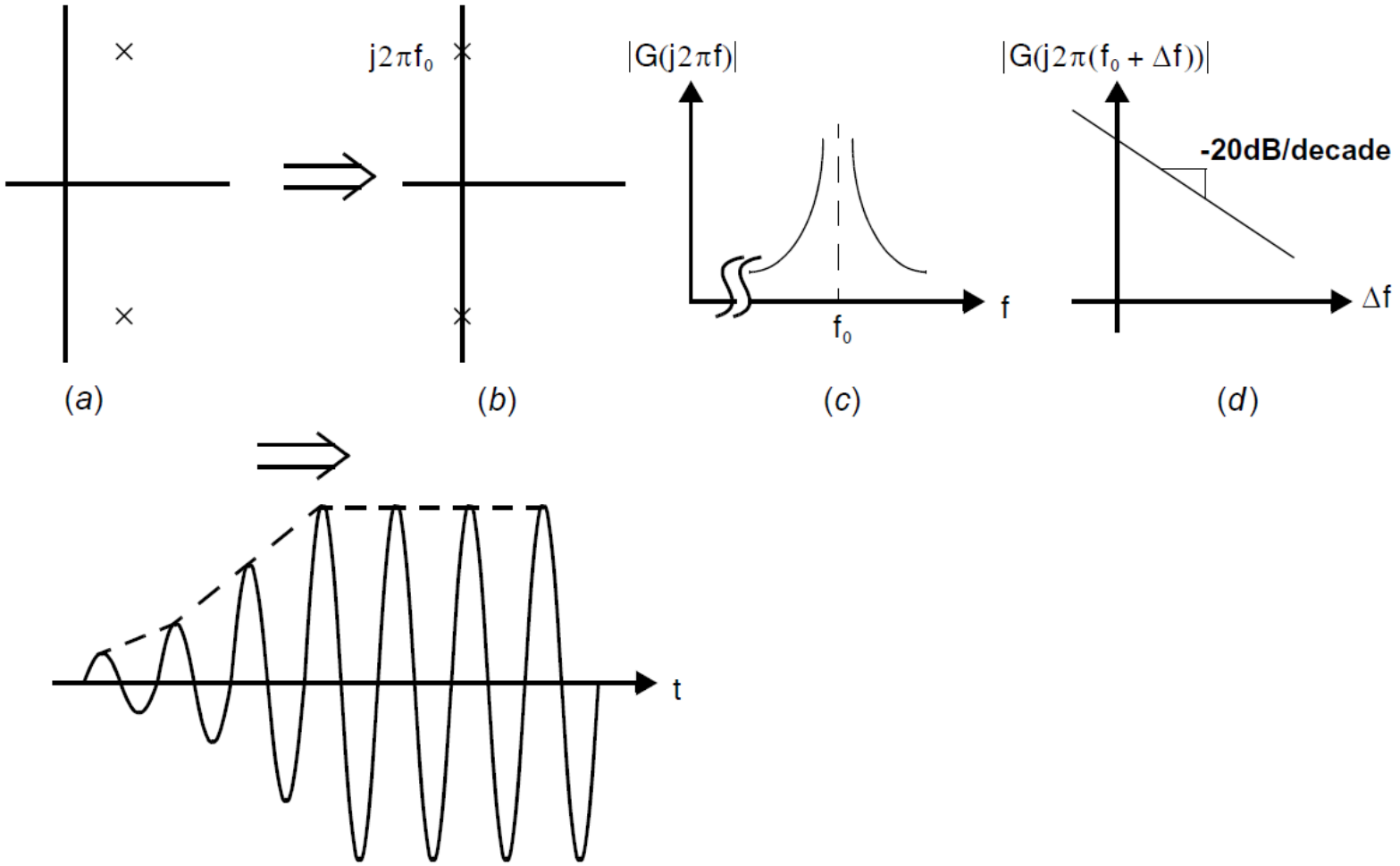
- A pure sinusoid will have a single tone at $1/T_o$
- A practical signal will have power in a range of frequencies around the pure tone (the carrier)



[Johns & Martin, 2012]

Oscillator Response

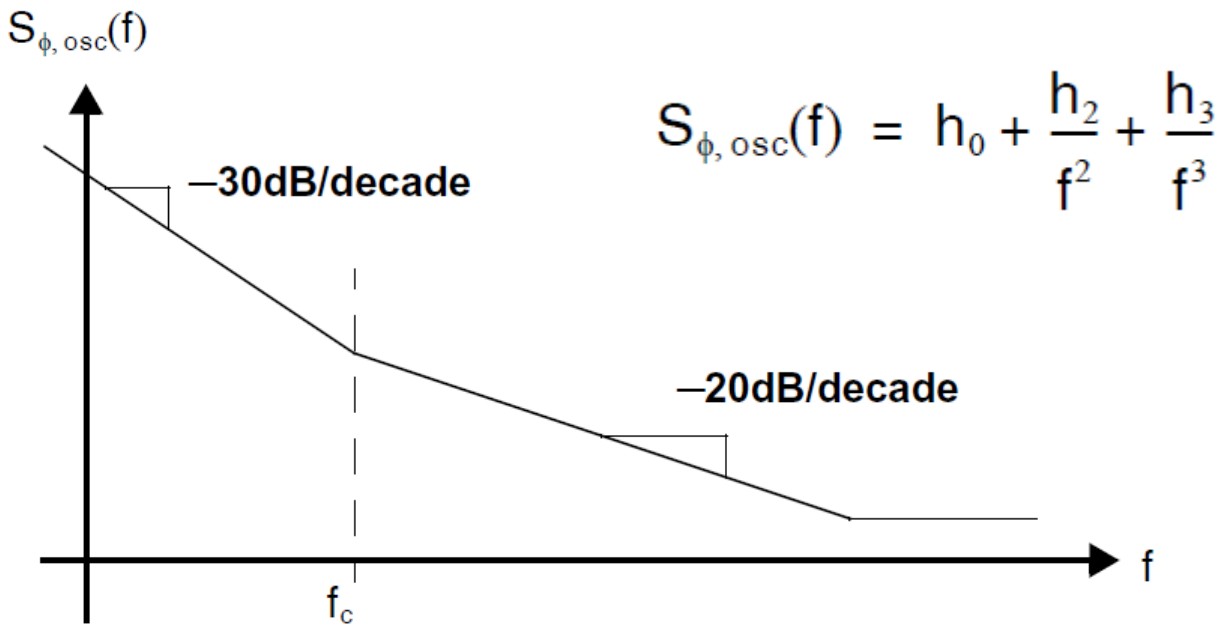
- The oscillator has a pole at f_o
- Away from the pole the magnitude decays at -20dB/decade



[Johns & Martin, 2012]

Oscillator Phase Noise

- 1st component: White noise not filtered by the oscillator (e.g., buffer noise)
- 2nd component: White noise up-converted and shaped by the oscillator response
- 3rd component: Flicker noise up-converted and shaped by the oscillator response



[Johns & Martin, 2012]

PLL Noise Sources

- Input and divider phase noise are filtered by the PLL transfer function (LPF) (output follows input within loop bandwidth)

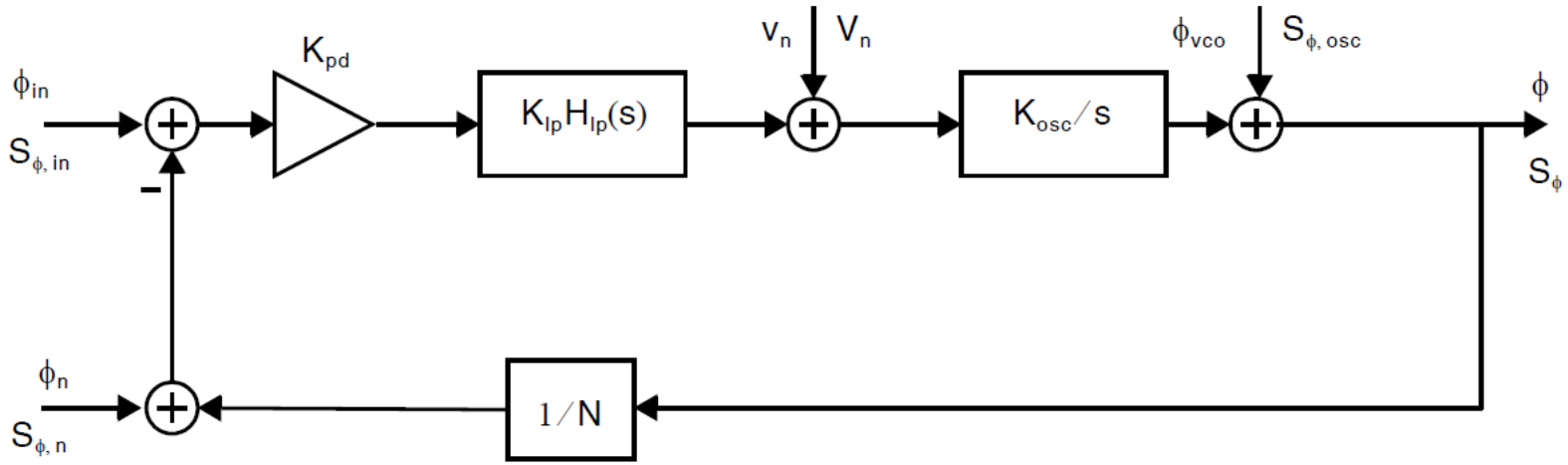
$$H(s) = \frac{K_{pd}K_{lp}K_{osc}H_{lp}(s)/s}{1 + L(s)}$$

- VCO phase noise sees a HPF (attenuated within loop bandwidth)

$$H_{osc}(s) = \frac{1}{1 + L(s)}$$

- Loop filter phase noise sees a BPF

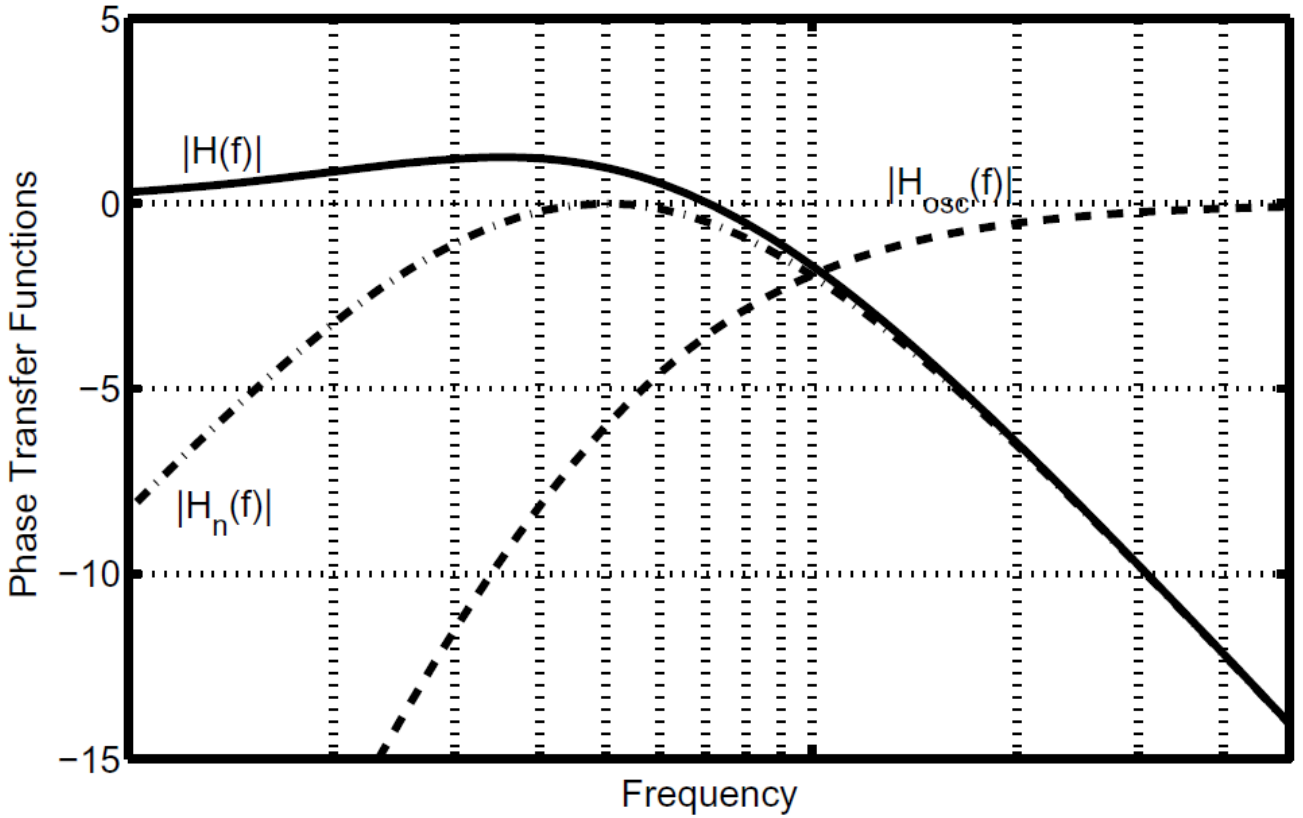
$$H_n(s) = \frac{K_{osc}/s}{1 + L(s)}$$



[Johns & Martin, 2012]

PLL Noise Sources

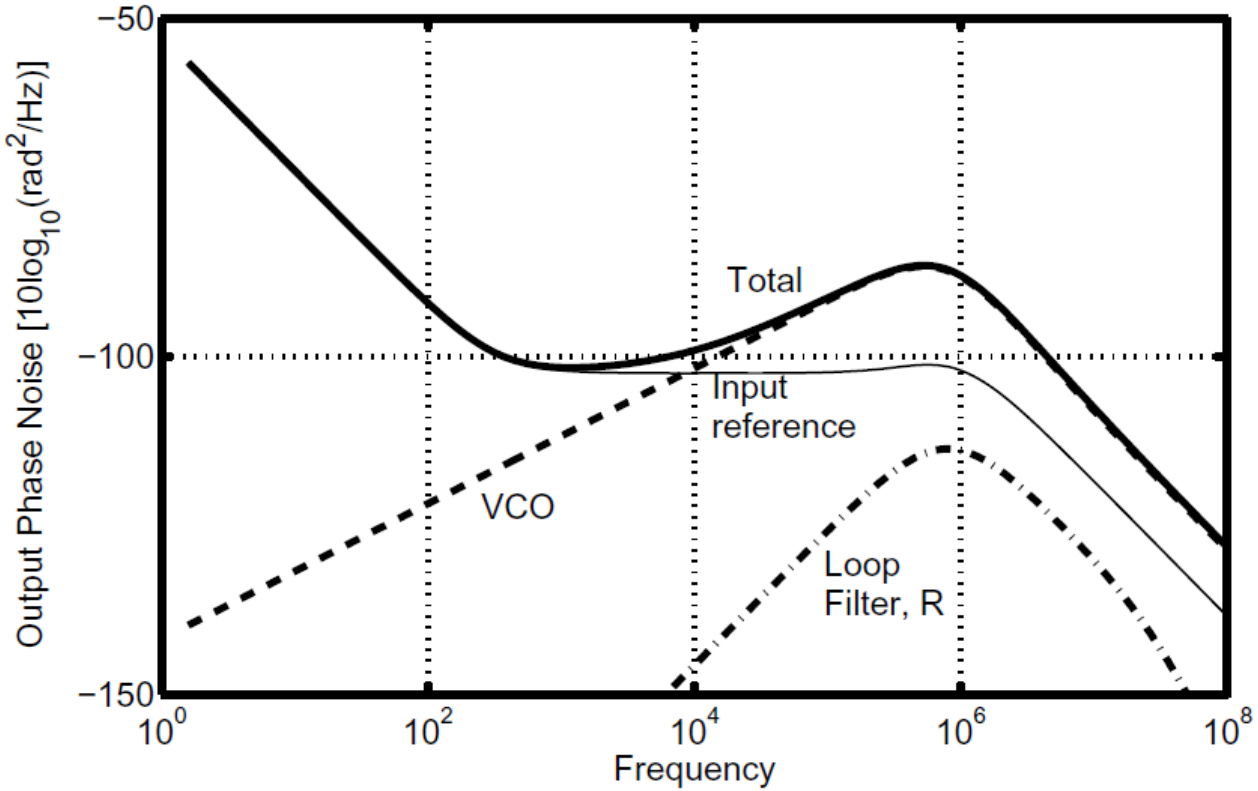
- The PLL loop bandwidth sets the cutoff frequency below which VCO phase noise is attenuated and above which input reference (and divider) phase noise is attenuated
- Solve Razavi RF Example 9.26 and 9.27



[Johns & Martin, 2012]

PLL Output Noise

- The example below ignores VCO white noise component ($h_0 = 0$)
- Assuming a high-quality (low-noise) reference
  - PLL loop bandwidth should be maximized to minimize the contribution of VCO phase noise to the PLL's output jitter



[Johns & Martin, 2012]

Thank you!

Assignments

- Read “pll_design.pdf”
  - Part of my MSc thesis (2010)