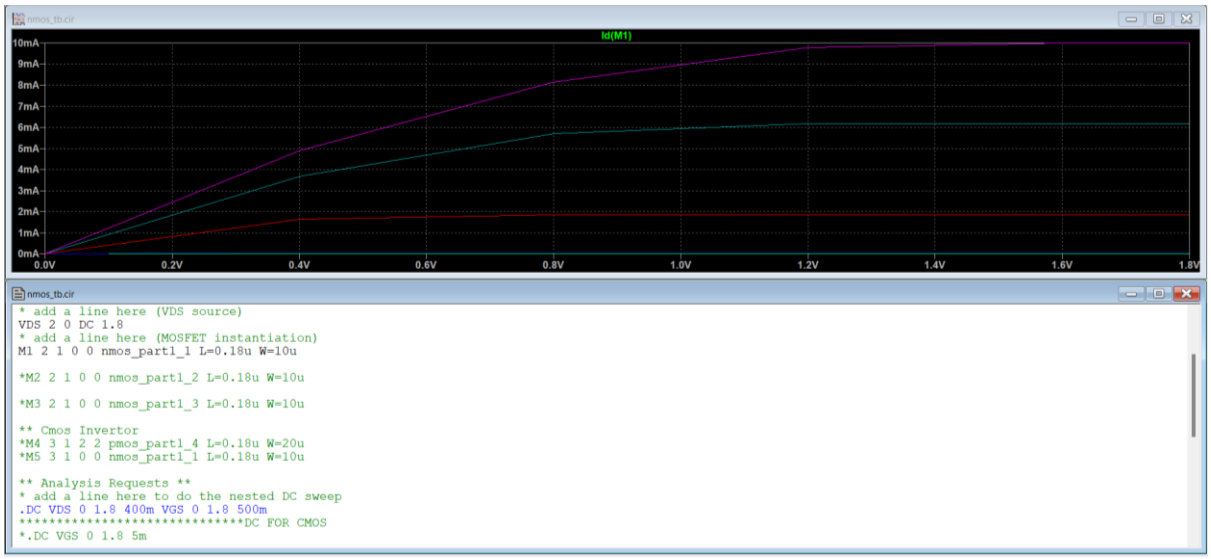
PART1:

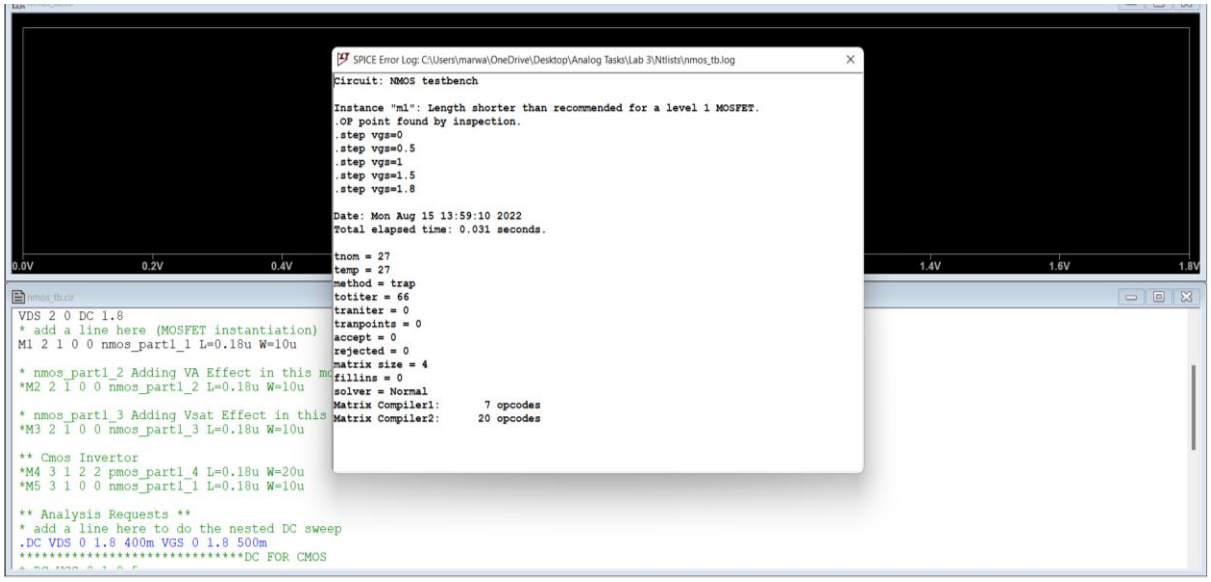
Question 1:

ID Vs VDS with different vgs .(DC SWEEP)



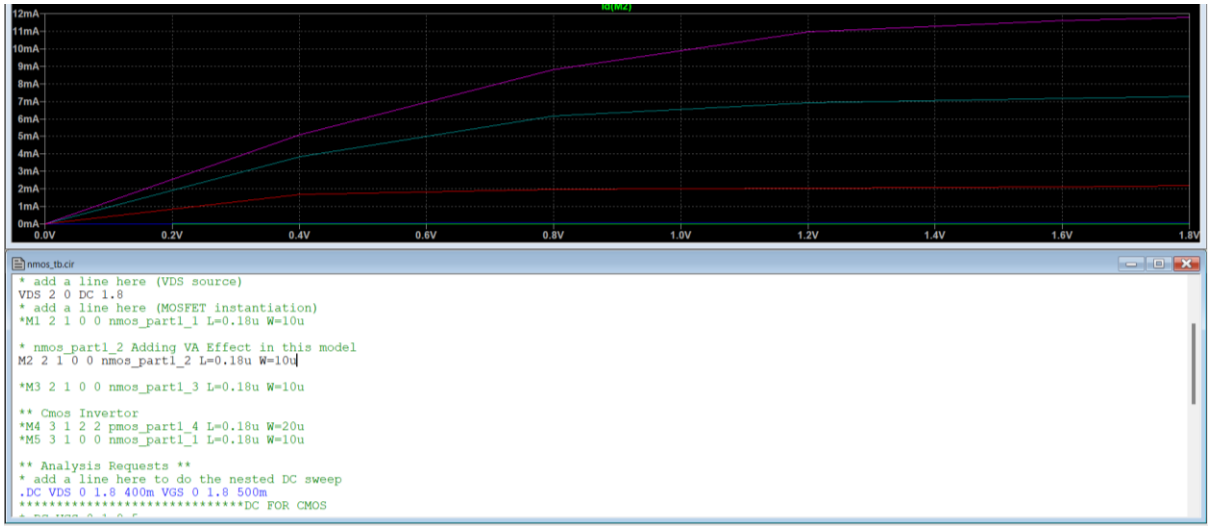
Nmos Model Used :

The Spice Error log Doesn’t recommend using Level 1 Model With This length it may be not Accurate (due to Short Channel Effect),

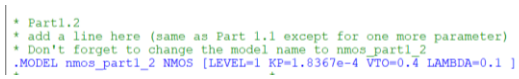


Question 2:

Added Early Effect (Ro Effect) you can See slope at the saturation region .

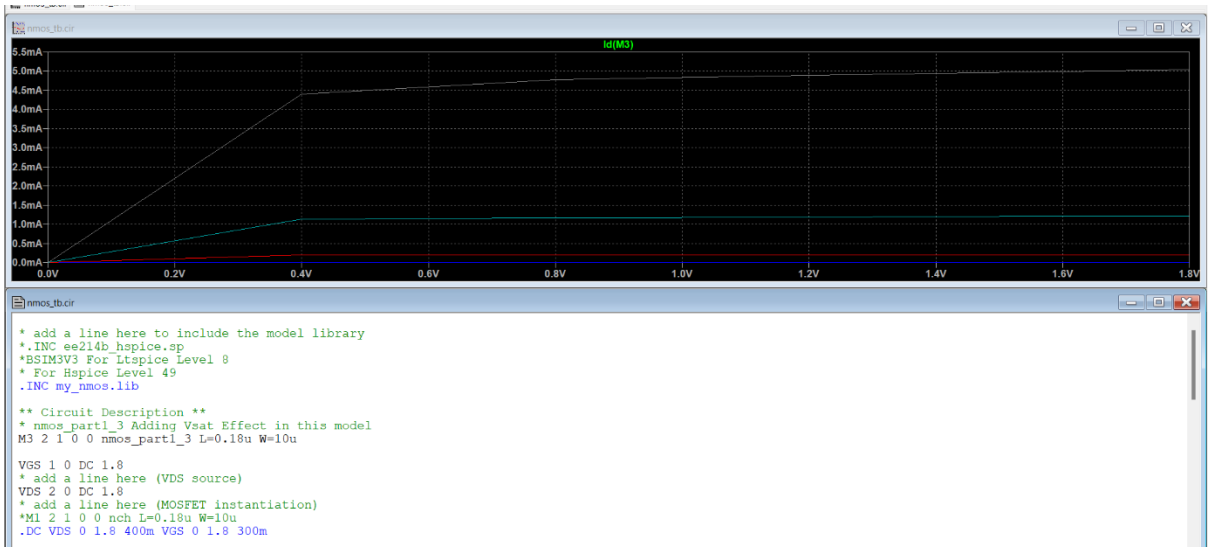


Model Used :



Question 3:

Velocity Saturation Effect Added.



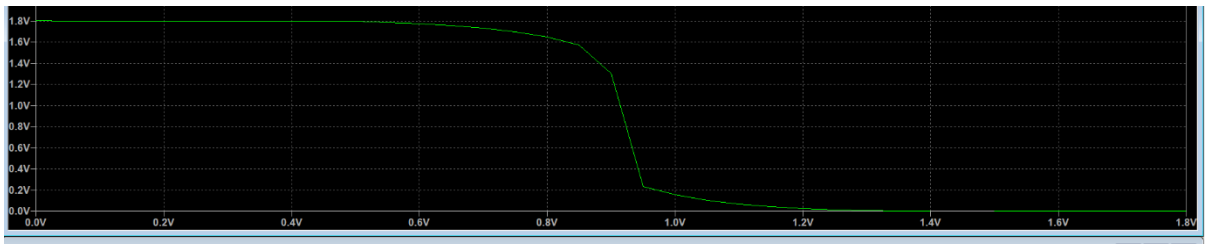
Model Used :

```
* Part 1.3
*.add a line here (same as Part 1.2 except for one more parameter)
.MODEL nmos_part1_3 NMOS [LEVEL=2 KP=1.8367e-4 VTO=0.4 LAMBDA=0.1 VMAX=3.34e5 ]
*-----------------------------------*
```

Question 4:

Vth must be -ve value (Pmos).

Cmos Invertor Dc Characteristics



Cmos Invertor Netlists

cmos_inv_dc.cir

```
CMOS inverter DC sweep


** Circuit Description **
* power supply
VDS 2 0 DC 1.8
*add a line here

* input
VIN 1 0 DC 0V
* circuit

*add two lines here (NMOS and PMOS instantiation)
** Cmos Invertor
M4 3 1 2 2 pmos_part1_4 L=0.18u W=20u
M5 3 1 0 0 nmos_part1_1 L=0.18u W=10u


*add a line here include the model file
* Including Libs
.INC my_nmos.lib
.INC my_pmos.lib
** Analysis Requests **
.DC VIN 0 1.8 0.05

** Outputs Requests **
.PROBE

.END
```

Pmos Library :

LTspice XVII - [my_pmos.lib]

File Edit View Simulate Tools Window Help

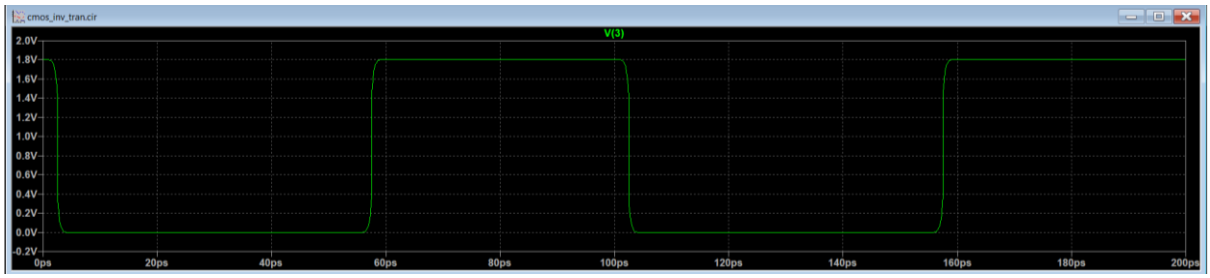
```
*Pmos Lib Question 1

* Part 1.4
.MODEL pmos_part1_4 PMOS [LEVEL=1 KP=91.835u VTO=-0.4 ]

*-----------------------------------*

* Adding Cj and CJSW Effects
* Part 1.6
.MODEL pmos_part1_6 PMOS [LEVEL=1 KP=91.835u VTO=-0.4 LAMBDA=0.1 CJ=1m CJSW=100p]
*-----------------------------------*
```

Nmos Library :

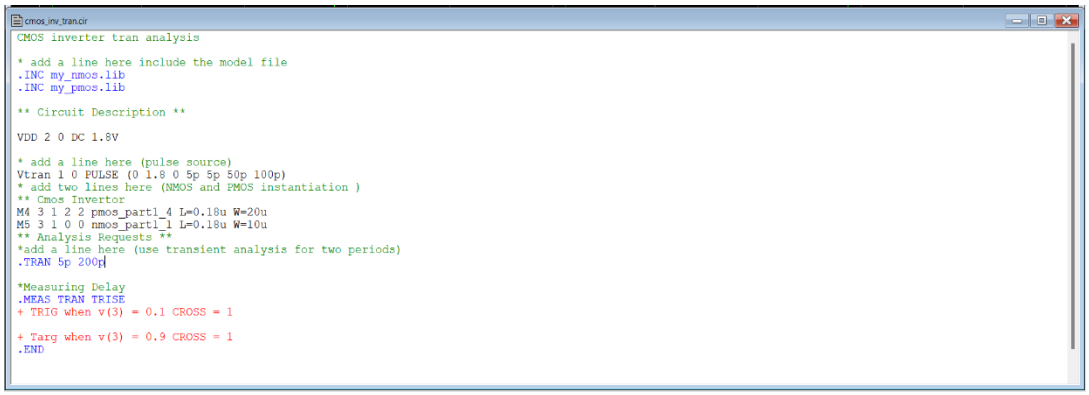
```
*----------------------------------*
* Part 1.1
.MODEL nmos_part1_1 NMOS [LEVEL=1 KP=183.67u VTO=0.4]

*----------------------------------*

* Part1.2
* add a line here (same as Part 1.1 except for one more parameter)
* Don't forget to change the model name to nmos_part1_2
.MODEL nmos_part1_2 NMOS [LEVEL=1 KP=1.8367e-4 VTO=0.4 LAMBDA=0.1 ]
*----------------------------------*

* Part 1.3
*.add a line here (same as Part 1.2 except for one more parameter)
.MODEL nmos_part1_3 NMOS [LEVEL=2 KP=1.8367e-4 VTO=0.4 LAMBDA=0.1 VMAX=3.34e5 ]
*----------------------------------*

* Part 1.6
* add a line here (same as Part 1.3 but you have to add CJ and CJSW. Take care of the units)
.MODEL nmos_part1_6 NMOS [LEVEL=1 KP=1.8367e-4 VTO=0.4 LAMBDA=0.1 CJ=1m CJSW=100p]
```

Question 5:

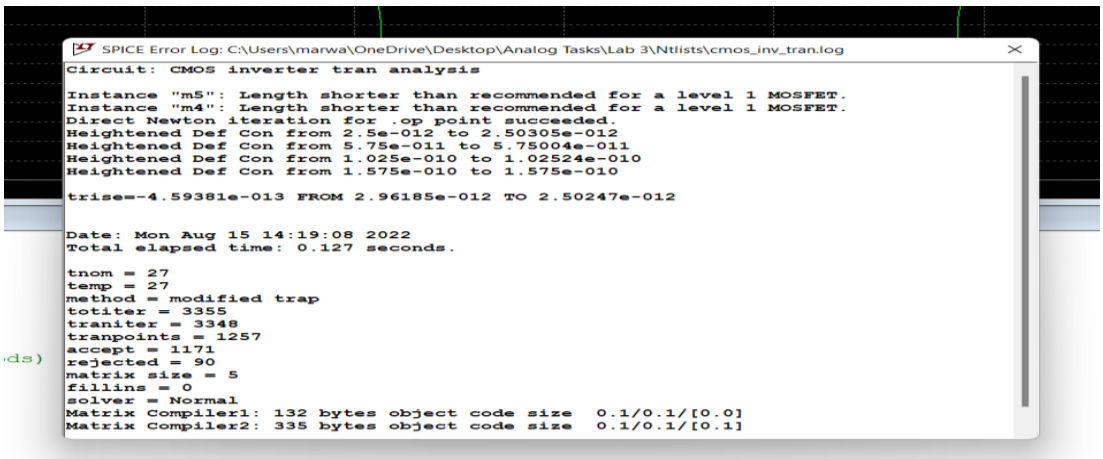
Transient Graph :



Netlist:

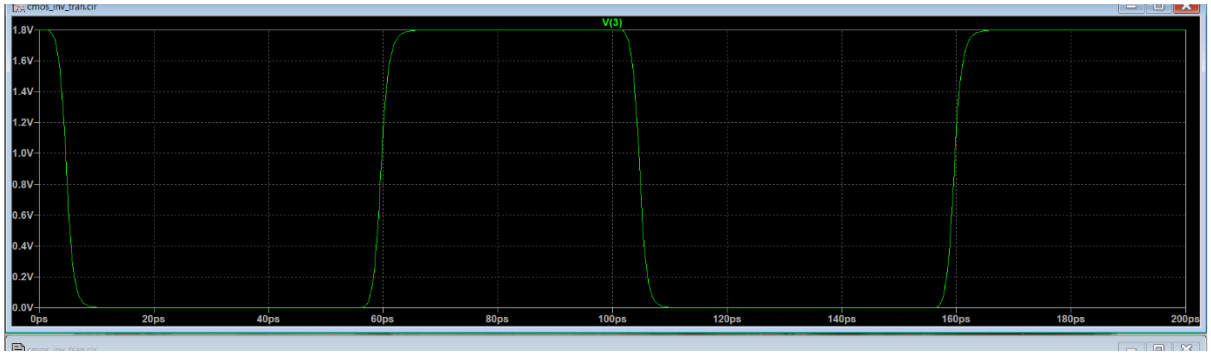


Delay Measurment:



Question 6:

Transient Graph :



Netlist:

cmos_inv_tran.cir

```
* add a line here include the model file
.INC my_nmos.lib
.INC my_pmos.lib

** Circuit Description **

VDD 2 0 DC 1.8V

* add a line here (pulse source)
Vtran 1 0 PULSE (0 1.8 0 5p 5p 50p 100p)
* add two lines here (NMOS and PMOS instantiation )
** Cmos Invertor
*M4 3 1 2 2 pmos_part1_4 L=0.18u W=20u
*M5 3 1 0 0 nmos_part1_1 L=0.18u W=10u


*** Part 6
** Cmos Invertor With Caps
M6 3 1 2 2 pmos_part1_6 L=0.18u W=20u PD=22u PS=22u AD=9p AS=9p
M7 3 1 0 0 nmos_part1_6 L=0.18u W=10u PD=10.9u PS=10.9u AD=4.5p AS=4.5p


** Analysis Requests **
*add a line here (use transient analysis for two periods)
.TRAN 5p 200p

*Measuring Delay
.MEAS TRAN TRISE
+ TRIG when v(3) = 0.1 CROSS = 1

+ Targ when v(3) = 0.9 CROSS = 1
.END
```

Delay Measurment:

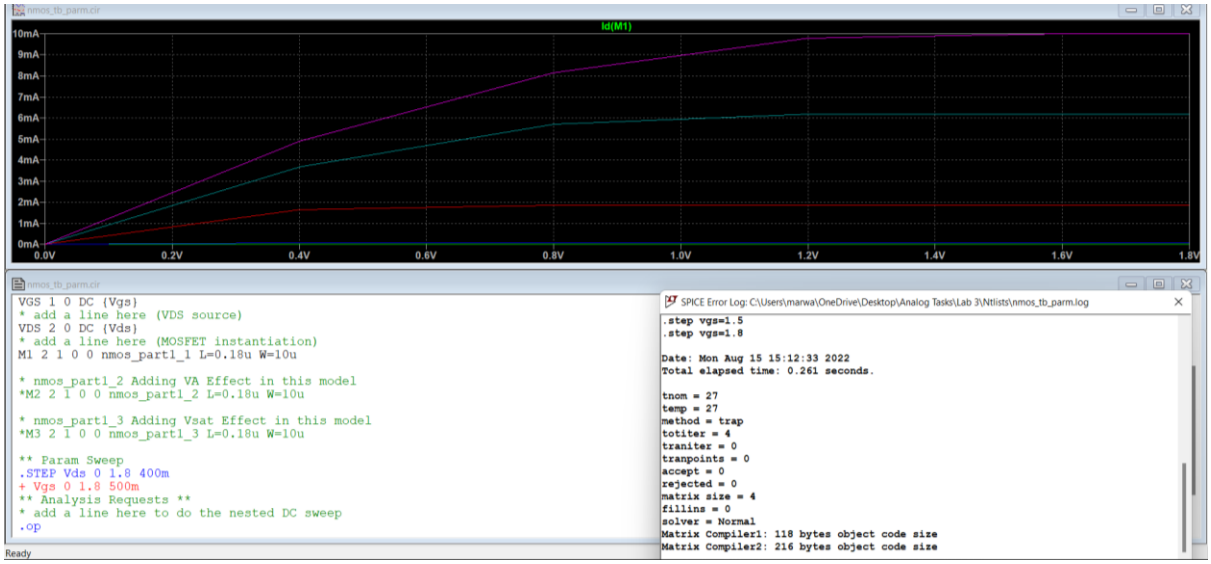
SPICE Error Log: C:\Users\marwa\OneDrive\Desktop\Analog Tasks\Lab 3\Ntlists\cmos_inv_tran.log

```
Circuit: CMOS inverter tran analysis

Instance "m7": Length shorter than recommended for a level 1 MOSFET.
Instance "m6": Length shorter than recommended for a level 1 MOSFET.
Direct Newton iteration for .op point succeeded.

trise=-1.98619e-012 FROM 6.70334e-012 TO 4.71715e-012


Date: Mon Aug 15 14:22:00 2022
Total elapsed time: 0.049 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2248
traniter = 2241
tranpoints = 1094
accept = 1081
rejected = 13
matrix size = 5
fillins = 0
solver = Normal
Matrix Compiler1: 150 bytes object code size  0.1/0.1/[0.0]
Matrix Compiler2: off  [0.1]/0.1/0.1
```

8u W=20u

PART2:

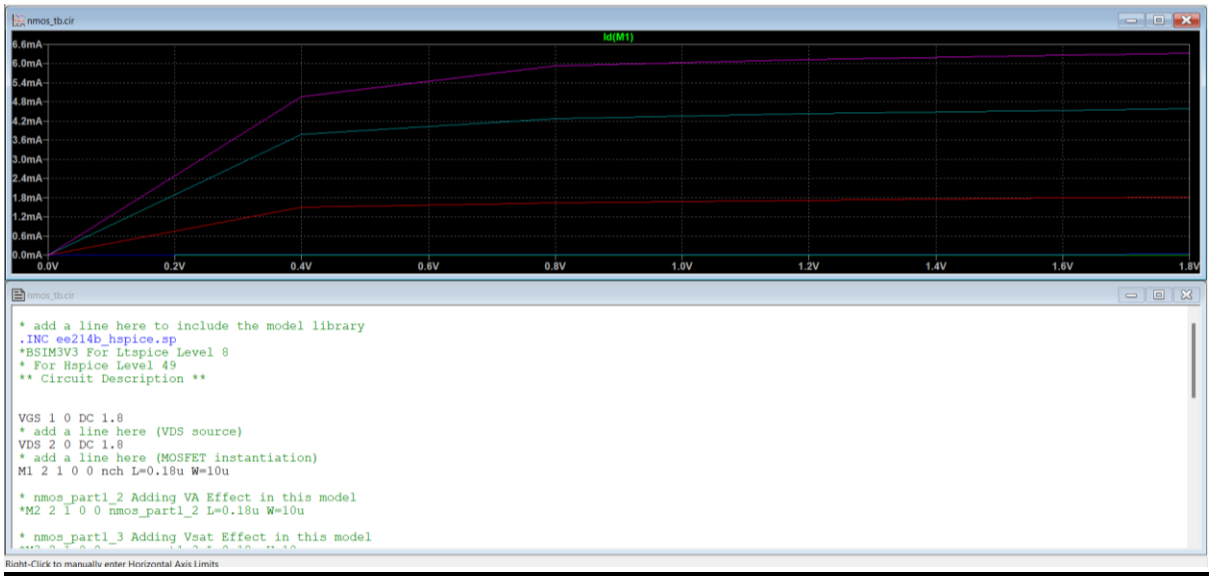
Question 1 :



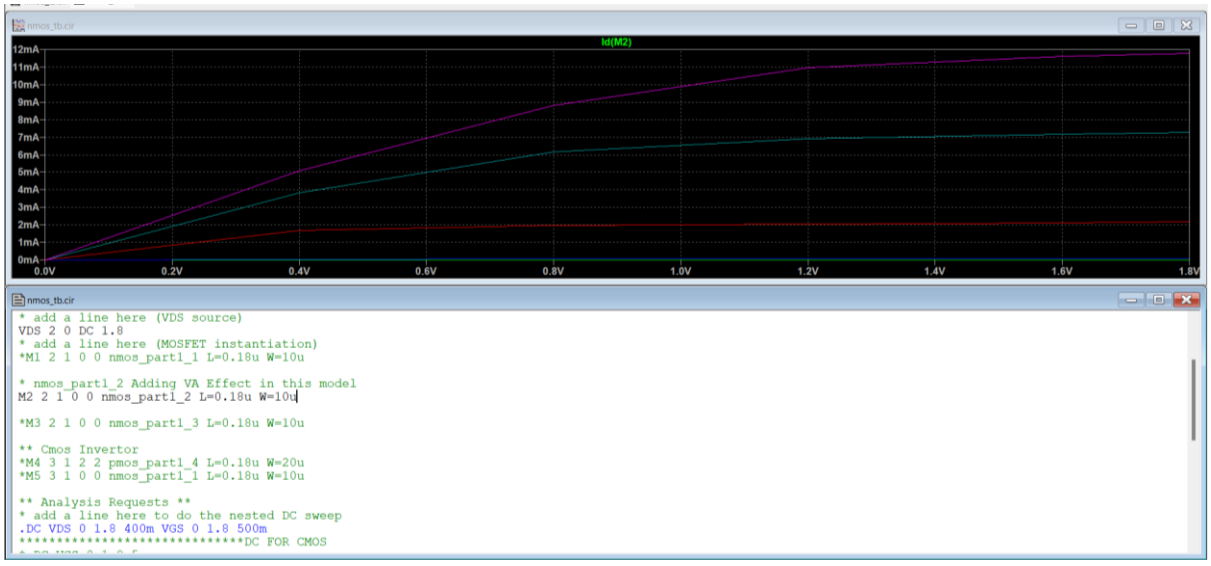
Using Dc Sweep is much faster about 8.5x Faster Than using Parametric Sweeps.

Question 2 :

The files uses BSIM3v3 the Level Parameter Must be Set to Level 8 @Ltspice.

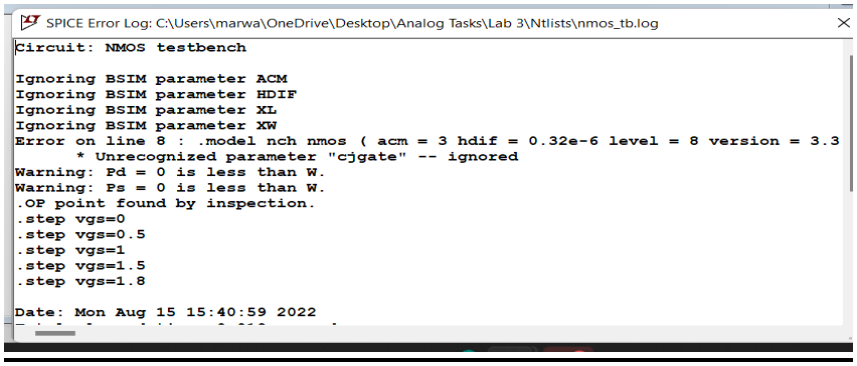


Level 1 Model :



Bsim3v3 is more Accurate as it uses more Advanced Models , But Level 1 Uses The Square law which is valid only With Long Channel devices so it didn't give accurate results for our 180n L Device As Shown.

Question 3 :



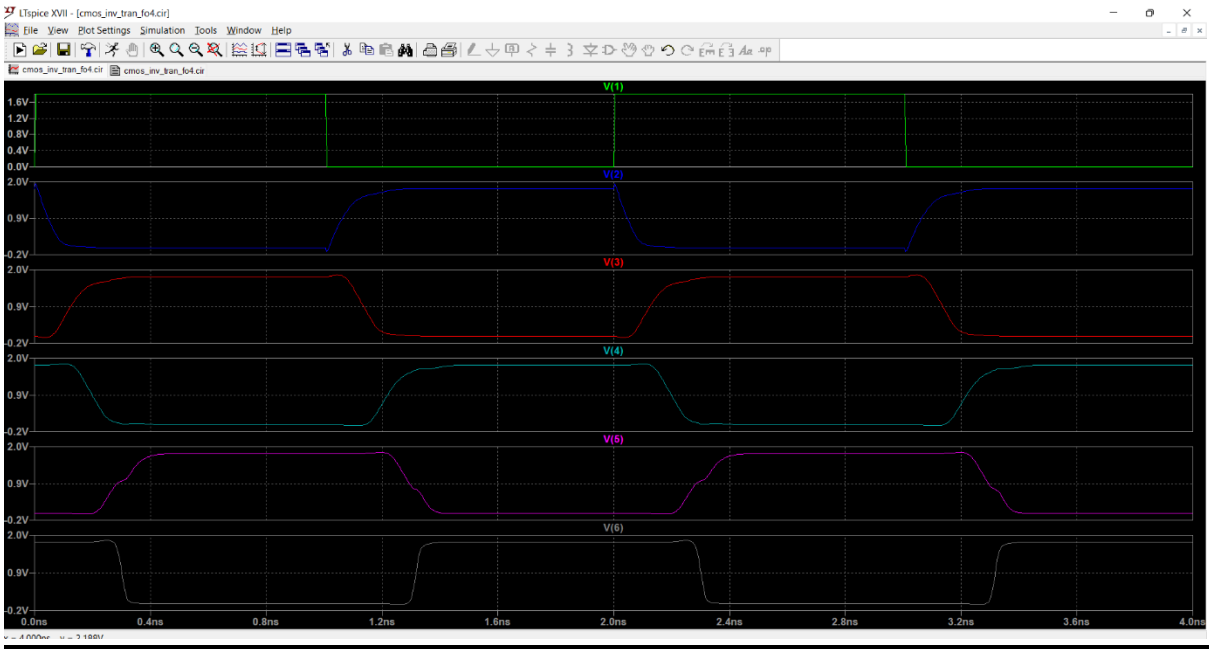
ACM	Area Calculation Method it Describe How to Calculate the area of Drain , Source Changing This will change in The Area of the Device and Capacitance.

HDIF	Length of highly Dopped Diffusion , will change The Capacitance of Source , Drain.
XL	Length for The Masking and Etching Process , It will Effect The Effective length of the Device.
XW	Width for The Masking and Etching Process , It will Effect The Effective Width of the Device.

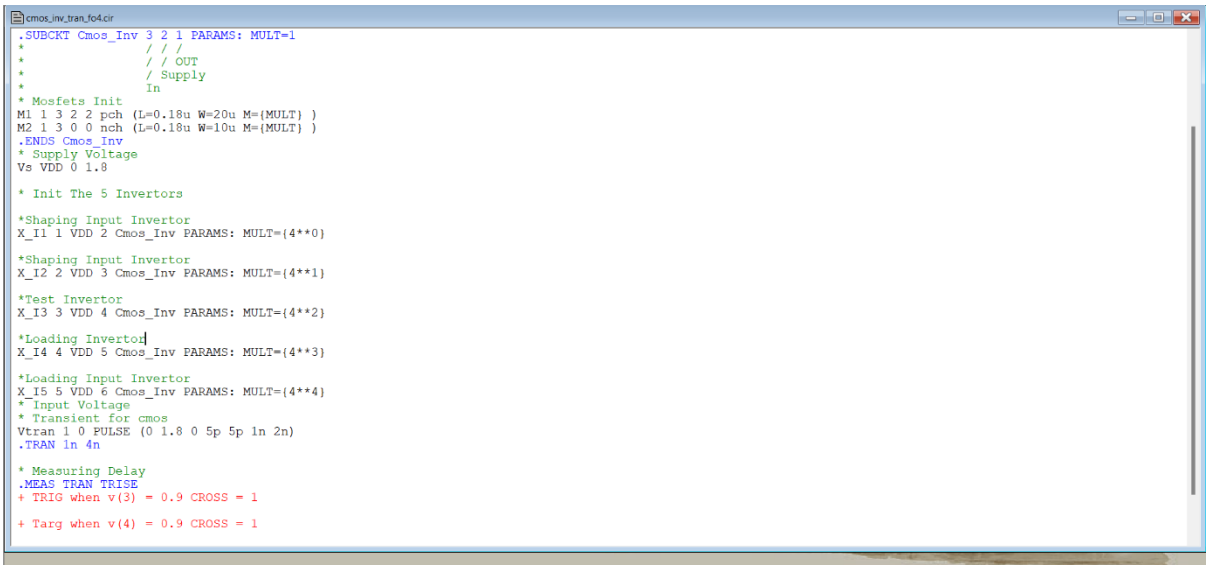
This BSIM Parameters are not supported in ltspice , if it was supported the area modifications will effect the caps that effects the speed of the transistor , and effective width may Effect the current.

Question 4 :

FO4 Graph :



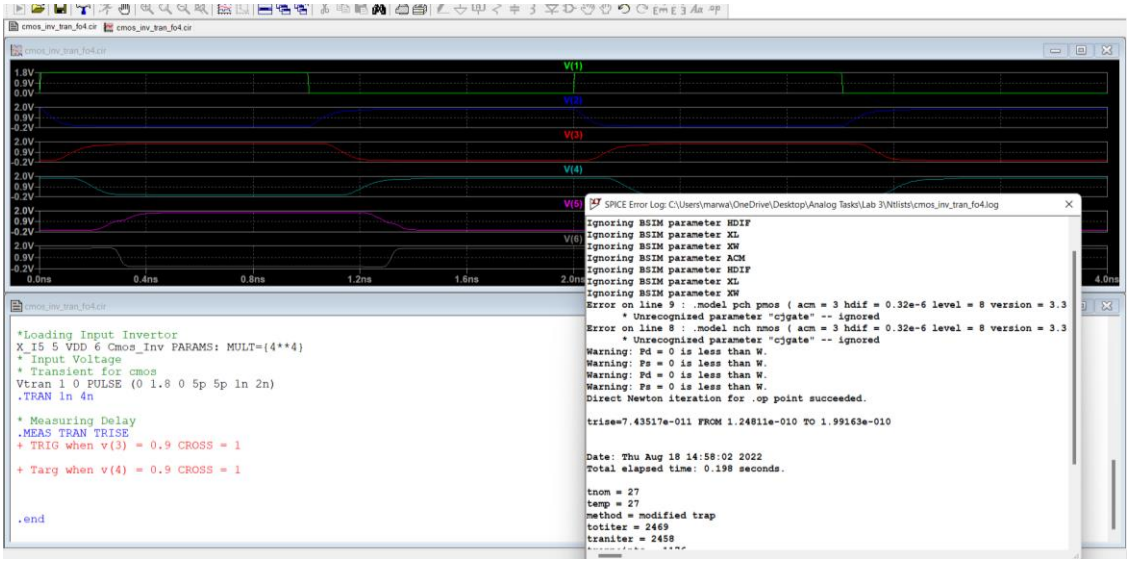
FO4 Netlist :



```
cmos_inv_tran_fo4.cir
.SUBCKT Cmos_Inv 3 2 1 PARAMS: MULT=1
*                / / /
*                / / OUT
*                / Supply
*                In
* Mosfets Init
M1 1 3 2 2 pch (L=0.18u W=20u M={MULT} )
M2 1 3 0 0 nch (L=0.18u W=10u M={MULT} )
.ENDS Cmos_Inv
* Supply Voltage
Vs VDD 0 1.8

* Init The 5 Invertors

*Shaping Input Invertor
X_I1 1 VDD 2 Cmos_Inv PARAMS: MULT={4**0}

*Shaping Input Invertor
X_I2 2 VDD 3 Cmos_Inv PARAMS: MULT={4**1}

*Test Invertor
X_I3 3 VDD 4 Cmos_Inv PARAMS: MULT={4**2}

*Loading Invertor
X_I4 4 VDD 5 Cmos_Inv PARAMS: MULT={4**3}

*Loading Input Invertor
X_I5 5 VDD 6 Cmos_Inv PARAMS: MULT={4**4}
* Input Voltage
* Transient for cmos
Vtran 1 0 PULSE (0 1.8 0 5p 5p 1n 2n)
.TRAN 1n 4n

* Measuring Delay
.MEAS TRAN TRISE
+ TRIG when v(3) = 0.9 CROSS = 1

+ Targ when v(4) = 0.9 CROSS = 1
```

Question 5 :

Measuring Delay :



```
*Loading Input Invertor
X_I5 5 VDD 6 Cmos_Inv PARAMS: MULT={4**4}
* Input Voltage
* Transient for cmos
Vtran 1 0 PULSE (0 1.8 0 5p 5p 1n 2n)
.TRAN 1n 4n

* Measuring Delay
.MEAS TRAN TRISE
+ TRIG when v(3) = 0.9 CROSS = 1

+ Targ when v(4) = 0.9 CROSS = 1


.end
```

```
SPICE Error Log: C:\Users\marwa\OneDrive\Desktop\Analog Tasks\Lab 3\Ntlists\cmos_inv_tran_fo4.log
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter ACM
Ignoring BSIM parameter HDIF
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Error on line 9 : .model pch pmos ( acm = 3 hdif = 0.32e-6 level = 8 version = 3.3
     * Unrecognized parameter "cjgate" -- ignored
Error on line 8 : .model nch nmos ( acm = 3 hdif = 0.32e-6 level = 8 version = 3.3
     * Unrecognized parameter "cjgate" -- ignored
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

trise=7.43517e-011 FROM 1.24811e-010 TO 1.99163e-010


Date: Thu Aug 18 14:58:02 2022
Total elapsed time: 0.198 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2469
traniter = 2458
```

Delay/Lamda = 826.13E-6

Delay For 65nm Tech = 26.8492p