Phase 1 Computer Architecture Project Report

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Instruction Opcodes

No	Instruction	Subcode
1	NOP	00000
2	NOT	00001
3	NEG	00010
4	INC	00011
5	DEC	00100
6	OUT	00101
7	IN	00110
8	MOV	00111
9	SWAP	01000
10	ADD	01001
11	ADDI	01010
12	SUB	01011
13	SUBI	01100
14	AND	01101
15	OR	01110
16	XOR	01111
17	CMP	10000
18	PUSH	10001
19	POP	10010
20	LDM	10011
21	LDD	10100
22	STD	10101
23	PROTECT	10110
24	FREE	10111
25	JZ	11000
26	JMP	11001
27	CALL	11010
28	RET	11011
29	RTI	11100

30	INTERRUPT	11101
31	RESET	11110

Instruction Bits Details:

General Form of all non-immediate instructions (16-bits):

5 bits	3 bits	3 bits	3 bits	2 bits
Opcode	Src 1	Src2	Destination	XX

Immediate Instructions (LDM, IADD) Form:

5 bits	3 bits	3 bits	3 bits	2 bits	16 bits
Opcode	Src 1	xxx	Destination	XX	Immediate Value

Examples of Instructions:

- **PUSH, OUT**

5 bits	3 bits	8 bits
Opcode	Src 1	XXXXXXXX

- **INC, DEC, NOT, MOV**

5 bits	3 bits	3 bits	3 bits	2
Opcode	Src 1	xxx	Destination	xx

- **ADD, SUB, AND, OR**

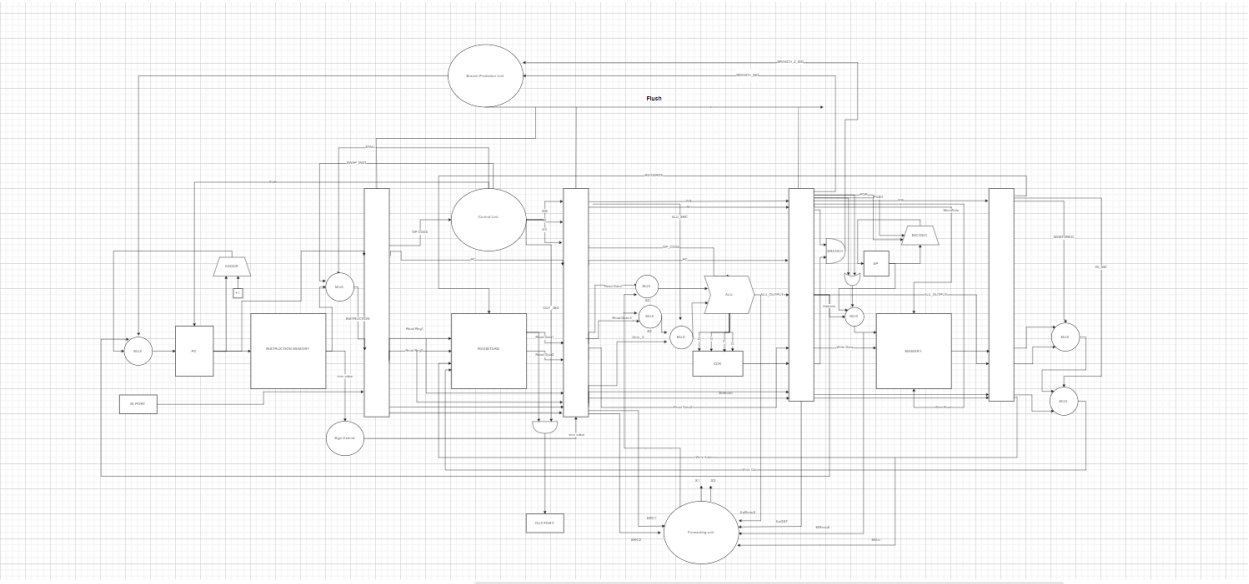
5 bits	3 bits	3 bits	3 bits	2 bits
Opcode	Src 1	Src2	Destination	XX

Control Signals Details:

Signal	Function
MemtoReg	Chooses Src for Wb either memory or Alu Output
AluSrc	Chooses if 2nd operand is read data or immediate value
RegWrite	Register Write Enable
MemWrite	Memory Write Enable
Stall	Stalls pipeline by sending NOP to Buffer
SwapInstruction	Indicates swap instruction switches operands and resends instruction
Branch0	JZ Operation
BranchU	JMP Operation
Push	Stack PUSH
Pop	STACK POP

InSig	IN port Enable
OutSig	OUT port Enable
Protect	PROTECTION BIT =1 FOR Current Write Address
Free	PROTECTION BIT =0 FOR Current Write Address
CallSig	Call Operation
Interrupt	Interrupt Operation
RetSig	RETURN
RTISig	RETURN + SAVED FLAGS
PcSrc	CHOOSE SOURCE FOR PROGRAM COUNTER
SpSig	Indicates Stack Operation

Design Schematic

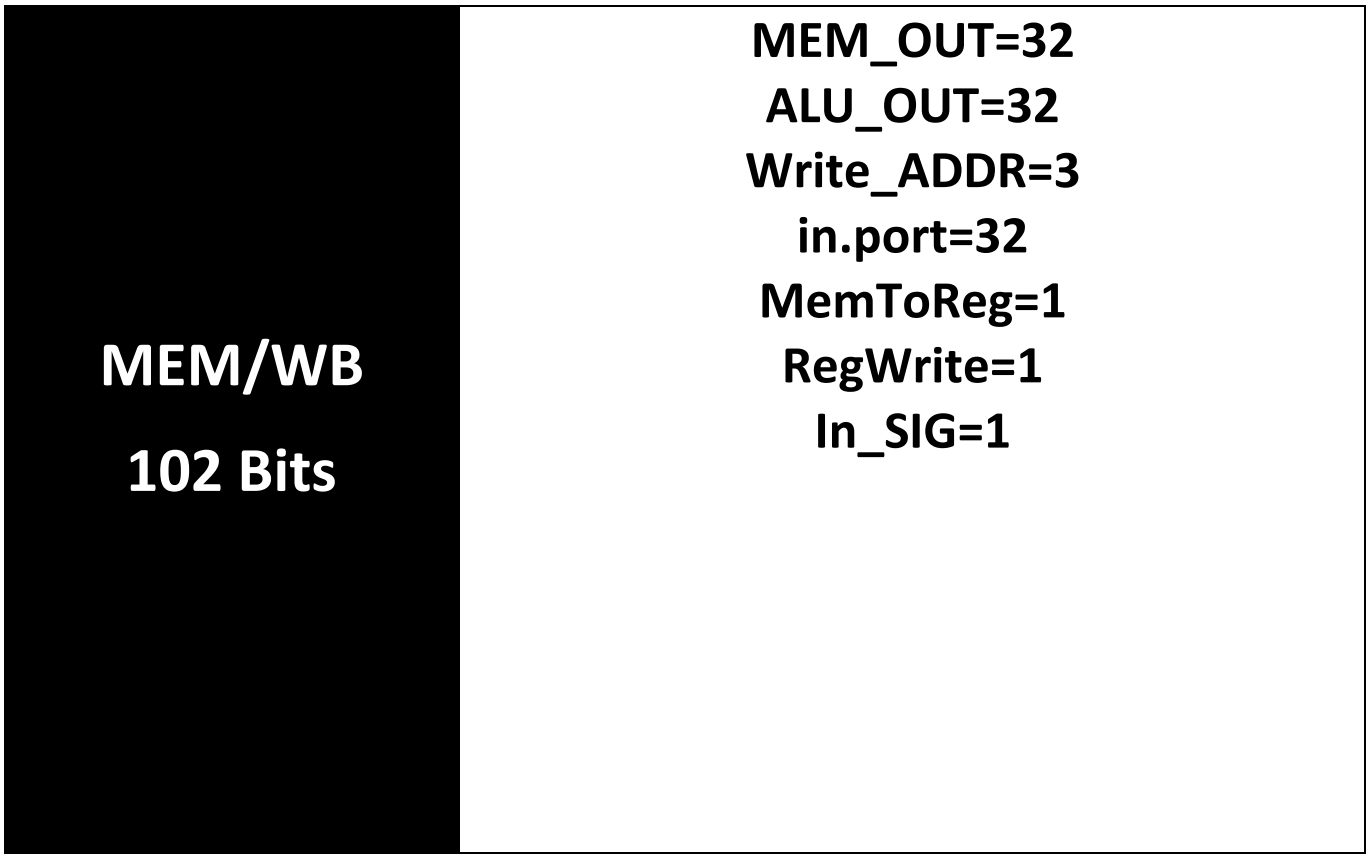


High Quality Image in ZIP FILE

PIPELINE BUFFERS

Buffer	Buffer Details
F/D 81 bits	PREV_STALL=1 PC=32 INSTRUCTION=16 INport=32
D/EX 174 bits	PC=32 Read Data=32 Read Data2=32 Write Addr=3 IN.PORT=32 IMM Value=32 MemToReg=1 AluSrc=1 RegWrite=1 MemWrite=1 Branch_Sig=1 Branch_Z_Sig=1 PUSH=1 POP=1 In_SIG=1 Protect,Free=2

EXEC/MEM 145 Bits	PC=32 ALU_OUTP=32 FLAGS=4 PUSH_VAL=32 Write_ADDR=3 in.port=32 MemToReg=1 RegWrite=1 MemWrite=1 Branch_Sig=1 Branch_Z= 1 PUSH=1 POP =1 In_SIG=1 Protect=1 Free=1



Pipeline Hazards

1) **Structural Hazards: Instructions using same hardware**
   Solution: By pipelining control signals and Write address and by using Stall Signal

2) **Data Hazards**
   Solution: Forwarding unit that has Full forwarding by forwarding either alu result or memory result to next in pipeline if source = destination

3) **Control Hazards: deals with branching**
   Solution: Using 1 bit branch prediction unit that stores previous branch history and uses it to predict and as a selector for pc source