Lab 2
Question Bank

1. **What software is used for programmable logic design in Lab 2?**
    - A) MATLAB
    - B) Simulink
    - C) Quartus
    - D) AutoCAD
    - **Correct Answer: C**
2. **Which languages does Quartus support for hardware description?**
    - A) Python and Java
    - B) VHDL and Verilog
    - C) C++ and Python
    - D) Assembly and C#
    - **Correct Answer: B**
3. **What is the first step in creating a symbol for a Verilog design in Quartus?**
    - A) Compile the design
    - B) Open the Verilog file and set it as the top-level entity
    - C) Test the functionality with a waveform
    - D) Create a new block diagram
    - **Correct Answer: B**
4. **In structured design, a 4-bit carry ripple adder is built using how many instances of a 1-bit full adder?**
    - A) Two
    - B) Three
    - C) Four
    - D) Five
    - **Correct Answer: C**
5. **What is the main characteristic of structured design circuits?**
    - A) Use of a single module
    - B) No need for modules
    - C) Breaking down into blocks and gathering at a top level
    - D) Sequential processing only

- **Correct Answer: C**

6. **What must be done after creating a symbol file for a Verilog design in Quartus?**
    - A) Save the file in PNG format
    - B) Set the file as a top-level entity for compilation
    - C) Email the file to the instructor
    - D) Print the design
    - **Correct Answer: B**
7. **Which of the following is a feature of Quartus software?**
    - A) Text editing only
    - B) Web browsing
    - C) Vector waveform simulation
    - D) Spreadsheet calculations
    - **Correct Answer: C**
8. **What is the output of a 1-bit full adder?**
    - A) One output representing sum only
    - B) Two outputs, sum and carry-out
    - C) Three outputs including carry-in
    - D) Four outputs for each input bit
    - **Correct Answer: B**
9. **For a 2x4 decoder designed in Verilog, what must be tested using a waveform?**
    - A) The functionality of the code
    - B) The color depth of the output
    - C) The speed of the processing
    - D) The size of the file
    - **Correct Answer: A**
10. **Which file must be set as the top-level entity in Quartus before compiling?**
    - A) The block diagram/schematic file
    - B) The main project file
    - C) Any file that is not a Verilog file
    - D) The file to be compiled
    - **Correct Answer: D**

11. **What is the role of a carry-in in a full adder circuit?**
    - A) It is ignored
    - B) It acts as an output only
    - C) It is an input that affects the sum and carry-out
    - D) It is used to program the circuit
    - **Correct Answer: C**
12. **How is a 4-bits full adder created in structured design?**
    - A) By initiating 4 full adders and connecting them with wires
    - B) By using a single full adder and replicating it digitally
    - C) Through external hardware only
    - D) By software simulation without any hardware
    - **Correct Answer: A**
13. **What must be done to the symbol file after it is created in Quartus?**
    - A) It must be deleted
    - B) It must be added to a block diagram
    - C) It must be converted to a waveform
    - D) It must be emailed for verification
    - **Correct Answer: B**
14. **What does the module symbol block in Quartus represent?**
    - A) A hardware component
    - B) An error in the code
    - C) A software plugin
    - D) A logical design element
    - **Correct Answer: D**
15. **In the context of Quartus, what is meant by 'compiling' a design?**
    - A) Printing the design on paper
    - B) Converting the design into machine-readable format
    - C) Uploading the design to the internet
    - D) Drawing the design manually
    - **Correct Answer: B**
16. **Which of the following is a correct representation of a structured design approach?**

- A) Only top-down
- B) Only bottom-up
- C) Either top-down or bottom-up
- D) Neither top-down nor bottom-up
- **Correct Answer: C**

17. **What is required before inserting a module symbol in a Quartus block diagram?**
    - A) Approval from Intel
    - B) Creating a symbol file
    - C) Printing the schematic
    - D) Saving the project as a PDF
    - **Correct Answer: B**
18. **What does the carry-out from one full adder connect to in a carry ripple adder?**
    - A) The carry-in of the next full adder
    - B) The output of the circuit
    - C) The input of the same adder
    - D) It is not connected to anything
    - **Correct Answer: A**
19. **In a Quartus project, what is the purpose of a waveform?**
    - A) To design the physical layout of a circuit
    - B) To test the functionality of the code or design
    - C) To display the project file size
    - D) To compile the design
    - **Correct Answer: B**
20. **What indicates that a Verilog file is set as the top-level entity in Quartus?**
    - A) The file is open in the editor
    - B) The file has a special icon
    - C) The file is selected for compilation
    - D) The file cannot be edited
    - **Correct Answer: C**

Question Bank for Lab 3: Instruction Memory Design

1. **What is the purpose of the instruction memory (IM) in a processor?**
    - A) To store data
    - B) To store and supply instructions
    - C) To execute instructions
    - D) To handle input/output operations
    - **Correct Answer: B**
2. **How is the instruction memory accessed during the instruction fetch stage?**
    - A) Randomly
    - B) Sequentially
    - C) Using an address provided by the program counter
    - D) All at once
    - **Correct Answer: C**
3. **What type of memory is used in the instruction memory design described in Lab 3?**
    - A) Dynamic RAM
    - B) Static RAM
    - C) Hard drive storage
    - D) Byte-addressable memory
    - **Correct Answer: D**
4. **How many locations does each instruction occupy in the instruction memory as described?**
    - A) One
    - B) Two
    - C) Four
    - D) Eight
    - **Correct Answer: C**
5. **In the MIPS architecture, how many bits is each instruction?**
    - A) 8 bits
    - B) 16 bits
    - C) 32 bits
    - D) 64 bits

- **Correct Answer: C**

6. **How are instructions fetched from the instruction memory?**
    - A) By reading a single location
    - B) By concatenating four consecutive bytes
    - C) By decoding the instruction first
    - D) By executing a subroutine
    - **Correct Answer: B**
7. **What is the Verilog data type used to define the memory locations in the instruction memory module?**
    - A) int
    - B) byte
    - C) bit
    - D) reg
    - **Correct Answer: D**
8. **What does the Verilog initial block do in the instruction memory module?**
    - A) Initializes variables
    - B) Defines module inputs and outputs
    - C) Stores instructions in the memory
    - D) Compiles the module
    - **Correct Answer: C**
9. **Which of the following is true about the instruction memory in the provided Verilog module?**
    - A) It is writable
    - B) It is only readable
    - C) It supports both read and write operations
    - D) None of the above
    - **Correct Answer: B**
10. **How is the 'add' instruction encoded in the instruction memory?**
    - A) **00000000 00100000 00010000 00100000**
    - B) **00000000 01100100 00101000 00100010**
    - C) **00000000 11100110 01000000 00100101**
    - D) **10001100 00100000 00000000 00001010**

- **Correct Answer: A**

11. **What MIPS instruction is represented by the code 00000000 01100100 00101000 00100010?**
    - A) Add
    - B) Subtract
    - C) OR
    - D) Load word
    - **Correct Answer: B**
12. **For the MIPS 32-bit processor, how is the lw instruction encoded?**
    - A) **00000000 00100000 00010000 00100000**
    - B) **00000000 01100100 00101000 00100010**
    - C) **00000000 11100110 01000000 00100101**
    - D) **10001100 00100000 00000000 00001010**
    - **Correct Answer: D**
13. **Which component provides the address to the instruction memory?**
    - A) Instruction register
    - B) Data memory
    - C) Program counter
    - D) Arithmetic logic unit
    - **Correct Answer: C**
14. **What is the result of concatenating four bytes from addresses 8 to 11 in the instruction memory?**
    - A) Represents an **add** instruction
    - B) Represents a **subtract** instruction
    - C) Represents an **OR** instruction
    - D) Represents a **load word** instruction
    - **Correct Answer: C**
15. **What does the instruction 10001100 00100000 00000000 00001010 perform in MIPS?**
    - A) Adds two registers
    - B) Subtracts two registers
    - C) Performs bitwise OR on two registers
    - D) Loads a word from memory into a register

- **Correct Answer: D**

16. **In a Verilog module, what does the output keyword define?**
    - A) A variable that the module modifies
    - B) A variable that the module can read and write
    - C) A variable that stores the module's result
    - D) A variable that the module sends out
    - **Correct Answer: D**
17. **What is required for a Verilog file to simulate a module effectively?**
    - A) High computational power
    - B) A detailed truth table
    - C) A waveform file to observe behavior
    - D) An external hardware setup
    - **Correct Answer: C**
18. **In Lab 3, what is the purpose of connecting the instruction memory module to the PC unit in the block diagram?**
    - A) To receive the current instruction address
    - B) To send data to the PC
    - C) To initialize the instruction memory
    - D) To configure the block diagram settings
    - **Correct Answer: A**
19. **Which stage of the MIPS pipeline is directly associated with the instruction memory?**
    - A) Instruction fetch stage
    - B) Instruction decode stage
    - C) Execution stage
    - D) Memory access stage
    - **Correct Answer: A**
20. **What is a key feature of the instruction memory in terms of its operation?**
    - A) It operates as combinational logic
    - B) It has internal state that changes over time
    - C) It requires a clock signal
    - D) It requires frequent resetting

- **Correct Answer: A**

21. **What assembly instruction corresponds to the machine code 00000000 11100110 01000000 00100101?**
    - A) Add
    - B) Subtract
    - C) OR
    - D) Load word
    - **Correct Answer: C**
22. **In Verilog, what does the reg keyword signify in the instruction memory design?**
    - A) A variable used for computation
    - B) A register that holds a temporary value
    - C) A storage element that retains its value between operations
    - D) A constant value that cannot be changed
    - **Correct Answer: C**
23. **How does the instruction memory handle the address input for fetching instructions?**
    - A) It adds an offset to the address
    - B) It multiplies the address by four
    - C) It uses the address to access four consecutive memory locations
    - D) It divides the address by four
    - **Correct Answer: C**
24. **Which of the following correctly describes the fetch operation for the sub instruction?**
    - A) Concatenates bytes from addresses 0 to 3
    - B) Concatenates bytes from addresses 4 to 7
    - C) Concatenates bytes from addresses 8 to 11
    - D) Concatenates bytes from addresses 12 to 15
    - **Correct Answer: B**
25. **What does the assign statement do in the instruction memory Verilog module?**
    - A) It assigns a permanent value to a variable
    - B) It dynamically assigns a value based on conditions
    - C) It assigns a concatenated value to the output

- D) It assigns an initial value during module instantiation
- **Correct Answer: C**

26. **Why is the instruction memory considered as part of the instruction fetch stage?**
    - A) Because it performs data storage
    - B) Because it decodes the fetched instruction
    - C) Because it supplies the instruction to the processor based on the address
    - D) Because it executes the fetched instruction
    - **Correct Answer: C**
27. **What is meant by 'byte-addressable memory' in the context of the instruction memory?**
    - A) Each address identifies a single bit
    - B) Each address identifies a single byte
    - C) Each address identifies multiple bytes
    - D) The memory does not use addresses
    - **Correct Answer: B**
28. **What is a characteristic of the memory used in the instruction memory module?**
    - A) It is volatile
    - B) It is non-volatile
    - C) It is magnetic
    - D) It is optical
    - **Correct Answer: A**
29. **In the given Verilog code, what is the significance of the square brackets [31:0] next to address_in and instruction?**
    - A) They indicate that these are arrays
    - B) They indicate the size of the data types
    - C) They indicate the number of operations performed
    - D) They indicate memory alignment requirements
    - **Correct Answer: B**
30. **Which instruction has the machine code 10001100 00100000 00000000 00001010 in the instruction memory?**
    - A) Add
    - B) Subtract

- C) OR
- D) Load word
- **Correct Answer: D**

31. **What does the MIPS assembly instruction or r8,r7,r6 perform?**
    - A) It adds r7 and r6, storing the result in r8
    - B) It subtracts r6 from r7, storing the result in r8
    - C) It performs a bitwise OR between r7 and r6, storing the result in r8
    - D) It loads a word from memory into r8 based on the address in r7 plus offset r6
    - **Correct Answer: C**
32. **How is the instruction sub r5,r4,r3 encoded in the instruction memory?**
    - A) **00000000 00100000 00010000 00100000**
    - B) **00000000 01100100 00101000 00100010**
    - C) **00000000 11100110 01000000 00100101**
    - D) **10001100 00100000 00000000 00001010**
    - **Correct Answer: B**
33. **What method is used to fetch a 32-bit instruction from the instruction memory?**
    - A) Reading one byte at a time
    - B) Reading all bytes at once
    - C) Concatenating four consecutive bytes
    - D) Fetching randomly from the memory
    - **Correct Answer: C**
34. **Why does the instruction memory not require a read control signal?**
    - A) Because it uses dynamic allocation
    - B) Because it automatically reads without input
    - C) Because it is treated as combinational logic
    - D) Because it uses a special type of memory
    - **Correct Answer: C**
35. **What is the typical use of the reg data type in the Verilog module for the instruction memory?**
    - A) To store the incoming data
    - B) To store the memory contents

- C) To generate output signals
- D) To control the module operations
- **Correct Answer: B**

36. **What happens when the instruction memory receives an address from the PC?**
    - A) It clears its memory
    - B) It updates the address
    - C) It fetches the corresponding instruction
    - D) It sends a signal to the PC
    - **Correct Answer: C**
37. **Which Verilog construct is used to create a symbol file for the instruction memory module?**
    - A) **initial** block
    - B) **module** statement
    - C) **assign** statement
    - D) **Create /Update** menu option
    - **Correct Answer: D**
38. **What is the end result of the concatenation process in the instruction memory?**
    - A) A 32-bit instruction
    - B) A 16-bit instruction
    - C) An 8-bit byte
    - D) A 64-bit instruction
    - **Correct Answer: A**
39. **Which tool is used to simulate the instruction memory module after it is designed?**
    - A) A physical test bench
    - B) A Verilog simulator
    - C) A waveform viewer
    - D) A logic analyzer
    - **Correct Answer: C**
40. **What does the process of 'synthesis' refer to in the context of running Verilog HDL code?**
    - A) Converting the code into machine-readable format
    - B) Merging multiple modules into one

- C) Testing the code for errors
- D) Documenting the code
- **Correct Answer: A**

Question Bank for Lab 4: Program Counter Unit and Related Components

1. **What is the primary function of the Program Counter (PC) in a processor?**
    - A) To store data temporarily
    - B) To execute instructions
    - C) To hold the address of the current instruction
    - D) To control input/output operations
    - **Correct Answer: C**
2. **How much is the program counter incremented to fetch the next instruction in MIPS-32?**
    - A) 2 bytes
    - B) 4 bytes
    - C) 8 bytes
    - D) 16 bytes
    - **Correct Answer: B**
3. **What type of circuitry is used to increment the PC in the described lab setup?**
    - A) Multiplexer
    - B) Adder
    - C) Decoder
    - D) Comparator
    - **Correct Answer: B**
4. **At what phase of the clock does the PC update its value according to the provided Verilog code?**
    - A) Positive edge
    - B) Negative edge
    - C) When the clock signal is high
    - D) When the clock signal is low
    - **Correct Answer: B**
5. **What is the main purpose of the pc32_adder module as described in the Verilog code?**
    - A) To subtract two numbers
    - B) To perform bitwise operations
    - C) To increment the PC by 4

- D) To reset the PC to zero
- **Correct Answer: C**

6. **Which component is responsible for selecting the new PC value in the IF stage?**
   - A) Adder
   - B) Program counter
   - C) Multiplexer
   - D) Instruction memory
   - **Correct Answer: C**
7. **In MIPS-32, why is the PC typically incremented by 4 to get the address of the next instruction?**
   - A) Because each instruction is 4 bytes long
   - B) Because it is more efficient than incrementing by 2
   - C) To skip over data memory
   - D) To align the instruction on a 16-byte boundary
   - **Correct Answer: A**
8. **What does the initial keyword do in the provided PC Verilog module?**
   - A) Defines the initial conditions of loops
   - B) Sets the initial value of **pc_out_bus**
   - C) Compiles the initial block first
   - D) Initializes the clock signal
   - **Correct Answer: B**
9. **Why is the program counter considered a critical part of the instruction fetch stage?**
   - A) It decodes the fetched instruction
   - B) It provides the address to fetch the next instruction
   - C) It performs arithmetic operations on the instructions
   - D) It stores the final results of computations
   - **Correct Answer: B**
10. **What is the result of adding 32'h00000004 to the adder_in_bus in the pc32_adder module?**
    - A) Resets the adder input
    - B) Decreases the adder input by 4
    - C) Increments the adder input by 4

- D) Multiplies the adder input by 4
- **Correct Answer: C**

11. **How is the PC typically updated in a sequential circuit like the one in Lab 4?**
    - A) Through asynchronous signals
    - B) At the clock's negative edge
    - C) Continuously, independent of the clock
    - D) Only when reset occurs
    - **Correct Answer: B**
12. **What function does a multiplexer perform in the context of selecting the PC's next value?**
    - A) It combines multiple signals into one
    - B) It chooses between several input signals based on a selector signal
    - C) It divides one input signal into multiple output signals
    - D) It amplifies the selected signal
    - **Correct Answer: B**
13. **In the IF stage, what is the purpose of incrementing the PC?**
    - A) To prepare the processor to execute the next instruction
    - B) To reduce the memory used by the program
    - C) To signal the end of program execution
    - D) To decode the current instruction
    - **Correct Answer: A**
14. **What role does the always@(negedge clk) statement play in the pc32 module?**
    - A) It triggers the module to reset
    - B) It causes the module to update at every positive edge of the clock
    - C) It ensures the module updates its output at every negative edge of the clock
    - D) It checks for errors in the clock signal
    - **Correct Answer: C**
15. **Why does the instruction memory only need to provide read access during the IF stage?**
    - A) Because instructions are never written back to the instruction memory
    - B) Because the instruction memory is also used as data memory
    - C) Because write operations are handled by another component

- D) Because the IF stage does not involve data writing
- **Correct Answer: A**

16. **What happens if the PC's next value is incorrectly calculated?**
    - A) The next instruction executes faster
    - B) The processor may fetch the wrong instruction
    - C) The PC resets itself automatically
    - D) The instruction memory is cleared
    - **Correct Answer: B**
17. **How does the design ensure that the instruction execution process is efficient?**
    - A) By incrementing the PC by 8 instead of 4
    - B) By using a complex set of adders and multiplexers
    - C) By minimizing the clock cycles between instructions
    - D) By synchronizing the PC update with the negative edge of the clock
    - **Correct Answer: D**
18. **What is the significance of 32'h00000004 in the pc32_adder module?**
    - A) It represents the reset value of the PC
    - B) It is the value added to the PC to fetch the next instruction
    - C) It is the default address of the instruction memory
    - D) It signifies an error in the PC calculation
    - **Correct Answer: B**
19. **In the MIPS-32 architecture, why is the PC incremented specifically by 4 bytes?**
    - A) Because the architecture is 32-bit, and each instruction is 4 bytes long
    - B) To ensure compatibility with older 16-bit architectures
    - C) To provide a buffer space between instructions
    - D) To align instructions on 8-byte boundaries for performance
    - **Correct Answer: A**
20. **What would be a likely consequence of a malfunction in the PC unit?**
    - A) Increased execution speed of instructions
    - B) Incorrect data being stored in registers
    - C) Disruption in the sequence of fetched instructions
    - D) Overflow of the instruction memory

- **Correct Answer: C**

21. **Which component directly interacts with the PC to fetch the correct instruction from memory?**
    - A) ALU
    - B) Register file
    - C) Adder
    - D) Instruction memory
    - **Correct Answer: D**
22. **What does the reg keyword indicate about pc_out_bus in the pc32 module?**
    - A) It is a temporary storage within the module
    - B) It is used to perform arithmetic operations
    - C) It must be a constant value
    - D) It can be modified asynchronously
    - **Correct Answer: A**
23. **Why is the pc32_adder module crucial for the instruction fetch process?**
    - A) It ensures that the PC holds the correct starting address at power-up
    - B) It modifies the instruction data before execution
    - C) It calculates the address of the next instruction to be fetched
    - D) It controls the overall timing of the processor
    - **Correct Answer: C**
24. **What does the term 'byte-addressable memory' imply in the context of the instruction memory?**
    - A) Each byte of memory can be independently addressed
    - B) Memory addressing skips every other byte
    - C) Each address points to two bytes of memory
    - D) The memory can only store byte-sized instructions
    - **Correct Answer: A**
25. **How is the always block in Verilog used in the context of the PC and adder modules?**
    - A) To initiate variables
    - B) To define conditions under which the module's output can change
    - C) To generate clock signals

- D) To create constants used within the module
- **Correct Answer: B**

26. **In the pc32 module, what role does the initial statement play?**
    - A) It specifies conditions for terminating the simulation
    - B) It sets an initial value for the PC at the start of simulation
    - C) It defines the maximum value the PC can hold
    - D) It configures the module's input parameters
    - **Correct Answer: B**

27. **What is the significance of the PC being a 32-bit register in MIPS-32 architecture?**
    - A) It indicates the processor can handle 32 operations simultaneously
    - B) It matches the 32-bit size of instructions
    - C) It limits the memory address space to 32 bits
    - D) It is used to enhance the clock speed of the processor
    - **Correct Answer: C**

28. **What does the adder module's output represent in the context of the PC unit?**
    - A) The current instruction's address
    - B) The next instruction's address
    - C) The last executed instruction's address
    - D) The address of the instruction to be executed after next
    - **Correct Answer: B**

29. **Which statement about the program counter's functionality is accurate?**
    - A) The PC can only increment in steps of 2 bytes at a time
    - B) The PC is updated based on the positive edge of the clock signal
    - C) The PC updates itself autonomously without needing a clock signal
    - D) The PC is written at the end of every clock cycle
    - **Correct Answer: D**

30. **What is the role of the negative edge-triggered behavior in the pc32 module?**
    - A) It prevents the PC from updating too frequently
    - B) It synchronizes the PC update with the end of instruction execution
    - C) It reduces the power consumption of the module
    - D) It is a required feature for all MIPS processors

- **Correct Answer: B**

31. **Why is there no write control signal required for the program counter?**
    - A) Because the PC is only written at setup
    - B) Because it is written at every clock cycle
    - C) Because the PC cannot be written to
    - D) Because it is not a register but a combinational logic circuit
    - **Correct Answer: B**

32. **How does the design of the PC contribute to the overall performance of the processor?**
    - A) By reducing the number of instructions executed
    - B) By increasing the rate at which instructions are fetched
    - C) By decreasing the clock frequency
    - D) By enlarging the instruction set
    - **Correct Answer: B**

33. **What does the pc32_adder specifically add to adder_in_bus to calculate adder_out_bus?**
    - A) 32'hFFFFFFFC
    - B) 32'h00000002
    - C) 32'h00000004
    - D) 32'h00000008
    - **Correct Answer: C**

34. **In what scenario might the program counter need to select between different potential next addresses?**
    - A) When there are multiple programs running simultaneously
    - B) When an interrupt occurs
    - C) During branch or jump instructions
    - D) Every instruction cycle
    - **Correct Answer: C**

35. **What is one advantage of having a dedicated adder for the PC in the MIPS architecture?**
    - A) It allows for faster data writes to memory
    - B) It enables quicker arithmetic calculations for all operations

- C) It ensures the next instruction address is ready promptly
- D) It simplifies the design of the ALU
- **Correct Answer: C**

36. **What does the constant 32'h00000004 represent in the context of MIPS instruction execution?**
    - A) The standard decrement value for stack operations
    - B) The offset for branch instructions
    - C) The increment value to fetch the next sequential instruction
    - D) The alignment requirement for memory operations
    - **Correct Answer: C**
37. **How does the system handle the program counter during branch instructions differently than during sequential execution?**
    - A) It uses a decrementer instead of an adder
    - B) It does not update the PC
    - C) It may use a different value calculated based on the branch condition
    - D) It pauses updating until the branch decision is confirmed
    - **Correct Answer: C**
38. **What aspect of the pc32 module ensures that the PC is updated correctly following the completion of an instruction's execution?**
    - A) The positive edge-triggered behavior
    - B) The use of a static value for all updates
    - C) The negative edge-triggered update mechanism
    - D) The use of a high-frequency clock
    - **Correct Answer: C**
39. **In the described setup, what ensures that the fetched instruction address is accurate?**
    - A) The unconditional use of the adder's output as the next PC value
    - B) The verification of each address by the instruction memory
    - C) The precise timing of the clock signal used for updating the PC
    - D) The feedback loop from the instruction decode stage
    - **Correct Answer: C**
40. **Why is the increment of the PC by 4 critical in achieving efficient instruction pipeline flow in MIPS?**

- A) It matches the instruction length, ensuring smooth and continuous flow
- B) It ensures that instructions are executed in the order they are fetched
- C) It prevents the execution of duplicate instructions
- D) It allows time for the instruction decode stage to complete
- **Correct Answer: A**

Question Bank for Lab 5: Instruction Decode and Register File Read

1. **What is the primary function of the Instruction Register (IR) in the ID stage?**
    - A) To execute the fetched instruction
    - B) To store and decode the fetched instruction
    - C) To transfer instructions to data memory
    - D) To send instructions directly to the output device
    - **Correct Answer: B**
2. **What does the Register file in MIPS-32 primarily contain?**
    - A) Instruction opcodes
    - B) Data for processing
    - C) All the 32 registers used by the processor
    - D) The program counter and instruction register
    - **Correct Answer: C**
3. **In MIPS-32, what is the bit width of each register within the Register file?**
    - A) 8 bits
    - B) 16 bits
    - C) 32 bits
    - D) 64 bits
    - **Correct Answer: C**
4. **What is the purpose of the shamt field in R-type MIPS instructions?**
    - A) It specifies the operation code
    - B) It indicates the register destination
    - C) It determines the number of bits to shift
    - D) It contains the immediate value for calculations
    - **Correct Answer: C**
5. **Which component of MIPS instruction is called the opcode?**
    - A) Op
    - B) Funct
    - C) Shamt
    - D) Rd
    - **Correct Answer: A**

6. **What is the typical use of the Rs field in MIPS instructions?**
    - A) Specifies the first register source operand
    - B) Holds the immediate value
    - C) Determines the shift amount
    - D) Indicates the jump address
    - **Correct Answer: A**
7. **In MIPS instruction formats, which field specifies the second register source operand?**
    - A) Rs
    - B) Rt
    - C) Rd
    - D) Shamt
    - **Correct Answer: B**
8. **Which of the following best describes I-type instructions?**
    - A) Used for arithmetic operations with three register operands
    - B) Used for immediate and data transfer instructions
    - C) Used exclusively for jump instructions
    - D) Does not involve registers
    - **Correct Answer: B**
9. **What role does the Funct field play in R-type instructions?**
    - A) Specifies the operation to be performed
    - B) Holds the immediate value
    - C) Determines the number of bits to shift
    - D) Indicates the jump target
    - **Correct Answer: A**
10. **What is the function of the sign extender in MIPS-32 ID stage?**
    - A) To reduce the size of the immediate value
    - B) To extend a 16-bit immediate value to 32 bits
    - C) To increment the program counter
    - D) To shift data within the registers
    - **Correct Answer: B**

11. **What does the immediate field in I-type instructions typically contain?**
    - A) The data to be processed
    - B) A data constant or an address offset
    - C) The destination register
    - D) The opcode for the instruction
    - **Correct Answer: B**
12. **For the instruction lw $s1, 100($s2), what does 100($s2) represent?**
    - A) A direct address in the memory
    - B) A label in the program
    - C) An offset of 100 from the address contained in $s2
    - D) The memory address contained in register $s1
    - **Correct Answer: C**
13. **Which field in the MIPS instruction format is used to specify the destination register for R-type instructions?**
    - A) Rs
    - B) Rt
    - C) Rd
    - D) Funct
    - **Correct Answer: C**
14. **In the instruction add $1, $2, $3, which register is used as the destination?**
    - A) $1
    - B) $2
    - C) $3
    - D) None of the above
    - **Correct Answer: A**
15. **What does the instruction beq $s1, $s2, label perform in MIPS architecture?**
    - A) It adds $s1 and $s2 and stores the result in **label**
    - B) It branches to **label** if $s1 equals $s2
    - C) It loads the word at the address **label** into $s1
    - D) It saves the contents of $s2 at the memory address **label**
    - **Correct Answer: B**

16. **Which type of MIPS instruction is used to perform jumps to specific addresses?**
    - A) R-type
    - B) I-type
    - C) J-type
    - D) S-type
    - **Correct Answer: C**
17. **In MIPS-32, how is the j target instruction encoded?**
    - A) With an opcode and a target address
    - B) With source and destination registers
    - C) With an immediate value and a shift amount
    - D) With function codes and register addresses
    - **Correct Answer: A**
18. **What happens in the MIPS pipeline during the ID stage?**
    - A) The instruction is fetched from memory
    - B) The instruction is executed
    - C) The results are written back to the register file
    - D) The instruction is decoded and the necessary registers are read
    - **Correct Answer: D**
19. **How does the instruction register (IR) assist in the instruction decode process?**
    - A) It temporarily stores the instruction while it is being decoded
    - B) It executes the instruction directly
    - C) It sends the instruction back to memory
    - D) It bypasses the decoding process
    - **Correct Answer: A**
20. **Which MIPS instruction format would be used for the command sub $1, $2, $3?**
    - A) I-type
    - B) R-type
    - C) J-type
    - D) S-type
    - **Correct Answer: B**
21. **What is encoded by the op field in an R-type instruction?**

- A) The specific operation to be performed
- B) Always set to zero for R-type instructions
- C) The register destination address
- D) The shift amount
- **Correct Answer: B**

22. **Which registers does the MIPS instruction add $1, $2, $3 use as operands?**
    - A) $1 and $2
    - B) $1 and $3
    - C) $2 and $3
    - D) $2, $3, and $1
    - **Correct Answer: C**
23. **How does the ID stage relate to the rest of the MIPS pipeline stages?**
    - A) It operates independently of the other stages
    - B) It is the first stage and initiates all other stages
    - C) It decodes instructions that are fetched in the IF stage
    - D) It directly interacts with the memory to fetch data
    - **Correct Answer: C**
24. **What is the role of the Rt field in an I-type MIPS instruction?**
    - A) Specifies the target register for the operation
    - B) Holds the value to be used as an immediate operand
    - C) Designates the register from which data will be loaded
    - D) Identifies the source register
    - **Correct Answer: D**
25. **Which field of an R-type instruction specifies the function or operation to be performed?**
    - A) Op
    - B) Shamt
    - C) Funct
    - D) Rd
    - **Correct Answer: C**
26. **In a typical MIPS execution, what happens after the ID stage if the instruction is a branch and the condition is true?**

- A) The program counter is incremented
- B) The program counter jumps to the target address
- C) The instruction is executed immediately
- D) The instruction is stored back into instruction memory
- **Correct Answer: B**

27. **What is the role of the shamt field in the instruction sll $1, $2, 10?**
    - A) It indicates the shift amount by 10 places
    - B) It specifies the function code
    - C) It designates the opcode for the instruction
    - D) It identifies the source register
    - **Correct Answer: A**
28. **What does the instruction ori $t1, $t2, 10 do in MIPS?**
    - A) Performs an OR operation on $t1 and $t2 with an immediate value of 10
    - B) Adds $t1 and $t2, storing the result in a location offset by 10
    - C) Loads the value from the memory address obtained by adding 10 to $t2 into $t1
    - D) Branches to the instruction 10 places ahead if $t1 equals $t2
    - **Correct Answer: A**
29. **Which part of the MIPS instruction format is used to extend the immediate value to 32 bits in I-type instructions?**
    - A) Op field
    - B) Funct field
    - C) Shamt field
    - D) None, it uses a separate sign extender unit
    - **Correct Answer: D**
30. **For the command beq $t1, $t2, end, what does end represent?**
    - A) A register containing the end address of the program
    - B) An immediate value added to the PC if the branch condition is true
    - C) A label that represents an address to branch to if $t1 equals $t2
    - D) A special register used to terminate the program
    - **Correct Answer: C**
31. **How does the ID stage interact with the register file in a MIPS processor?**

- A) It writes the results of computations back to the register file
- B) It reads the necessary registers to decode the instruction
- C) It bypasses the register file entirely for faster execution
- D) It clears the register file for the next set of instructions
- **Correct Answer: B**

32. **What is typically stored in the IR after an instruction is fetched?**
    - A) The next set of instructions to be executed
    - B) The binary code of the fetched instruction
    - C) The results of the previously executed instruction
    - D) Data fetched from the data memory
    - **Correct Answer: B**
33. **In the MIPS architecture, what happens during the decode phase of the instruction lw $t0, 8($t1)?**
    - A) The value at the memory address $t1 + 8 is computed
    - B) The instruction is executed and the data is loaded into $t0
    - C) The opcode is identified and the registers $t0 and $t1 are read
    - D) The program counter is updated to the address 8 bytes ahead
    - **Correct Answer: C**
34. **What does the MIPS assembly instruction addi $t0, $t0, 4 specifically instruct the processor to do?**
    - A) Add 4 to the value in register $t0 and store the result back in $t0
    - B) Load the value from the memory address $t0 + 4 into $t0
    - C) Store the value of $t0 into the memory location that is 4 units away
    - D) Jump four places forward in the instruction sequence
    - **Correct Answer: A**
35. **Which type of instruction uses both the rs and rt fields as source registers and rd as the destination register?**
    - A) I-type
    - B) R-type
    - C) J-type
    - D) S-type
    - **Correct Answer: B**

36. **What is the primary purpose of the sign extender in the ID stage of MIPS?**
    - A) To convert 32-bit instructions into 64-bit formats
    - B) To prepare 32-bit addresses for branch instructions
    - C) To extend the immediate field of I-type instructions to 32 bits
    - D) To compress the opcode fields for storage efficiency
    - **Correct Answer: C**
37. **In which MIPS instruction format is the shamt field irrelevant and typically set to zero?**
    - A) R-type
    - B) I-type
    - C) J-type
    - D) All types
    - **Correct Answer: B**
38. **Which MIPS field is crucial for determining the operation in I-type instructions like addi or ori?**
    - A) **rd**
    - B) **rt**
    - C) **rs**
    - D) **op**
    - **Correct Answer: D**
39. **What does the MIPS instruction j address do?**
    - A) Jumps to execute the instruction at the specified address
    - B) Adds the **address** to the current PC value
    - C) Stores the **address** into the jump register
    - D) Compares the **address** with the PC to decide the next instruction
    - **Correct Answer: A**
40. **How does the ID stage handle the decoding of jump (J-type) instructions?**
    - A) It uses the **shamt** and **funct** fields to determine the jump target
    - B) It directly utilizes the 26-bit address encoded in the instruction
    - C) It retrieves the jump address from the register file
    - D) It calculates the jump destination using the ALU
    - **Correct Answer: B**

Question Bank for Lab 6: Register File

1. **What is the primary role of the Register File in the MIPS architecture?**
    - A) To store intermediate computation results
    - B) To execute load and store instructions
    - C) To control data flow to and from the ALU
    - D) To manage the program counter
    - **Correct Answer: A**
2. **How many registers does the MIPS standard register file contain?**
    - A) 16
    - B) 24
    - C) 32
    - D) 64
    - **Correct Answer: C**
3. **What is the bit width of each register in the MIPS register file?**
    - A) 8 bits
    - B) 16 bits
    - C) 32 bits
    - D) 64 bits
    - **Correct Answer: C**
4. **In the Register File, what does the Write Enable signal control?**
    - A) The ability to read from registers
    - B) The ability to write to registers
    - C) The clock speed of register access
    - D) The selection of register for the operation
    - **Correct Answer: B**
5. **During which part of the clock cycle does the register file write occur in the MIPS architecture?**
    - A) At the positive edge of the clock
    - B) At the negative edge of the clock
    - C) During the high state of the clock
    - D) When the clock is low

- **Correct Answer: A**

6. **How many read ports does the MIPS register file have?**
   - A) One
   - B) Two
   - C) Three
   - D) Four
   - **Correct Answer: B**
7. **What is the purpose of the Register File's read ports?**
   - A) To input data into the registers
   - B) To output the contents of specified registers
   - C) To control which registers are written to
   - D) To supply power to the registers
   - **Correct Answer: B**
8. **Which of the following best describes the function of RS and RT in the Register File?**
   - A) They specify which registers to write data into
   - B) They are used to determine the clock frequency
   - C) They indicate which registers to read data from
   - D) They control the Write Enable signal
   - **Correct Answer: C**
9. **What happens if the Write Enable signal is not active when the clock edge occurs?**
   - A) Data is written to all registers
   - B) Data is read from the specified registers
   - C) No data is written to the register
   - D) The register file resets all values
   - **Correct Answer: C**
10. **In the Verilog code for the Register File, what initial value is assigned to register 1?**
    - A) 0
    - B) 1
    - C) 15
    - D) 100
    - **Correct Answer: B**

11. **Which register typically contains a fixed value of zero in MIPS-32?**
    - A) $0
    - B) $31
    - C) $16
    - D) $1
    - **Correct Answer: A**
12. **How are the outputs OutA and OutB in the Register File determined?**
    - A) Based on the values of **RS** and **RT**
    - B) Based on the value of **RD**
    - C) Randomly at each clock cycle
    - D) By the last write operation
    - **Correct Answer: A**
13. **Which statement about the register number inputs to the Register File is true?**
    - A) They are all 32 bits wide
    - B) They are all 5 bits wide
    - C) They are not necessary for operations
    - D) They are dynamically assigned by the CPU
    - **Correct Answer: B**
14. **What is the typical size of data lines carrying values to and from the Register File in MIPS?**
    - A) 8 bits
    - B) 16 bits
    - C) 32 bits
    - D) 64 bits
    - **Correct Answer: C**
15. **Which register is used to store the result of sum = x + y in the provided MIPS code example?**
    - A) $t0
    - B) $t1
    - C) $t2
    - D) $0
    - **Correct Answer: A**

16. **What function does the RD input serve in the Register File module?**
    - A) It specifies the register to be read
    - B) It specifies the register to be written
    - C) It controls the Write Enable signal
    - D) It dictates the operation to be performed
    - **Correct Answer: B**
17. **Which operation in the Register File is likely to occur at the positive edge of the clock if Write Enable is active?**
    - A) Data is read from the register specified by **RS**
    - B) Data is written into the register specified by **RD**
    - C) All registers are reset to zero
    - D) The contents of all registers are output simultaneously
    - **Correct Answer: B**
18. **What is the role of DataIn in the Register File?**
    - A) It specifies which register to read
    - B) It is the data to be written to the register specified by **RD**
    - C) It is the data output from the register file
    - D) It controls which registers are to be accessed
    - **Correct Answer: B**
19. **How is data integrity maintained during a write operation in the Register File?**
    - A) By using a high clock frequency
    - B) Through the use of multiple write ports
    - C) By writing only at the positive clock edge
    - D) By disabling reads during writes
    - **Correct Answer: C**
20. **What is the initial value of register 31 in the provided Register File setup?**
    - A) 0
    - B) 1
    - C) 100
    - D) 32
    - **Correct Answer: C**

21. **What must be true for a write operation to occur in the Register File?**
    - A) **WriteEnb** must be active and the clock must be at the positive edge
    - B) **RS** and **RT** must be specified
    - C) **OutA** and **OutB** must be equal
    - D) All registers must be empty
    - **Correct Answer: A**
22. **In a MIPS system, why is the register file crucial for arithmetic operations like addition?**
    - A) It provides storage for the program counter
    - B) It facilitates communication between the CPU and main memory
    - C) It stores operands and results of arithmetic operations
    - D) It decodes the instructions before execution
    - **Correct Answer: C**
23. **What happens to the register specified by RD when WriteEnb is deactivated?**
    - A) It is cleared to zero
    - B) It retains its previous value
    - C) It is incremented by one
    - D) It is set to the value of **DataIn**
    - **Correct Answer: B**
24. **Which type of MIPS instructions primarily interacts with the Register File for loading values?**
    - A) Logic instructions
    - B) Arithmetic instructions
    - C) Control flow instructions
    - D) Load/store instructions
    - **Correct Answer: D**
25. **In the Verilog code for the Register File, what happens when WriteEnb is set to 1 and the clock transitions from low to high?**
    - A) The register specified by **RS** is read
    - B) The register specified by **RD** is written with **DataIn**
    - C) The outputs **OutA** and **OutB** are updated
    - D) All registers are reset to their initial values

- **Correct Answer: B**

26. **What is the purpose of the OutA and OutB outputs in the Register File?**
    - A) They provide data for arithmetic operations
    - B) They determine which registers are to be written next
    - C) They send the clock signal to other components
    - D) They activate the Write Enable signal
    - **Correct Answer: A**
27. **Which scenario best utilizes the dual read ports of the Register File?**
    - A) Writing data to a single register
    - B) Reading from two registers simultaneously to perform an ALU operation
    - C) Resetting all registers to initial values
    - D) Outputting the contents of the Register File to external devices
    - **Correct Answer: B**
28. **How does the Register File ensure fast access to operands for the ALU?**
    - A) By allowing simultaneous read operations from two registers
    - B) By performing parallel write operations to all registers
    - C) By incrementing the program counter
    - D) By storing the results of ALU operations
    - **Correct Answer: A**
29. **What condition must be met for the Register File to execute a write operation on the specified RD register?**
    - A) The **RS** register must be empty
    - B) The **WriteEnb** signal must be low
    - C) There must be a matching data in **OutA** and **OutB**
    - D) The **WriteEnb** signal must be high and the clock edge must be positive
    - **Correct Answer: D**
30. **Why are initial values pre-loaded into some registers in the Register File as shown in the Verilog code?**
    - A) To provide default data for testing
    - B) To speed up the processing by pre-loading frequent values
    - C) To prevent errors during the first read operations
    - D) All MIPS Register Files require initial values

- **Correct Answer: A**

31. **How is the value of a specific register accessed during a MIPS instruction execution?**
    - A) By specifying the register number in **RD**
    - B) By using the **RS** or **RT** input to specify the register
    - C) By toggling the **WriteEnb** signal
    - D) By performing a reset on the Register File
    - **Correct Answer: B**
32. **What ensures that data is not inadvertently written to the Register File?**
    - A) The fixed size of the **DataIn** line
    - B) The use of the **WriteEnb** control signal
    - C) Automatic clearing of the **DataIn** after each operation
    - D) Lock mechanisms within each register
    - **Correct Answer: B**
33. **In what way does the Register File interact with the ALU in a MIPS system?**
    - A) It supplies operands for the ALU operations
    - B) It directs the ALU to perform specific operations
    - C) It stores the results of ALU operations
    - D) It controls the ALU clock signal
    - **Correct Answer: A**
34. **Why might a MIPS processor stall during an operation involving the Register File?**
    - A) If there is a mismatch between the **RS** and **RT** values
    - B) If the Register File is full and cannot accept new data
    - C) If the required registers are not available immediately
    - D) If the Write Enable signal is inactive when needed
    - **Correct Answer: C**
35. **What would be a typical sequence for using the Register File in a MIPS assembly operation like add $t0, $t1, $t2?**
    - A) Read $t1 and $t2, perform addition, write result to $t0
    - B) Write inputs to $t1 and $t2, read from $t0
    - C) Reset all registers, perform addition, store result externally
    - D) Check all registers for availability, perform addition in ALU

- **Correct Answer: A**

36. **What determines the specific registers from which data is read in the Register File?**
    - A) The values of **OutA** and **OutB**
    - B) The control signals from the ALU
    - C) The input values at **RS** and **RT**
    - D) The Write Enable signal status
    - **Correct Answer: C**
37. **Which registers would typically be used to store the operands in a MIPS instruction like sub $t0, $t1, $t2?**
    - A) $t0 for both operands and result
    - B) $t1 and $t2 as operands, $t0 as the result
    - C) All operations use $0 as the operand
    - D) $t1 as the operand, $t0 and $t2 as results
    - **Correct Answer: B**
38. **What happens to the Register File during a context switch in a MIPS processor?**
    - A) It is cleared to prevent data leakage
    - B) It retains its data unless explicitly cleared
    - C) All registers are set to their initial values
    - D) It is disabled until the context switch completes
    - **Correct Answer: B**
39. **Which MIPS instruction directly tests the functionality of the Register File's write capability?**
    - A) **lw $t0, 4($t1)** - Load word into $t0
    - B) **sw $t0, 12($t1)** - Store word from $t0
    - C) **addi $t0, $t0, 4** - Add immediate to $t0
    - D) **andi $t0, $t1, 10** - AND immediate with $t0
    - **Correct Answer: B**
40. **In the Register File, what ensures data is available immediately after a write operation at the next clock edge?**
    - A) The high speed of the clock
    - B) The dual-port nature of the register file
    - C) The non-blocking assignment used in Verilog code

- D) The synchronous design of the write operation
- **Correct Answer: D**

Question Bank for Lab 7: ALU Unit

1. **What is the primary function of the ALU in the MIPS architecture?**
    - A) To store data
    - B) To manage the control unit
    - C) To perform arithmetic and logic operations
    - D) To handle interrupts
    - **Correct Answer: C**
2. **What does the ALU use to determine the specific operation to perform?**
    - A) The opcode directly from the instruction
    - B) A separate ALU control unit
    - C) The program counter
    - D) Direct user input
    - **Correct Answer: B**
3. **Which type of operation does the ALU perform for load and store instructions?**
    - A) Multiplication
    - B) Division
    - C) Addition
    - D) Subtraction
    - **Correct Answer: C**
4. **What does the ALU control unit output to control the ALU operations?**
    - A) A single-bit flag
    - B) A set of control lines (4 bits)
    - C) An 8-bit status register
    - D) A 32-bit instruction
    - **Correct Answer: B**
5. **Which ALU operation is typically used for branch instructions like beq?**
    - A) Addition
    - B) Subtraction
    - C) Logical AND
    - D) Logical OR
    - **Correct Answer: B**

6. **How does the ALU handle R-type instructions compared to I-type instructions?**
    - A) Uses a different set of registers
    - B) Performs operations based only on immediate values
    - C) Uses register values for operations
    - D) Does not perform any operations
    - **Correct Answer: C**
7. **What is the purpose of the zero flag in the ALU's output?**
    - A) Indicates whether the result of the operation is zero
    - B) Counts the number of operations performed
    - C) Determines if the operation should repeat
    - D) Signals an overflow error
    - **Correct Answer: A**
8. **What is the result of the ALU operation when alucontrol is set to perform an AND operation?**
    - A) The addition of two inputs
    - B) The subtraction of two inputs
    - C) The bitwise AND of two inputs
    - D) The bitwise OR of two inputs
    - **Correct Answer: C**
9. **In the context of MIPS, what does the ALU do when performing the lw instruction?**
    - A) Calculates the effective address by subtracting the immediate value from the base register
    - B) Calculates the effective address by adding the immediate value to the base register
    - C) Directly loads the value from memory into a register
    - D) Stores the value from a register into memory
    - **Correct Answer: B**
10. **What is the function of the alucontrol signal 4'b0010?**
    - A) Perform OR operation
    - B) Perform ADD operation
    - C) Perform SUB operation
    - D) Perform NOR operation

- **Correct Answer: B**

11. **Which component directs the ALU to perform specific operations in MIPS-32?**
    - A) The main control unit
    - B) The register file
    - C) The ALU control unit
    - D) The program counter
    - **Correct Answer: C**
12. **For which purpose is the slt operation used in MIPS?**
    - A) To add two numbers
    - B) To subtract two numbers
    - C) To compare two numbers and set a register if the first is less than the second
    - D) To load a value from memory
    - **Correct Answer: C**
13. **What determines the specific function like ADD or SUB within the ALU for R-type instructions?**
    - A) The **opcode** field
    - B) The **funct** field
    - C) The **shamt** field
    - D) The **rd** field
    - **Correct Answer: B**
14. **How does the ALU handle the result of an operation if it equals zero?**
    - A) It sets a register to one
    - B) It triggers an interrupt
    - C) It sets the zero flag to one
    - D) It resets the ALU
    - **Correct Answer: C**
15. **What is the significance of the beq instruction's operation within the ALU?**
    - A) It multiplies two values
    - B) It subtracts two values and branches if the result is zero
    - C) It adds an offset to the program counter unconditionally
    - D) It performs a bitwise NOR operation

- **Correct Answer: B**

16. **In what scenario does the ALU use a sign-extended immediate value?**
    - A) When executing **R-type** instructions
    - B) When executing logical operations
    - C) When calculating memory addresses for **I-type** instructions
    - D) When the **funct** field specifies an immediate operation
    - **Correct Answer: C**
17. **What does the ALUSrc control signal affect in the ALU's operation?**
    - A) Chooses between register and immediate values as the second operand
    - B) Selects the type of arithmetic operation to perform
    - C) Determines whether the operation should loop
    - D) Switches between addition and subtraction only
    - **Correct Answer: A**
18. **What role does the alucontrol module play in determining ALU operations?**
    - A) It specifies the registers to be used
    - B) It generates control signals based on the instruction type and function code
    - C) It manages data flow into and out of the ALU
    - D) It stores the results of ALU operations
    - **Correct Answer: B**
19. **Which ALU operation would be used for the AND instruction in MIPS?**
    - A) **4'b0000**
    - B) **4'b0001**
    - C) **4'b0010**
    - D) **4'b0110**
    - **Correct Answer: A**
20. **How does the ALU decide to perform the NOR operation?**
    - A) It is the default operation for all instructions
    - B) It is triggered by a specific **funct** code when **aluop** is for **R-type** instructions
    - C) It is selected when the zero flag needs to be reset
    - D) It uses the opcode directly from the instruction
    - **Correct Answer: B**

21. **What is the result of the ALU if the operation is subtraction and the operands are equal?**
    - A) The zero flag is set to zero
    - B) The zero flag is set to one
    - C) The ALU result is set to one
    - D) The ALU triggers an overflow
    - **Correct Answer: B**
22. **Which input to the ALU determines if the operation should be addition, subtraction, or a logic function?**
    - A) The **zero** flag
    - B) The **aluresult**
    - C) The **alucontrol**
    - D) The **a** and **b** inputs
    - **Correct Answer: C**
23. **What is the function of the zero output from the ALU?**
    - A) It indicates whether the ALU operation resulted in a non-zero value
    - B) It is used to determine branching decisions in control operations
    - C) It resets the ALU for the next operation
    - D) It indicates an overflow has occurred
    - **Correct Answer: B**
24. **Which of the following best describes the ALU's role in the MIPS architecture?**
    - A) It only performs arithmetic operations
    - B) It functions independently without any control signals
    - C) It serves as the central processing unit performing all logical and arithmetic operations
    - D) It only handles data storage and retrieval operations
    - **Correct Answer: C**
25. **How does the ALU handle the slt (set on less than) instruction?**
    - A) It subtracts one operand from the other and sets a register if the result is negative
    - B) It adds the operands and checks if the result is less than a third operand
    - C) It compares the operands directly and stores the result in a register

- D) It sets the zero flag based on a comparison of the operands
- **Correct Answer: A**

26. **What is required for the ALU to perform an OR operation?**
    - A) The **alucontrol** must indicate an OR operation with a specific control code
    - B) The operands must be pre-processed to remove any zero bits
    - C) The zero flag must be set prior to the operation
    - D) A special OR unit must be enabled in the ALU
    - **Correct Answer: A**
27. **Which operation does the alucontrol signal 4'b0110 specify?**
    - A) ADD
    - B) SUB
    - C) OR
    - D) AND
    - **Correct Answer: B**
28. **For which type of instruction does the ALU typically not use the funct field to determine the operation?**
    - A) **R-type**
    - B) **I-type**
    - C) **J-type**
    - D) **S-type**
    - **Correct Answer: B**
29. **What does the alucontrol value of 4'b0111 generally signify in ALU operations?**
    - A) Perform an AND operation
    - B) Perform an OR operation
    - C) Perform an addition
    - D) Set on less than (slt)
    - **Correct Answer: D**
30. **What is the role of the funct field in conjunction with the aluop input in determining ALU behavior?**
    - A) It is used to select the register operands
    - B) It defines the specific operation within the broad category defined by **aluop**
    - C) It determines the type of arithmetic operation without any other inputs

- D) It overrides the **aluop** input when set to a non-zero value
- **Correct Answer: B**

31. **In the ALU, what results in the zero output being asserted (set to 1)?**
    - A) The operation produces a positive result
    - B) The operation results in any non-zero outcome
    - C) The operation yields a zero as the result
    - D) The operation involves subtraction
    - **Correct Answer: C**
32. **How is the beq instruction processed in the ALU?**
    - A) By adding the operands
    - B) By subtracting and setting the program counter if the result is zero
    - C) By performing a bitwise AND operation
    - D) By loading the result into a register
    - **Correct Answer: B**
33. **What would the ALU do if the aluop is set for a subtraction but the funct code indicates addition?**
    - A) It will perform the subtraction
    - B) It defaults to an addition operation
    - C) The operation is determined by the higher priority **funct** field
    - D) The ALU will stall and require a reset
    - **Correct Answer: C**
34. **When does the ALU perform a NOR operation?**
    - A) When the operands are equal
    - B) When the **alucontrol** is set to **4'b1100**
    - C) As a default for undefined control settings
    - D) Only during specific branch operations
    - **Correct Answer: B**
35. **What is the effect of an ALU operation setting the zero flag during a branch instruction?**
    - A) It forces the branch to be taken
    - B) It cancels the branch operation
    - C) It has no effect on the branch decision

- D) It is used to update the program counter conditionally
- **Correct Answer: D**

36. **Which of the following ALU operations is directly associated with the control signal for R-type instructions?**
    - A) Load operations
    - B) Store operations
    - C) Operations defined by the **funct** field
    - D) Fixed operations like addition or subtraction regardless of the instruction
    - **Correct Answer: C**
37. **What determines the second operand in the ALU when performing I-type instructions like lw or sw?**
    - A) The value directly from a specified register
    - B) The immediate value sign-extended to 32 bits
    - C) The result of a previous ALU operation
    - D) A fixed offset defined in the architecture
    - **Correct Answer: B**
38. **How does the ALU contribute to the calculation of the next program counter value in branch instructions?**
    - A) It calculates the sum of the current program counter and an offset
    - B) It determines if the branch condition has been met
    - C) It directly sets the program counter to the target address
    - D) It has no role in calculating the program counter
    - **Correct Answer: B**
39. **Which ALU control line setting allows for the addition operation needed in lw and sw instructions?**
    - A) **4'b0000**
    - B) **4'b0001**
    - C) **4'b0010**
    - D) **4'b0111**
    - **Correct Answer: C**
40. **What is the ALU's response when an unsupported alucontrol setting is provided?**
    - A) It performs a default operation like ADD

- B) It generates an interrupt signal
- C) It may result in unpredictable behavior
- D) It ignores the operation and sets the **zero** flag
- **Correct Answer: C**

Question Bank for Lab 8: Branch Unit

1. **What is the main purpose of the Branch Unit in the MIPS architecture?**
    - A) To perform arithmetic operations
    - B) To direct the execution flow based on comparison results
    - C) To store data into memory
    - D) To fetch instructions from memory
    - **Correct Answer: B**
2. **What operation does the ALU perform for a beq instruction?**
    - A) Addition
    - B) Subtraction
    - C) Multiplication
    - D) Division
    - **Correct Answer: B**
3. **How is the Branch Target Address (BTA) calculated in MIPS?**
    - A) By adding the sign-extended offset to the register value
    - B) By subtracting the sign-extended offset from PC
    - C) By multiplying the sign-extended offset with PC
    - D) By adding the sign-extended offset to PC+4
    - **Correct Answer: D**
4. **What does the PCsrc signal determine in the branch unit?**
    - A) Whether to perform a read or write operation
    - B) Which register to use for storing data
    - C) Which path to follow for the next instruction address
    - D) The operation type in the ALU
    - **Correct Answer: C**
5. **Why is the offset in branch instructions shifted left by 2 bits?**
    - A) To convert it into a byte address
    - B) To align it to word boundaries
    - C) To increase the branching range
    - D) To simplify the hardware design
    - **Correct Answer: B**

6. **What condition must be true for the beq instruction to result in a branch (i.e., taking the branch)?**
    - A) The comparison in the ALU results in a non-zero
    - B) The **zero** flag from the ALU is set
    - C) The **zero** flag from the ALU is not set
    - D) The branch control signal is not set
    - **Correct Answer: B**
7. **What is the role of the shift logic unit in the branch unit's operation?**
    - A) To determine the direction of the branch
    - B) To adjust the offset to word boundaries
    - C) To shift the program counter left
    - D) To perform the branch comparison
    - **Correct Answer: B**
8. **When is the PCsrc signal set to 1 in a branch instruction?**
    - A) Always, regardless of the ALU comparison
    - B) When the branch condition is met
    - C) When the branch condition is not met
    - D) When the offset is zero
    - **Correct Answer: B**
9. **What does the ALU's zero output indicate in the context of a beq instruction?**
    - A) The operation resulted in an overflow
    - B) The two operands are equal
    - C) The two operands are not equal
    - D) The operation resulted in a non-zero value
    - **Correct Answer: B**
10. **How is the BTA used after it is calculated by the branch unit?**
    - A) It is stored back into the register file
    - B) It is sent to the ALU for further computation
    - C) It replaces the current PC if the branch is taken
    - D) It is discarded if the branch is not taken
    - **Correct Answer: C**

11. **What type of instruction uses the Branch Unit in MIPS?**
    - A) Arithmetic instructions
    - B) Load/store instructions
    - C) Conditional branch instructions
    - D) Unconditional jump instructions
    - **Correct Answer: C**
12. **Which component outputs the PCsrc signal in the branch unit?**
    - A) The ALU
    - B) The shift logic unit
    - C) The main control unit
    - D) The register file
    - **Correct Answer: C**
13. **What happens to the PCsrc signal if the operands in a beq instruction are not equal?**
    - A) It is set to 1
    - B) It is set to 0
    - C) It triggers an interrupt
    - D) It has no change and retains its previous state
    - **Correct Answer: B**
14. **Which signal from the ALU is crucial for the branch unit to function properly?**
    - A) The overflow flag
    - B) The carry-out flag
    - C) The zero flag
    - D) The negative flag
    - **Correct Answer: C**
15. **In a beq instruction, what does the zero output from the ALU interact with to generate the PCsrc signal?**
    - A) The opcode of the instruction
    - B) The function field of the instruction
    - C) The branch control signal from the main control unit
    - D) The immediate field of the instruction
    - **Correct Answer: C**

16. **Why is the offset in a branch instruction sign-extended?**
    - A) To allow for both positive and negative offsets
    - B) To increase the instruction size to 32 bits
    - C) To comply with the MIPS addressing mode
    - D) To ensure correct alignment in memory
    - **Correct Answer: A**
17. **What is the primary function of the PCsrc signal in the branch unit?**
    - A) To select between two different ALU operations
    - B) To choose between the incremented PC and the branch target address
    - C) To reset the program counter to zero
    - D) To signal an overflow condition
    - **Correct Answer: B**
18. **How does the branch unit affect the flow of execution in a MIPS processor?**
    - A) It stops the processor when a branch is taken
    - B) It redirects the execution to another part of the program based on a condition
    - C) It performs arithmetic operations required by branch instructions
    - D) It stores the results of branch operations in the register file
    - **Correct Answer: B**
19. **Which component is responsible for calculating the branch target address (BTA)?**
    - A) The shift logic unit
    - B) The ALU
    - C) The branch unit
    - D) The control unit
    - **Correct Answer: C**
20. **What triggers the branch unit to potentially alter the program counter (PC)?**
    - A) The instruction is a load or store type
    - B) The **zero** flag and the branch control signal are appropriately set
    - C) The instruction requires an immediate value
    - D) Any arithmetic operation is performed
    - **Correct Answer: B**

21. **What is the result of shifting the sign-extended immediate left by 2 bits in a branch instruction?**
    - A) It adjusts the offset to be word-aligned
    - B) It doubles the offset value
    - C) It converts the offset to a byte address
    - D) It reduces the offset to fit within the instruction format
    - **Correct Answer: A**
22. **In the branch unit, what is the role of adding PC+4 to the shifted immediate value?**
    - A) To calculate the return address
    - B) To determine the branch target address
    - C) To update the program counter unconditionally
    - D) To reset the ALU for the next operation
    - **Correct Answer: B**
23. **What dictates whether the next instruction address will be PC+4 or the branch target address?**
    - A) The type of operation performed by the ALU
    - B) The outcome of the condition checked by the branch unit
    - C) The type of the next instruction in the program
    - D) The immediate value of the current instruction
    - **Correct Answer: B**
24. **Why is the immediate field of a branch instruction shifted left by two bits?**
    - A) To facilitate faster calculation by the ALU
    - B) To ensure compatibility with different MIPS versions
    - C) To align the address to word boundaries as MIPS is word-addressable
    - D) To simplify the design of the shift logic unit
    - **Correct Answer: C**
25. **What component directly influences the PCsrc output in the branch unit?**
    - A) The sign-extender
    - B) The ALU's zero flag combined with the branch control signal
    - C) The instruction memory
    - D) The program counter itself
    - **Correct Answer: B**

26. **What operation is performed to compute the Branch Target Address (BTA)?**
    - A) Multiplication of PC+4 with the shifted immediate
    - B) Addition of PC+4 and the shifted immediate
    - C) Subtraction of the shifted immediate from PC+4
    - D) Logical AND of PC+4 and the shifted immediate
    - **Correct Answer: B**
27. **When does the branch unit not change the program counter to the branch target address?**
    - A) When the **beq** comparison is true
    - B) When the **beq** comparison is false
    - C) When the branch control signal is not asserted
    - D) When the shifted immediate is zero
    - **Correct Answer: B**
28. **What ensures that branch addresses are correctly aligned in MIPS?**
    - A) The immediate value is always positive
    - B) The immediate field is zero-extended
    - C) The immediate field is shifted left by two bits
    - D) The PC is incremented by 4
    - **Correct Answer: C**
29. **How does the branch unit interact with the ALU and the main control unit to perform its function?**
    - A) It uses the ALU's result to decide the next PC and gets a signal from the control unit to execute
    - B) It sends data to the ALU for computation
    - C) It controls the ALU's operation modes directly
    - D) It receives the opcode from the control unit to select the operation
    - **Correct Answer: A**
30. **What would happen if the zero flag from the ALU is set and the branch control signal is active?**
    - A) The branch is not taken, and PC is set to PC+4
    - B) The branch is taken, and PC is set to the branch target address
    - C) The branch instruction is ignored

- D) An interrupt is triggered to handle the branch
- **Correct Answer: B**

31. **Which statement correctly describes the branch unit's operation in a beq instruction when the operands are equal?**
    - A) The PC is incremented by 4 regardless of operand equality
    - B) The PC remains unchanged
    - C) The PC is set to the branch target address calculated by the unit
    - D) The PC automatically jumps to the start of the program
    - **Correct Answer: C**
32. **What is the significance of the PCsrc signal being set high by the branch unit?**
    - A) It indicates an error in computation
    - B) It directs the fetching of the next sequential instruction
    - C) It signals the multiplexer to select the branch target address as the new PC
    - D) It resets the ALU for a new operation
    - **Correct Answer: C**
33. **In which case would the branch unit not alter the PC to the branch target address even if the zero flag is set?**
    - A) The branch control signal is not active
    - B) The offset is not shifted correctly
    - C) The immediate field is not sign-extended
    - D) The PC+4 calculation is incorrect
    - **Correct Answer: A**
34. **What happens when the PCsrc signal is low after a branch condition is checked?**
    - A) The PC is set to the branch target address
    - B) The PC continues to the next sequential instruction (PC+4)
    - C) The PC is reset to zero
    - D) The execution jumps to an exception handling routine
    - **Correct Answer: B**
35. **Which component is critical for calculating the branch target address in the branch unit?**
    - A) The shift logic unit
    - B) The adder used to sum PC+4 and the shifted immediate

- C) The multiplexer that selects between PC+4 and BTA
- D) The register file that supplies operands
- **Correct Answer: B**

36. **Why is the offset field in a branch instruction sign-extended?**
    - A) To ensure it can represent both forward and backward branches
    - B) To match the 32-bit architecture of MIPS
    - C) To increase the processing speed of the branch unit
    - D) To simplify the logic design of the ALU
    - **Correct Answer: A**
37. **What role does the shifted immediate play in computing the branch target address?**
    - A) It specifies the exact memory address for the branch
    - B) It acts as a multiplier to determine how far to jump
    - C) It provides a word-aligned offset used in the address calculation
    - D) It is used as a direct input to the PC without additional processing
    - **Correct Answer: C**
38. **How does the branch unit determine if the next instruction address is the incremented PC or the branch target address?**
    - A) By checking the opcode of the instruction
    - B) Based on the outcome of the ALU operation and the branch control signal
    - C) By always selecting the branch target address for efficiency
    - D) By using a random selection method for unpredictability
    - **Correct Answer: B**
39. **What is the effect of the branch control signal on the branch unit's operation?**
    - A) It determines which register values to compare
    - B) It activates the unit to compute the branch target address
    - C) It sets the zero flag in the ALU
    - D) It directly sets the PC to the branch target address
    - **Correct Answer: B**
40. **Why must the offset in branch instructions be manipulated (shifted and sign-extended) before use?**
    - A) To convert it into a usable form for address calculation
    - B) To ensure it does not affect the base operation of the ALU

- C) To align it with the system's memory architecture
- D) To prevent overflow in the address calculation
- **Correct Answer: A**

Question Bank for Lab 9: Data Memory and Write Back Stage

1. **What is the primary role of Data Memory in the MIPS architecture?**
    - A) To perform arithmetic operations
    - B) To store and retrieve data during program execution
    - C) To manage the control signals for the ALU
    - D) To decode instructions
    - **Correct Answer: B**
2. **During which stage is Data Memory accessed in the MIPS pipeline?**
    - A) Instruction Fetch
    - B) Instruction Decode
    - C) Execution
    - D) Memory Access
    - **Correct Answer: D**
3. **What is the function of the MemRead signal in Data Memory?**
    - A) It enables writing data to memory
    - B) It enables reading data from memory
    - C) It selects between multiple memory units
    - D) It resets the memory to its initial state
    - **Correct Answer: B**
4. **Which of the following describes the MemWrite signal's function?**
    - A) It triggers a read operation from Data Memory
    - B) It triggers a write operation to Data Memory
    - C) It controls the address bus to Data Memory
    - D) It provides a clock signal to Data Memory
    - **Correct Answer: B**
5. **In the MIPS architecture, what is typically stored in Data Memory during the 'store word' (sw) instruction?**
    - A) The contents of the program counter
    - B) The address of the next instruction
    - C) The data from a specified register
    - D) The result of an ALU operation

- **Correct Answer: C**

6. **How is the address for reading or writing in Data Memory usually calculated?**
    - A) By the ALU, adding the base register to the sign-extended immediate
    - B) Directly by the instruction register
    - C) Using a dedicated adder in the memory unit
    - D) By shifting the program counter
    - **Correct Answer: A**
7. **What happens during the Write Back stage for a load instruction in MIPS?**
    - A) Data from the ALU is written back to a register
    - B) Data from Data Memory is written back to a register
    - C) The address for the next instruction is calculated
    - D) The instruction is decoded again to verify data integrity
    - **Correct Answer: B**
8. **Which multiplexer's output is crucial for the Write Back stage in load/store architecture?**
    - A) The one selecting between two register addresses
    - B) The one selecting data to be written to the register file
    - C) The one determining whether to use ALU or memory data
    - D) The one controlling read or write operations to memory
    - **Correct Answer: C**
9. **For R-type instructions, what does the Write Back stage typically involve?**
    - A) Writing the result from Data Memory to a register
    - B) Storing the PC in the register file
    - C) Writing the ALU result into the register file
    - D) Sending the ALU output back to the instruction decoder
    - **Correct Answer: C**
10. **What is the role of the MemtoReg control signal?**
    - A) It determines whether to perform a memory operation
    - B) It selects the source of data for writing back to the register file
    - C) It configures the memory address bus
    - D) It signals the ALU to initiate calculations

- **Correct Answer: B**

11. **Which type of memory operation does not involve the Data Memory unit directly?**
    - A) Load word
    - B) Store word
    - C) Arithmetic operations
    - D) Branch operations
    - **Correct Answer: C**
12. **What is the significance of the address bus in Data Memory operations?**
    - A) It carries the opcode for the current instruction
    - B) It specifies the exact location in memory for read or write operations
    - C) It transmits the write data to the memory
    - D) It resets the memory contents
    - **Correct Answer: B**
13. **How does the write_data_bus function in the context of Data Memory?**
    - A) It specifies the data to be written to memory
    - B) It carries the address of the data to be written
    - C) It reads data from the memory
    - D) It selects the memory bank
    - **Correct Answer: A**
14. **What ensures data integrity during a write operation in Data Memory?**
    - A) The **read** signal
    - B) The **write** signal being active during the clock's positive edge
    - C) Data being latched on the negative edge of the clock
    - D) The multiplexer selecting the correct data path
    - **Correct Answer: B**
15. **Which hardware component is directly involved in transferring data from Data Memory to the register file?**
    - A) ALU
    - B) Control unit
    - C) Multiplexer
    - D) Program counter

- **Correct Answer: C**

16. **What is a potential outcome of the read_data_bus being active in Data Memory?**
    - A) The data from the specified memory address is output
    - B) Data is written into the specified memory address
    - C) The address bus is cleared
    - D) The **write_data_bus** is deactivated
    - **Correct Answer: A**
17. **In the context of MIPS, when is the MemRead signal typically asserted?**
    - A) During the execution of any arithmetic operation
    - B) When data needs to be fetched from memory into a register
    - C) After writing data to the memory
    - D) Before an instruction is fetched from the instruction memory
    - **Correct Answer: B**
18. **What dictates the action of the Data Memory unit during a clock cycle?**
    - A) The state of the **MemRead** and **MemWrite** signals at the clock's negative edge
    - B) The type of instruction being executed
    - C) The data present on the **address_bus**
    - D) The state of the **MemRead** and **MemWrite** signals at the clock's positive edge
    - **Correct Answer: D**
19. **What does the Data Memory unit in MIPS primarily interact with to perform its functions?**
    - A) The register file directly
    - B) The instruction register
    - C) The ALU for address calculations
    - D) The PC for instruction fetching
    - **Correct Answer: C**
20. **Which statement best describes the write_data_bus in the context of the MIPS Data Memory?**
    - A) It's used to select which data to write into the memory
    - B) It carries the data that will be stored in the memory at the specified address
    - C) It determines the memory address where data will be read
    - D) It signals whether the current operation involves writing to memory

- **Correct Answer: B**

21. **What is typically the source of the data written to Data Memory in a sw instruction?**
    - A) The data comes directly from the ALU
    - B) The data is provided by the instruction decoder
    - C) The data comes from a specified register as determined by the instruction
    - D) The data is always a fixed value defined in the instruction
    - **Correct Answer: C**
22. **How does the MIPS architecture typically handle data transfer from Data Memory to the register file?**
    - A) Through direct connection without any control signals
    - B) Using a dedicated bus that bypasses the ALU
    - C) Through a multiplexer that selects data based on the **MemtoReg** signal
    - D) By direct transfer at the negative edge of the clock
    - **Correct Answer: C**
23. **What happens during the Memory Access stage for a sw instruction in MIPS?**
    - A) Data is written to the register file
    - B) Data is read from Data Memory and written to a register
    - C) Data from a register is written to an address in Data Memory
    - D) The ALU calculates the effective address but no data movement occurs
    - **Correct Answer: C**
24. **Which condition must be met for data to be written to Data Memory?**
    - A) The **MemRead** signal must be high
    - B) The **MemWrite** signal must be high and occur at the positive edge of the clock
    - C) Data must be available on the **write_data_bus**
    - D) Both **MemRead** and **MemWrite** signals must be active
    - **Correct Answer: B**
25. **During a lw instruction, what determines the register into which data is written?**
    - A) The **rt** field of the instruction
    - B) The **rs** field of the instruction
    - C) The ALU result
    - D) The **MemtoReg** signal

- **Correct Answer: A**

26. **What is the purpose of the MemtoReg signal in the Write Back stage?**
    - A) It selects whether to write the ALU result or data from memory to the register file
    - B) It determines which register should be written to
    - C) It controls the memory address calculation
    - D) It signals the memory to perform a read operation
    - **Correct Answer: A**
27. **In the MIPS datapath, how is the address for a sw instruction computed?**
    - A) By adding the base register value to the immediate field
    - B) By subtracting the immediate field from the base register
    - C) By multiplying the base register with the immediate field
    - D) By the shift left logical operation on the immediate field
    - **Correct Answer: A**
28. **Which register typically holds the data to be stored in memory during a sw instruction?**
    - A) **rd**
    - B) **rs**
    - C) **rt**
    - D) The program counter
    - **Correct Answer: C**
29. **What is the function of the read_data_bus in Data Memory operations?**
    - A) It specifies the memory address for read operations
    - B) It carries the data read from the specified memory address
    - C) It holds the data to be written to memory
    - D) It selects the memory bank for operation
    - **Correct Answer: B**
30. **How is the Write Back stage important in the context of lw and R-type instructions?**
    - A) It is only active for **R-type** instructions to write the ALU result
    - B) It decides which operation to perform next in the pipeline
    - C) It ensures that the correct data, whether from the ALU or memory, is written to the register file

- D) It resets the registers to prepare for the next instruction
- **Correct Answer: C**

31. **What ensures that only the correct data is written to Data Memory during a sw instruction?**
    - A) The **MemtoReg** signal
    - B) The **MemWrite** signal being high during the positive clock edge
    - C) The **write_data_bus** carrying the correct register data
    - D) All of the above
    - **Correct Answer: D**
32. **Which component is responsible for selecting the data source for the register file in the Write Back stage?**
    - A) The control unit
    - B) A 2X1 multiplexer
    - C) The ALU
    - D) The instruction register
    - **Correct Answer: B**
33. **How does the MemRead signal affect the operation of Data Memory?**
    - A) It prevents any write operation
    - B) It allows reading data from the specified address
    - C) It clears the data at the address before reading
    - D) It increments the address automatically
    - **Correct Answer: B**
34. **In a typical MIPS machine, when does the Write Back stage occur?**
    - A) After the instruction is fetched
    - B) Immediately after the instruction is decoded
    - C) Following the memory access stage
    - D) Before the execution stage
    - **Correct Answer: C**
35. **What role does the write_data_bus play during the sw instruction?**
    - A) It transmits the address to which data should be written
    - B) It carries the data that is to be stored in memory
    - C) It fetches data from the register file

- D) It controls whether the data is written to memory
- **Correct Answer: B**

36. **Which multiplexer setting is used to determine the destination register in the Write Back stage for a lw instruction?**
    - A) The **RegDst** signal
    - B) The **ALUSrc** signal
    - C) The **Branch** signal
    - D) The **MemtoReg** signal
    - **Correct Answer: A**
37. **How does the MIPS architecture ensure that data memory operations do not interfere with instruction fetch operations?**
    - A) By using separate memory units for instructions and data
    - B) By disabling the instruction fetch during memory operations
    - C) By prioritizing instruction fetch over memory operations
    - D) By using a cache system
    - **Correct Answer: A**
38. **What is the primary outcome of the MemWrite signal being activated?**
    - A) Data is read from memory to the register file
    - B) The program counter is incremented
    - C) Data is written to the memory address specified by the ALU
    - D) An interrupt is triggered to handle memory overflow
    - **Correct Answer: C**
39. **Which register holds the data to be written into memory during a sw instruction?**
    - A) The destination register (**rd**)
    - B) The source register (**rs**)
    - C) The temporary register (**rt**)
    - D) The stack pointer register
    - **Correct Answer: C**
40. **What does the MemtoReg control signal specifically dictate in the Write Back stage?**
    - A) Whether the data from memory or the ALU result is written to the register file
    - B) Whether the memory should perform a read or write operation

- C) Which register should receive the data in the register file
- D) How the ALU should process the next instruction
- **Correct Answer: A**

Question Bank for Lab 10: Control Unit

1. **What is the primary function of the Control Unit in the MIPS architecture?**
    - A) To execute instructions
    - B) To store data
    - C) To generate control signals based on the instruction opcode
    - D) To perform arithmetic operations
    - **Correct Answer: C**
2. **During which stage of the MIPS pipeline does the Control Unit operate?**
    - A) Instruction Fetch
    - B) Instruction Decode
    - C) Execution
    - D) Memory Access
    - **Correct Answer: B**
3. **What does the Control Unit use to determine control signals for each instruction?**
    - A) The function code
    - B) The opcode field
    - C) The immediate value
    - D) The register addresses
    - **Correct Answer: B**
4. **Which control signal does the Control Unit set to enable writing to the register file?**
    - A) RegWrite
    - B) ALUSrc
    - C) PCSrc
    - D) MemRead
    - **Correct Answer: A**
5. **In the context of R-type instructions, what ALUOp signal does the Control Unit generate?**
    - A) **00**
    - B) **01**
    - C) **10**
    - D) **11**

- **Correct Answer: C**

6. **For a 'load word' (lw) instruction, what control signals are asserted?**
    - A) RegWrite, MemRead, ALUSrc
    - B) MemWrite, ALUSrc, PCSrc
    - C) RegWrite, MemWrite, Branch
    - D) ALUSrc, PCSrc, Branch
    - **Correct Answer: A**
7. **Which signal indicates that the ALU should perform a subtraction for the 'beq' instruction?**
    - A) **ALUOp 01**
    - B) **ALUOp 10**
    - C) **ALUOp 00**
    - D) **ALUOp 11**
    - **Correct Answer: A**
8. **What role does the Control Unit play in setting the PCSrc signal?**
    - A) It sets PCSrc to 1 for all instructions
    - B) It sets PCSrc to 1 for branch instructions when the branch condition is met
    - C) It sets PCSrc to 0 to always choose the next sequential instruction
    - D) It has no role in setting the PCSrc signal
    - **Correct Answer: B**
9. **How does the Control Unit affect the Data Memory's behavior during a 'store word' (sw) instruction?**
    - A) It activates MemRead
    - B) It deactivates MemWrite
    - C) It activates MemWrite
    - D) It deactivates MemRead
    - **Correct Answer: C**
10. **What signal combination is used by the Control Unit to ensure data is written to a register during a 'load word' (lw) instruction?**
    - A) RegWrite high, MemtoReg high
    - B) RegWrite low, MemtoReg high
    - C) RegWrite high, ALUSrc high

- D) RegWrite low, ALUSrc low
- **Correct Answer: A**

11. **In the Control Unit, which signal is crucial for selecting the ALU operation for arithmetic instructions?**
    - A) PCSrc
    - B) MemtoReg
    - C) ALUOp
    - D) RegDst
    - **Correct Answer: C**
12. **Which control signal is necessary for the 'beq' instruction to check for equality?**
    - A) MemRead
    - B) ALUSrc
    - C) RegWrite
    - D) Branch
    - **Correct Answer: D**
13. **What effect does the MemtoReg signal have during the execution of a load instruction?**
    - A) It instructs the memory to store data
    - B) It selects the data from memory to be written to the register file
    - C) It chooses the next instruction to fetch
    - D) It triggers an ALU add operation
    - **Correct Answer: B**
14. **For which type of instruction is the RegDst signal particularly relevant?**
    - A) I-type
    - B) J-type
    - C) R-type
    - D) S-type
    - **Correct Answer: C**
15. **What is the significance of the Branch control signal in MIPS?**
    - A) It determines whether the current instruction will write to a register
    - B) It directs the ALU to perform specific operations
    - C) It indicates whether a branch should be taken based on ALU zero output

- D) It controls the flow of data into the ALU
- **Correct Answer: C**

16. **During which operations is the MemWrite signal activated?**
    - A) Load operations
    - B) Store operations
    - C) Arithmetic operations
    - D) Branch operations
    - **Correct Answer: B**
17. **What role does the ALUSrc signal play in the MIPS Control Unit?**
    - A) It selects the type of arithmetic operation in the ALU
    - B) It determines whether the ALU's second operand is an immediate value or from a register
    - C) It configures the ALU for read operations
    - D) It sets the ALU for write operations
    - **Correct Answer: B**
18. **Which control signal is irrelevant for the execution of the 'beq' instruction?**
    - A) ALUSrc
    - B) RegWrite
    - C) Branch
    - D) ALUOp
    - **Correct Answer: B**
19. **How does the Control Unit configure the datapath for a 'sw' instruction?**
    - A) It sets MemtoReg high and ALUSrc high
    - B) It sets RegWrite high and MemWrite high
    - C) It sets MemWrite high and ALUSrc high
    - D) It sets RegWrite high and ALUSrc high
    - **Correct Answer: C**
20. **What does the RegDst control signal determine in the Control Unit's operation?**
    - A) It chooses between two different register write addresses in R-type instructions
    - B) It selects the operation to be performed by the ALU
    - C) It determines whether to read or write to memory

- D) It specifies whether to branch
- **Correct Answer: A**

21. **Which control signal combination is used for a jump instruction in the Control Unit?**
    - A) RegWrite low, ALUSrc low, Branch high
    - B) RegWrite high, ALUSrc high, Branch low
    - C) RegWrite low, ALUSrc low, Branch low
    - D) RegWrite low, ALUSrc high, Branch low
    - **Correct Answer: C**
22. **In the context of the Control Unit, what does a MemRead signal high and a MemWrite signal low indicate?**
    - A) A store operation is being performed
    - B) An arithmetic operation is in progress
    - C) A load operation is being performed
    - D) No operation is being performed on the data memory
    - **Correct Answer: C**
23. **What is the primary effect of the Branch signal being high?**
    - A) The next instruction address is taken from the branch target
    - B) The instruction at the branch target is executed immediately
    - C) Data is written to the instruction memory
    - D) An arithmetic operation is triggered in the ALU
    - **Correct Answer: A**
24. **For an R-type instruction, which of the following signal settings is correct?**
    - A) RegDst high, ALUSrc low, ALUOp **10**
    - B) RegDst low, ALUSrc high, ALUOp **00**
    - C) RegDst high, ALUSrc high, ALUOp **01**
    - D) RegDst low, ALUSrc low, ALUOp **11**
    - **Correct Answer: A**
25. **How does the Control Unit handle the sw instruction regarding ALUSrc and MemWrite?**
    - A) ALUSrc low, MemWrite high
    - B) ALUSrc high, MemWrite high
    - C) ALUSrc low, MemWrite low

- D) ALUSrc high, MemWrite low
- **Correct Answer: B**

26. **What control signals are essential for a load word (lw) instruction to execute correctly?**
    - A) ALUSrc, RegWrite, MemRead
    - B) ALUSrc, RegWrite, MemWrite
    - C) ALUSrc, Branch, MemWrite
    - D) ALUSrc, Branch, MemRead
    - **Correct Answer: A**
27. **What does setting the MemtoReg signal high accomplish?**
    - A) It directs the memory to store the current data
    - B) It instructs the register file to write the data coming from memory
    - C) It configures the ALU to pass the memory address
    - D) It causes the PC to skip to the next instruction
    - **Correct Answer: B**
28. **Which instruction type uses the control signal setting of RegDst low, ALUSrc high, and MemtoReg high?**
    - A) R-type
    - B) I-type
    - C) J-type
    - D) S-type
    - **Correct Answer: B**
29. **For the beq instruction, which of the following is an accurate setting of control signals?**
    - A) ALUSrc low, RegWrite low, Branch high
    - B) ALUSrc high, RegWrite high, Branch low
    - C) ALUSrc high, RegWrite low, Branch high
    - D) ALUSrc low, RegWrite high, Branch high
    - **Correct Answer: A**
30. **Which component in the Control Unit determines whether the operation involves the data memory?**
    - A) The opcode field

- B) The function code
- C) The **MemRead** and **MemWrite** signals
- D) The **RegDst** and **RegWrite** signals
- **Correct Answer: C**

31. **How is the ALUOp signal used in controlling ALU behavior?**
    - A) It selects the specific operation to be performed based on the instruction type
    - B) It determines whether the ALU should be activated
    - C) It chooses the register from which to read data
    - D) It directs whether the operation will involve memory access
    - **Correct Answer: A**
32. **What sequence does the Control Unit follow to execute an addi instruction?**
    - A) Activate RegWrite, set ALUSrc high, ALUOp **00**
    - B) Deactivate MemWrite, set ALUSrc low, ALUOp **10**
    - C) Activate Branch, set ALUSrc high, ALUOp **01**
    - D) Activate MemRead, set RegDst high, ALUOp **00**
    - **Correct Answer: A**
33. **Which settings of the Control Unit are correct for a store word (sw) instruction?**
    - A) RegWrite high, MemWrite high, MemRead low
    - B) RegWrite low, MemWrite high, MemRead low
    - C) RegWrite high, MemWrite low, MemRead high
    - D) RegWrite low, MemWrite low, MemRead high
    - **Correct Answer: B**
34. **What determines the function of the ALU for R-type instructions in the Control Unit?**
    - A) The immediate field of the instruction
    - B) The **RegDst** signal
    - C) The **ALUOp** signal
    - D) The **Branch** signal
    - **Correct Answer: C**
35. **In a MIPS Control Unit, which signal ensures that the branch condition has been met before altering the program counter?**
    - A) MemtoReg

- B) ALUSrc
- C) Branch
- D) ALUOp
- **Correct Answer: C**

36. **Which condition triggers the MemWrite signal in the Control Unit?**
    - A) When data needs to be read from memory
    - B) When an arithmetic operation must be stored
    - C) When data must be written to memory
    - D) When a branch condition is met
    - **Correct Answer: C**
37. **How does the Control Unit interact with the ALU to perform operations?**
    - A) By sending direct data inputs to the ALU
    - B) By setting ALU control signals based on the opcode
    - C) By programming the ALU to perform fixed functions
    - D) By bypassing the ALU for most operations
    - **Correct Answer: B**
38. **What role does the RegDst signal play in instruction execution?**
    - A) It selects the destination register for arithmetic results
    - B) It determines the data path for memory operations
    - C) It chooses the ALU operation directly
    - D) It directs the flow of data from memory to the register file
    - **Correct Answer: A**
39. **Why is the MemRead signal important for a load instruction?**
    - A) It enables the instruction memory to output data
    - B) It allows data to be fetched from data memory to the register file
    - C) It prevents the ALU from performing unnecessary operations
    - D) It triggers a write-back operation to the register file
    - **Correct Answer: B**
40. **Which signal combination is specific to the execution of the load word (lw) instruction?**
    - A) MemRead high, MemWrite low, RegWrite high

- B) MemRead low, MemWrite high, RegWrite low
- C) MemRead high, MemWrite high, RegWrite high
- D) MemRead low, MemWrite low, RegWrite high
- **Correct Answer: A**

Question Bank for Lab 11: Single Cycle vs. Pipelined MIPS Processors

1. **What is a single cycle MIPS processor designed to do?**
    - A) Execute multiple instructions in one clock cycle
    - B) Execute one instruction per multiple clock cycles
    - C) Execute one instruction per one clock cycle
    - D) Execute multiple instructions simultaneously without any clock
    - **Correct Answer: C**
2. **Which component is crucial for controlling the operations of a single cycle MIPS processor?**
    - A) Control Unit
    - B) ALU
    - C) Data Memory
    - D) Program Counter
    - **Correct Answer: A**
3. **What is the main disadvantage of a single cycle MIPS processor?**
    - A) Increased complexity
    - B) Decreased reliability
    - C) Longer clock cycle times
    - D) More power consumption
    - **Correct Answer: C**
4. **In a single cycle MIPS processor, what determines the length of the clock cycle?**
    - A) The fastest instruction
    - B) The average speed of all instructions
    - C) The slowest instruction
    - D) The most frequently used instruction
    - **Correct Answer: C**
5. **What is the main advantage of pipelining in a MIPS processor?**
    - A) Reduces the clock cycle length
    - B) Allows multiple instructions to be executed in one cycle
    - C) Simplifies the control unit
    - D) Decreases power consumption

- **Correct Answer: B**

6. **How many stages are there in a typical MIPS pipeline?**
    - A) Three
    - B) Four
    - C) Five
    - D) Six
    - **Correct Answer: C**
7. **Which stage of the MIPS pipeline is responsible for fetching instructions?**
    - A) Instruction Decode (ID)
    - B) Execution (EX)
    - C) Memory Access (MEM)
    - D) Instruction Fetch (IF)
    - **Correct Answer: D**
8. **What role do pipeline registers play in a pipelined MIPS processor?**
    - A) They store data permanently like memory
    - B) They enhance the clock speed
    - C) They buffer intermediate results between stages
    - D) They replace the control unit
    - **Correct Answer: C**
9. **Which instruction stage computes the branch target address?**
    - A) IF
    - B) ID
    - C) EX
    - D) MEM
    - **Correct Answer: C**
10. **In pipelined MIPS, what does the MEM stage primarily handle?**
    - A) Register writing
    - B) Instruction decoding
    - C) Data memory access
    - D) Branch calculation
    - **Correct Answer: C**

11. **What is the purpose of the Write Back (WB) stage in a pipelined MIPS processor?**
    - A) To fetch the next instruction
    - B) To decode the current instruction
    - C) To write results back to the register file
    - D) To execute arithmetic operations
    - **Correct Answer: C**
12. **How does pipelining affect the execution of instructions in a MIPS processor?**
    - A) Increases the number of clock cycles per instruction
    - B) Reduces the execution time of each instruction
    - C) Allows each instruction to be completed in one cycle
    - D) Decreases the instruction throughput
    - **Correct Answer: B**
13. **What is the 'critical path' in a single cycle MIPS processor?**
    - A) The sequence of instructions
    - B) The longest possible path that any instruction can take through the circuit
    - C) The shortest possible path that any instruction can take through the circuit
    - D) The path used by branch instructions
    - **Correct Answer: B**
14. **Why does pipelining improve efficiency in MIPS processors?**
    - A) It reduces the need for control signals
    - B) It executes all instructions in a single cycle
    - C) It overlaps the execution of multiple instructions
    - D) It eliminates the need for a clock
    - **Correct Answer: C**
15. **What is the main reason for using pipeline registers in a MIPS processor?**
    - A) To increase data storage capacity
    - B) To separate and buffer stages of instruction processing
    - C) To enhance the processing speed of the ALU
    - D) To control the instruction flow
    - **Correct Answer: B**

16. **What challenge does pipelining address in the context of MIPS processor performance?**
    - A) The complexity of the control unit
    - B) The inefficiency of using hardware resources in single cycle processors
    - C) The storage of large data
    - D) The need for multiple ALUs
    - **Correct Answer: B**
17. **How does the length of the clock cycle in a pipelined MIPS compare to that in a single cycle MIPS?**
    - A) It is longer in a pipelined MIPS
    - B) It is the same in both
    - C) It is shorter in a pipelined MIPS
    - D) It varies more in a pipelined MIPS
    - **Correct Answer: C**
18. **Which MIPS processor type can execute multiple instructions simultaneously?**
    - A) Single cycle MIPS
    - B) Super scalar MIPS
    - C) Pipelined MIPS
    - D) Multi-threaded MIPS
    - **Correct Answer: C**
19. **What is a disadvantage of the pipelined MIPS processor compared to single cycle?**
    - A) It uses more power
    - B) It is more complex to implement
    - C) It is slower
    - D) It requires more memory
    - **Correct Answer: B**
20. **Which of the following best describes the impact of pipelining on individual MIPS instruction latency?**
    - A) It increases latency
    - B) It decreases latency
    - C) It has no impact on latency
    - D) It makes latency variable

- **Correct Answer: C**

21. **What does the term 'stalling' refer to in the context of a pipelined MIPS processor?**
    - A) Increasing the clock speed
    - B) Decreasing the clock speed
    - C) Delaying the execution of instructions to resolve hazards
    - D) Stopping the clock altogether
    - **Correct Answer: C**
22. **Why is a load instruction considered the 'slowest' in a single cycle MIPS implementation?**
    - A) Because it uses the least amount of hardware resources
    - B) Because it does not interact with the ALU
    - C) Because it requires multiple cycles to complete
    - D) Because it passes through all stages of the data path, accumulating the most delays
    - **Correct Answer: D**
23. **What factor limits the cycle time in a single cycle MIPS processor?**
    - A) The fastest instruction
    - B) The average time of all instructions
    - C) The time taken by the slowest instruction
    - D) The number of instructions
    - **Correct Answer: C**
24. **How does the clock cycle time in a single cycle processor affect its performance?**
    - A) Longer cycle times generally improve performance
    - B) Shorter cycle times generally degrade performance
    - C) Longer cycle times generally reduce performance
    - D) Cycle time has no effect on performance
    - **Correct Answer: C**
25. **In a pipelined processor, why are separate stages required?**
    - A) To allow for simultaneous execution of different parts of multiple instructions
    - B) To increase the number of instructions that can be stored
    - C) To simplify the control logic
    - D) To decrease the overall power consumption

- **Correct Answer: A**

26. **Which pipeline stage is primarily responsible for calculating address values for memory operations?**
    - A) IF
    - B) ID
    - C) EX
    - D) MEM
    - **Correct Answer: C**
27. **What does the IF stage do in a pipelined MIPS processor?**
    - A) It fetches the next instruction from memory
    - B) It decodes the fetched instruction
    - C) It executes arithmetic operations
    - D) It writes results back to the registers
    - **Correct Answer: A**
28. **During which pipeline stage is the actual data memory read or write operation performed?**
    - A) IF
    - B) ID
    - C) EX
    - D) MEM
    - **Correct Answer: D**
29. **What happens during the WB stage of a pipelined MIPS processor?**
    - A) The program counter is updated
    - B) Instructions are fetched from memory
    - C) Data or results are written back to the register file
    - D) Arithmetic or logic calculations are performed
    - **Correct Answer: C**
30. **What is the impact of pipelining on the throughput of a MIPS processor?**
    - A) It decreases throughput
    - B) It increases throughput
    - C) It has no impact on throughput
    - D) It makes throughput unpredictable

- **Correct Answer: B**

31. **Which of the following best describes the function of pipeline registers?**
    - A) They temporarily store data between each stage of the pipeline
    - B) They permanently store the results of computations
    - C) They are used to store instructions only
    - D) They increase the clock speed
    - **Correct Answer: A**
32. **How do pipeline registers affect the data flow between stages?**
    - A) They eliminate the need for control signals
    - B) They allow each stage to operate independently
    - C) They decrease the data throughput
    - D) They store all data until the program completes
    - **Correct Answer: B**
33. **What is the benefit of having separate resources for each stage in a pipelined processor?**
    - A) It reduces the cost of the processor
    - B) It allows multiple instructions to be processed at the same time
    - C) It simplifies the processor design
    - D) It requires less power
    - **Correct Answer: B**
34. **Which stage of the MIPS pipeline would you associate with the initial reading of registers?**
    - A) IF
    - B) ID
    - C) EX
    - D) MEM
    - **Correct Answer: B**
35. **What is typically the slowest stage in the MIPS pipeline and why?**
    - A) IF, because fetching instructions requires accessing memory
    - B) ID, because decoding can be complex
    - C) EX, because of the complexity of arithmetic operations
    - D) MEM, because memory operations can be slow

- **Correct Answer: D**

36. **In a pipelined MIPS processor, what ensures that data is correctly passed from one stage to the next?**
    - A) The control unit
    - B) Pipeline registers
    - C) The ALU
    - D) The main memory
    - **Correct Answer: B**
37. **Why is instruction fetch (IF) critical in the operation of a pipelined MIPS processor?**
    - A) It is the only stage that interacts with memory
    - B) It determines the overall speed of the processor
    - C) Without it, no other stages can proceed
    - D) It consumes the most energy
    - **Correct Answer: C**
38. **What challenge does instruction decode (ID) present in a pipelined architecture?**
    - A) It is difficult to implement
    - B) It can introduce data hazards
    - C) It is the slowest stage
    - D) It uses the most hardware resources
    - **Correct Answer: B**
39. **How does the execution (EX) stage in a pipeline differ from a single-cycle processor's execution phase?**
    - A) It is faster in a single-cycle processor
    - B) It handles more instructions simultaneously
    - C) It only performs arithmetic operations
    - D) It is identical in both types of processors
    - **Correct Answer: B**
40. **Which MIPS pipeline stage directly affects the performance of branch instructions?**
    - A) IF
    - B) ID
    - C) EX
    - D) MEM

- **Correct Answer: C**