وَقُل رَّبِّ زِدْنِي عِلْمًا

Analog CMOS IC Design training @ ITI

Under supervision of Dr.Hesham omran

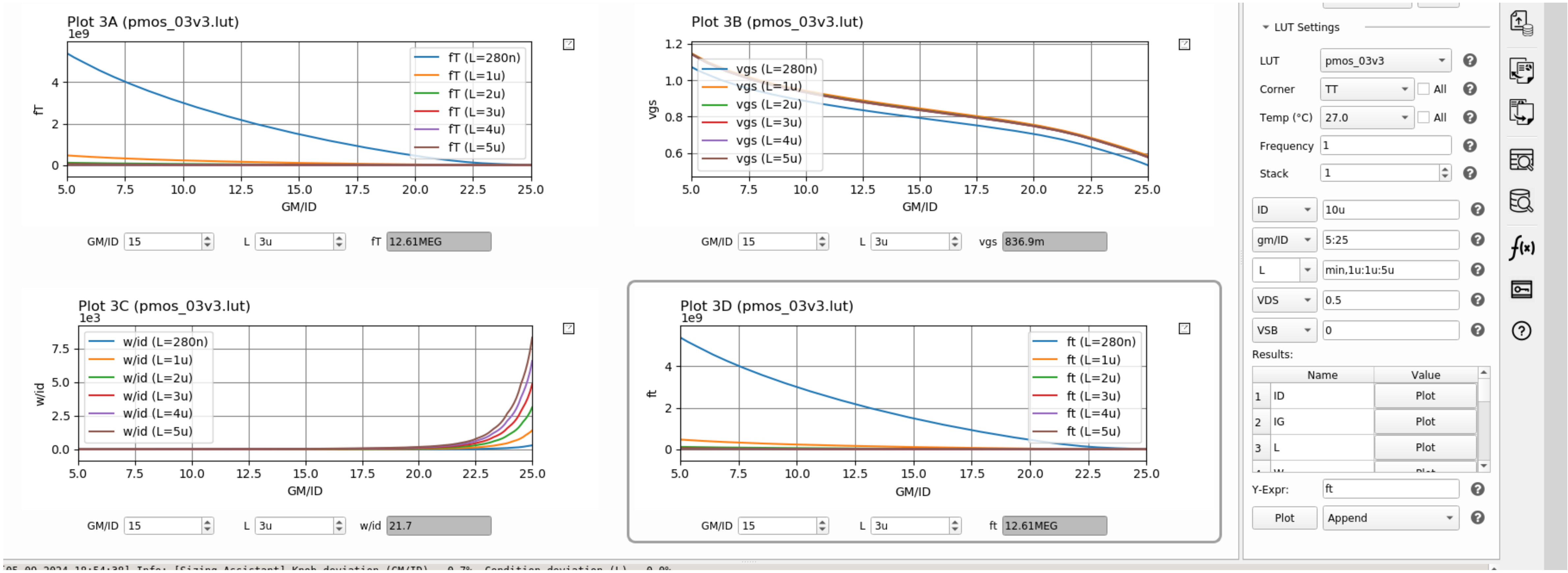
Lab 11 (Mini Project 02)
Fully-Differential Folded Cascode OTA + CMFB circuit
Tools : Analog Designer's Toolbox (ADT) + Cadence

Mohamed nasser

ECE Senior 1 Student @ ASU

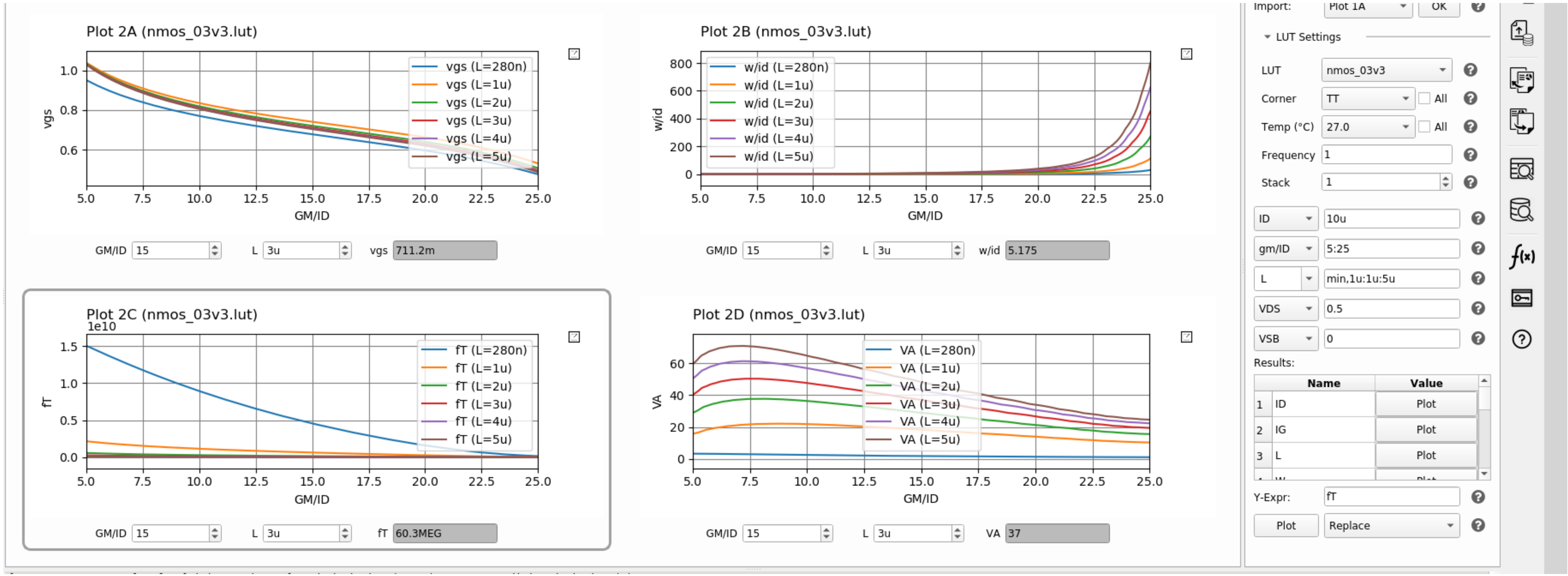
Gm/id Methodology

- Pmos

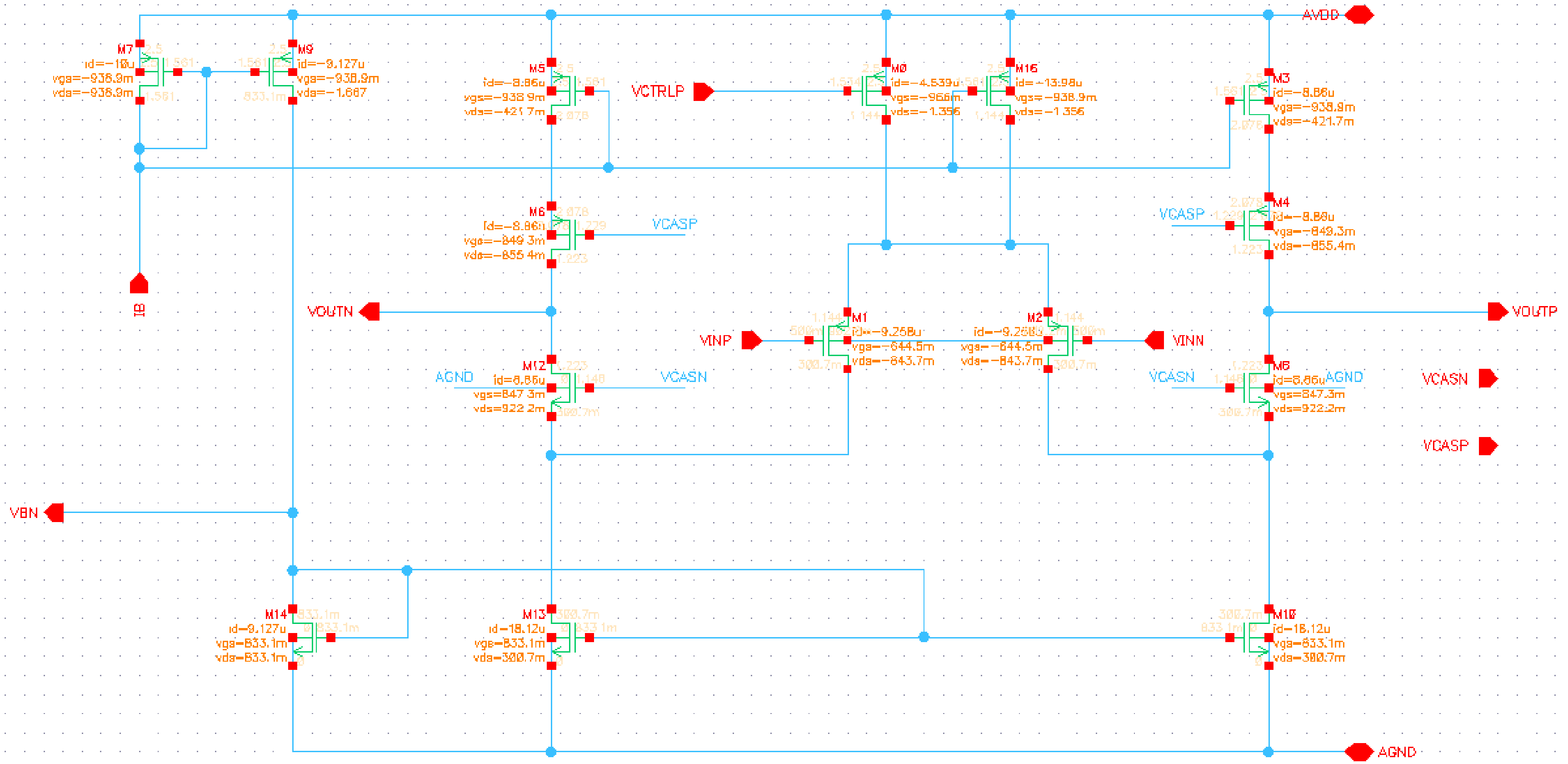


Gm/id Methodology

- Nmos



Folded+ CMFB network



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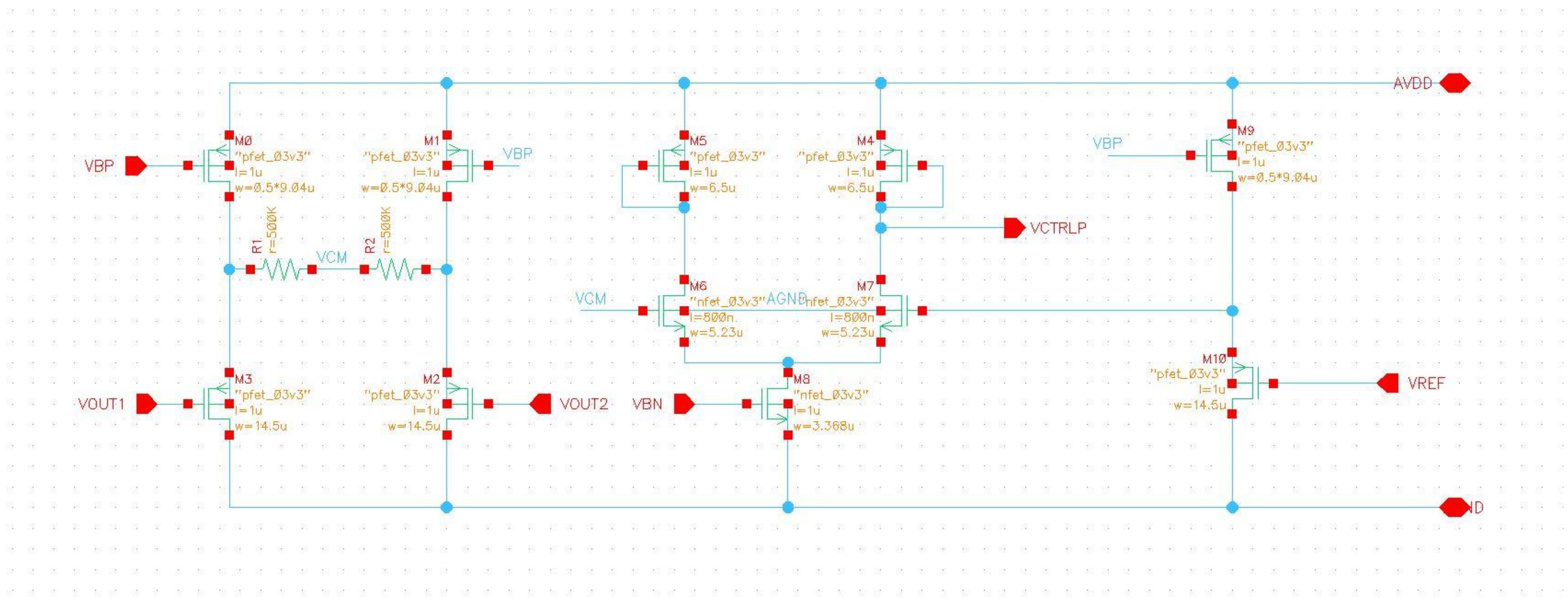


Hand Analysis

- Settling time spec:

$$ts = \frac{4.6}{t} = \frac{4.6}{Bwcl} \Rightarrow Bwcl = \frac{4.5}{100n} = 46M\ \frac{rad}{sec} = \mathbf{7.3M\ hz}$$

$$GBW = Wu = Acl * BWcl = 2 * Bwcl = 90M\frac{rad}{sec} = \mathbf{14.6\ Mhz}$$

$$GBW = \frac{gm(ip)}{cout} = \frac{gm(ip)}{Cl + Cf(1-B)} = \frac{gm(ip)}{Cl + \frac{3}{4}Cf} \Rightarrow gm(ip) = 130\ us, let\ gm = 160\ us$$

$$assuming\ \frac{gm}{id} = 20\ for\ in.pairs \Rightarrow \boldsymbol{IB1 = 9u}\ \text{"}to\ get\ margin\ and\ self\ loading\text{"}$$

- Dc open loop gain and CL gain specs:

$$LG = \frac{Vout}{If} * Aol(R) = \frac{Vout}{VfB} * Aol = \frac{Cf}{Cf + Cs + cself} * Aol = \frac{1}{4} * Aol \geq 60dB \Rightarrow \boldsymbol{Aol \geq 73\ dB}$$

- From phase margin spec:

$$PMcl = 90 - \arctan\left(\frac{wucl}{wpnd}\right) \geq 70 \Rightarrow Wpnd = 3\ Wucl$$

$$we\ know\ that\ GX = \frac{1}{4}Wucl \Rightarrow GX = Wpnd \Rightarrow \boldsymbol{PMol \geq 37}$$

Hand Analysis

- ❑ $we\ will\ use\ split\ ratio = 1$

$$IB2 = IB1 = 9u$$

- ❑ $assuming\ \frac{gm}{id}\ and\ L\ as\ a\ first\ step\ to\ make\ the\ design\ easier$:
- ❑ Using charts ::

- $input\ pairs$: $\frac{gm}{id} = 20\ , l = 400n \Rightarrow \boldsymbol{w = 85u}$
- $current\ source\ devices\ (nmos)$: $\frac{gm}{id} = 10, L = 1u \Rightarrow \boldsymbol{w = 8.25u}$
- $current\ source\ devices(pmos)$: $\frac{gm}{id} = 10\ , l = 1u \Rightarrow \boldsymbol{w = 18u}$
- $cascode\ devices$: $\frac{gm}{id} = 15\ , L = 500n \Rightarrow \boldsymbol{w = 25u}$ **pmos & 7 u nmos**

Hand Analysis

- $Vcacp \leq VDD - VGS(5) - V*(4)$

$$VGS(4) = 848.7m$$

$$V*(5) = \frac{2}{\frac{gm}{id}} = 200\ mv$$

$$\boldsymbol{Vcasp \leq 1.45\ V}$$

- $Vcasn = VGS(3) + V*(2)$

$$V*(2) = \frac{2}{\frac{gm}{id}} = 200\ mv$$

$$VGS(3) \Rightarrow From\ ADT = 752.3m$$

$$\boldsymbol{Vcasn \geq 960\ mv}$$

- CMIR range :

$$CMIR_{high}: VDD - V*(6) - Vin \geq Vth(1)$$

$$Vth(1) = 750\ \text{mv}, \text{V}*(6) = 200\text{mv}$$

$$Vin \leq 1.55\ v$$

$$CMIR_{LOW}: Vcasn - VGS(3) - v*(3) - vin \leq Vth(1)$$

$$Vth(1) = 750\ \text{mv}, \text{V}*(3)140\ mv, \text{VGS}(3) = 752\ \text{mv}, \textbf{let}\ \boldsymbol{Vcasn = 1.1\ v}$$

$$\boldsymbol{vin \geq -0.54\ mv}$$

cockpit

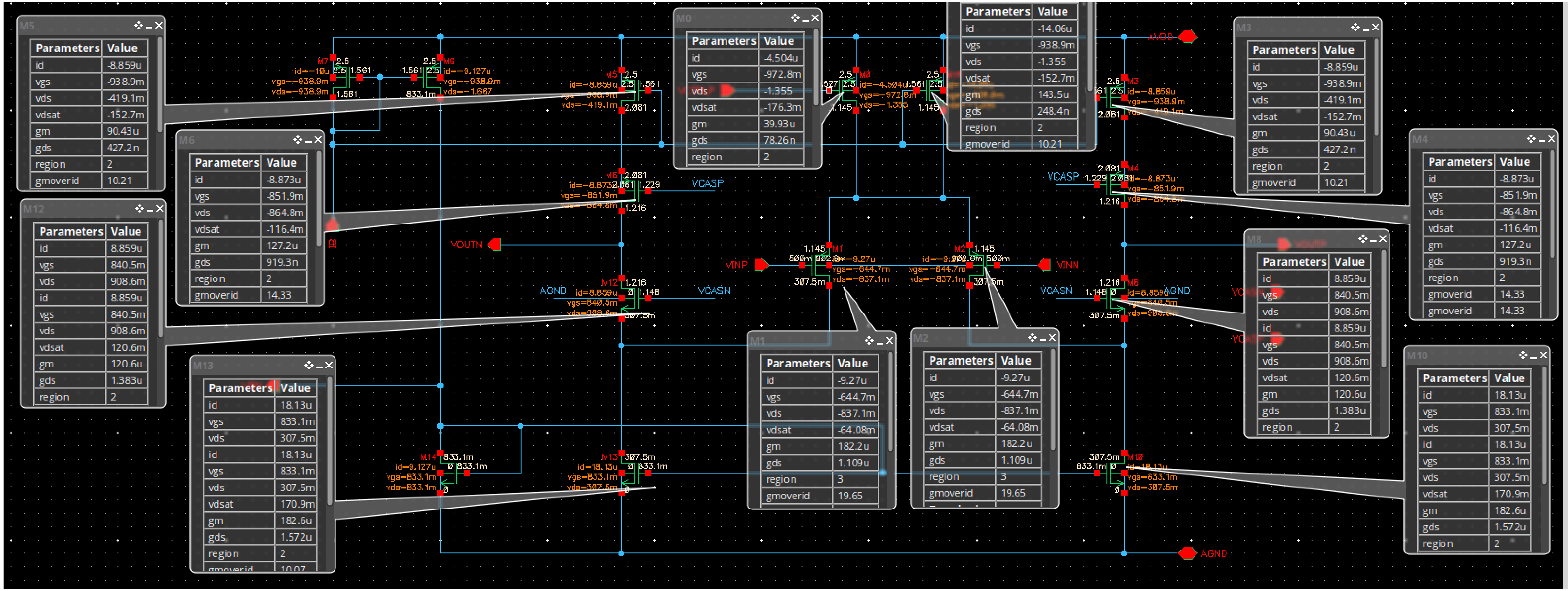
- Getting accurate sizing from cockpit adt

Design Variable	Value	Output Variable	Nominal
M1a(ID)	9u	VCASCP	1.229
M1a(L)	400n	VBP	1.559
M2a(L)	1u	VCMFB	1.558
M3a(L)	500n	VINP	500m
M4a(L)	500n	VINN	500m
M5a(L)	1u	M1a(W)	84.63u
M6(L)	1u	M2a(W)	8.423u
M1a(GM/ID)	20	M3a(W)	6.778u
M2a(GM/ID)	10	M4a(W)	23.53u
M3a(GM/ID)	15	M5a(W)	18.08u
M4a(GM/ID)	15	M6(W)	34.85u
M5a(GM/ID)	10	MVBN(W)	8.423u
M6(GM/ID)	10	MVBP(W)	18.08u
VDD[Nominal]	2.5	MVCMFB(W)	34.85u

Design Variable	Value	Output Variable	Nominal
M1a(ID)	9u	DC Gain	10.78k
M1a(L)	400n	BW	5.041k
M2a(L)	1u	GBW	54.37MEG
M3a(L)	500n	UGF	54.12MEG
M4a(L)	500n	PM	77.81
M5a(L)	1u	Total Input ...	79.83u
M6(L)	1u	Thermal Inpu...	383.1a
M1a(GM/ID)	20	Input Referre...	3.034m
M2a(GM/ID)	10	Area	247.2p
M3a(GM/ID)	15	Cgg	123.2f
M4a(GM/ID)	15	Itotal	36u
M5a(GM/ID)	10	VDD	2.5
M6(GM/ID)	10	VIN_CM	500m
VDD[Nominal]	2.5	VOUT_CM	1.25

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters



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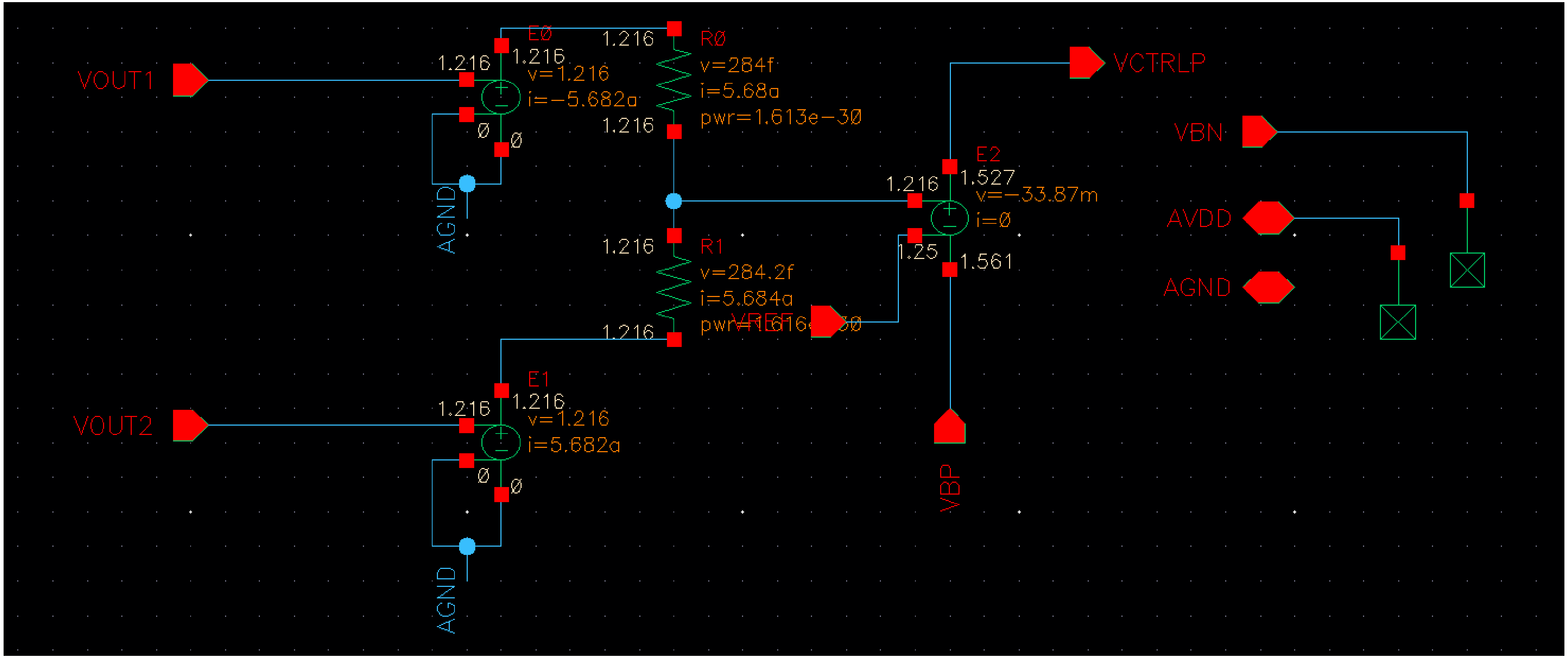

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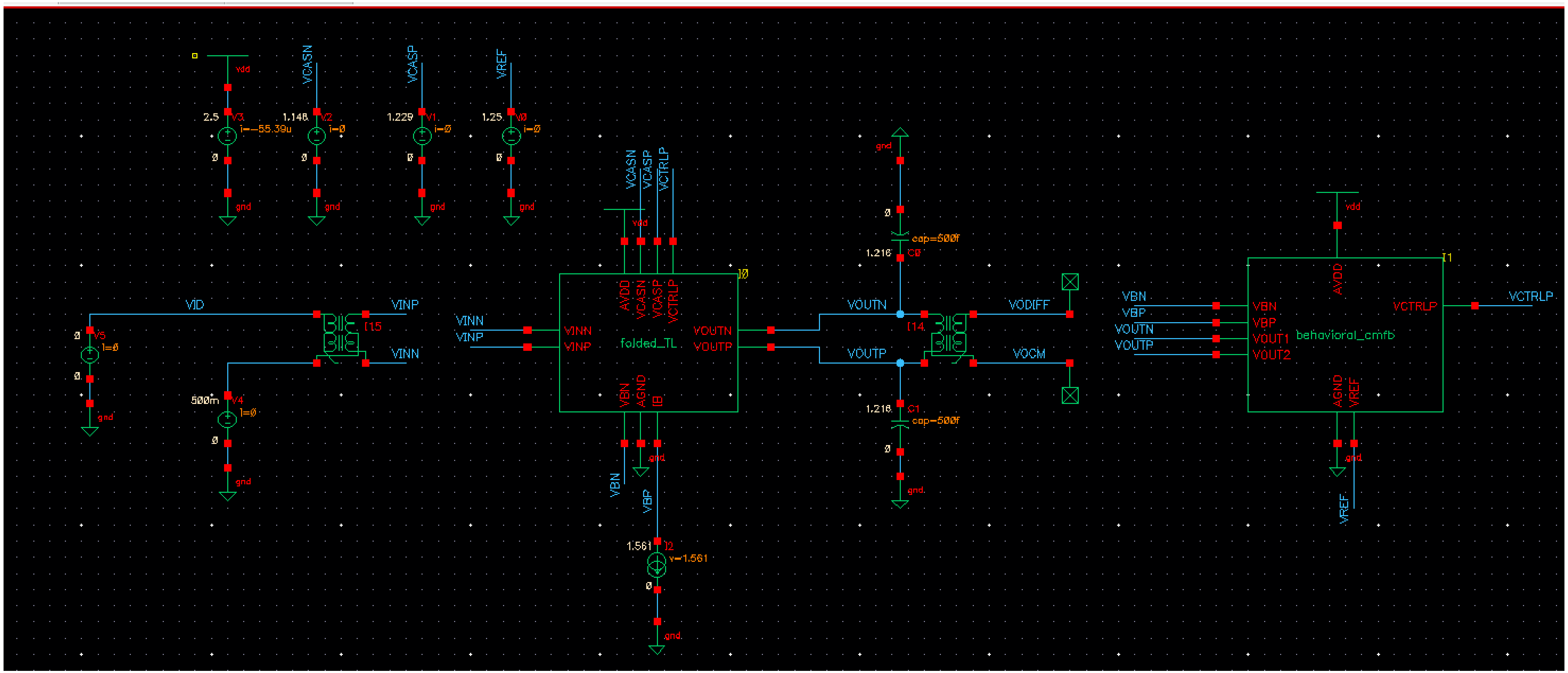


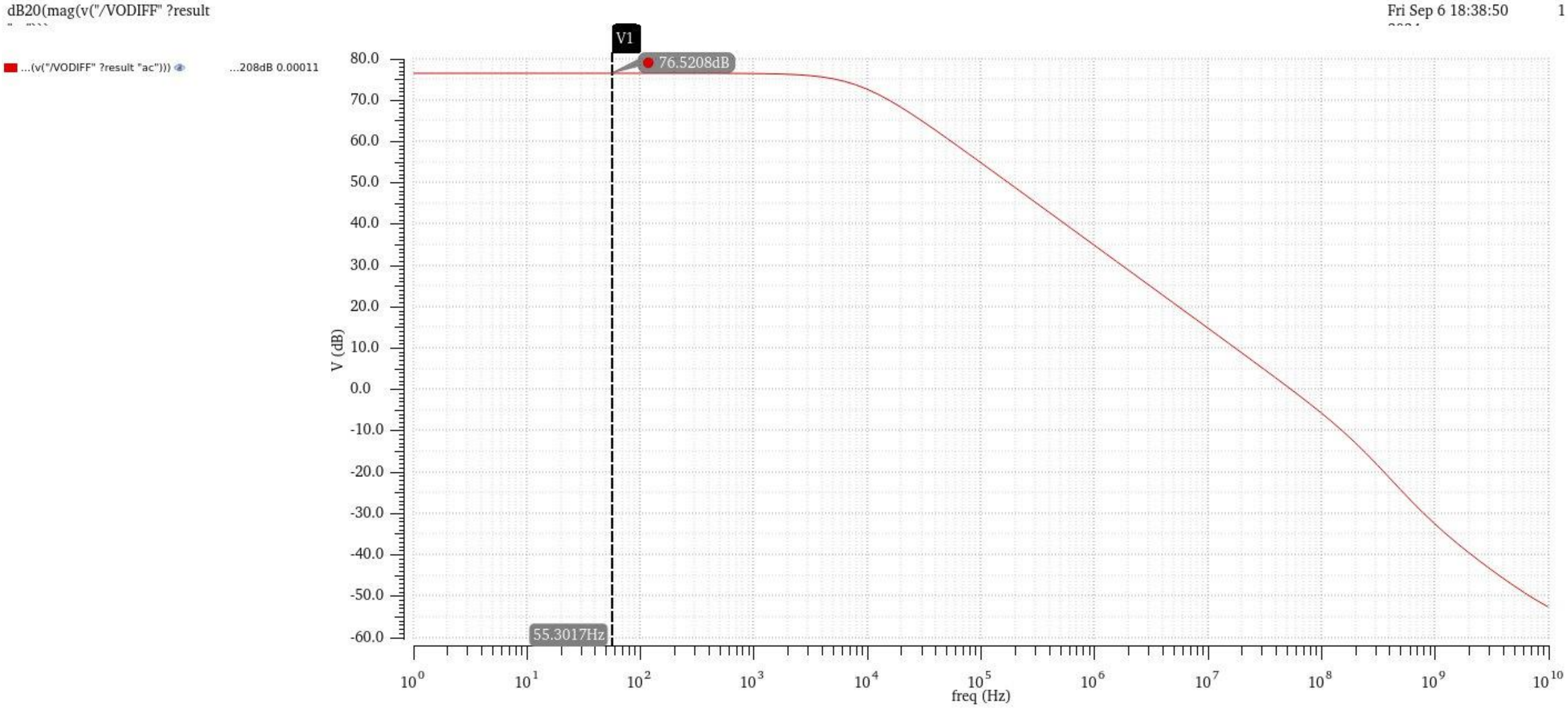
PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- What is the CM level at the OTA output?
  - $Vocm = 1.22\ v$

- What are the differential input and output voltages of the error amplifier? What is the relation between them?
  - $diff\ input = 0.027v \quad ,difoutput = 0.027 \quad ,Acmfb = 1$

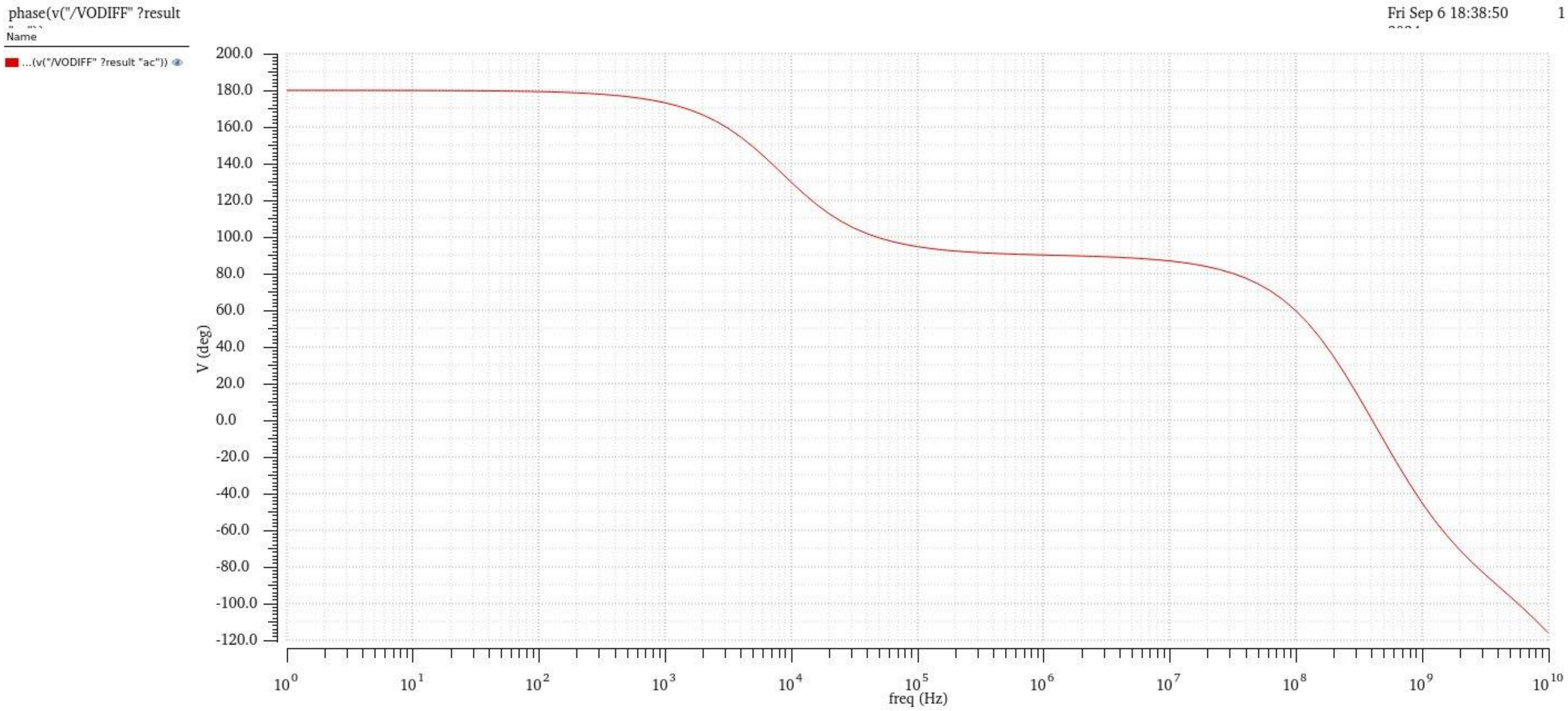
PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- Diff small signal ccs
  - Plot diff gain (magnitude in dB and phase) vs frequency.



PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- phase vs frequency



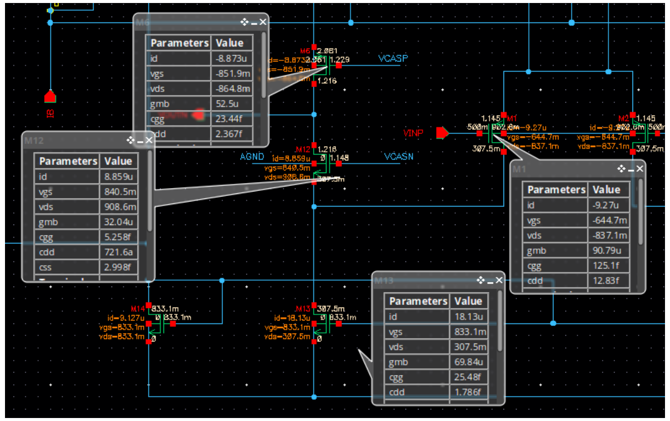
PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:tb_part3:1	phase(v("/VODIFF" ?result "ac"))				
lab11:tb_part3:1	AO	6.7k			
lab11:tb_part3:1	AO_dB	76.52			
lab11:tb_part3:1	dB20(mag(v("/VODIFF" ?result "...				
lab11:tb_part3:1	GBW	56.3M			
lab11:tb_part3:1	UGF	55.77M			
lab11:tb_part3:1	BW	8.383k			
lab11:tb_part3:1	dB20(phase(v("/VODIFF" ?result ...				
lab11:tb_part3:1	phaseMargin(VF("/VODIFF"))	-106.9			
lab11:tb_part3:1	(phaseMargin(VF("/VODIFF")) + 1...	73.12			

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

- ❑Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis) indices is from cockpit 456 M 41M 37.75



$$GBW = \frac{gm1}{cout} = \frac{gm1}{2pi(cl + Cself_{ota})} = \frac{182\text{us}}{0.5\text{p} + 50\text{f}} \approx 52 \text{ Mhz}$$

$$Aol = G_M R_{out} = gm1 * (((g_{m4}+g_{mb4}) * r_{o4} * r_{o5})||((g_{m3}+g_{mb3}) * r_{o3} * (r_{o2}||r_{o1})) =$$
$$182us(\ (179u * \frac{1}{919n} * \frac{1}{427n})||(152us * \frac{1}{1.383u} * (1/1.57\text{u} \ || \ 1/1.1\text{u}) \approx 6825$$

$$BW = \frac{1}{2pi * (Cl + c_{self}) * Rout} \approx 7.7 \text{ khz}$$

	Simulation	Hand analysis
Ao	6700	6825
GBW	56 Mhz	52 Mhz
BW	8.4 K	7.7 k

PART 4: Open-Loop OTA Simulation (Actual CMFB)

- CMFB design :
- $error\ amplifier$
  - $Pmos\ DC\ is\ same\ as\ MX\ adjusting\ 20\%\ of\ current$
  - $Input\ Nmos\ \ =>\ \ gm/id = 20\ , l = 500n\ , i = 7.2u/2\ , => W = 13u$
  - $Tail\ CS\ \ =>\ \ supply\ 0.4\ i_{tail}\ of\ folded\ (W * 0.4)$

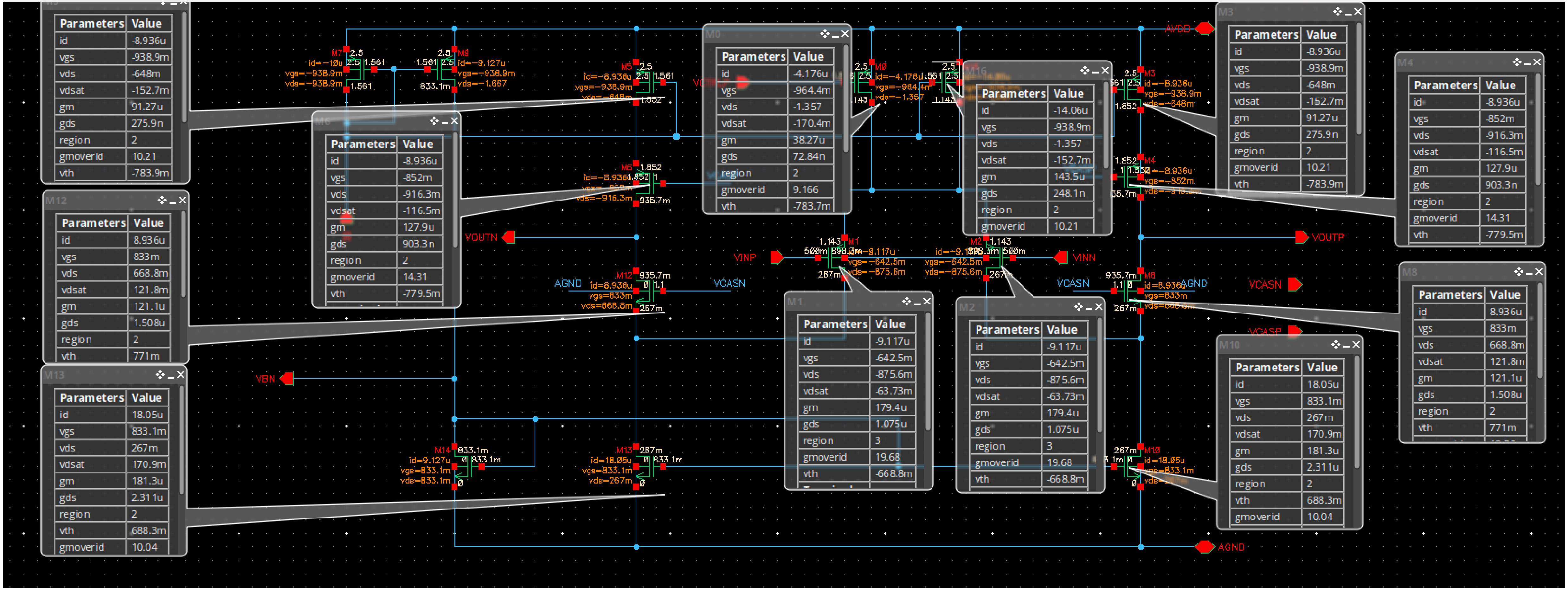
- $CD\ \ =>\ \ to\ avoid\ loading$
  - $Pmos\ cs\ supply\ 0.25\ Current\ supplied\ By\ M5\ in\ folded\ W5 * 0.25$
  - $Pmos\ input :\ l = 1u\ , i = 9u/4\ , gm/id = 15\ \ =>\ \ w = 14.5u$

- $Vref\ value :$
  - $Best\ Vref\ value =\ 950\ mv\ Maximizing\ swing\ \ 2v* =>\ \ 1.5\ (VDD - |VGSP| + V*p)$

- $Total\ current\ consumption\ = 14u\ \ <\ 50\%\ of\ folded$

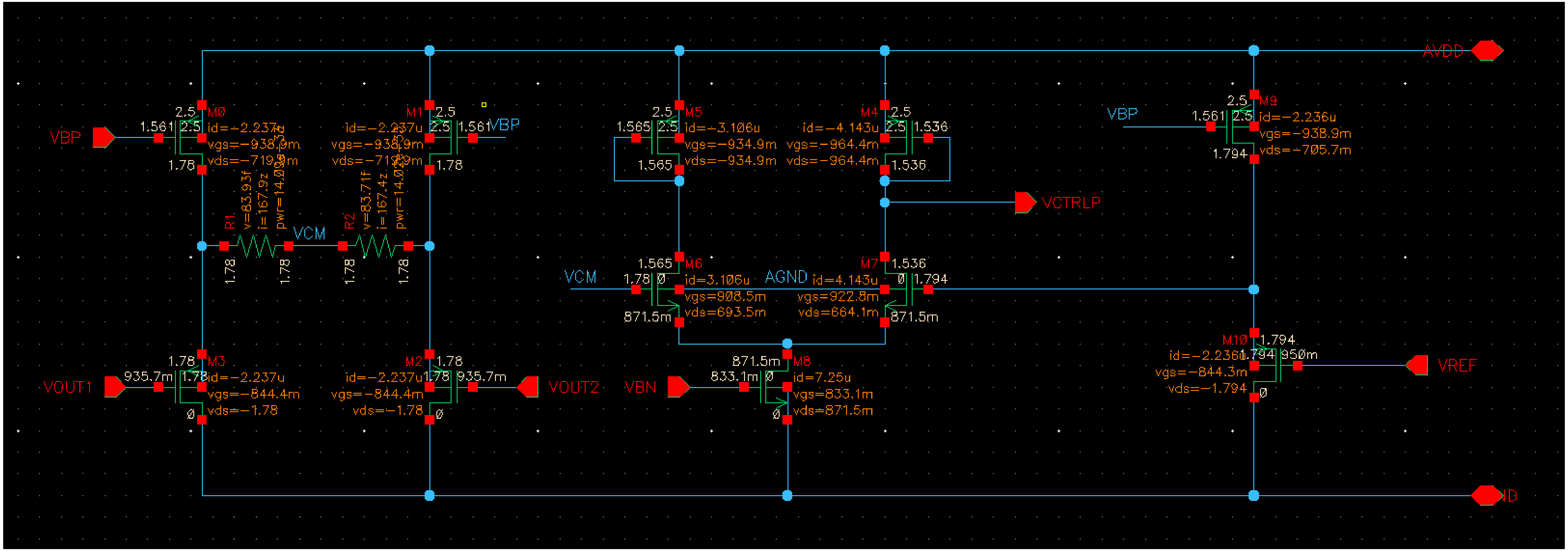
PART 4: Open-Loop OTA Simulation (Actual CMFB)

- Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters



PART 4: Open-Loop OTA Simulation (Actual CMFB)

- ❑ Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters



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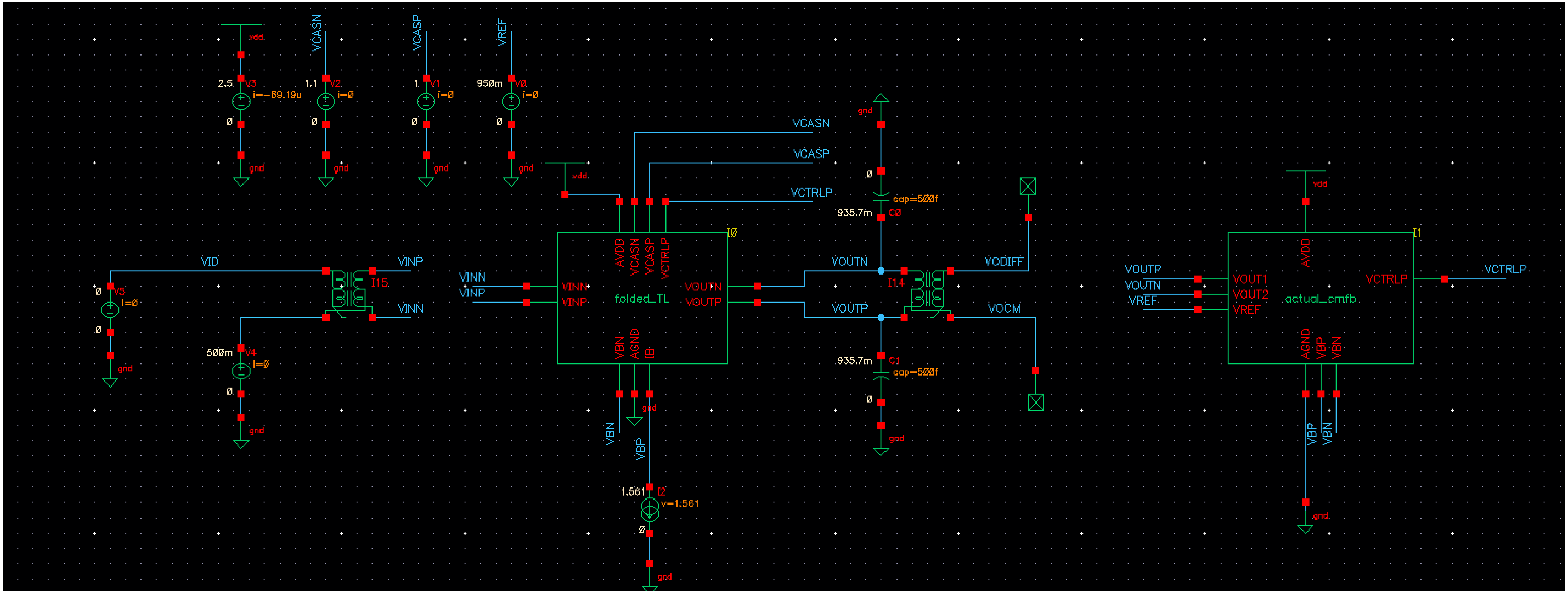


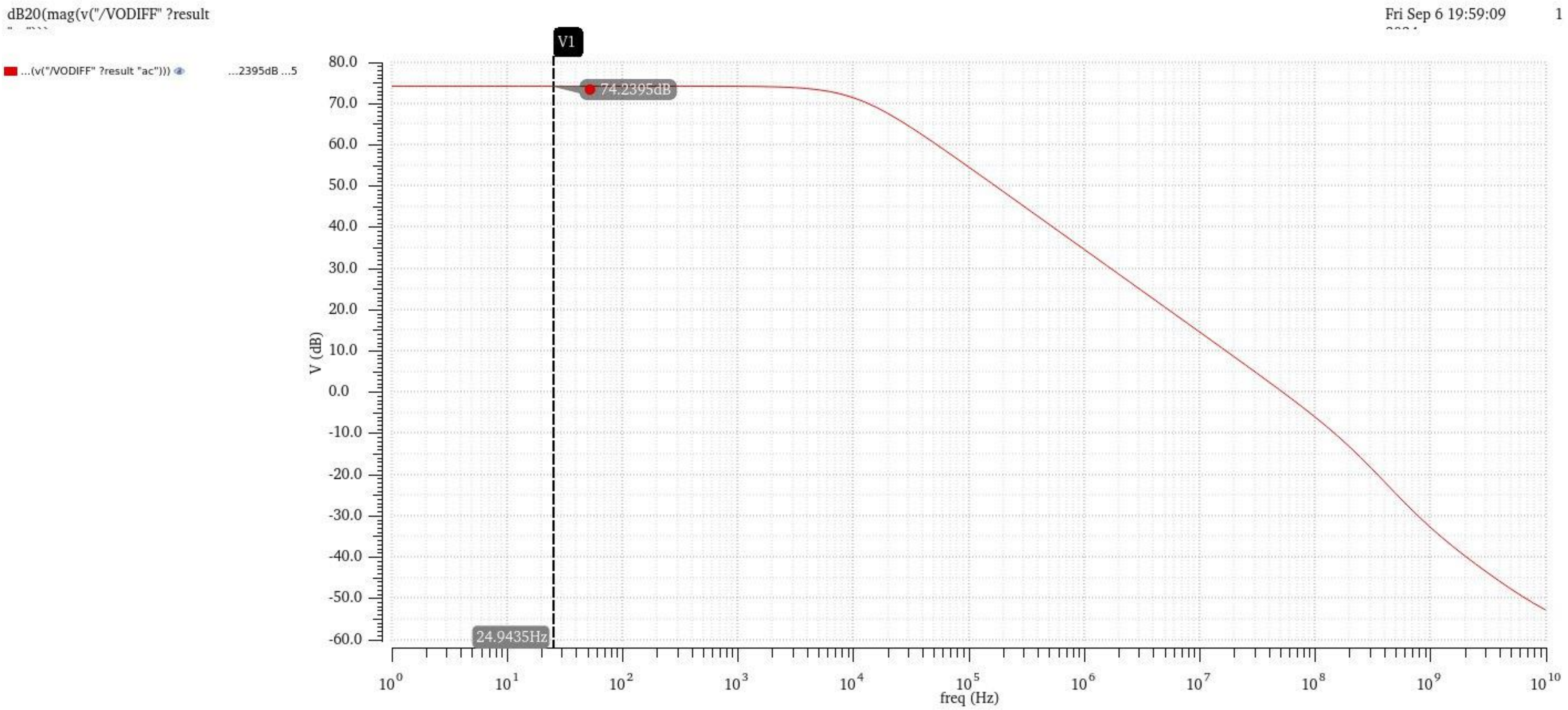
PART 4: Open-Loop OTA Simulation (Actual CMFB)

- ❑What is the CM level at the OTA output? Why?
- ➢ $\approx 936\ mv\ as\ the\ cmfb\ network\ adjust\ M6\ current\ to\ maitain\ the\ v_{ocm}\ neer\ to \approx vref$ $but\ as\ Mx\ in\ error\ amplifier\ and\ M6\ in\ folded\ has\ differant\ Vds\ it\ will\ be\ hard$ $to\ have\ error = 0$

- ❑What are the differential input and output voltages of the error amplifier? What is the relation between them?
- ➢ $diff\ input = 0.014\ \ , dif output = 0.029\ \ \ , Acmfb \approx 2\ "Gian\ of\ error\ amplifier"$

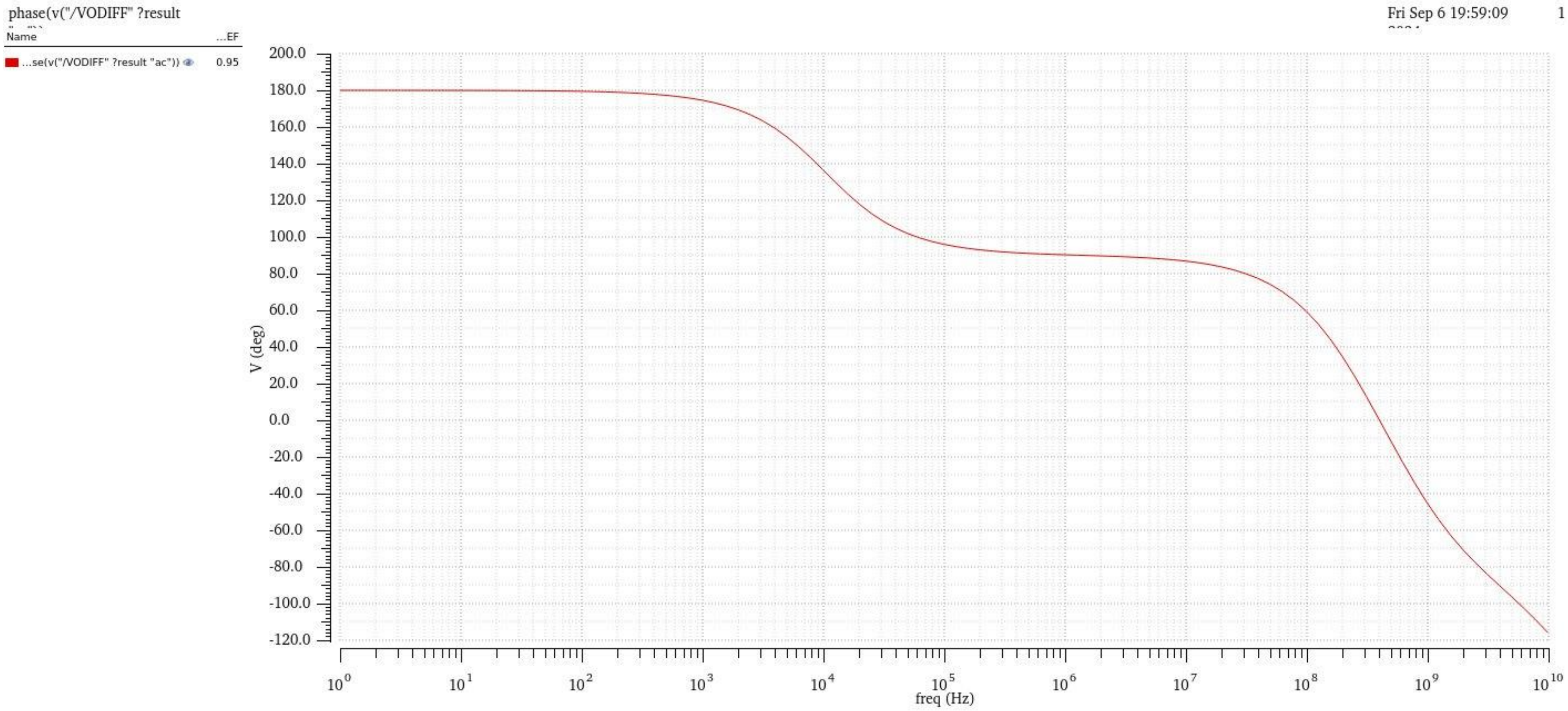
PART 4: Open-Loop OTA Simulation (Actual CMFB)

- Diff small signal ccs
  - Plot diff gain (magnitude in dB and phase) vs frequency.



PART 4: Open-Loop OTA Simulation (Actual CMFB)

- phase vs frequency



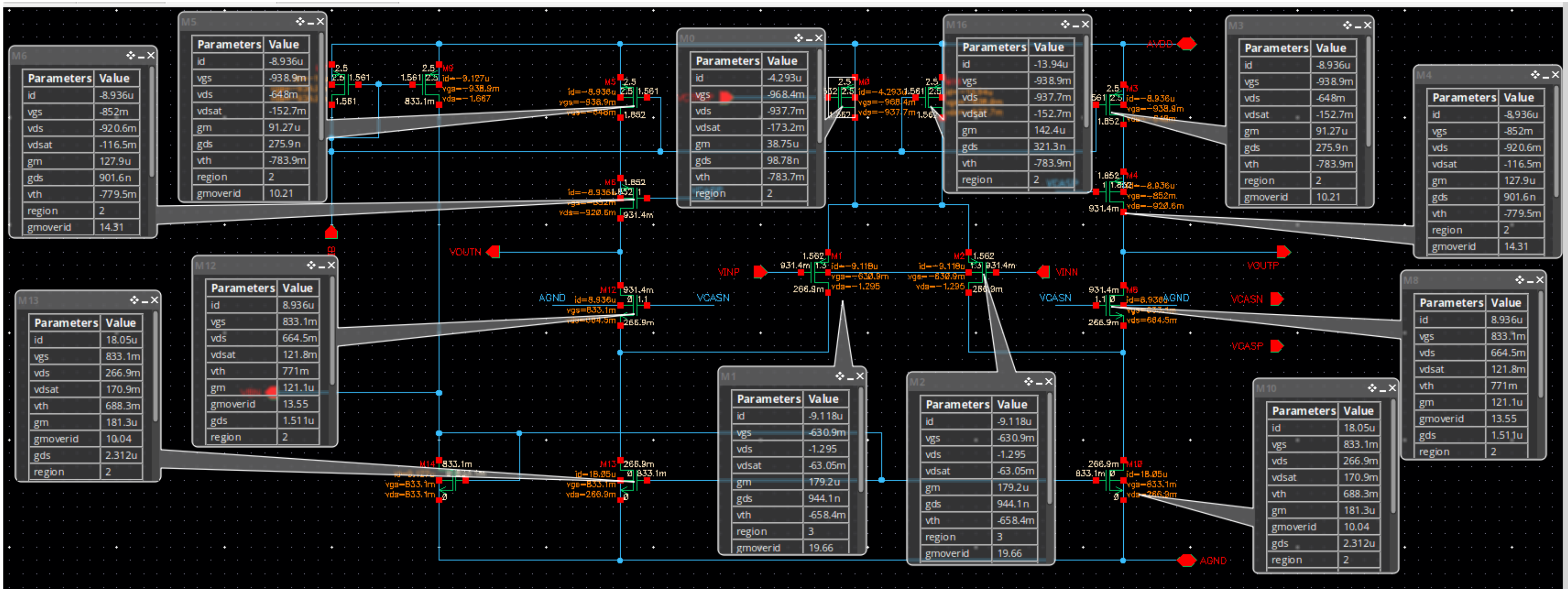
PART 4: Open-Loop OTA Simulation (Actual CMFB)

❑Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:tb_part4:1	phase(v("/VODIFF" ?result "ac"))				
lab11:tb_part4:1	Ao	5.152k			
lab11:tb_part4:1	A0_dB	74.24			
lab11:tb_part4:1	GBW	54.7M			
lab11:tb_part4:1	UGF	53.98M			
lab11:tb_part4:1	BW	10.59k			
lab11:tb_part4:1	dB20(mag(v("/VODIFF" ?result "...				
lab11:tb_part4:1	PM	-106.7			
lab11:tb_part4:1	(PM + 180)	73.3			

PART 5: Closed Loop Simulation (AC and STB Analysis)

- ❑ Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters



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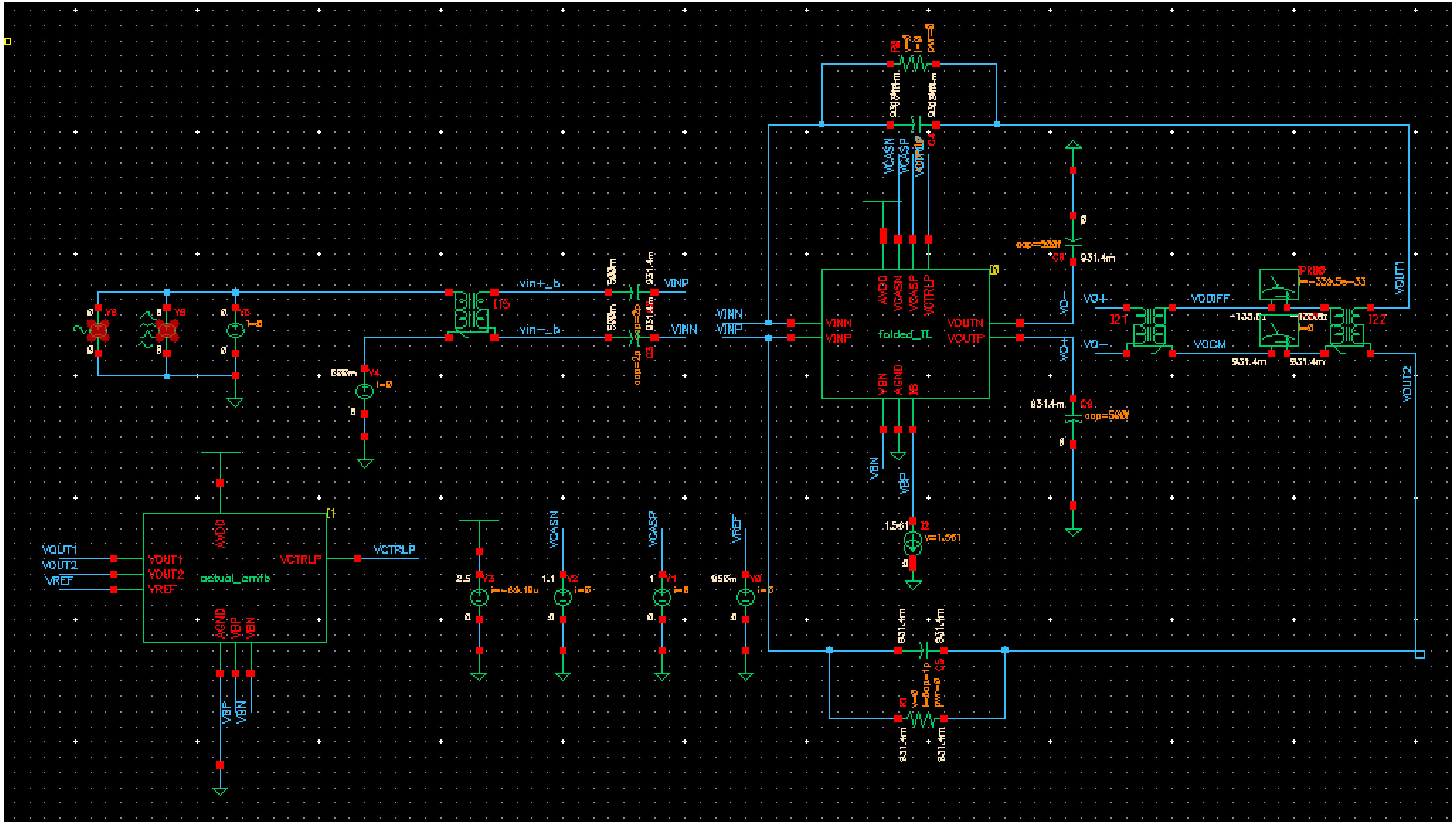

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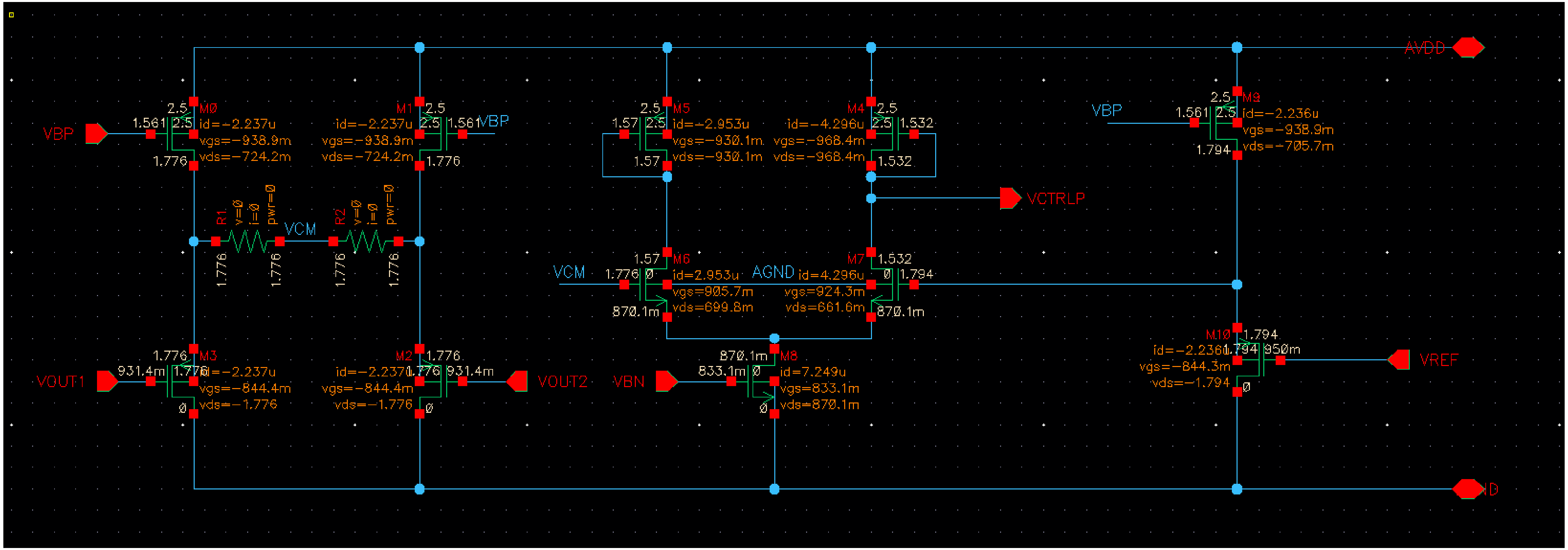


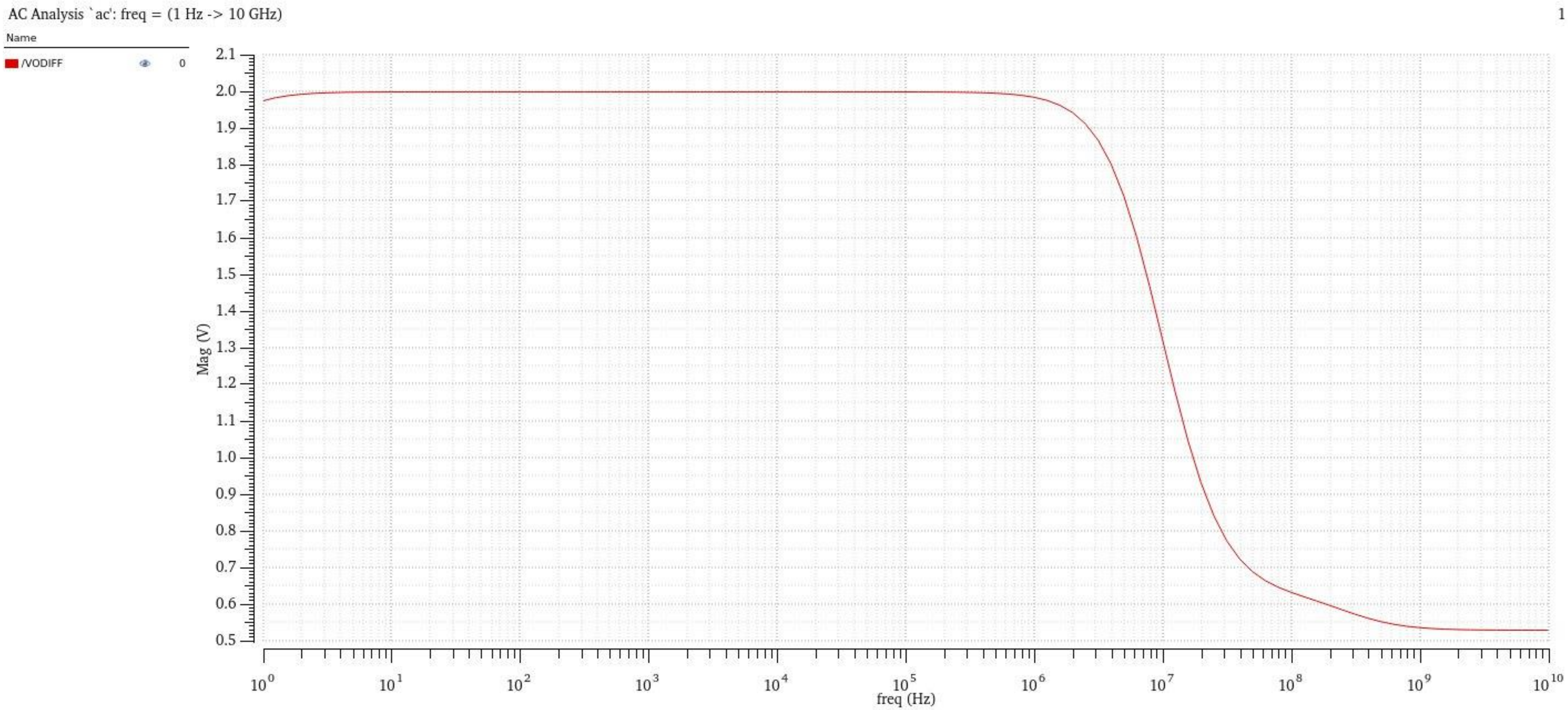
PART 5: Closed Loop Simulation (AC and STB Analysis)

- What is the CM level at the OTA output? Why?
  - $932\ mv\ , as\ the\ cmfb\ network\ works\ at\ making\ vocm = vref\ , but\ the\ appearnt\ error\ is\ due\ to\ the\ low\ gain\ of\ error\ gain$

- What is the CM level at the OTA input? Why?
  - $932mv = Vocm\ , in\ dc\ Cin\ is\ O.C\ , the\ cmfb\ adjust\ Vocm\ and\ Vocm\ adjust\ \ due\ to\ small\ dc\ res. we\ used$, @ low freq it is unity feed back but flipped !

PART 5: Closed Loop Simulation (AC and STB Analysis)

- Plot VODIFF vs frequency



PART 5: Closed Loop Simulation (AC and STB Analysis)

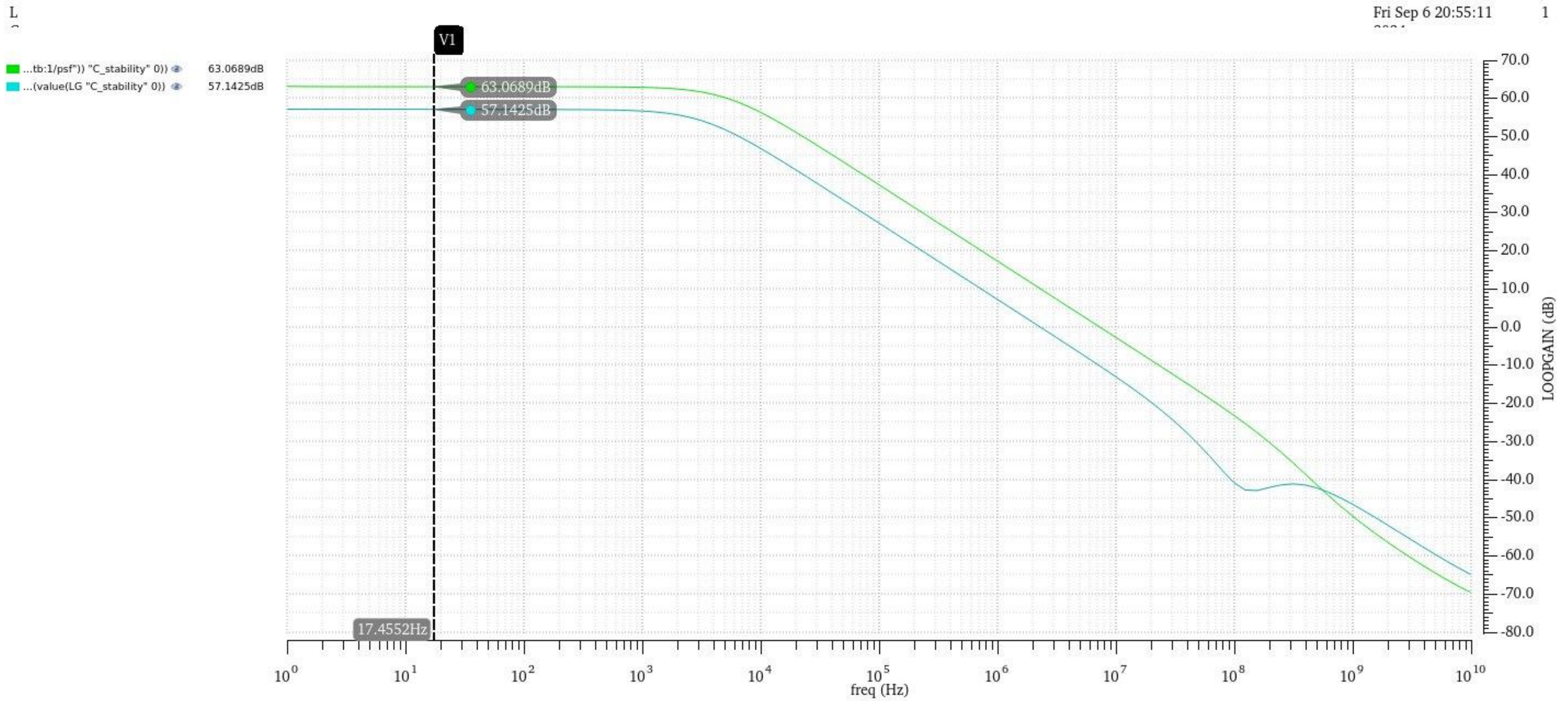
- Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

lab11:part5_tb:1	Acl	1.999			
lab11:part5_tb:1	GBW_cl	17.71M	> 14.4M		pass
lab11:part5_tb:1	BW_cl	8.95M	> 7.16M		pass

PART 5: Closed Loop Simulation (AC and STB Analysis)

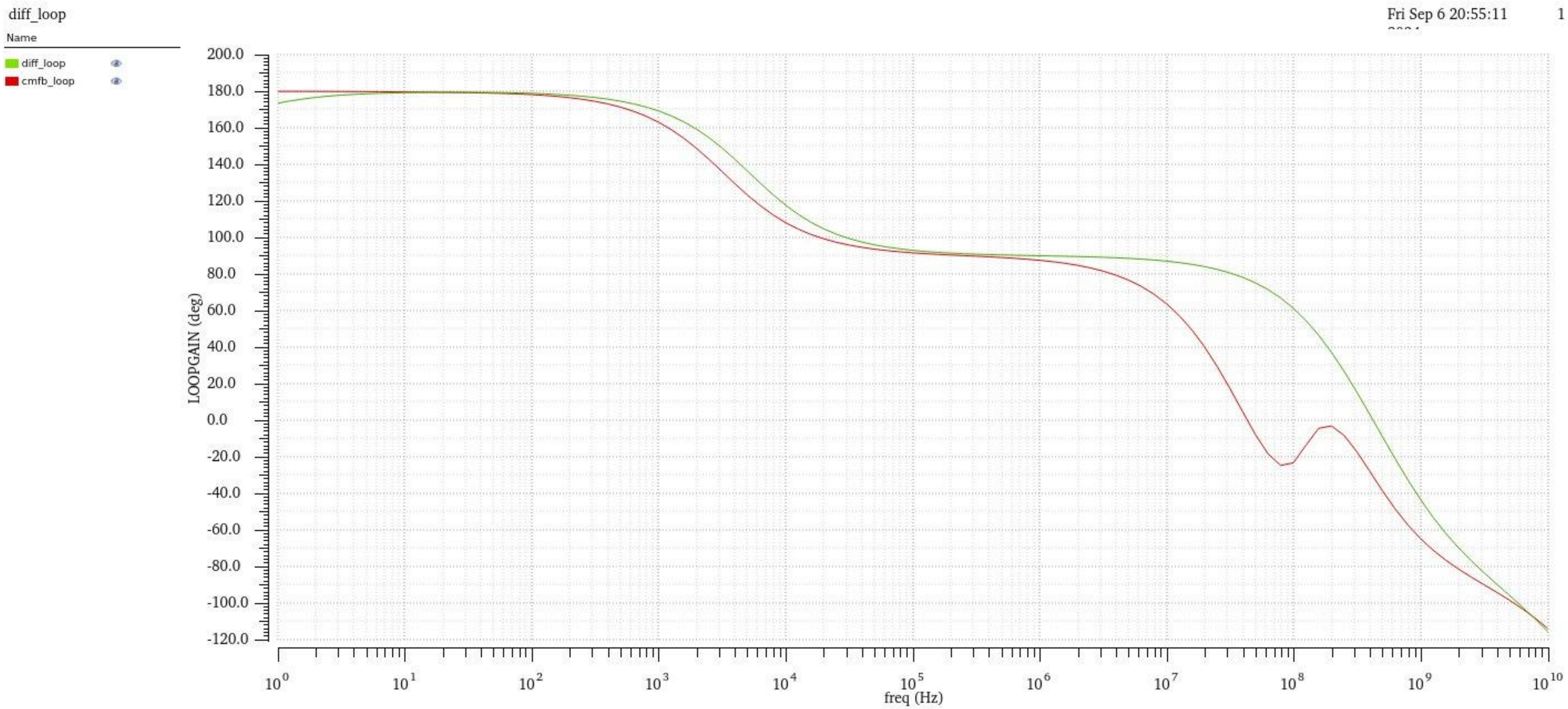
- Plot loop gain in dB and phase vs frequency for the two simulations overlaid.

Diff loop has higher gain



PART 5: Closed Loop Simulation (AC and STB Analysis)

- phase vs frequency for the two simulations overlaid.



PART 5: Closed Loop Simulation (AC and STB Analysis)

- Compare GBW and PM of diff and CM loops. Comment.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:part5_tb:1	cmfb_LG_PM	83.84			
lab11:part5_tb:1	cmfb_LG				
lab11:part5_tb:1	cmfb_GBW_LG	2.323M			
lab11:part5_tb:1	cmfb_DC loop gain	722.6			

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:part5_tb:1	diff_LG_PM	87.82			
lab11:part5_tb:1	diff_LG				
lab11:part5_tb:1	diff_GBW_LG	7.381M			
lab11:part5_tb:1	diff_DC loop gain	1.44k			

- $PM\ of\ diff\ loop\ is\ higher \quad \Rightarrow\ More\ stable$

- $BW_{cmfb} = \frac{GBW_{cmfb}}{DC\ gain\ \_cmfb} = 3215hz$

$$BW_{diff} = \frac{GBW_{diff}}{DC\ gain\ \_diff} = 5125$$

$$t_{diff} = 0.62\ t_{cmfb} \Rightarrow \boldsymbol{diff\ loop\ is\ faster}$$

PART 5: Closed Loop Simulation (AC and STB Analysis)

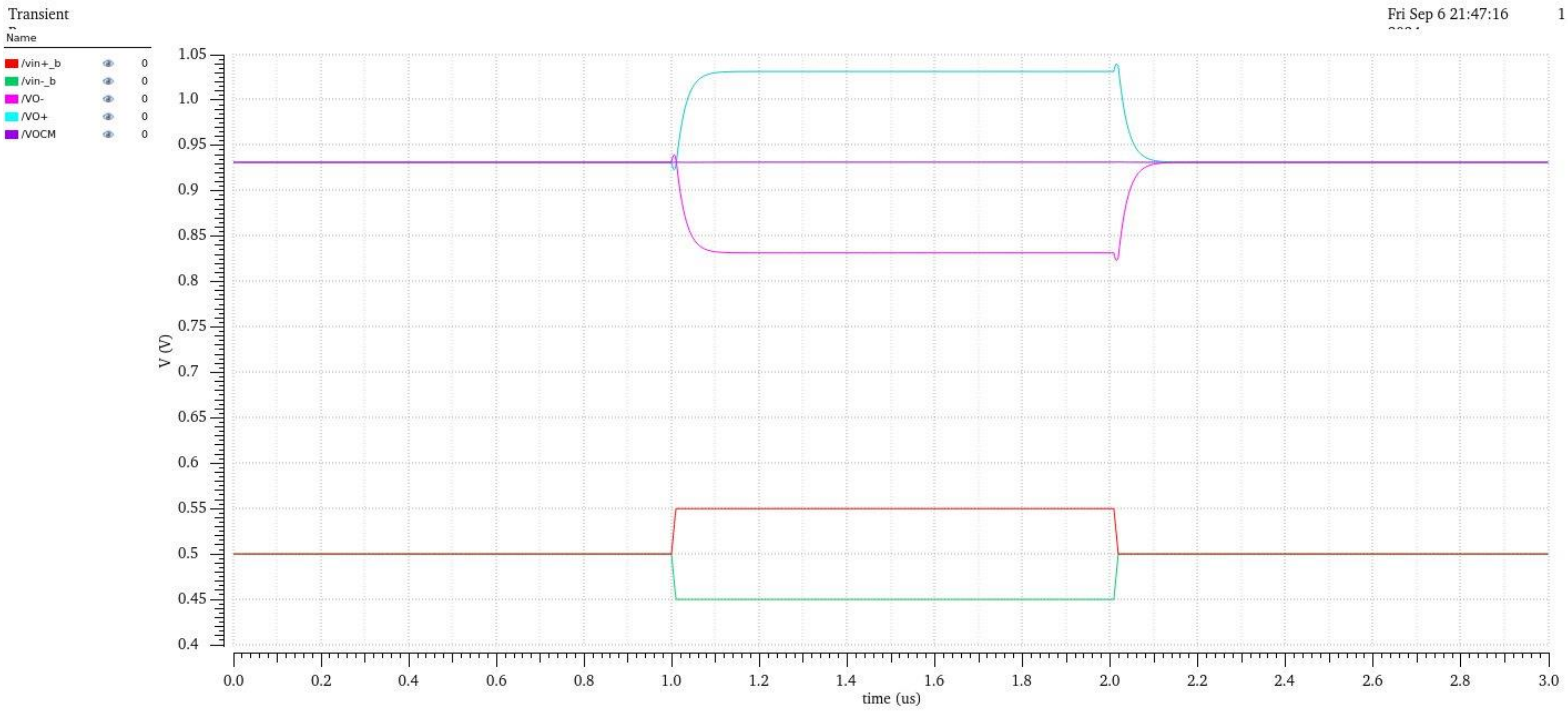
- Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment

	Open loop (B=1)	LG IN Closed loop(B=1/5)
Dc loop gain	6.7 K	1.4K
GBW	54 Mhz	7.4 M hz

- $Closing\ the\ loop\ gives\ us$
- $cout = \ Cl + Cf(1-B)\ \uparrow\uparrow GBW\ \downarrow\downarrow$
- $LG\ = B * Aol\ => \ B\ = \frac{Cf}{Cf+Cs+cself} = \frac{1}{4}$
- $GX = \ B * \ GBW\_ol$
- Closing the loop decreased the GBW and DC loop gain.

PART 6: Closed Loop Simulation (Transient Analysis)

- ❑Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid



PART 6: Closed Loop Simulation (Transient Analysis)

❑ Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

- No , just coupling , yes both are stable with adequate PM.

❑ Calculate the 1% settling time and compare it to the required specification.

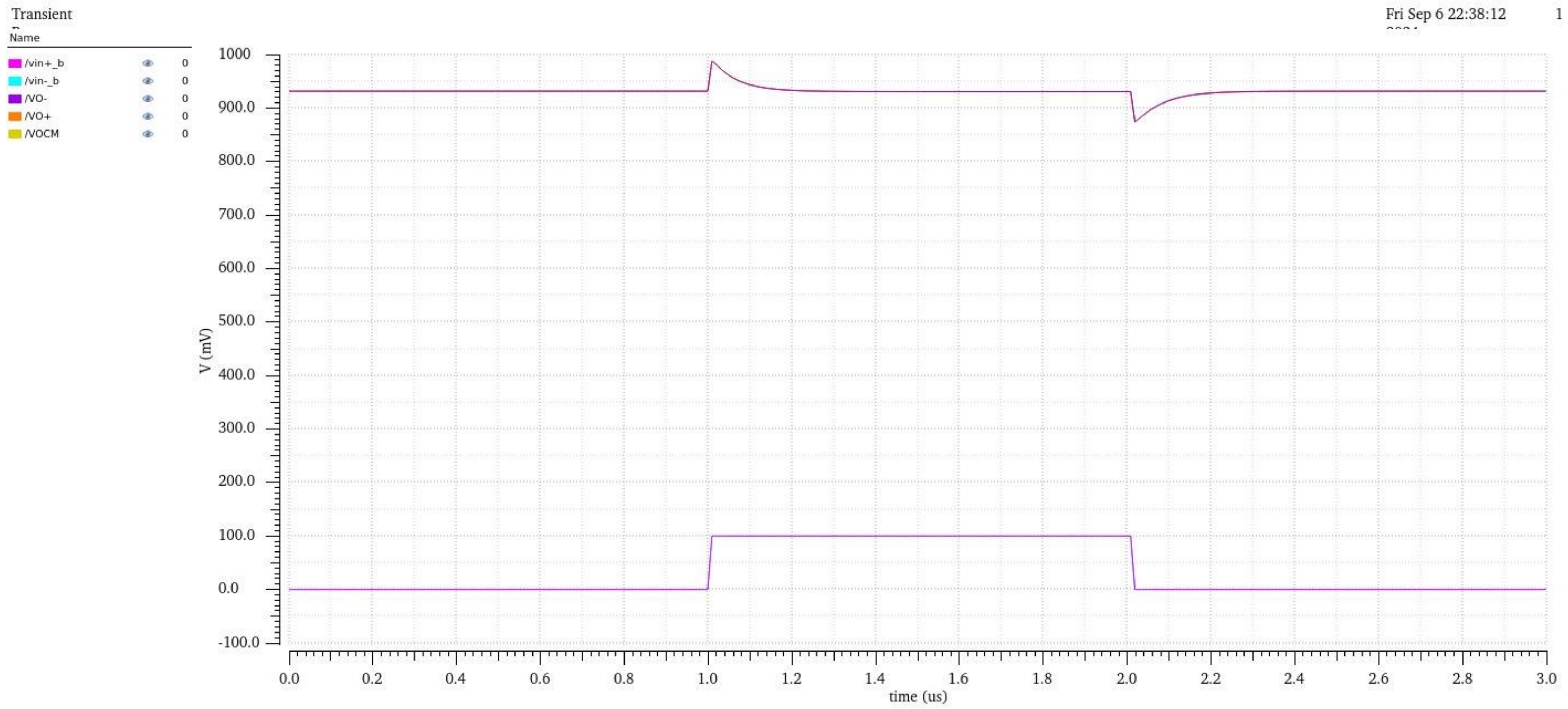
Test	Output	Nominal	Spec	Weight	Pass/Fail
lab11:part5_tb:1	/vin+_b				
lab11:part5_tb:1	/vin-_b				
lab11:part5_tb:1	/VO-				
lab11:part5_tb:1	/VO+				
lab11:part5_tb:1	/VOCM				
lab11:part5_tb:1	riseTime(v("/VODIFF" ?result "tr...	94.89n			

	spec	achieved
Rise time	100n	94n

❑ If the specification was not satisfied , what design changes could be a possible solution? Increase gm of input pair

PART 6: Closed Loop Simulation (Transient Analysis)

- ❑Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid



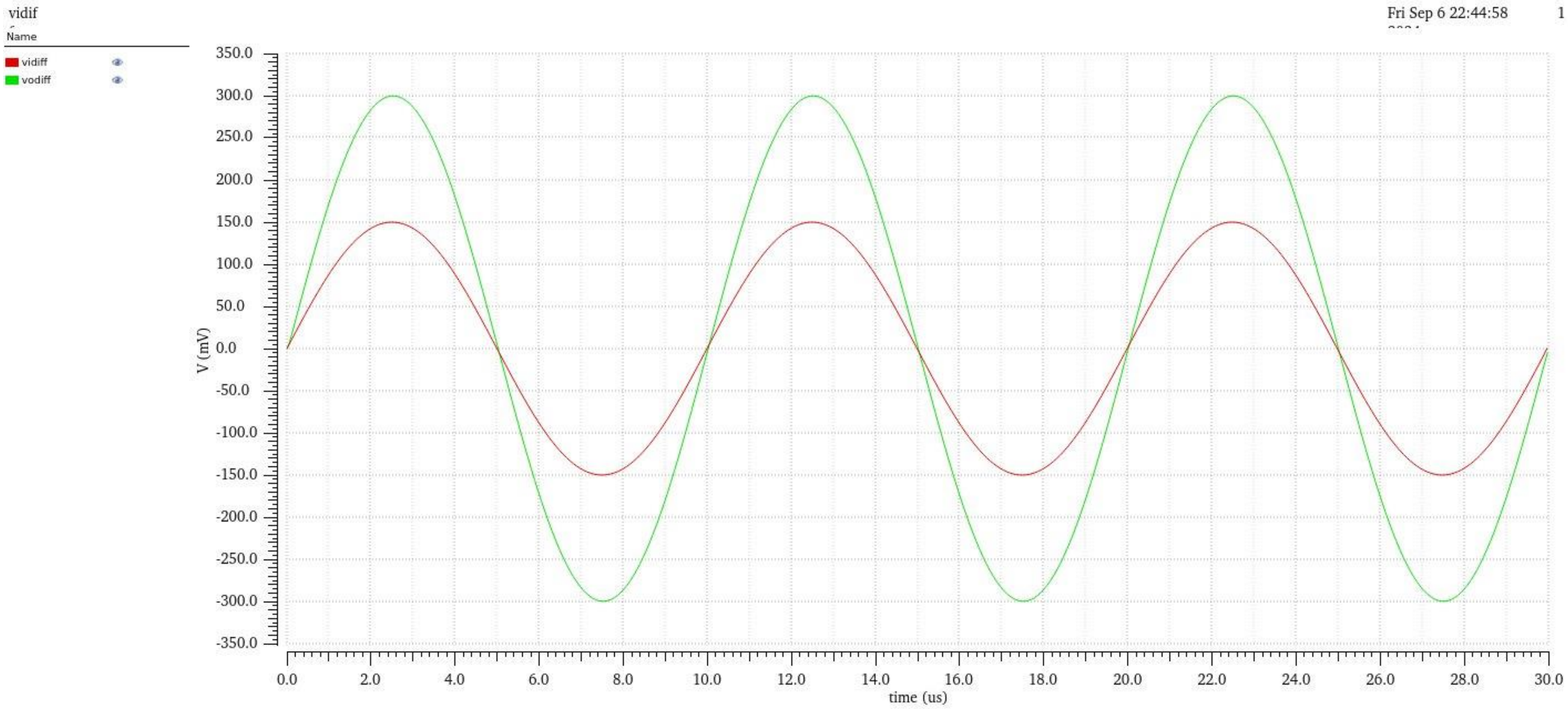
PART 6: Closed Loop Simulation (Transient Analysis)

- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

- No , just coupling , yes both are stable with adequate PM.

PART 6: Closed Loop Simulation (Transient Analysis)

❑Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.



PART 6: Closed Loop Simulation (Transient Analysis)

❑ Calculate the diff input and output peak-to-peak swings and the closed loop gain.

lab11:part5_tb:1	vid				
lab11:part5_tb:1	vod				
lab11:part5_tb:1	pp_vod	599.5m			
lab11:part5_tb:1	pp_vid	300m			
lab11:part5_tb:1	clgain	1.999			

PART 6: Closed Loop Simulation (Transient Analysis)

❑Swing spec