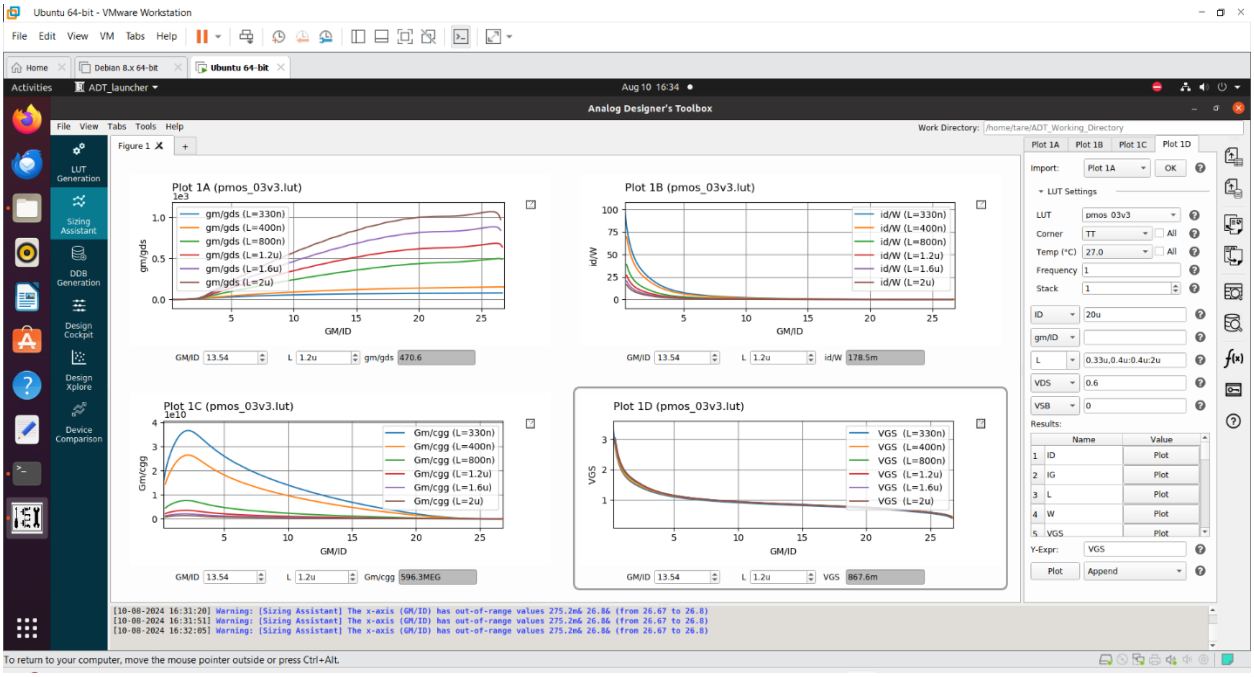
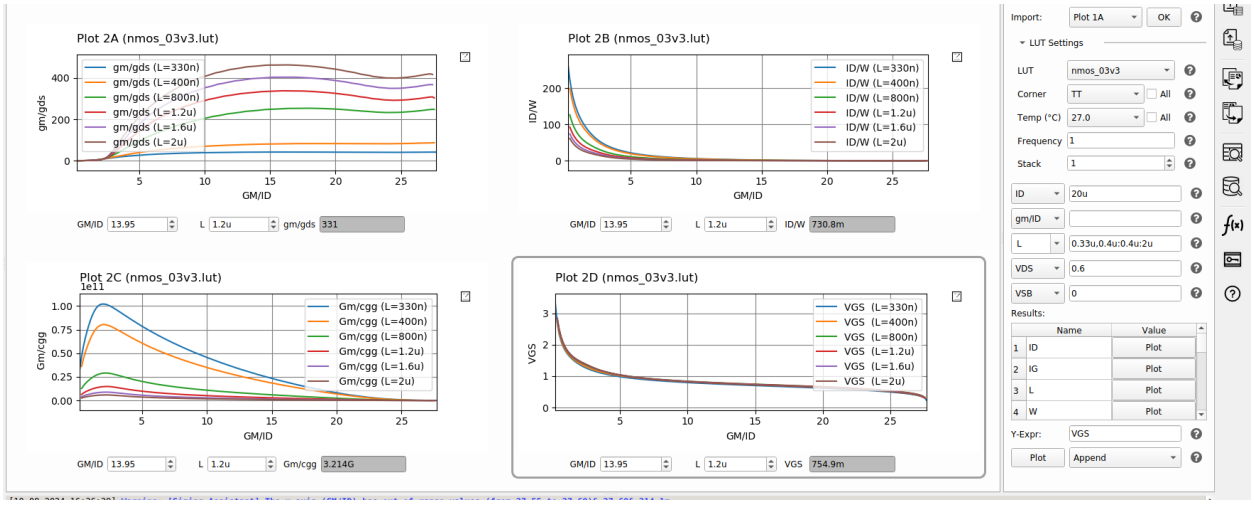
Lab 7

1- plot the following design charts vs gm/ID for PMOS



2- plot the following design charts vs gm/ID for NMOS



3- Detailed design procedure and hand analysis.

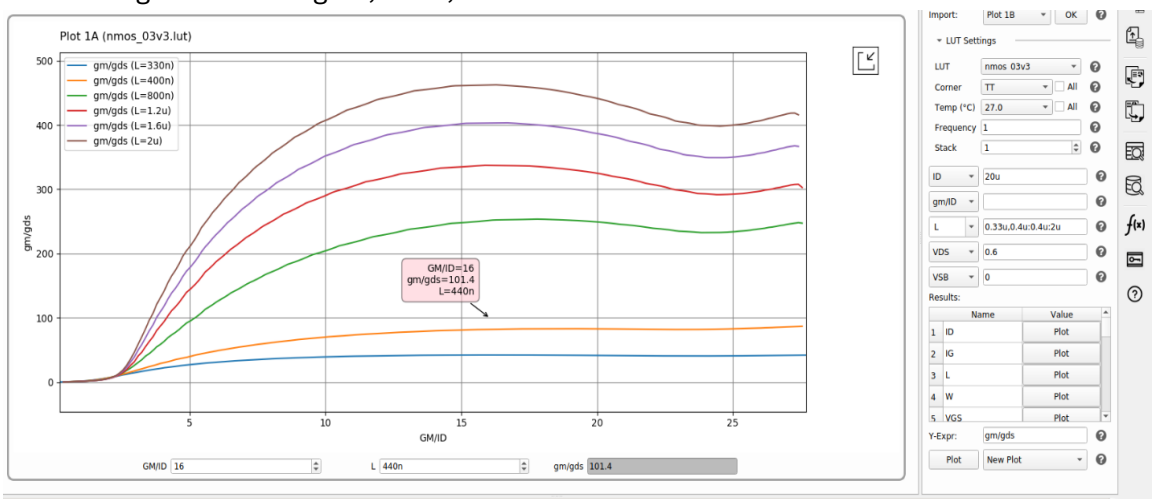
3.1 Input pairs :

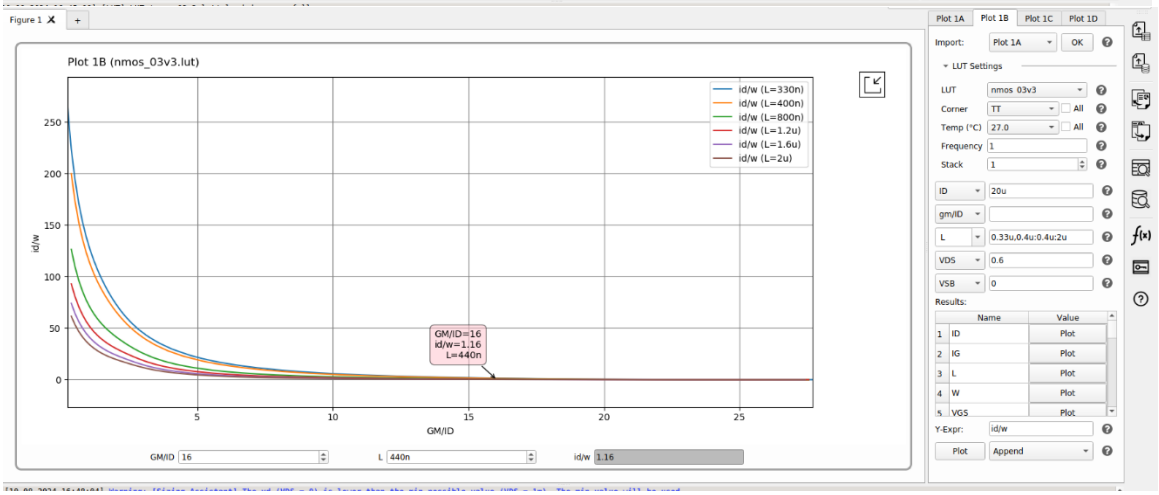
:: From GBW condition => gm=314 us

:: Let gm/id =16 “gain related”

Then Id=20 uA:

:: Assuming ro2=ro4 ==> gm1,2*ro1,2>=100





- **L1,2 =440 n**
- **W1,2 =w/id *id=17.24 u**

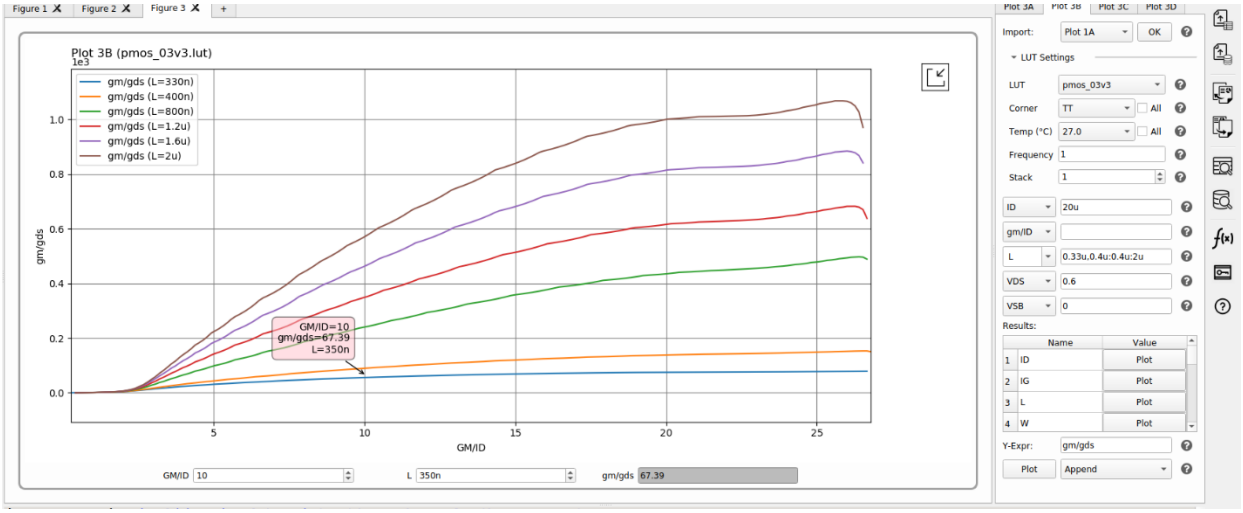
Input Pairs	
W	**17.24 u**
L	**440 n**
Gm	**314 us**
ID	**20 uA**
Gm/id	**16**
Vdsat	**98.6 mv**
Vov	**24 mv**
V*	**125.1 mv**

3.2 CM load :

Condition : gds< 3.14

Let gm/id =10 => 200 Then :: Gm/gd >= 63.7

Getting length ::

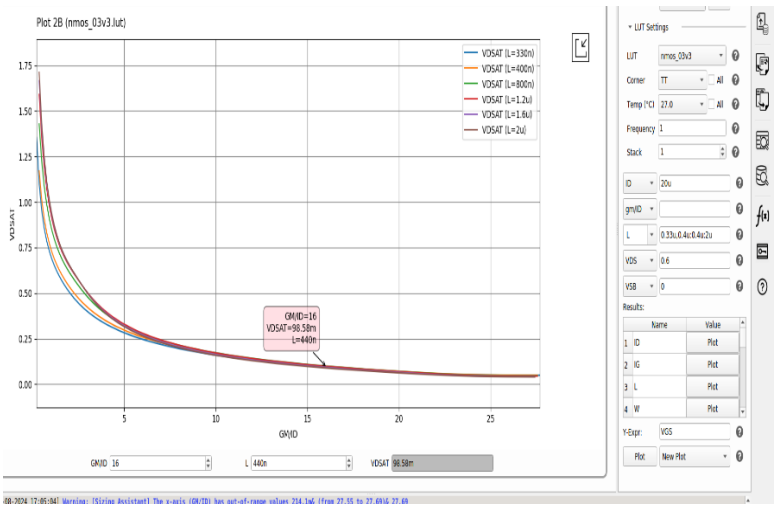


:: L=350 n

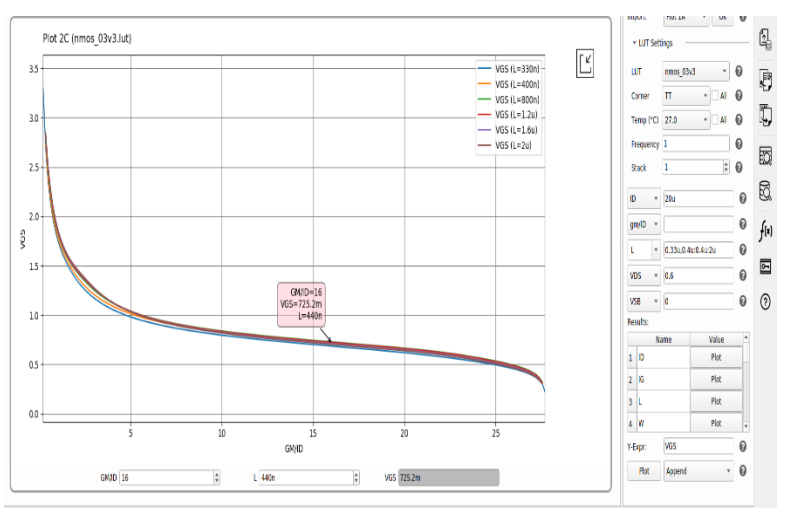
Getting gm/id Valid Range ::

Vgs3.4 >= vin,max + VDsat1,2 -VGS1,2

:: Getting VGS 1,2 and VDsat1,2



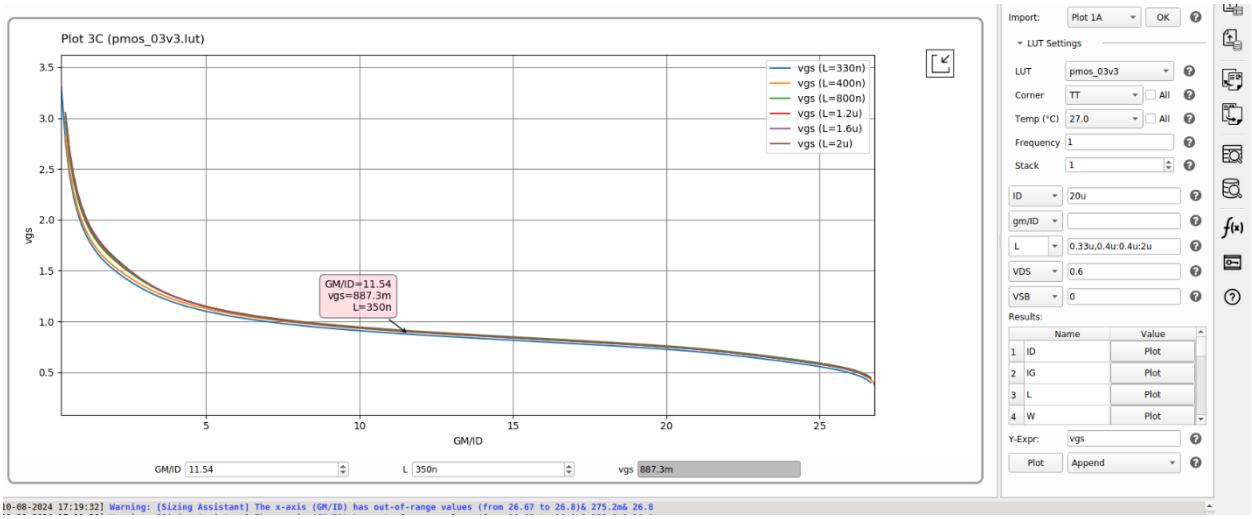
Vdsat1,2=98.6 mv



VGS1,2=725 mv

:: SO VGS3.4 >=0.873 V

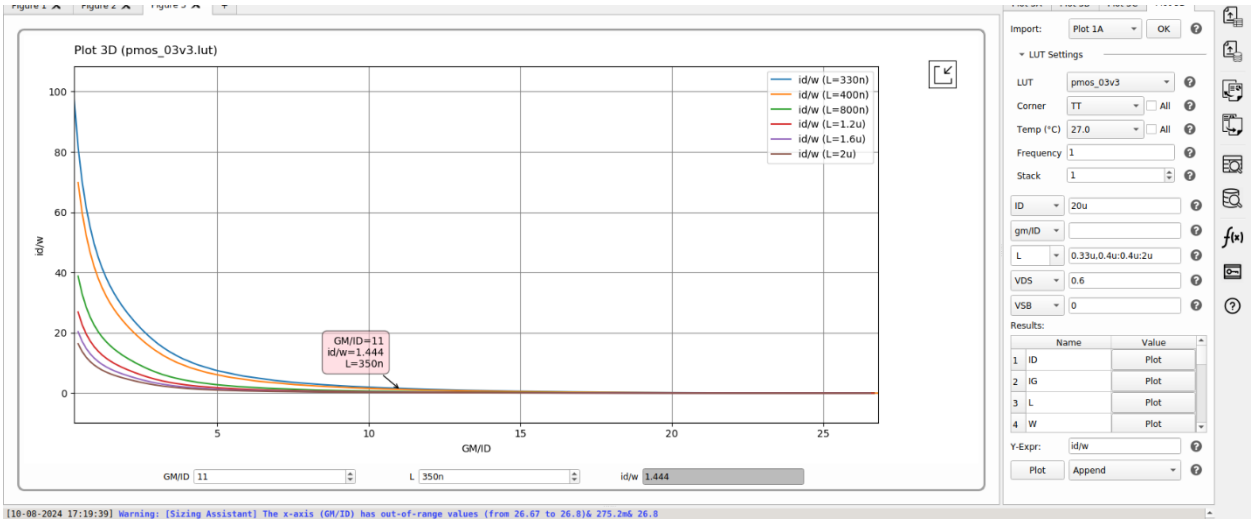
:: Getting gm/id range



:: Gm/id Must be smaller than 11.5

Taking gm/id = 11 => to be deeper into sat.

:: Getting W



:: W= (w/id)* id =13.8 u

CM load	
W	13.8 u
L	350 n
Gm	220 us
ID	20 uA
Gm/id	11
Vdsat	161 mv
Vov	132 mv
V*	182 mv

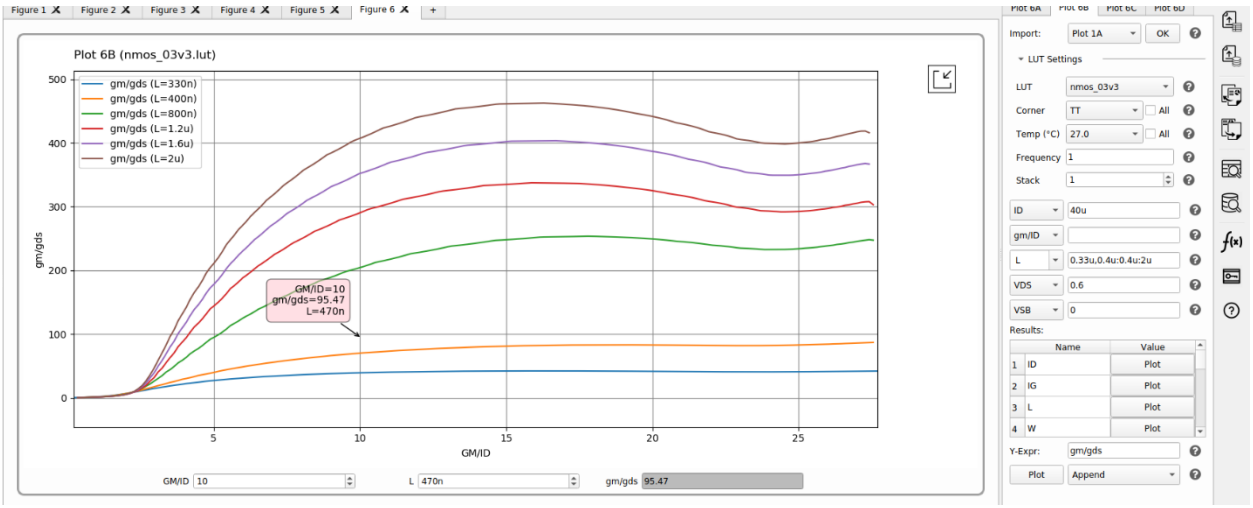
3.3 Current Mirror

:: Id=40 uA

:: AVcm < 0.01 ➔ 1/2gm3,4*ro5 <0.01

ro5< 227.3 k => gds5 < 4.4 us :: let gm/id =10 :: Id=40 uA => gm5=400 us

:: gm/gds > 91 => Getting L

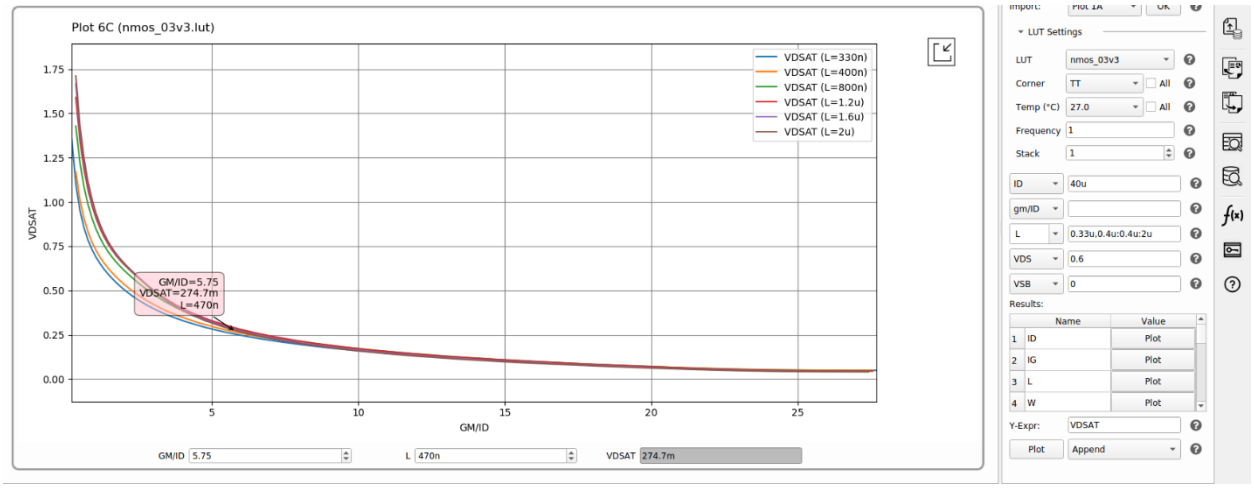


::L=470 n

Getting real gm/id Range ::

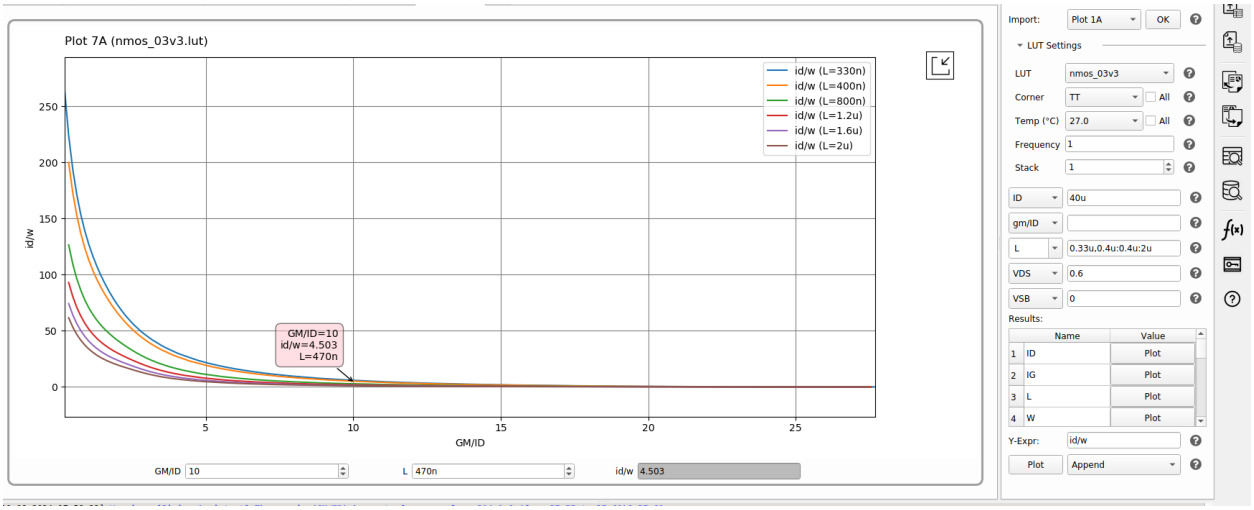
Vin min – Vgs1,2 – Vdsat 5 >=0

VGS1,2 = 725 mv and Vin,min= 1v ➔ VDsat5 <= 275 mv



Gm/id > 5.75 ➔ Take gm/id = 10

:: Getting W5



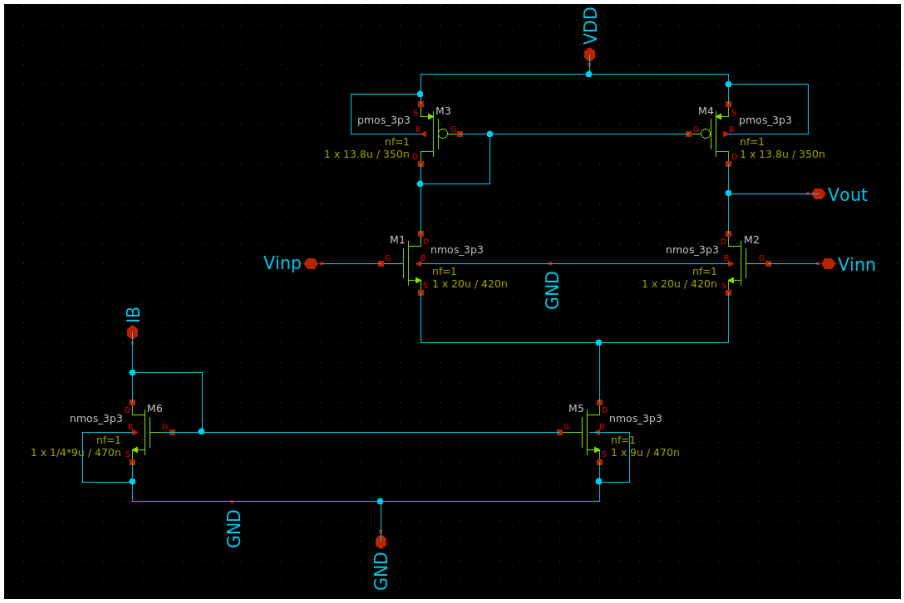
::W =8.9 u

CM load	
W	8.9 u
L	470 n
Gm	400 us
ID	40 uA
Gm/id	10
Vdsat	201 mv
Vov	134 mv
V*	201 mv

M6 :

Same as M5 but width = w5 *1/4

4- Schematic of the OTA showing sizing of the transistors: after tuning




```
gbw = 1.002608e+07
 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
      model           nmos_3p3.8           nmos_3p3.8          pmos_3p3.12
         gm          0.00010318          0.000389433           0.00021717
       gmbs          3.50075e-05          0.000135275          8.4263e-05
        gds          8.74141e-07          5.25056e-06          2.46721e-06
        vds             0.838493             0.419962             0.893454
      vdsat             0.170836             0.165833             0.156161
        vgs             0.838499             0.838499             0.893456
        vth             0.702339             0.709572              0.76832
         id                1e-05          3.83581e-05          1.91791e-05
        cgd          2.39224e-18          -5.01895e-18          3.87522e-17
        cdb         -3.17358e-16          -1.25786e-15         -1.96251e-15

 BSIM4v5: Berkeley Short Channel IGFET Model-4
     device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
      model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
         gm           0.00021717          0.000321291          0.000321291
       gmbs          8.4263e-05          8.35871e-05          8.35871e-05
        gds          2.46721e-06          3.72088e-06          3.72088e-06
        vds             0.893454             0.486567             0.486567
      vdsat             0.156161            0.0932733            0.0932733
        vgs             0.893456             0.830026             0.830026
        vth              0.76832             0.821073             0.821073
         id          1.91791e-05          1.91791e-05          1.91791e-05
        cgd          3.87522e-17          2.52206e-17          2.52206e-17
        cdb         -1.96251e-15          -1.12124e-15         -1.12124e-15

binary raw file "OTA_TB.raw"
```

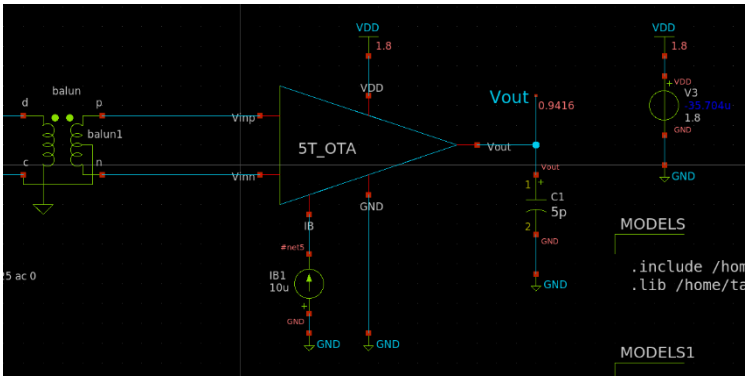
- Is current (and gm) in the input pair exactly equal?

⇨ Yes

- What is DC voltage at VOUT? Why?

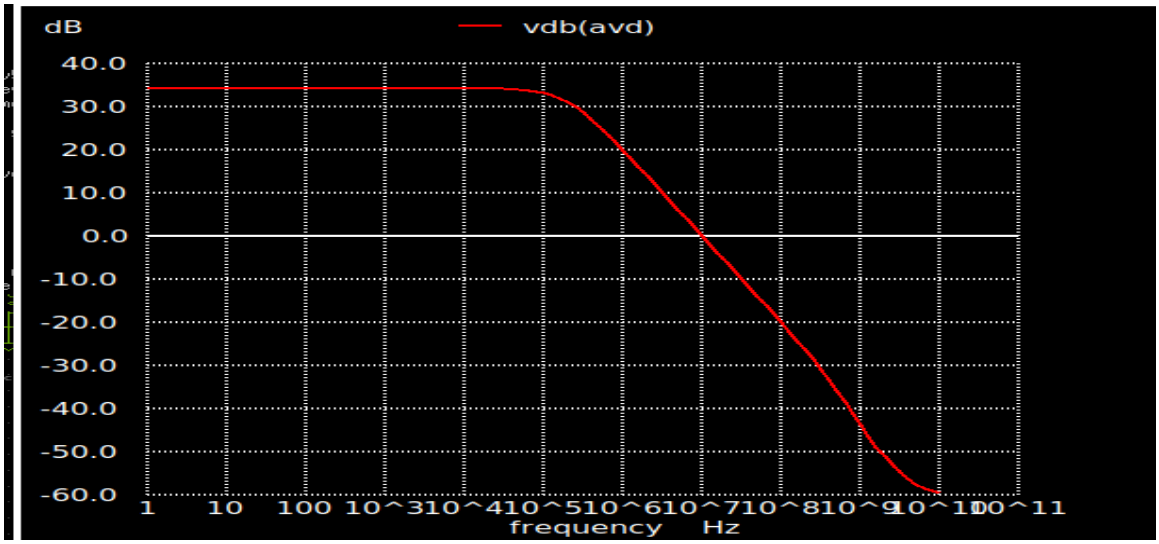
⇨ 0.94

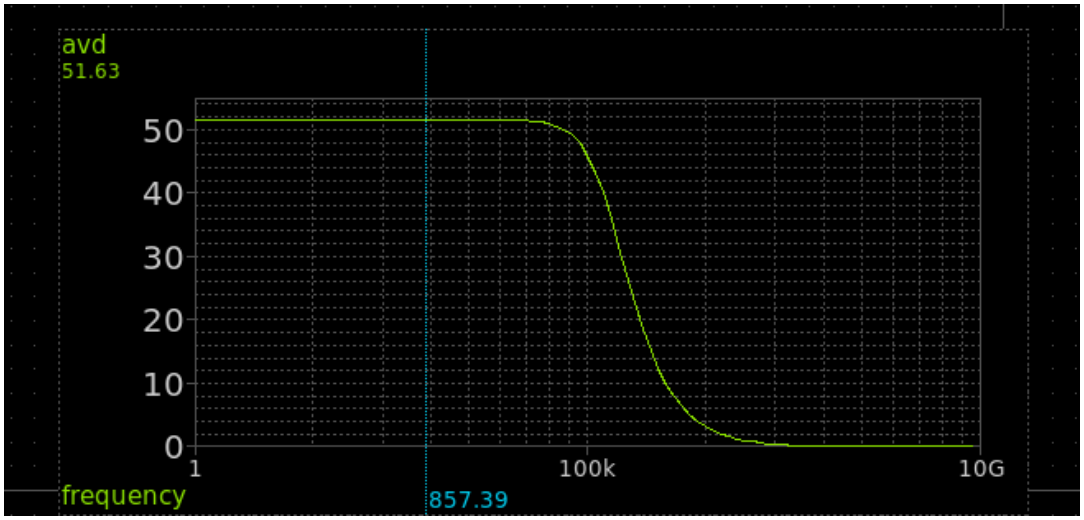
⇨ At Vid =0 Vout follows Vf mirror node =VDD-VGS3,4 = 0.9 V



5- Diff small signal ccs:

Plot diff gain (in dB) vs frequency.

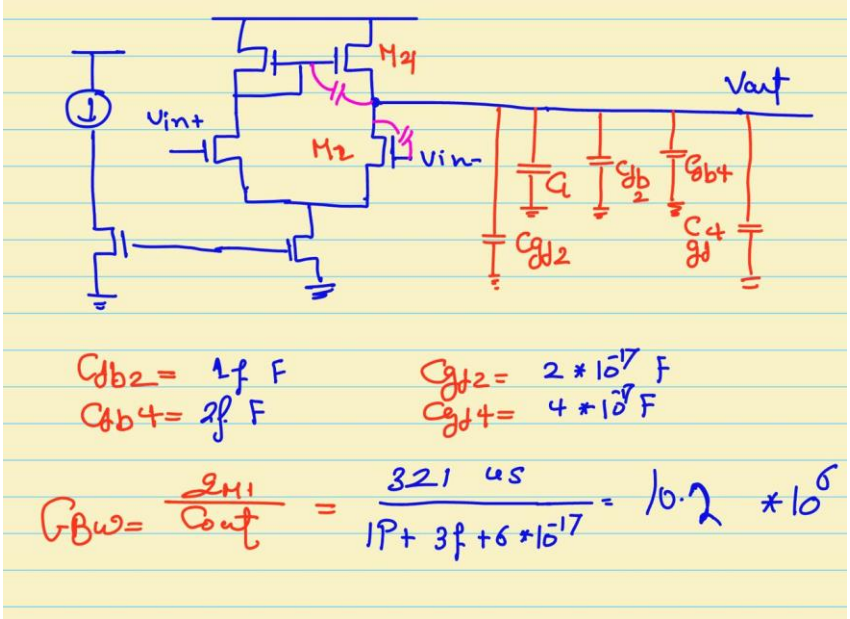





```
f2                    =  1.942043e+05
peak = 5.162645e+01
f2 = 1.942043e+05
gbw = 1.002608e+07
 BSIM4v5: Berkeley Short Channel IGFET Model-4
```

• **Compare simulation results with hand calculations in a table.**

	Simulation	Hand analysis
Avd	51.6	Gain=gm1*(ro2//ro4)=52
GBW	10 Mhz	Gbw =gm1/cout=10.2 Mhz

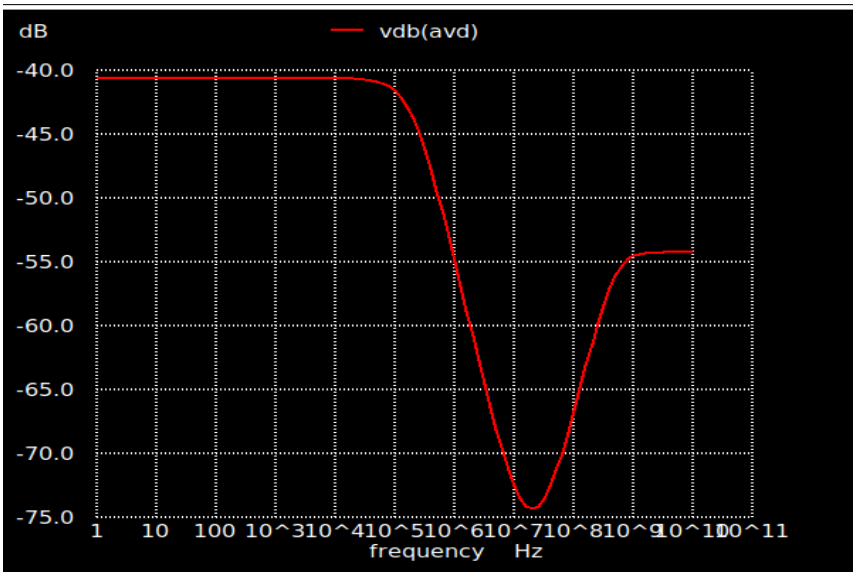


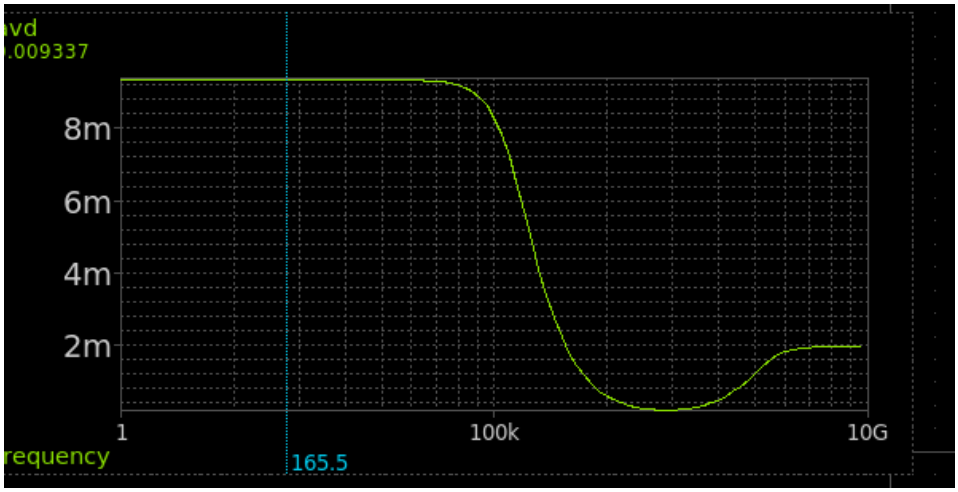
- **gm1=321 us**
- **gm2=321 us**
- **gds2=3.72 us**
- **gds4=2.46 us**

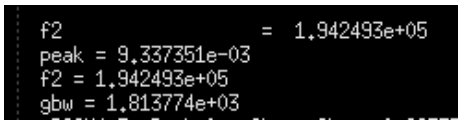
- **Hand analysis are higher**

6- CM small signal ccs:

- Plot CM gain in dB vs frequency.
- **Compare simulation results with hand calculations in a table.**







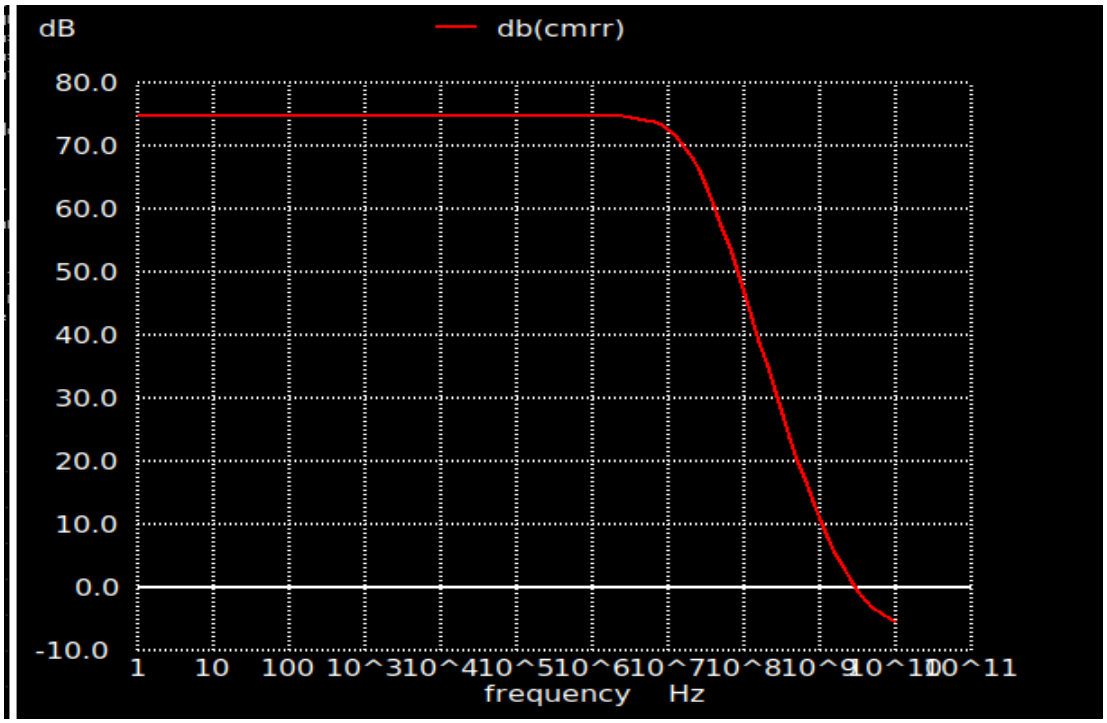
	Simulation	Hand analysis
Avd	9 * 10^-3	1/(2gm3,4 *1/gds5)=12 * 10^-3

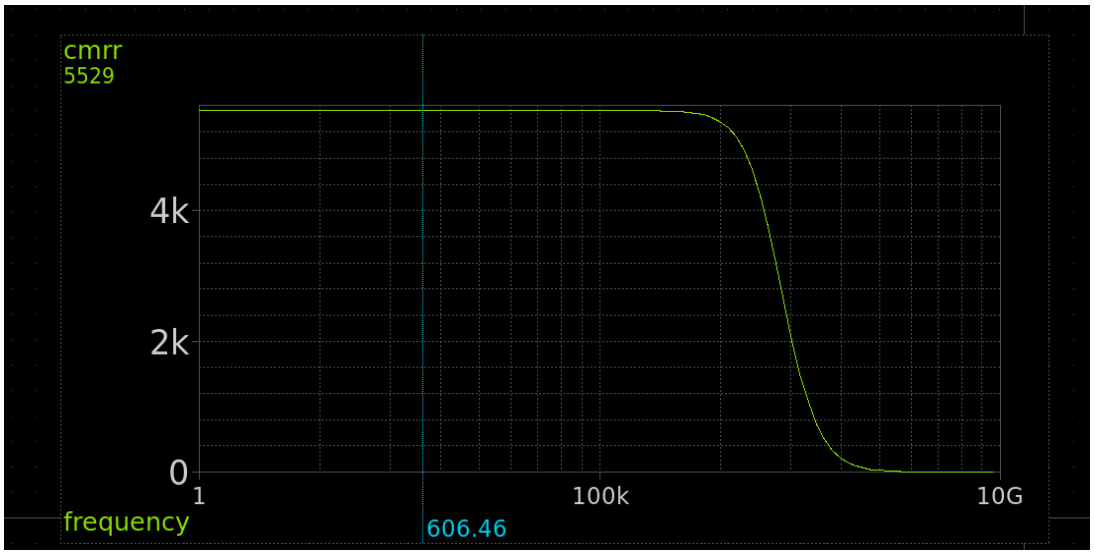
- ⇨ **gm3,4=217 us**
- ⇨ **gds5=5.25 us**

:: Hand analysis are higher

7- CMRR:.

- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.
- **Compare simulation results with hand calculations in a table**



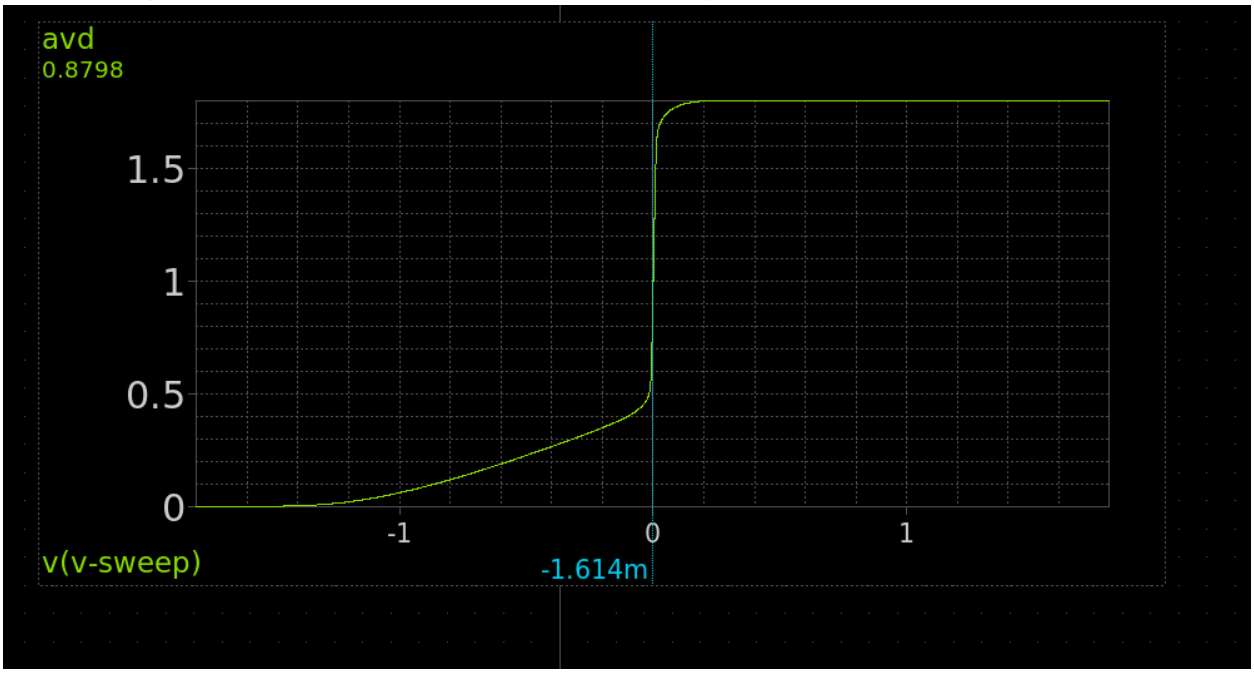


	Simulation	Hnad analysis
CMRR	**5529 (74.8 db)**	**gm1,2(gds2+gds4)^-1*2gm3,4(1/gds5)=5200 (74.32 db)**

::Hand analysis are smaller

8- large signal ccs:.

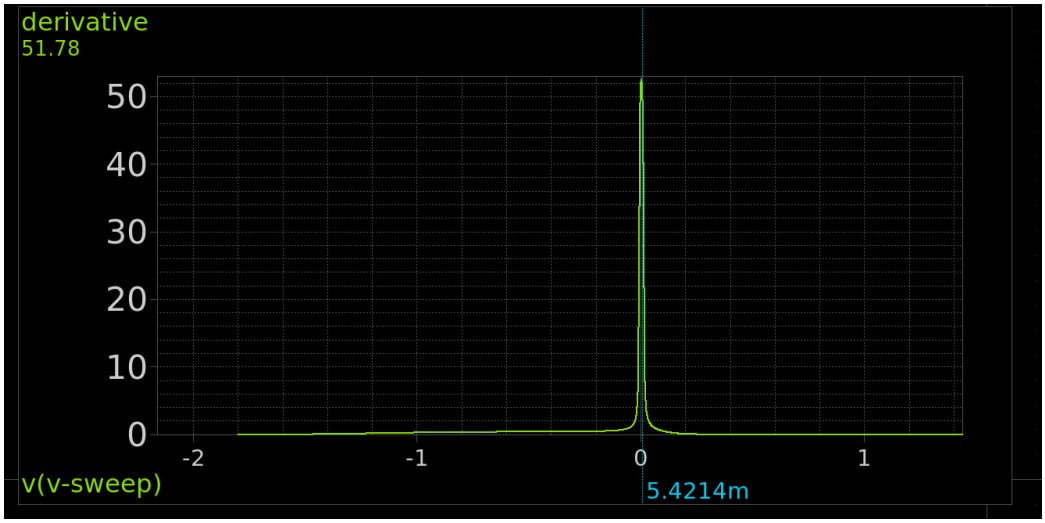
- Plot VOUT vs VID.
- From the plot, what is the value of Vout at VID = 0? Why?



:: Vout @ VID=0 follow VF = VDD-VGS3,4 = 0.9 v

4	W	13.85u
5	VGS	898.4m
6	VDS	600m

- **Plot the derivative of VOUT vs VID. Compare the peak with Avd.**


derivative
51.78
50
40
30
20
10
0
-2
-1
0
1
v(v-sweep)
5.4214m

9- (Optional) CM large signal ccs (GBW vs VICM):
   - Use AC analysis (1Hz, 1 point only).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use parametric sweep (not DC sweep) VICM = 0:10m:VDD.

10- PART 4: Closed-Loop OTA Simulation

Is the current (and gm) in the input pair exactly equal? Why?

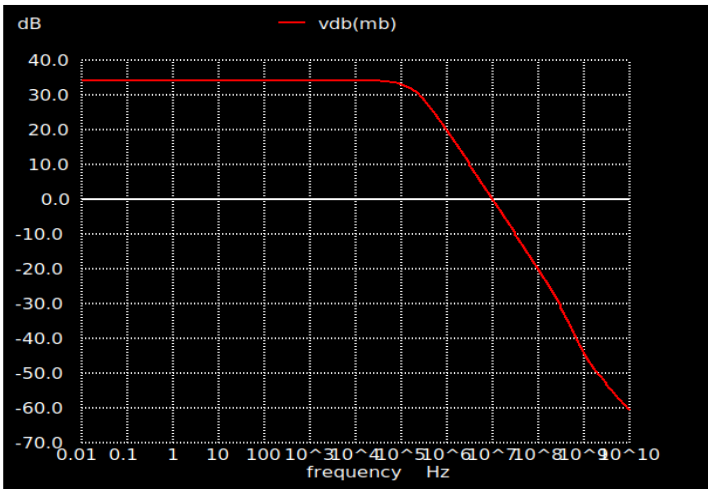
⇨ **No , as Vid is not zero due to error , so there is some sort of steering**

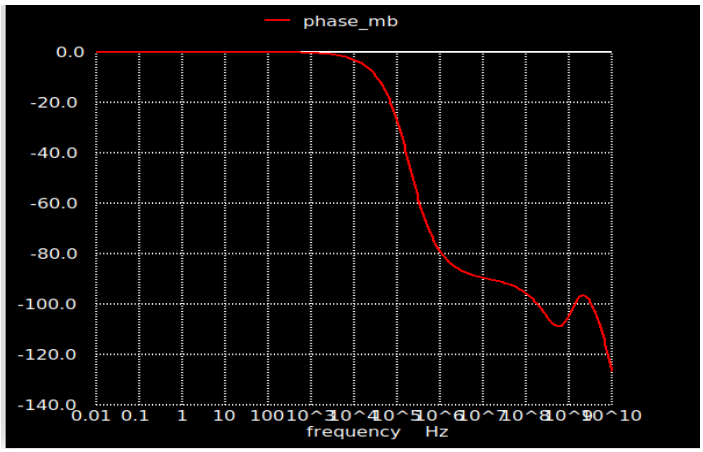
Calculate the mismatch in Id and gm.

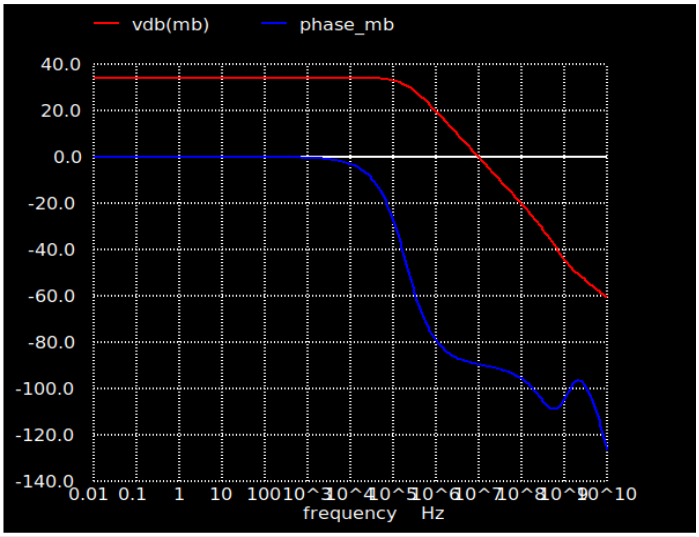
```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
     model           nmos_3p3.8           nmos_3p3.8          pmos_3p3.12
        gm          0.000100318          0.000374961          0.000211154
      gmbs          3.50075e-05          0.000130316          8.20081e-05
       gds          8.74141e-07          1.15746e-05          2.56163e-06
       vds             0.838493             0.264806             0.752517
     vdsat             0.170836             0.165643             0.154269
       vgs             0.838499             0.838499             0.891638
       vth             0.702339             0.709843             0.769038
        id                1e-05          3.72181e-05          1.84358e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
     model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
        gm          0.000214404           0.0003122          0.000316671
      gmbs          8.31828e-05          8.74413e-05          8.87246e-05
       gds          2.42776e-06          3.11209e-06          3.31346e-06
       vds             0.891636              0.78266             0.643541
     vdsat             0.154796            0.0903198            0.0912812
       vgs             0.891638             0.782661             0.785182
       vth             0.768329             0.778789             0.779307
        id          1.87823e-05          1.84358e-05          1.87823e-05

gm_mismatch = 4.471590e-06
id_mismatch = 3.465610e-07
binary raw file "OTA_TB.raw"
ngspice 1 -> 
```

11- (2) Loop Gain:

- **Plot loop gain in dB and phase vs frequency. Show the results in the console.**







• Compare DC gain and GBW with those obtained from open-loop simulation. Comment.

```
bw                =  1.917852e+05
pm_deg            =  -8.945972e+01
dominant_pole_f   =  9.818358e+06
loop_gain         =  3.418592e+01
gbw = 9.819989e+06
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

	Open loop	Closed loop
Gain	**34.25 db**	**34.1 db**
GBW	**10 meg**	**9.8 Mhz**

Comment :: open loop gain is bigger as closed loop gain is $\frac{A_{OL}}{A_{OL}\beta+1}$

• Show the operating point at VICM in the middle of the CMIR.

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm4.m0
     model           nmos_3p3.8           nmos_3p3.8          pmos_3p3.12
        gm         0.000100272          0.000398574          0.000218495
      gmbs         3.49949e-05          0.000138468           8.5024e-05
       gds         8.70549e-07          5.70936e-06           3.127e-06
       vds             0.84498             0.406042            0.553223
     vdsat            0.170918             0.168887                0.16
       vgs            0.844986             0.844986             0.90004
       vth             0.70874             0.711686            0.769795
        id               1e-05          3.99966e-05          1.97373e-05

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x1.xm3.m0          m.x1.xm2.m0          m.x1.xm1.m0
     model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
        gm         0.000224477          0.000315833           0.00032153
      gmbs         8.71153e-05          8.51934e-05          8.67747e-05
       gds         2.57098e-06          2.75171e-06          3.33544e-06
       vds            0.900039             0.840718             0.493902
     vdsat            0.159856            0.0987629             0.100774
       vgs             0.90004              0.84072             0.843946
       vth            0.769988             0.821246             0.820662
        id         2.02593e-05          1.97373e-05          2.02593e-05

ngspice 1 ->
```

- **Compare simulation results (DC gain and GBW) with hand calculations in a table.**

	simulation	hand calculation
DC gain	34.1 db	1*gm1,2(gds2+gds4)^-1=52
GBW	9.8 Mhz	Gbw =gm1/cout=10.2 Mhz

- ⇨ **gm1=321 us**
- ⇨ **gm2=315 us**
- ⇨ **gds2=2.75 us**
- ⇨ **gds4=3.12 us**

::Hand analysis are Bigger