

وَقُلْ رَبِّ زِدْنِي عِلْمًا

Analog CMOS IC Design training @ ITI
Under supervision of Dr.Hesham omran

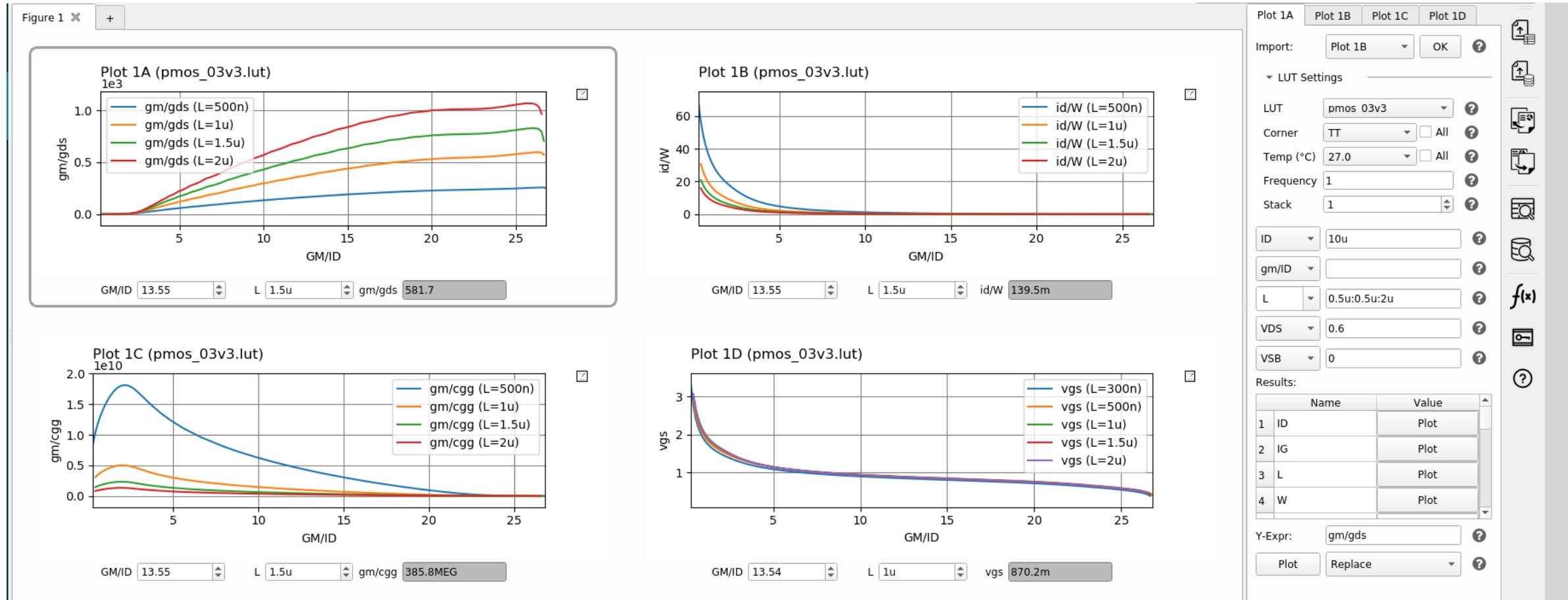
Lab 09 (Mini Project 01)
Two-Stage Miller OTA
Using gm/id Design methodology
Tools : Analog Designer's Toolbox (ADT) + Cadence

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ECE Senior 1 Student @ ASU

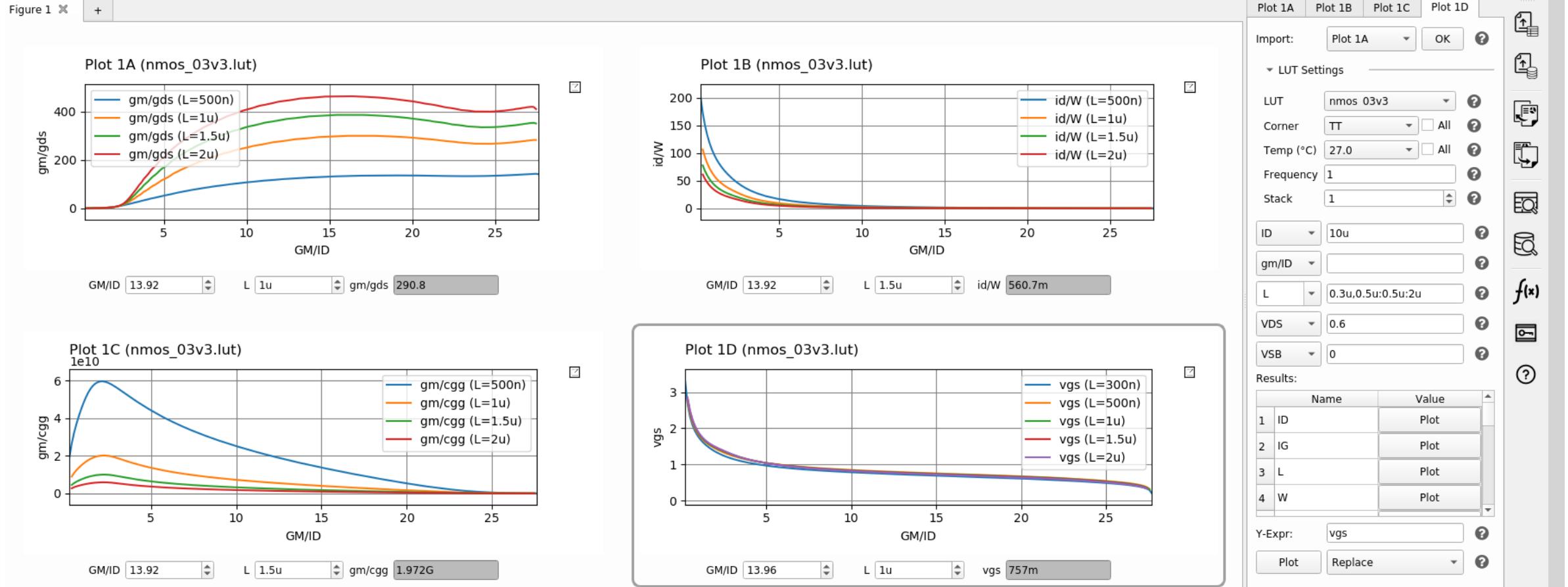
Gm/id Methodology

Pmos



Gm/id Methodology

Nmos



Outline

specifications

- Topology selection
- Hand analysis
- Design of 1st stage input pair
- Design of 1st stage current mirror load
- Design of 1st stage tail current source
- Design of 2nd stage input
- Design of 2nd stage current source
- Offset Removing
- Compensation resistance and capacitance
- Sizing and simulation results

Specs

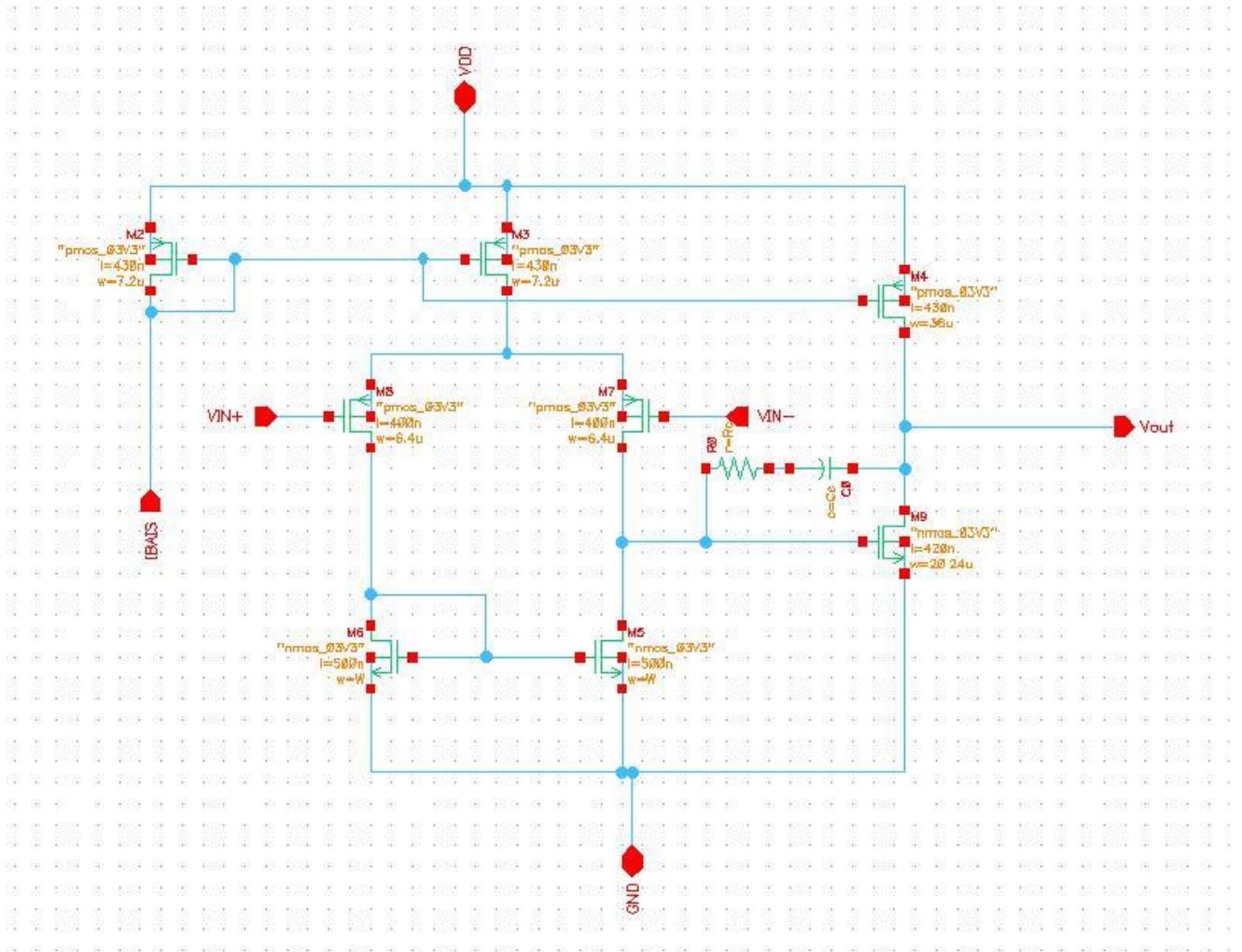
Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	5V/ μ s	5V/ μ s

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Topolgy selection

- Why Pmos input pair
- Due to Low CMIR , Pmos is more happier With Low ranges Than Nmos



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Hand Analysis

□ PM spec $P_m > 70 \Rightarrow \frac{G_{m2}}{C_L} \approx \frac{4G_{m1}}{C_C}$

Let : $C_c = 1.8p \Rightarrow GM_2 = GM_1$, GM_1 and GM_2 are truscon. Of stage 1 and 2

Thus : $G_{M1} = 11G_{M2}$

□ From rise time Spec ($t_{rise} = 2.2\tau$) : $\tau_{CL} = \frac{1}{\omega_{p,CL}} = \frac{A_{CL}}{\omega_u}$
UGF=31.4 rad/s

We know that: $UGf = \frac{G_{M1}}{C_C} \Rightarrow G_{M1} = g_{M8}$

Thus : $g_{M8} >= 62.8 \text{ us} \Rightarrow G_{M2} = g_{M9} >= 628.2 \text{ :: ration must stay constant}$

□ Assuming same gm/id for M8 and M9 $\Rightarrow id(M9) = 10 id(M8)$ margin is only 70

□ $SR >= 5v/\mu s : SR = \frac{I_1}{C_C} \Rightarrow i_1 >= 9 \mu A$

from Power spec : Let $I_1 = 10 \mu s = 2iD(1^{\text{st}} \text{ stage In. pair}) \Rightarrow I_2 = iD(2^{\text{nd}} \text{ stage In.}) = 50 \mu$

Hand Analysis

- $\frac{gm}{id} > 12.56$: for input pairs

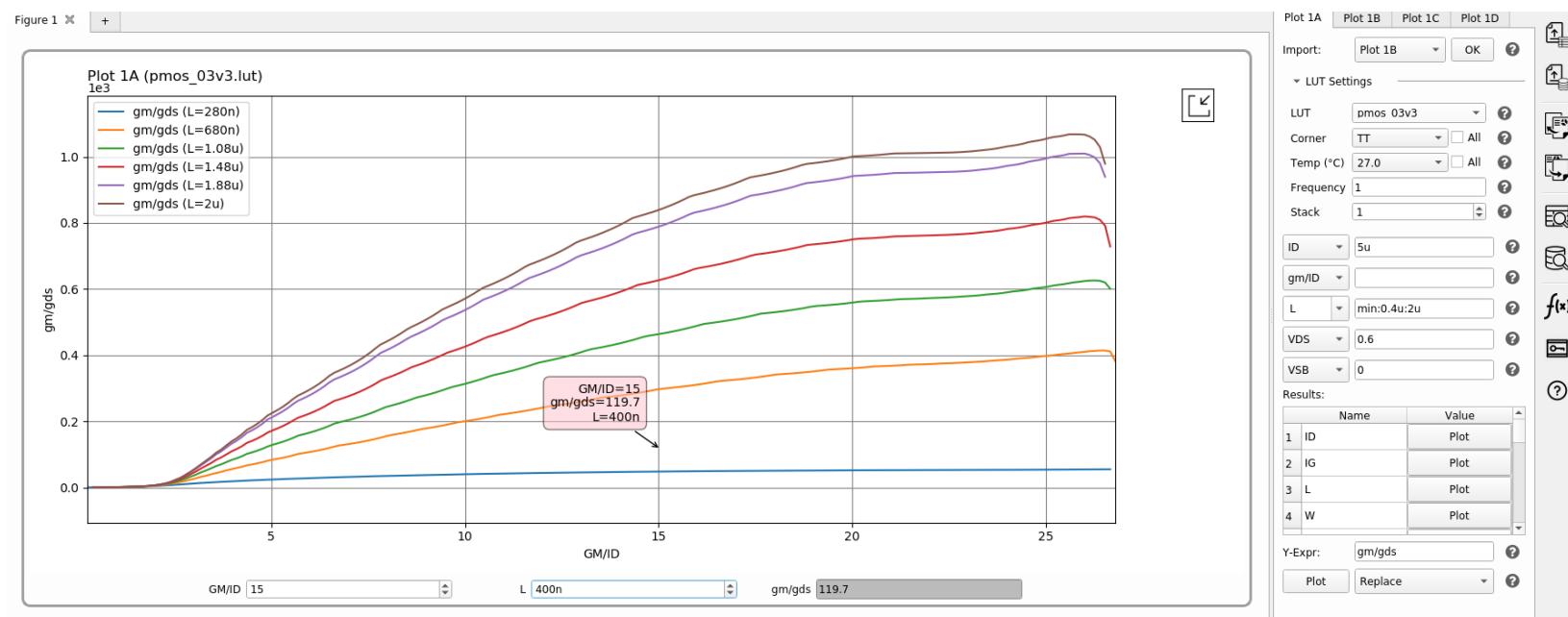
- $Ess < 0.05\% : Ess = \frac{1}{LG}, LG > 2000$
let $Aol1 > 50, Aol2 > 40$

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Design of 1st stage input pair

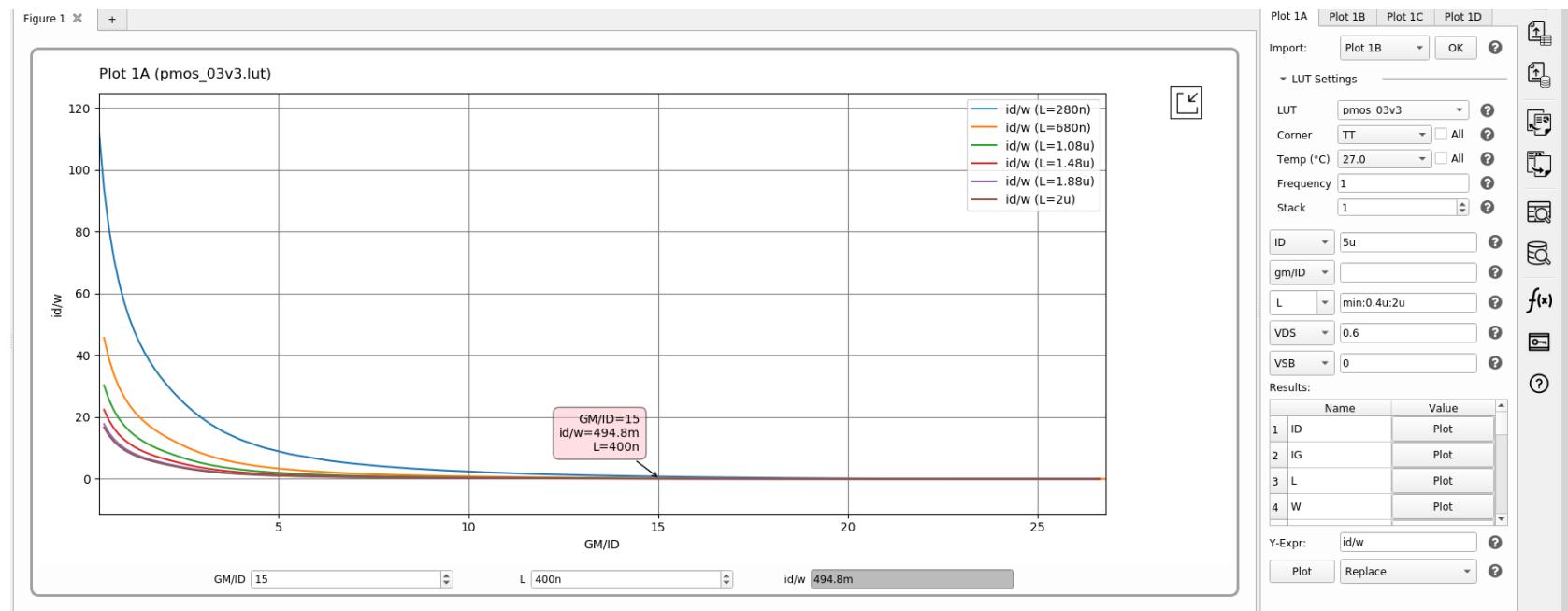
- Next, we need to find the channel length to get the required gain
- For simplicity, assume M7, and M5 have same gds
- Let : gm/id=15 $A_v = \frac{g_m r_o}{2} > 50 \rightarrow \text{Let: } gds7 = gds5 < 0.75\mu\text{s}$
$$A_v = \frac{g_m r_o}{2} \rightarrow \frac{g_m}{g_{ds}} > 100$$
- From the design chart, we find that required length is L = 0.4 um



Design of 1st stage input pair

□ Going to the ID/W chart

$\frac{I_d}{W} = 0.49 \rightarrow \underline{\text{W=10.2 u}}$: we may need to increase it if UGF is at edge



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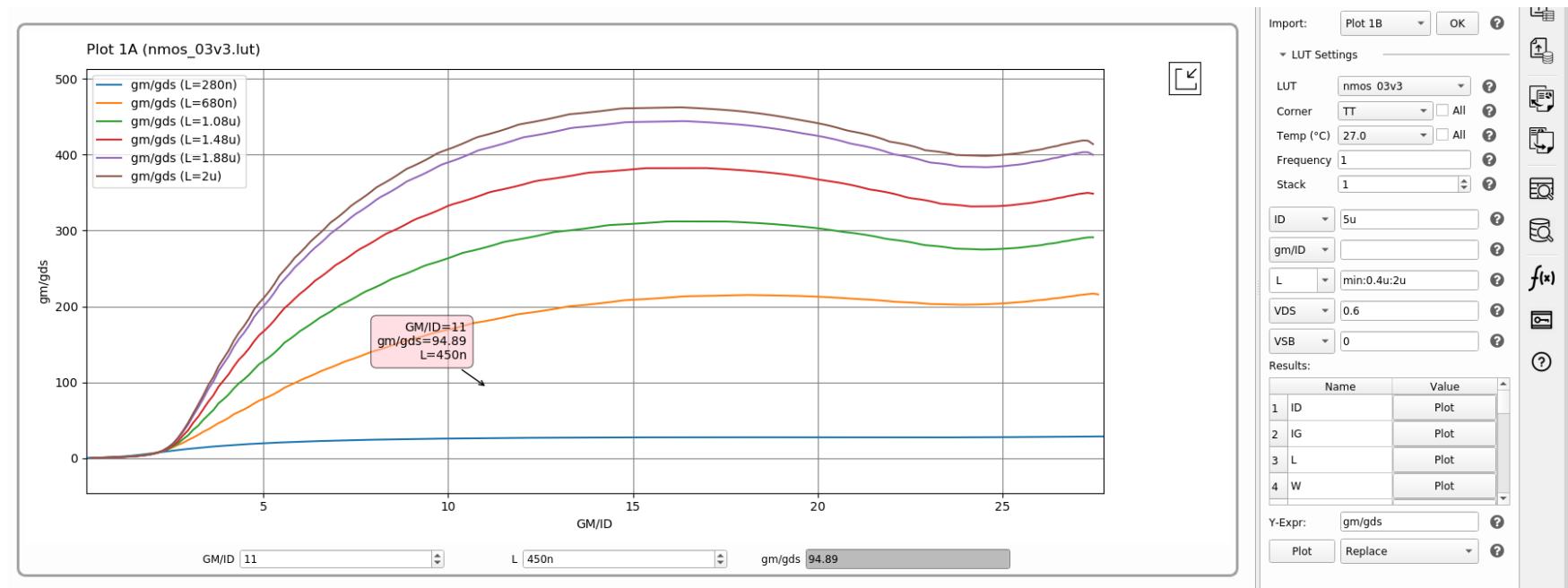
Design of 1st stage current mirror load

- From the DC gain spec select the length of the current mirror load

$$g_{ds5,6} = \frac{I_D}{V_A} < 0.75 \mu S$$

- $V_A = I_D r_o$ slightly decreases with gm/ID (weak dependence)
- Assume an arbitrary but enough gm/ID, e.g., gm/ID = 11

$$\text{gm/id}=11 \rightarrow g= 55 \mu S \rightarrow \text{gm/gds} \geq 75 \rightarrow L = 450n$$



Design of 1st stage current mirror load

- The design of the current mirror load is determined by CMIR, noise, and output swing specs

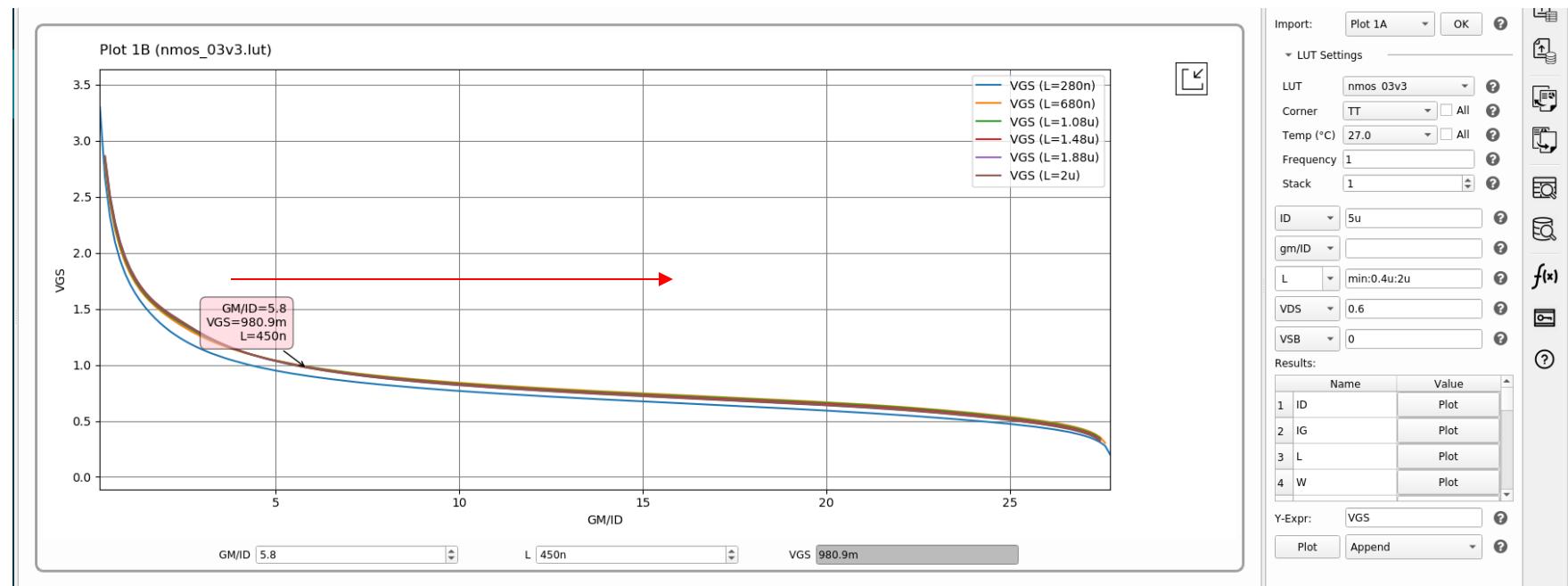
$$V_{gs5,6} - cmirlow < v_{th7,8}$$

$$v_{gs5,6} < 976 \text{ mV}$$

- Get Valid gm/id Range , To make sure our Assumed gm/id Is ok

From curve valid Range for gm/id is]5.8,max]

So our assumed gm/id is ok



Design of 1st stage current mirror load

- Leave W for now !!!**
- We will know why later

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Design of 1st stage tail current source

$$A_{vCM} = \frac{V_{out}}{V_{iCM}} \approx -\frac{1}{2g_{m7,8}r_o3}$$

$$CMRR = \frac{A_v}{A_{vCM}}$$

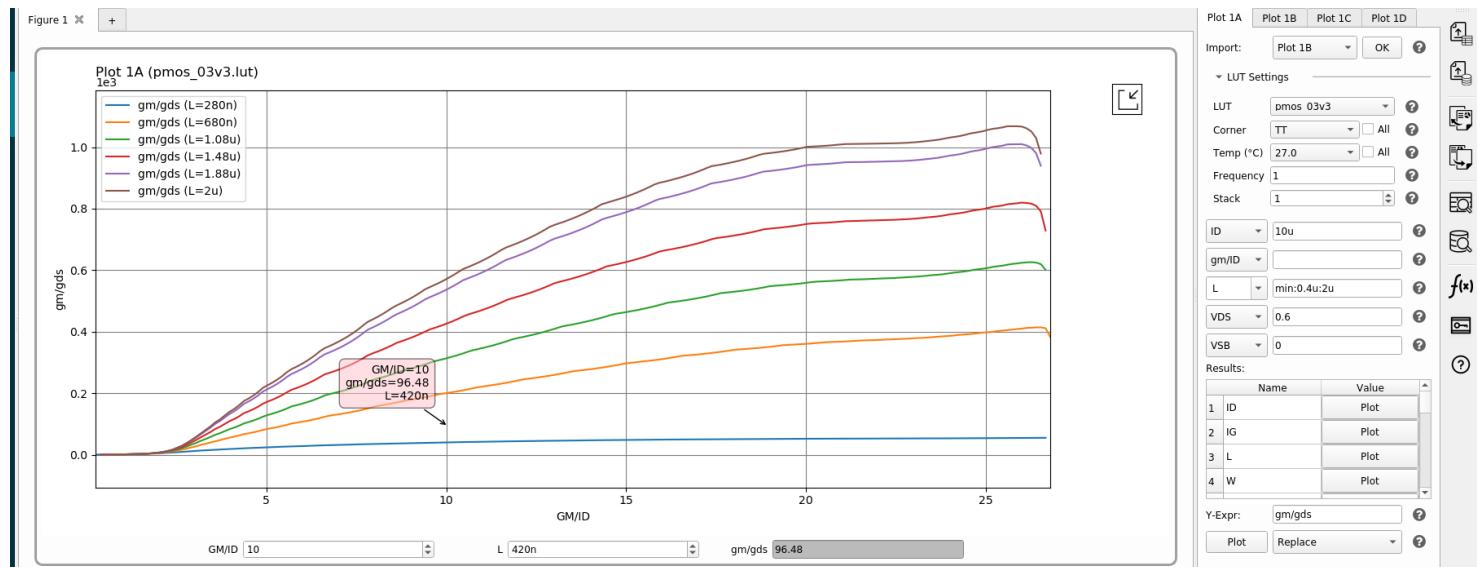
- Long channel length means large output resistance: good CMRR @DC and good mirroring (less CLM)
 - But large area → large parasitic cap: CMRR degrade at high frequencies
- Large gm/ID (small V^{*}): wide CMIR and wide swing
 - But large area → large parasitic cap: ...
 - And more sensitivity to systematic V_{GS} errors (e.g., IR drops)

Design of 1st stage tail current source

$$|A_{vCM}| = \left| \frac{V_{out}}{V_{iCM}} \right| \approx \left| -\frac{1}{2g_{m4,5}r_o} \right| = -34.1 \text{ db} \rightarrow g_{ds5} < 1.1 \mu\text{S}$$

- $V_A = I_D r_o$ slightly decreases with gm/ID (weak dependence)
- Assume an arbitrary but large gm/ID, e.g., gm/ID = 10
- We prefer larger L than needed in CM, to get more control by Gate

$$\frac{g_m}{I_D} = 10 \rightarrow g_m = 100 \mu\text{S} \quad \frac{g_m}{g_{ds}} > 90 \rightarrow \underline{L = 420 \text{ n}}$$

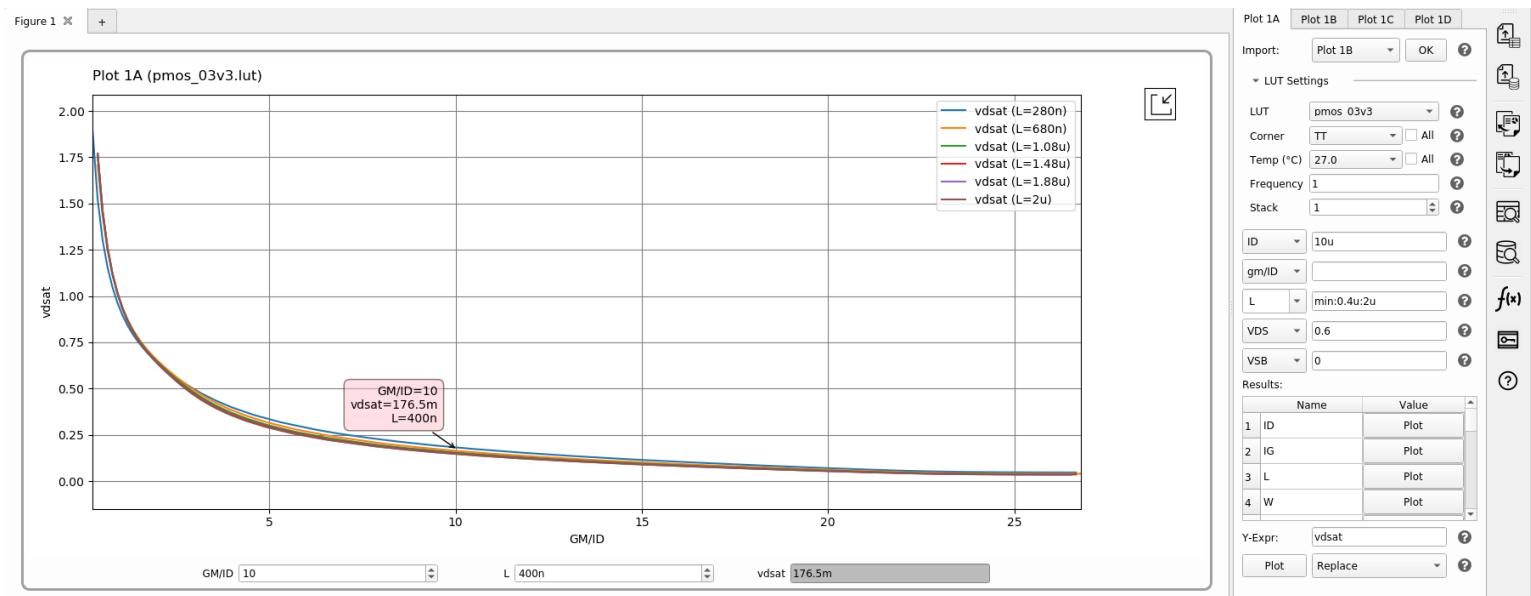


Design of 1st stage tail current source

- The design is completed by CMIR, and validation of assumed gm/id

$$vdd - vdsat3 - cmirhigh > vth7,8$$
$$vdsat3 < 1.8 - vth7,8 - 1 \Rightarrow vdsat3 < 25mV$$

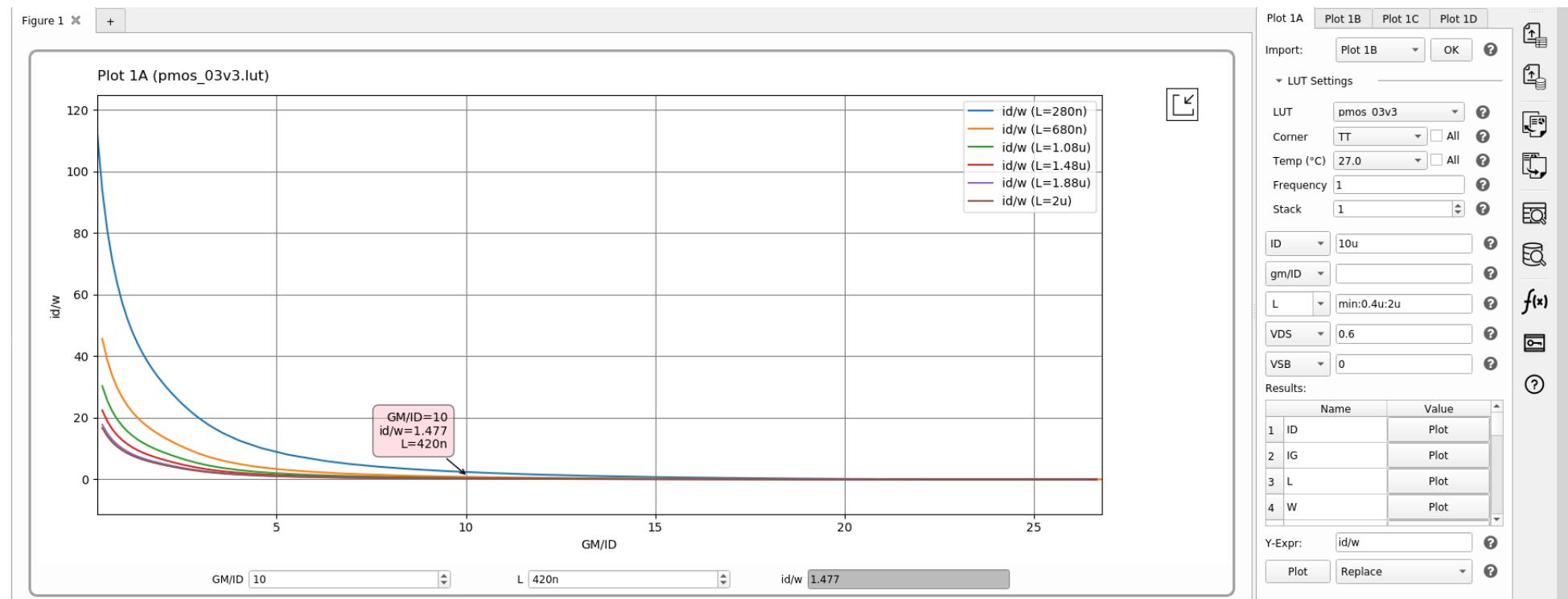
- This can no be achieved even in WI, so a reasonable *cmirhigh* would be Around **850mv**, But may affect CM performance , so a little bit smaller is better
- Our gm/id is Ok for assumed Range



Design of 1st stage tail current source

□ Going to the ID/W chart

$$\frac{I_d}{W} = 1.47 \rightarrow W \approx 6.8 \mu\text{m}$$



1st Stage Sizing Results

1 ST Stage	Input Pairs	Cm load	Current source
gm/id	15	11	10
W	10.2u	Not now!!!	6.8u
L	400n	450n	420n
V*	135.7m	184.4m	202.6m
V _{dsat}	111.6m	154.9m	176.7m
V _{ov}	63.84m	113.6m	156.8m

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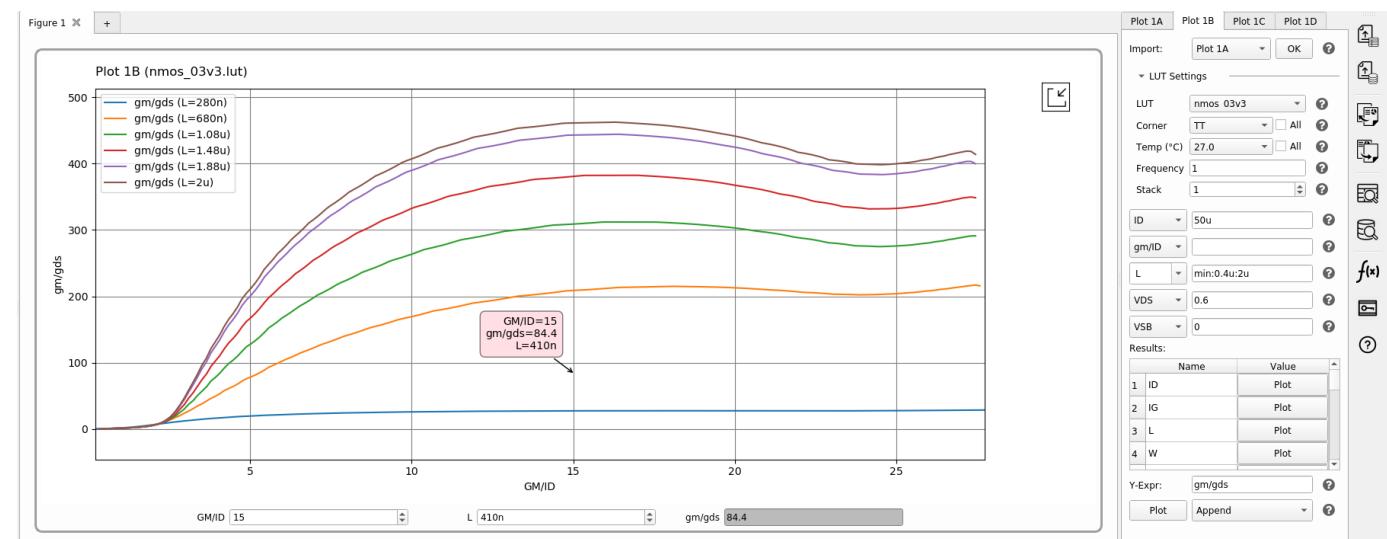
Design of 2nd stage input

- Next, we need to find the channel length to get the required gain
- For simplicity, assume M7, and M5 have same gds
- Let : gm/id=15

$$A_v = g_m r_o > 80 \quad , \text{gm}=750 \text{ us} \rightarrow \text{By letting : } gds_9 = gds_4 < 9 \text{ us}$$

$$A_v = \frac{g_m r_o}{2} \rightarrow \frac{g_m}{g_{ds}} > 80$$

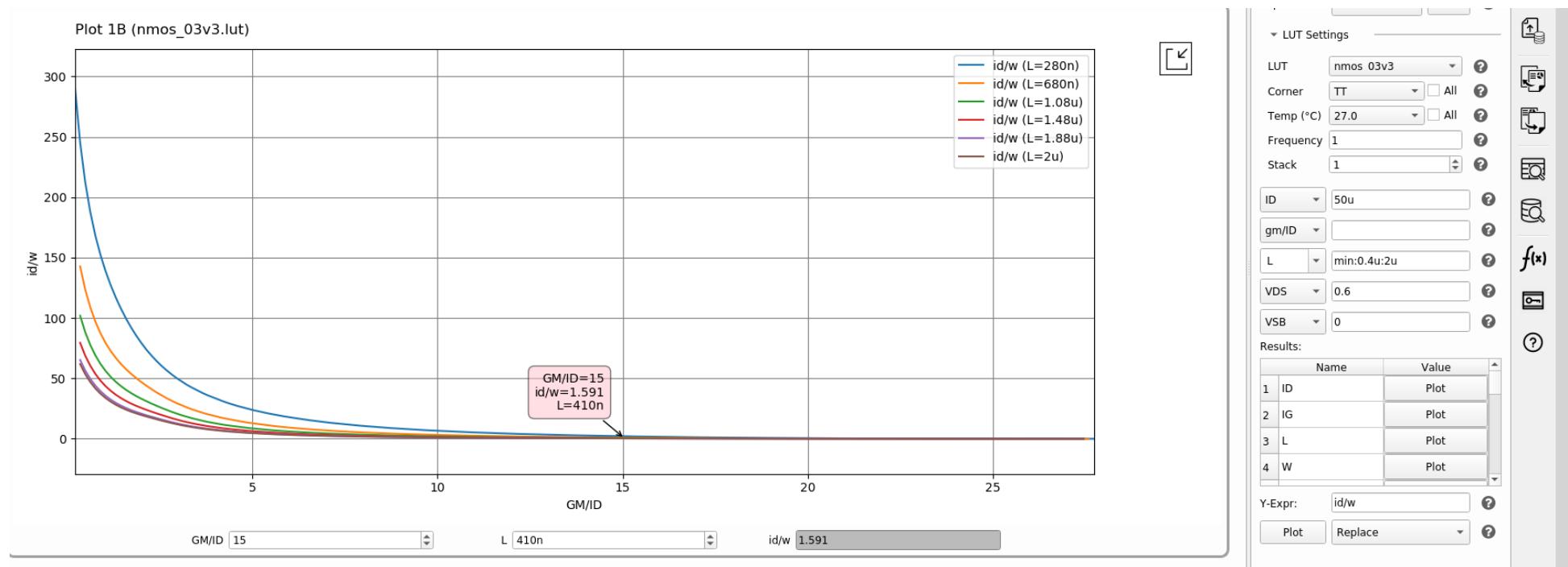
- From the design chart, we find that required length is L = 410 um



Design of 2nd stage input

- ❑ Going to the ID/W chart

$$\frac{I_d}{W} = 1.59, I=50\text{u} \rightarrow W = 34.4 \text{ um}$$



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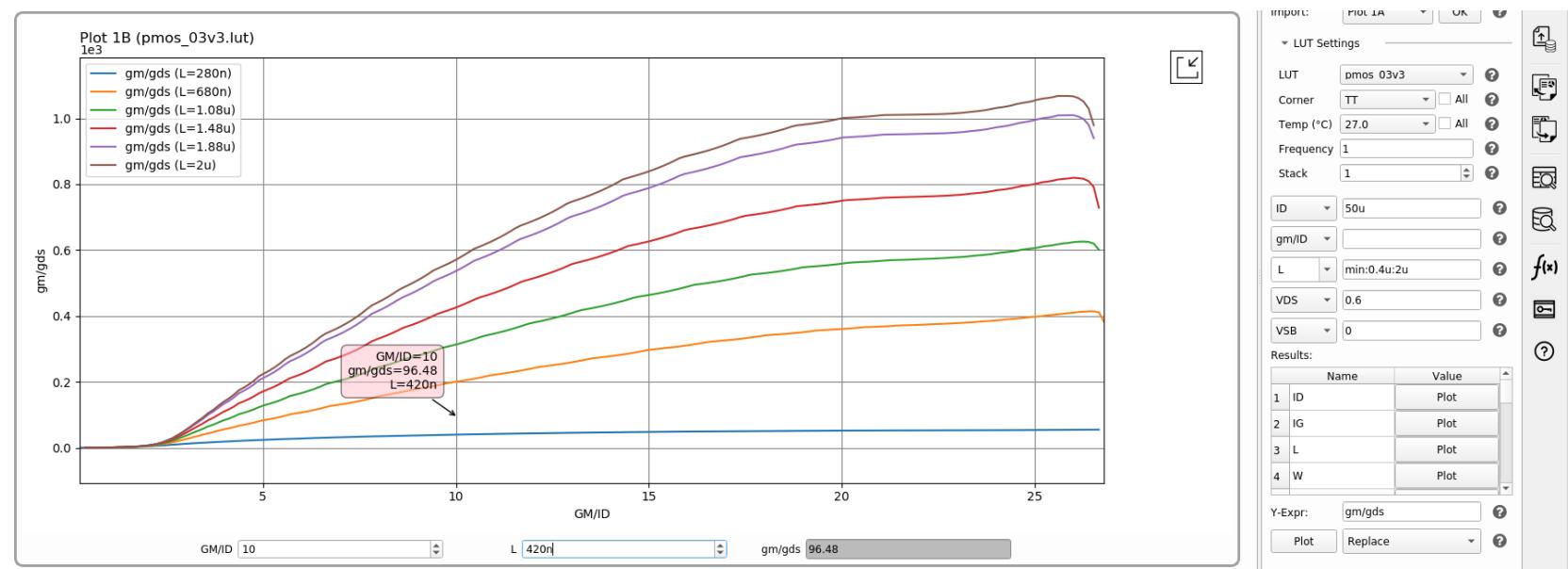
Design of 2nd stage current source

- From the DC gain spec select the length of the current mirror load

$$gds \leq 9\mu s$$

- Assume an arbitrary Small , as CS is preferred with large V*,L e.g., gm/ID = 10

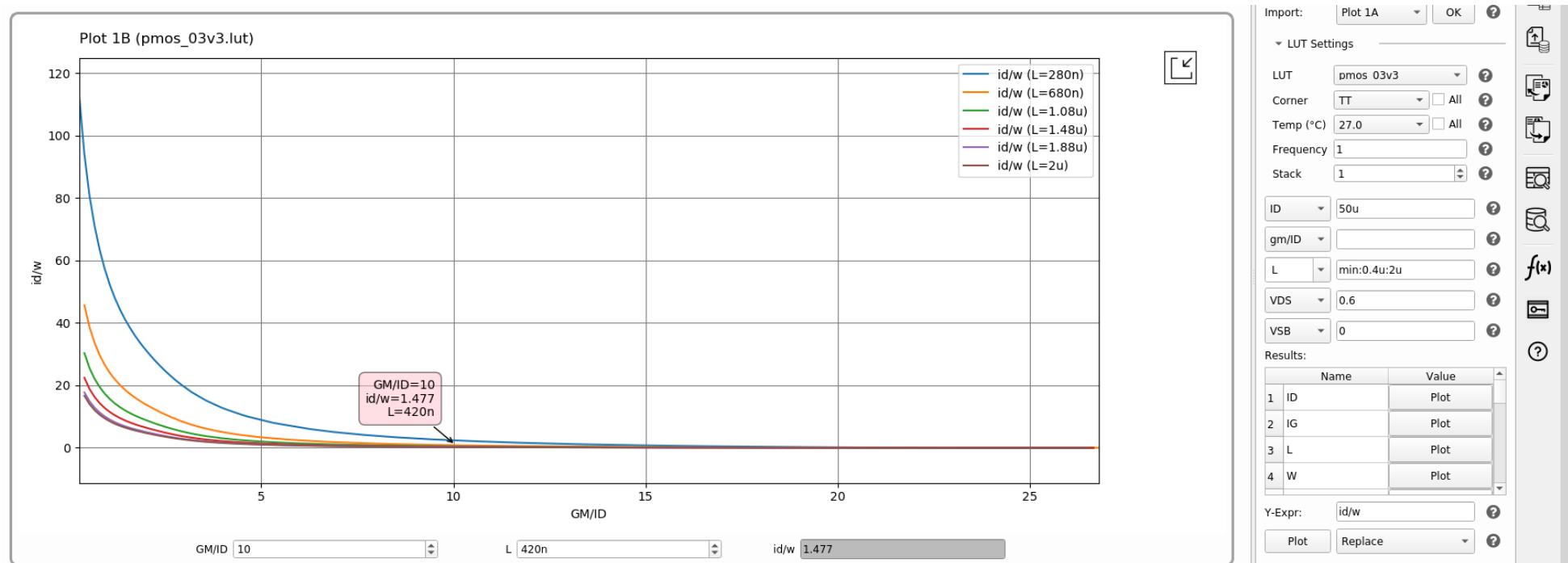
$gm/id=10 \rightarrow g=500 \mu S \rightarrow gm/gds \geq 56 \rightarrow L = 420 n$ “To have same L of Mirroring mosfets”



Design of 2nd stage current source

❑ Going to the ID/W chart

$$\frac{I_d}{W} = 1.47, I=50\text{u} \rightarrow W = 34 \text{ um}, \text{ take suitable } W \text{ for good Mirroring ratios}$$



2nd Stage Sizing Results

2 nd Stage	Input NMOS	CS Pmos
Gm/id	15	10
W	34.4	34u
L	410n	420n
V _{dsat}	108m	176.7m
V*	135.9m	199 mv
V _{ov}	40.36m	156.8m

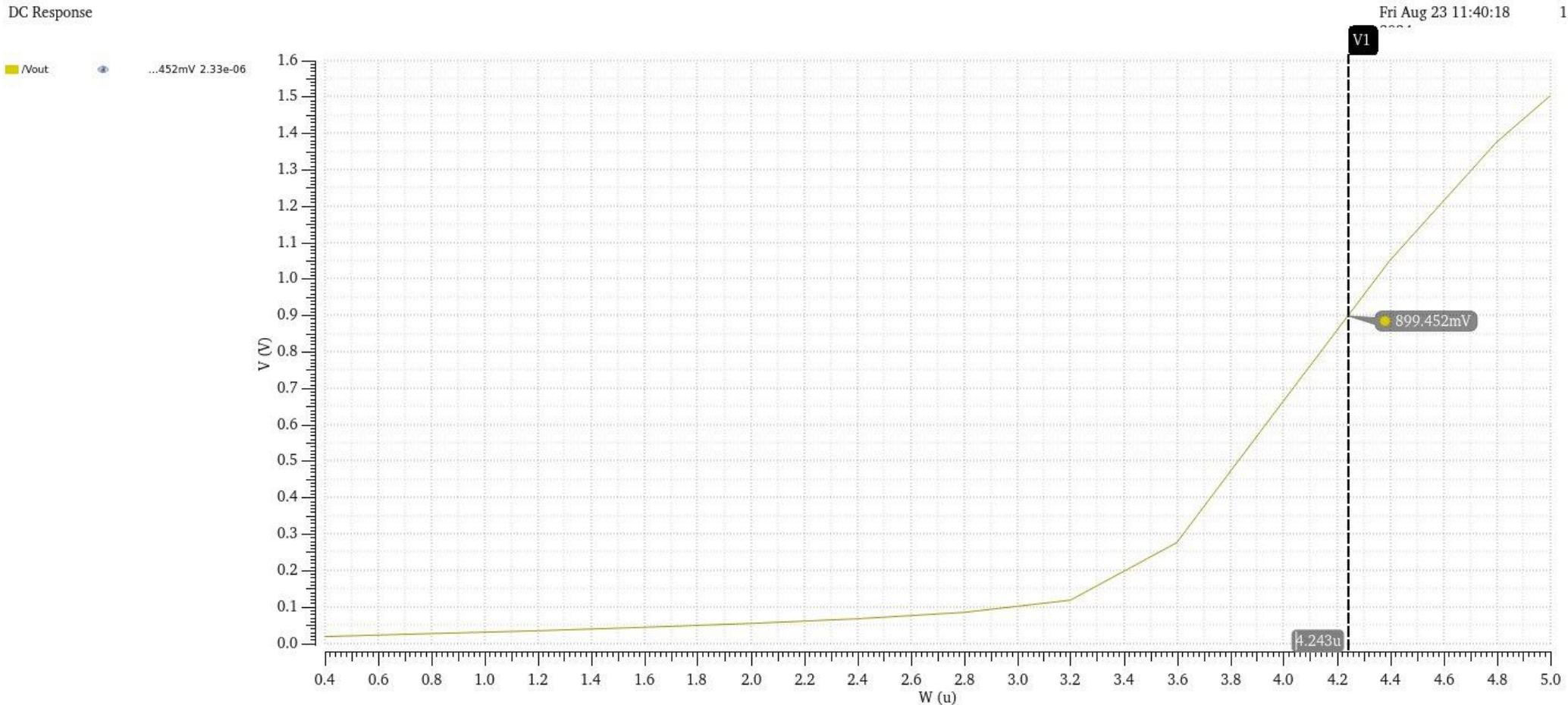
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- ❑ **Offset Removing**
- ❑ Compensation resistance and capacitance
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Offset Removing

- I prefer to watch this lec. by Dr.Hesham omran [LINK](#)
- Note that V_o of 1st stage Follows Mirroring(forced) Node and It is the VGS of 2nd stage input , meaning we have 2 current sources in parallel in 2nd stage , to avoid difference between currents from pmos (50u) and current from input Nmos, We will make sure that the 2 currents are equal by adjusting VGS of input Nmos
- We will swap W of 1st stage cm load to get $V_{o2,cm}=0.9$,to give max swing
- the reason we do this is because V_{out} may be near to VDD or gnd , As It is a high impedance node(ill defined) , so we want to make sure it is $VDD/2$

Offset Removing



- ❑ The W of 1st stage cm load to remove offset is **4.24u**
- ❑ Note that: op pint of M5,6 are not we set , as W changed ,but we will make sure it meets the specs

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Compensation resistance and capacitance

- ❑ Cc is used to make poles splitting , Making 1st stage pole dominant
- ❑ Rc is used to make The Feedforward Zero at infinity ,aiming to have higher stability
- ❑ We already Take Cc = 0.4 Cl = 1.8p F
- ❑ Rc to make The Feedforward Zero at infinity = $\frac{1}{gm9}$ = 1.33k Ω

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- **Sizing and simulation results**

Sizing

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W	10.2u	4.24u	6.8u
L	400n	450n	420n
V*	135.7m	184.4m	202.6m
V _{dsat}	111.6m	154.9m	176.7m
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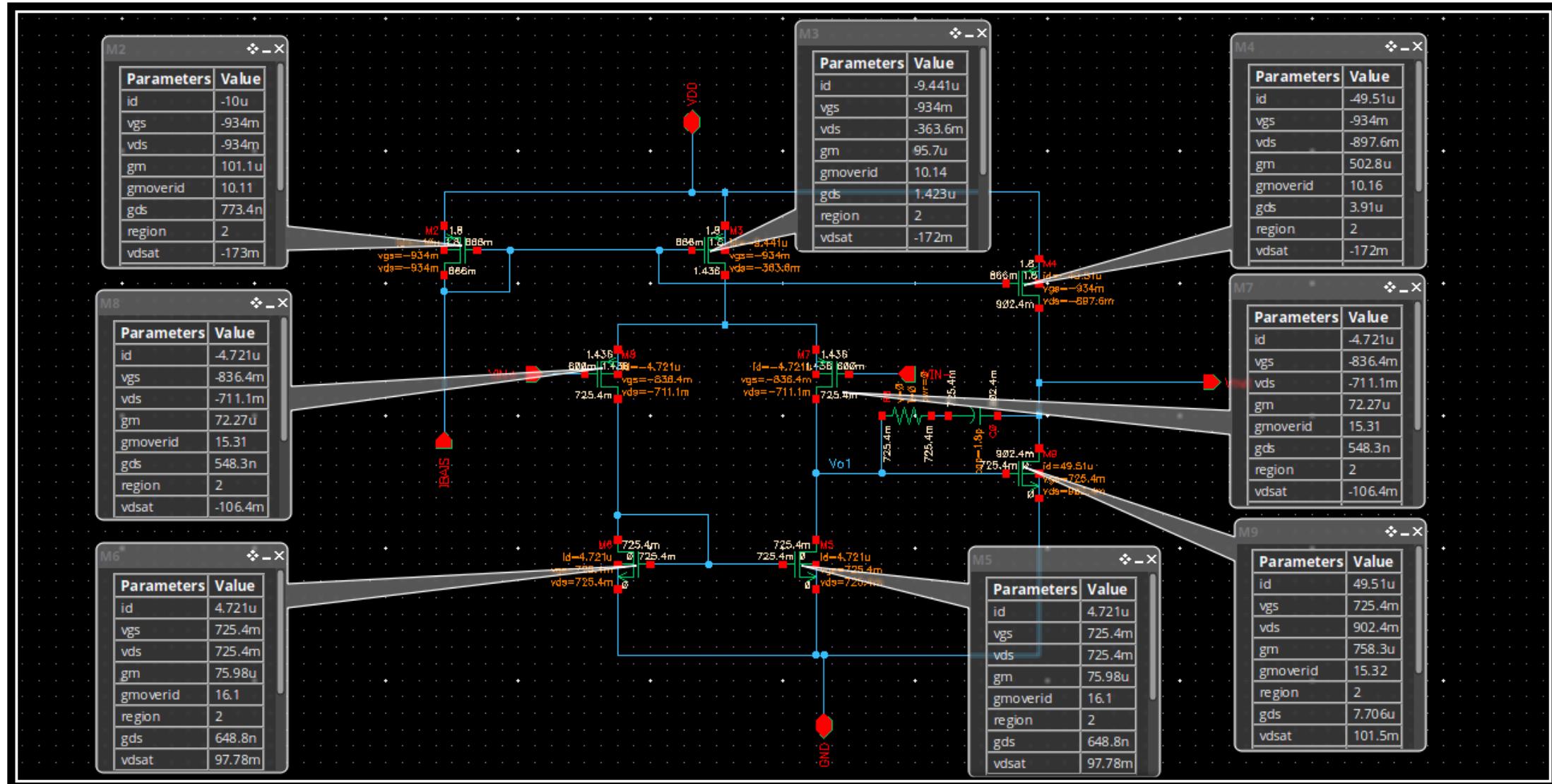
2 ND Stage	Input NMOS	CS Pmos
Gm/id	15	10
W	34.4	34u
L	410n	420n
V _{dsat}	108m	176.7m
V*	135.9m	199m
V _{ov}	40.36m	156.8m

Open-Loop OTA Simulation results

- **the OTA and bias circuit with DC node voltages**
- Diff small signal ccs
- CM small signal ccs
- CMRR
- Diff large signal ccs
- CM large signal ccs
- CM large signal ccs (GBW vs VICM)

the OTA and bias circuit with DC node voltages

OP



the OTA and bias circuit with DC node voltages

- Is the current (and gm) in the input pair exactly equal?
 - Yes , as VID=0 => no current steering

- What is DC voltage at the output of the first stage? Why?
 - 725mv , Because Vout1 follows Mirroring Node , While Mirroring is the VGS of Cm load , **VGS=725 mv** , Well defind node

- What is DC voltage at the output of the second stage? Why?
 - **902 mv** ,as we forced M9 and M4 to have same biasing current , Vout must be centered around Vdd/2

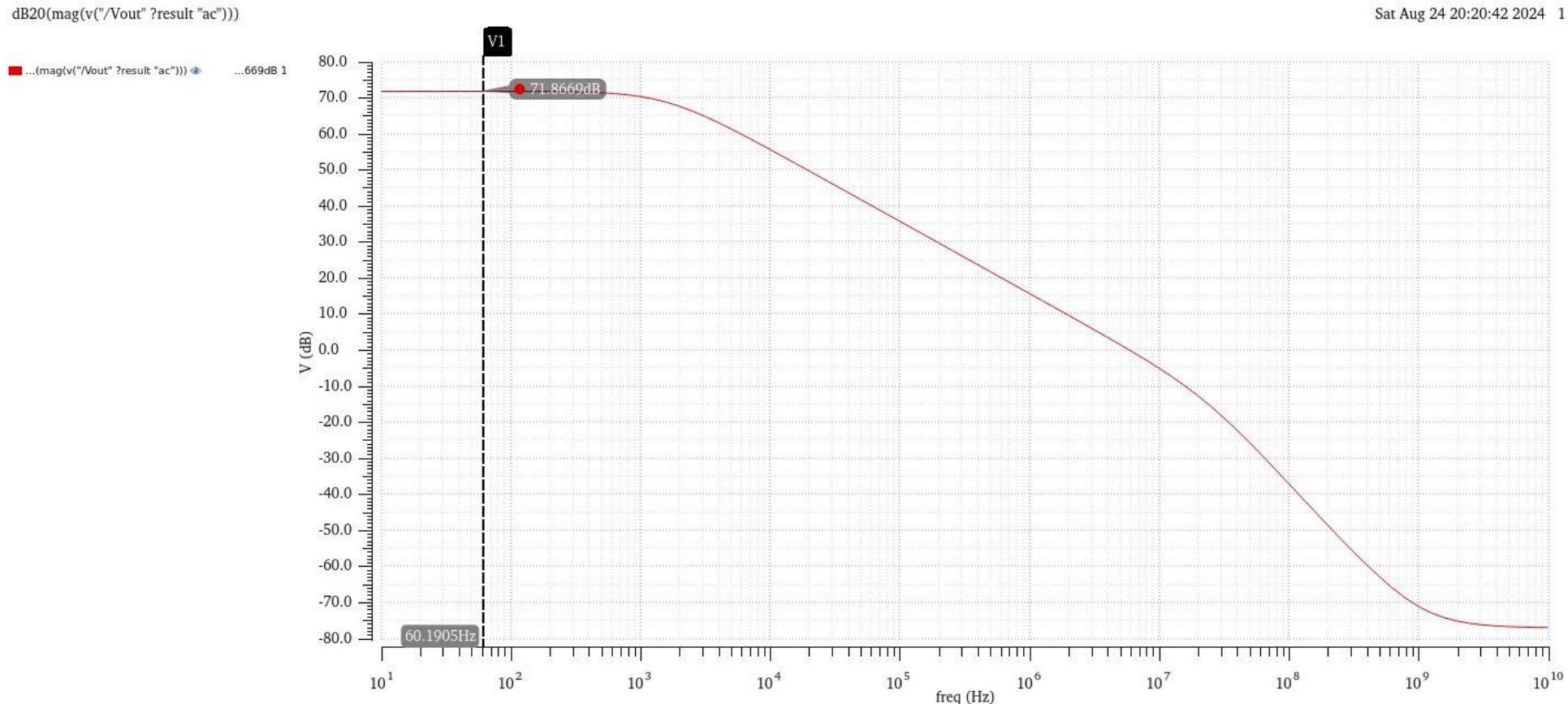
- If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?). If you are using PMOS input pair, body effect may cause CMIR to extend till GND (why?)
 - As $|v_{sb}|$ increase V_{th} increase , the condition of saturation is $|V_{gd}| < |V_{th}|$, as V_{th} increase the V_{gd} can reach higher values and stay in saturation , that means higher V_g for nmos and lower V_g for pmos

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Diff small signal ccs

- Plot diff gain (in dB) vs frequency.



- The margins we take gave bigger gain , as long we meet other specs no need for Tuning

Diff small signal ccs

- Plot diff gain (in dB) vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
5T OTA:Miller_TB:1	/Vout				
5T OTA:Miller_TB:1	fu	6.033M	> 5M		pass
5T OTA:Miller_TB:1	A0I_dB	71.87	> 66		pass
5T OTA:Miller_TB:1	AoI	3.923k	> 2000		pass
5T OTA:Miller_TB:1	BWol	1.57k			
5T OTA:Miller_TB:1	G BW	6.173M			

- The margins we take gave bigger gain , as long we meet other specs no need for Tuning
- If we aim to low power may be make tuning to remove excess gain

Diff small signal ccs

- Compare simulation results with hand calculations in a table.

$$Avd = Avd1 * Av2 = gm7,8(ro7,8||ro5,6) * (gm9 * (ro9||ro4)) = 3919$$

$$gm9 = 758 \text{ us}, ro9 = 130k \Omega, ro7,8 = 1.82M \Omega, ro5,6 = 1.54M \Omega, gm7,8 = 72 \text{ us}, ro4 = 255k \Omega$$

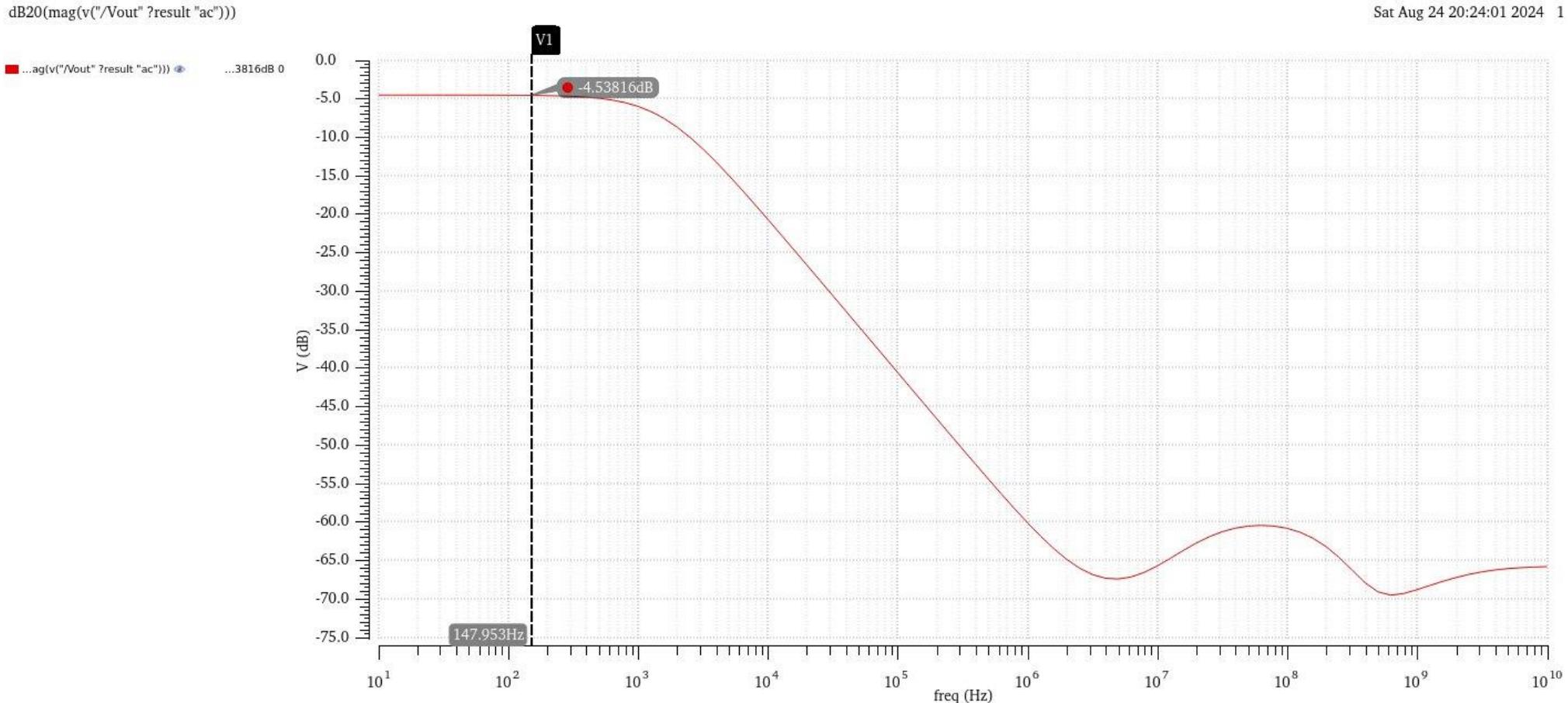
	Hand analysis	Simulation
Avd	71.8 dB	71.9 dB

Open-Loop OTA Simulation results

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CM small signal ccs

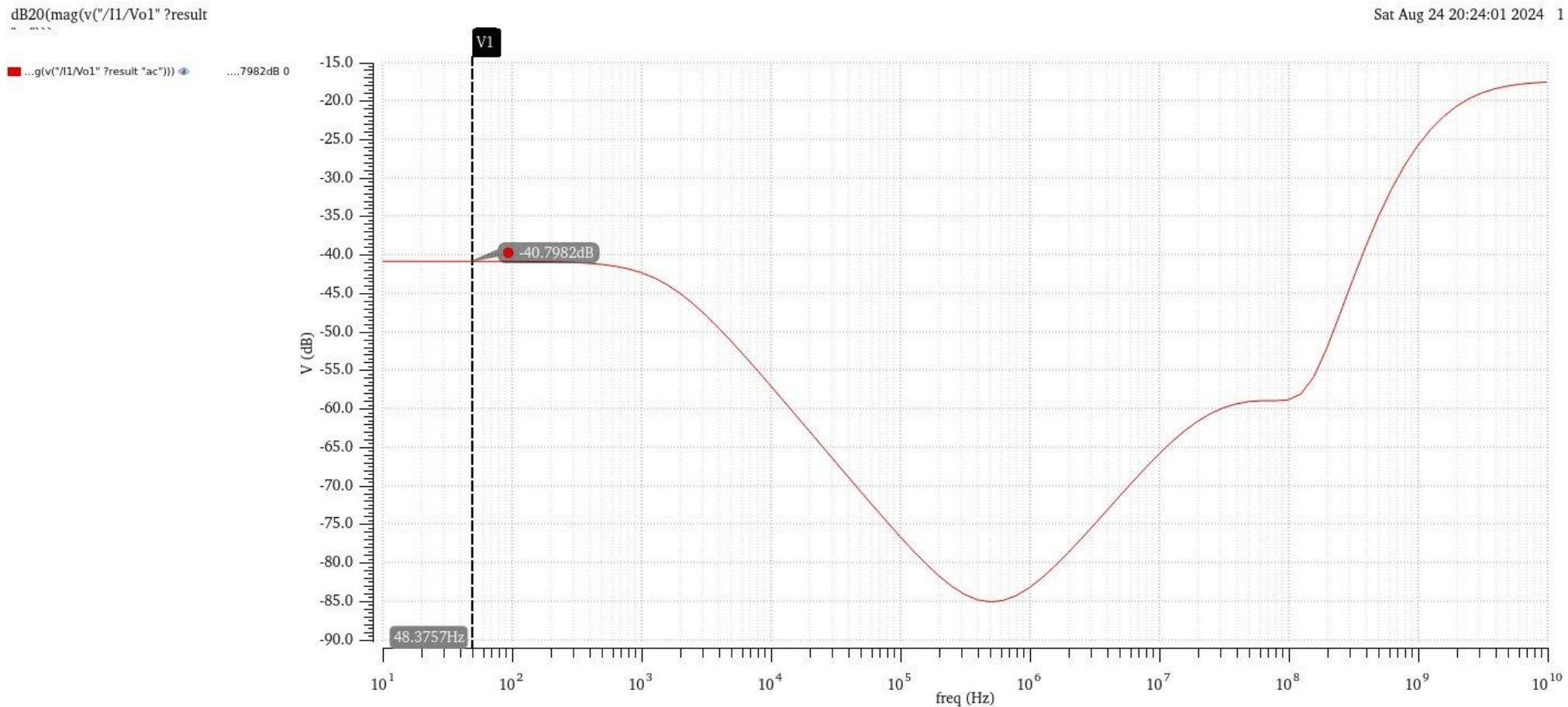
- Plot CM gain in dB vs frequency. **2 stages**



- Note that this is A_{vcm} of The entire 2 stages not the 1st stage only

CM small signal ccs

□ Plot CM gain in dB vs frequency. **1st stage only**



□ Note that this is A_{vcm} 1st stage only

CM small signal ccs

- Compare simulation results with hand calculations in a table.

$$Avcm_{overall} = Avcm1 * Av2 = \frac{1}{2 * gm5,6 * ro3} * (gm9 * (ro9||ro4)) = 0.609$$
$$gm5,6 = 76 \text{ us}, ro3 = 704k \Omega, gm9 = 758 \text{ us}, ro9 = 130k \Omega, ro4 = 255k \Omega$$

	Hnad analysis	Simulation
Avcm	-4.3 dB	-4.53 dB

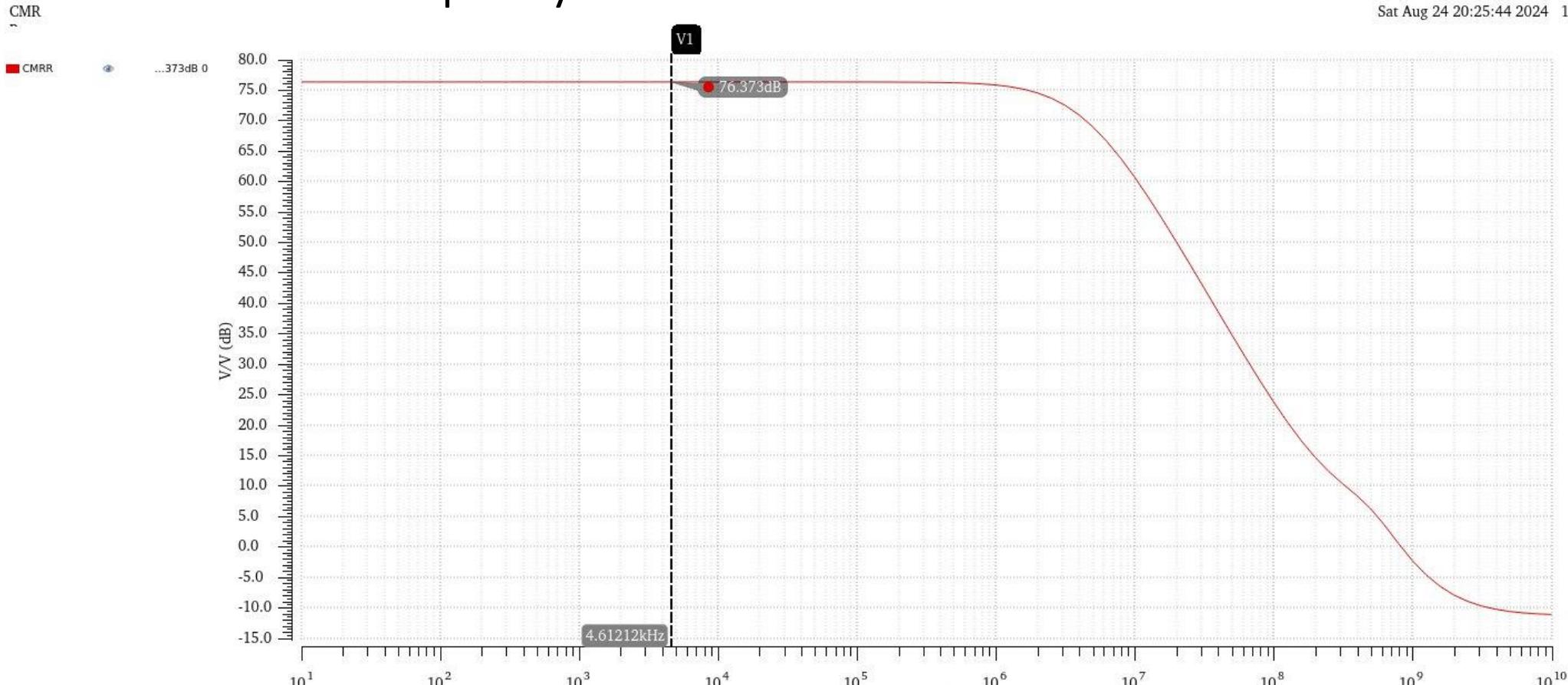
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CMRR

Plot CMRR in dB vs frequency.

Sat Aug 24 20:25:44 2024 1



ST_OTA:Miller_TB:1	CMRR			
ST_OTA:Miller_TB:1	CMMR_spec	76.37	> 74	pass

CMRR

- Compare simulation results with hand calculations in a table.

$$Cmrr = \frac{Avd}{Acm} = (gm7,8 * (ro7,o||ro5,6)) * (2gm5,6 * r03)$$

$$ro7,8 = 1.82M \Omega, ro5,6 = 1.54M \Omega, gm7,8 = 72 \mu s, gm5,6 = 76 \mu s, r03 = 704k \Omega$$

$$Cmrr = 6426 = 76.1 \text{ dB}$$

	Simulation	Hand analysis
$Cmrr$	76.1 dB	76.37 dB

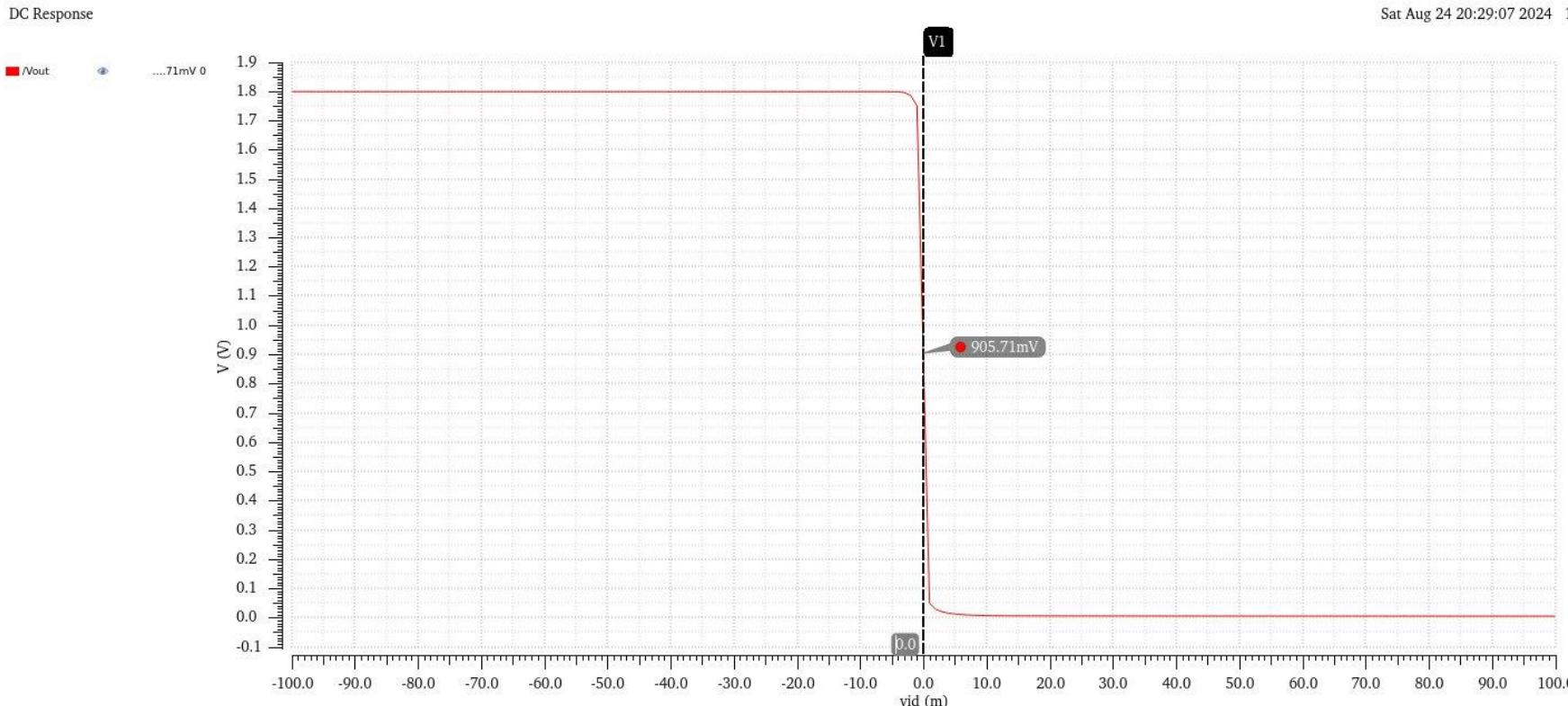
- Simulation result are better than hand analysis.

Open-Loop OTA Simulation results

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Diff large signal ccs

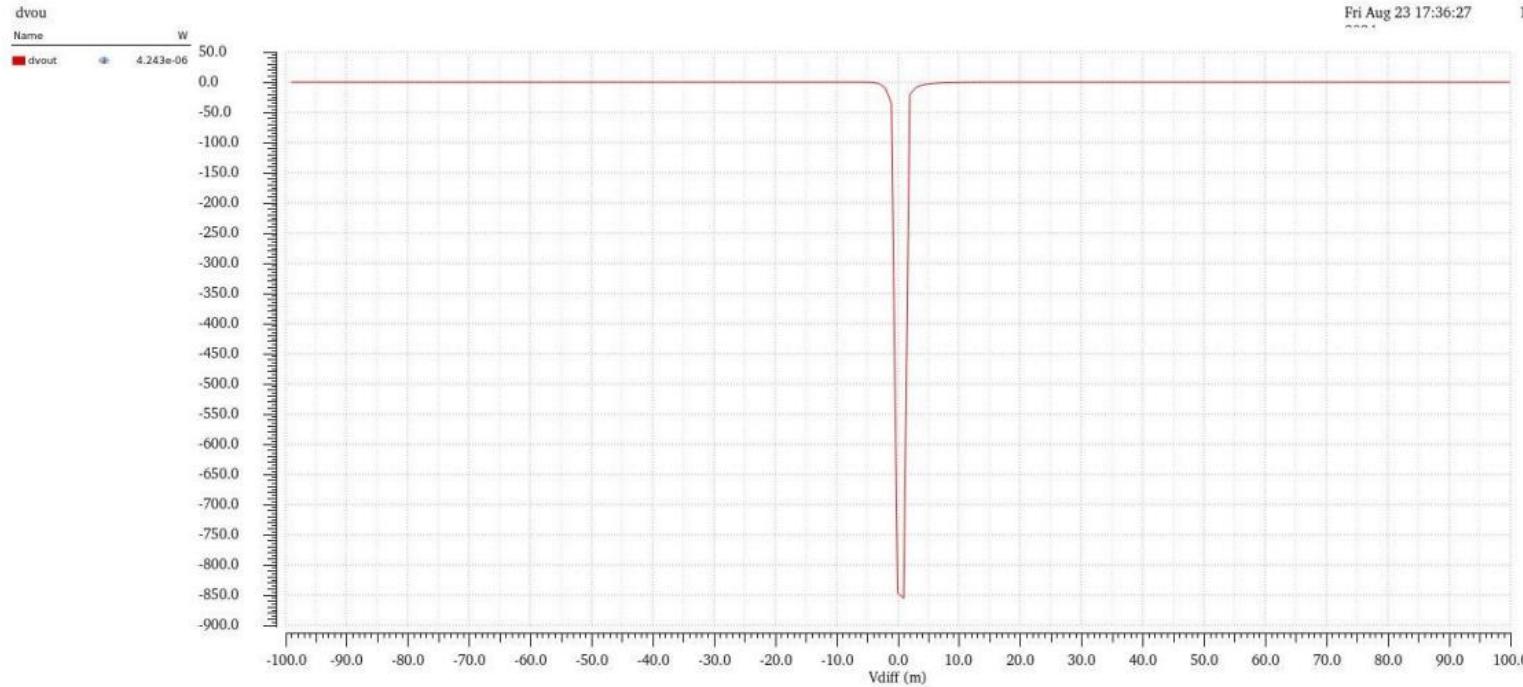
- ☐ Plot VOUT vs VID.



- ☐ what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.
 - 905mv , same as obtained from DC op sim.

Diff large signal ccs

- Plot the derivative of VOUT vs VID.



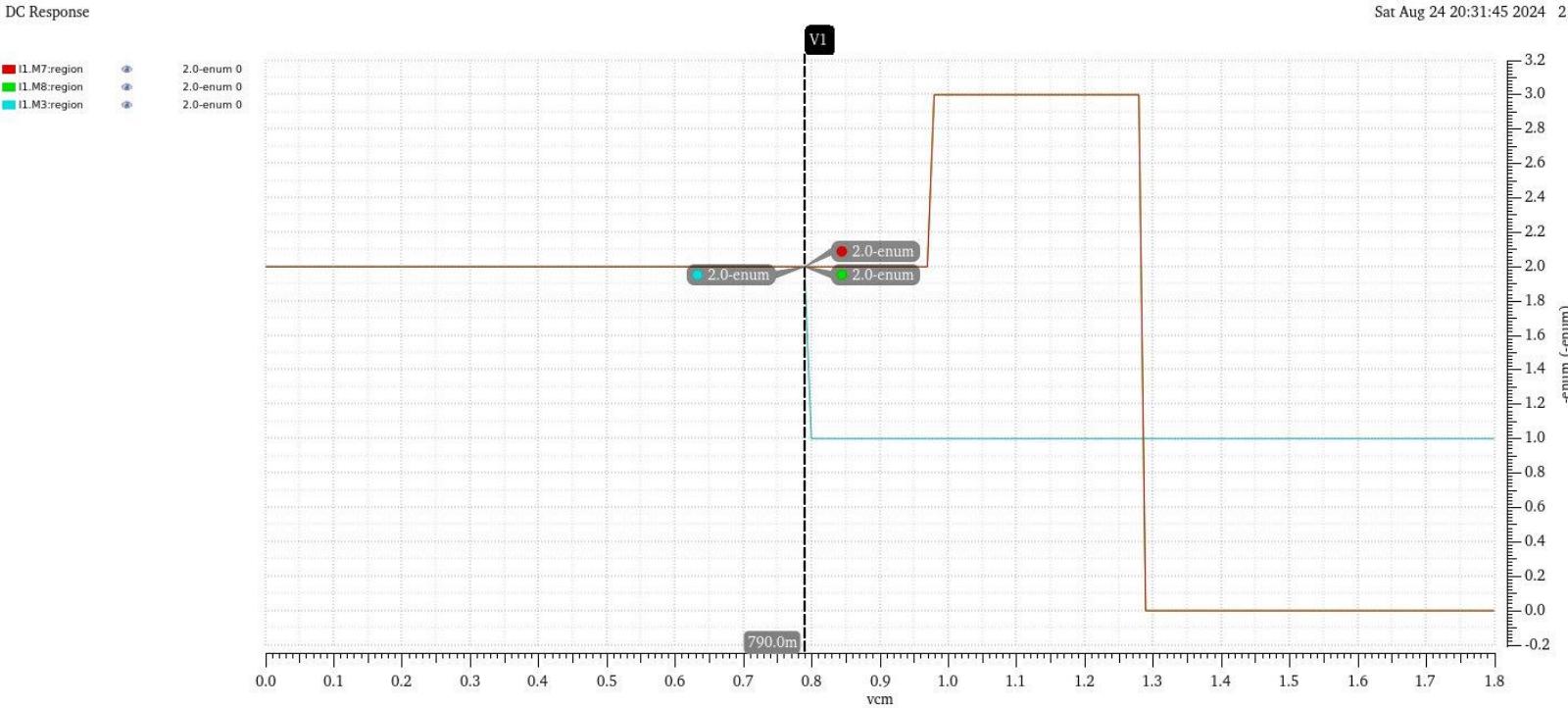
- Is the peak less than the value of Avd obtained from ac analysis? Why?
 - Yes , because the gain of fully diff amp is very sensitive to Vid,LS , the amp region of operation is very limited and even in this region gain is not constant decrease if Vid increased , to increase linearity we may use Rs in order to extend region of operation, and due to large step in simulation the sample at which gain = LG is missed

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CM large signal ccs

- Plot “region” OP parameter vs V_{CM} for the input pair and the tail current source



- Find the CM input range (CMIR). Compare with hand analysis(page 21) in a table.

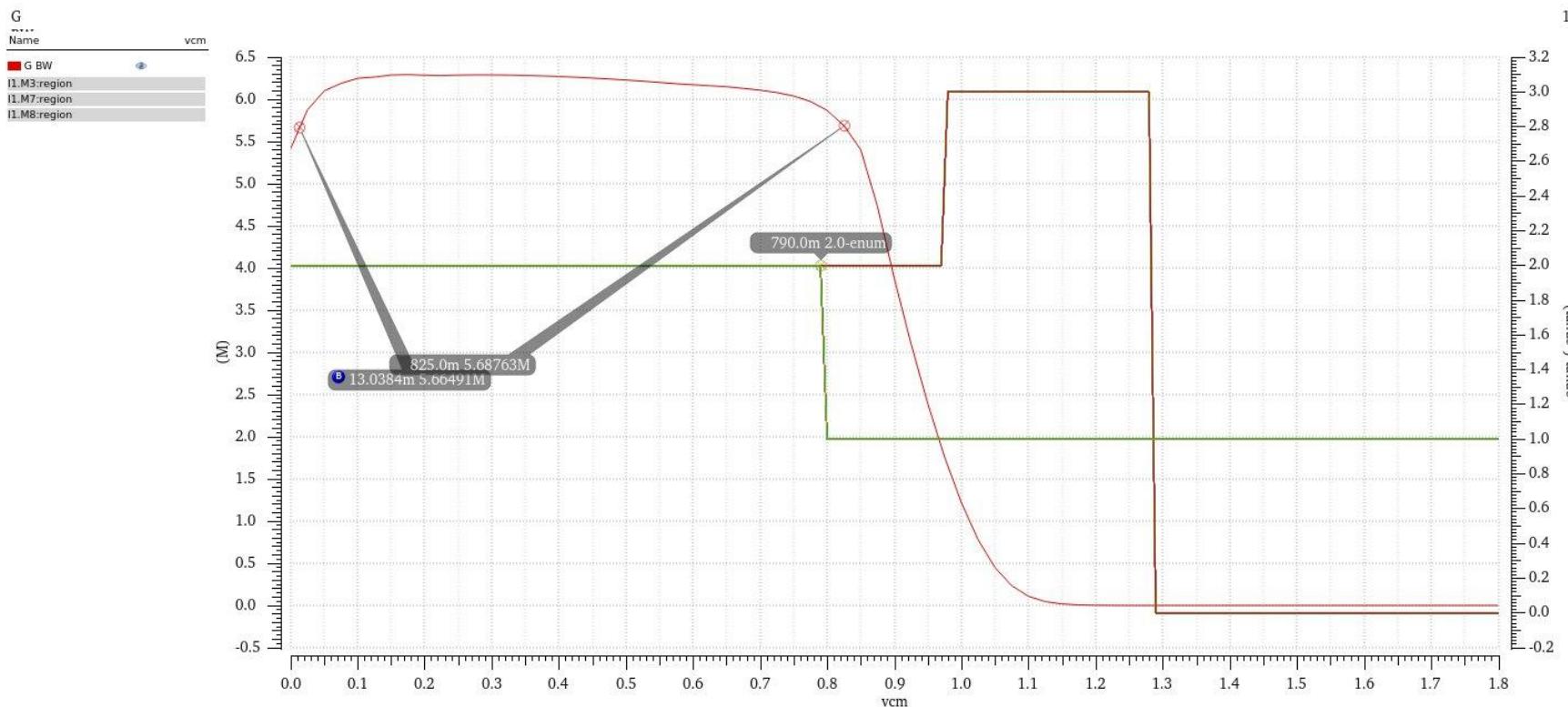
	Hnad analysis	Simulation
High	850 mv	790 mv
Low	0	0 v

Open-Loop OTA Simulation results

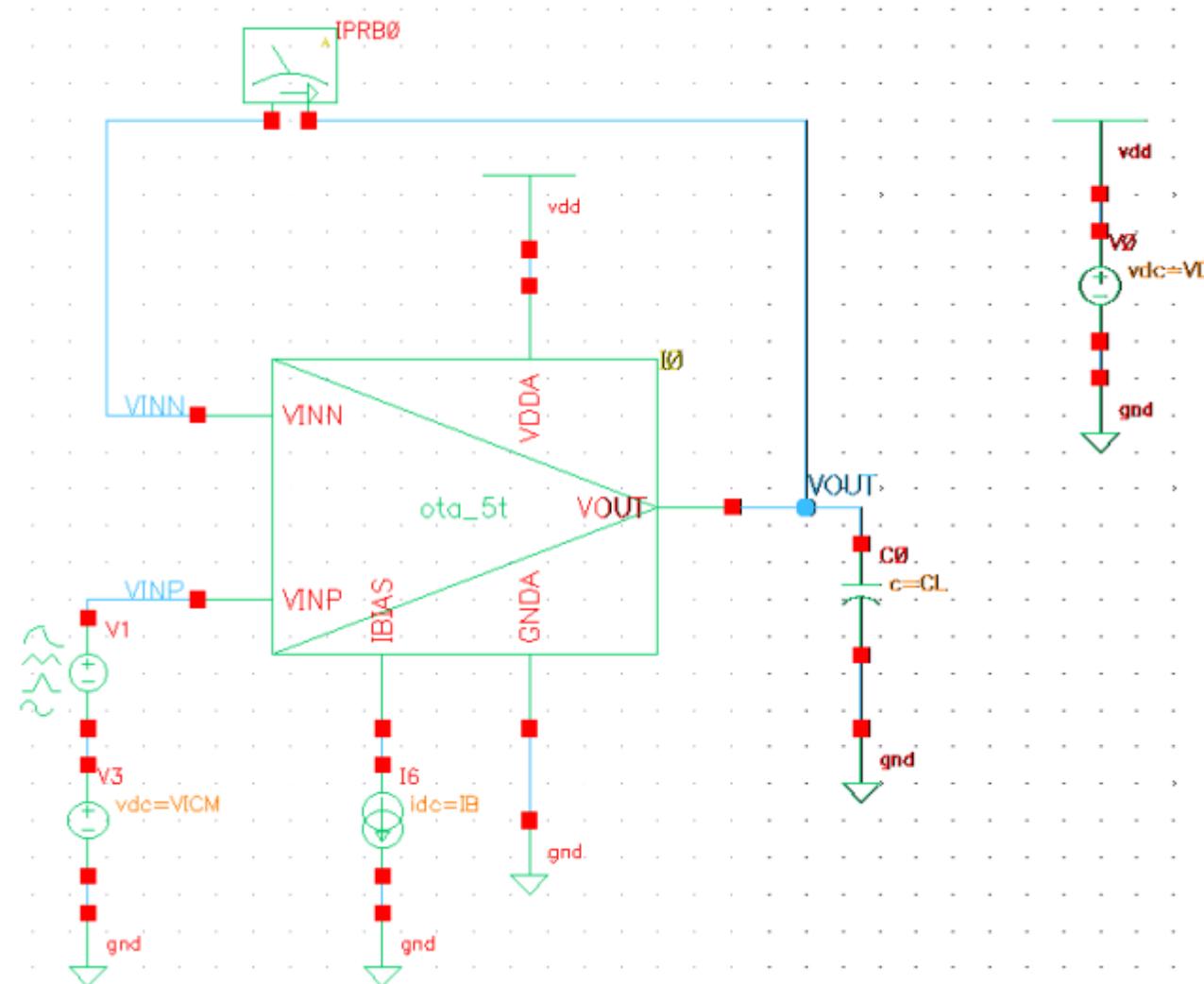
- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs
- CMRR
- Diff large signal ccs
- CM large signal ccs
- **CM large signal ccs (GBW vs VICM)**

CM large signal ccs (GBW vs VICM)

- CM large signal ccs (GBW vs VICM)
- Calculate the input range as the range
- Range=812 mv



Closed-Loop OTA Simulation



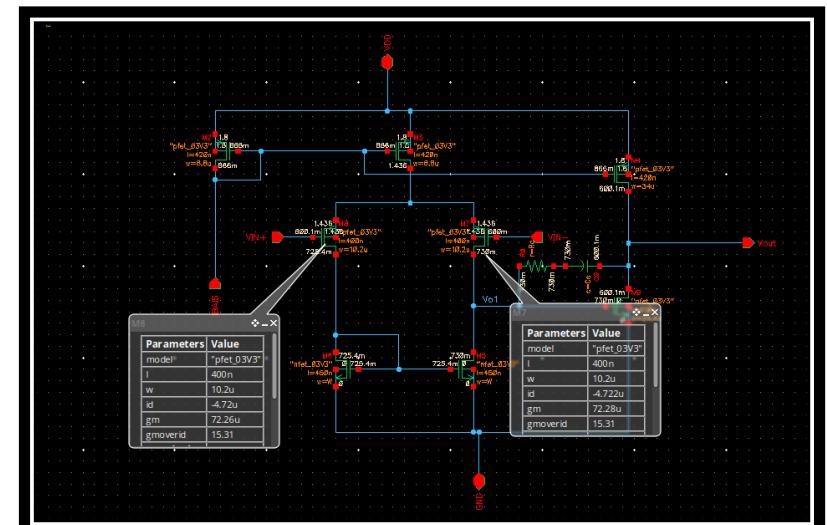
Closed-Loop OTA Simulation

❑ **OTA and the bias circuit with DC OP**

- ❑ Loop gain
- ❑ Slew rate
- ❑ Settling time

OTA and the bias circuit with DC OP

- ❑ Are the DC voltages at the input terminals of the op-amp exactly equal? Why?
 - No, the delta $|(v_{in+}) - (v_{in-})|$ at input terminals = $1/LG$, so as long the LG is not infinity the delta will not be zero
 - ❑ Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?
 - No, as it is the V_{gs} of CM load , and that CM load is Current mode biasing, so it's V_{gs} depends on current through it , and that current is a little bit higher than open loop with $v_{idac}=0$, as there is current steering this time , making V_{gs} bigger
 - ❑ Is the current (and gm) in the input pair exactly equal? Why?
 - As there is current steering due to the $\Delta/2$, making the pos input branch with higher current , so higher gm



Closed-Loop OTA Simulation

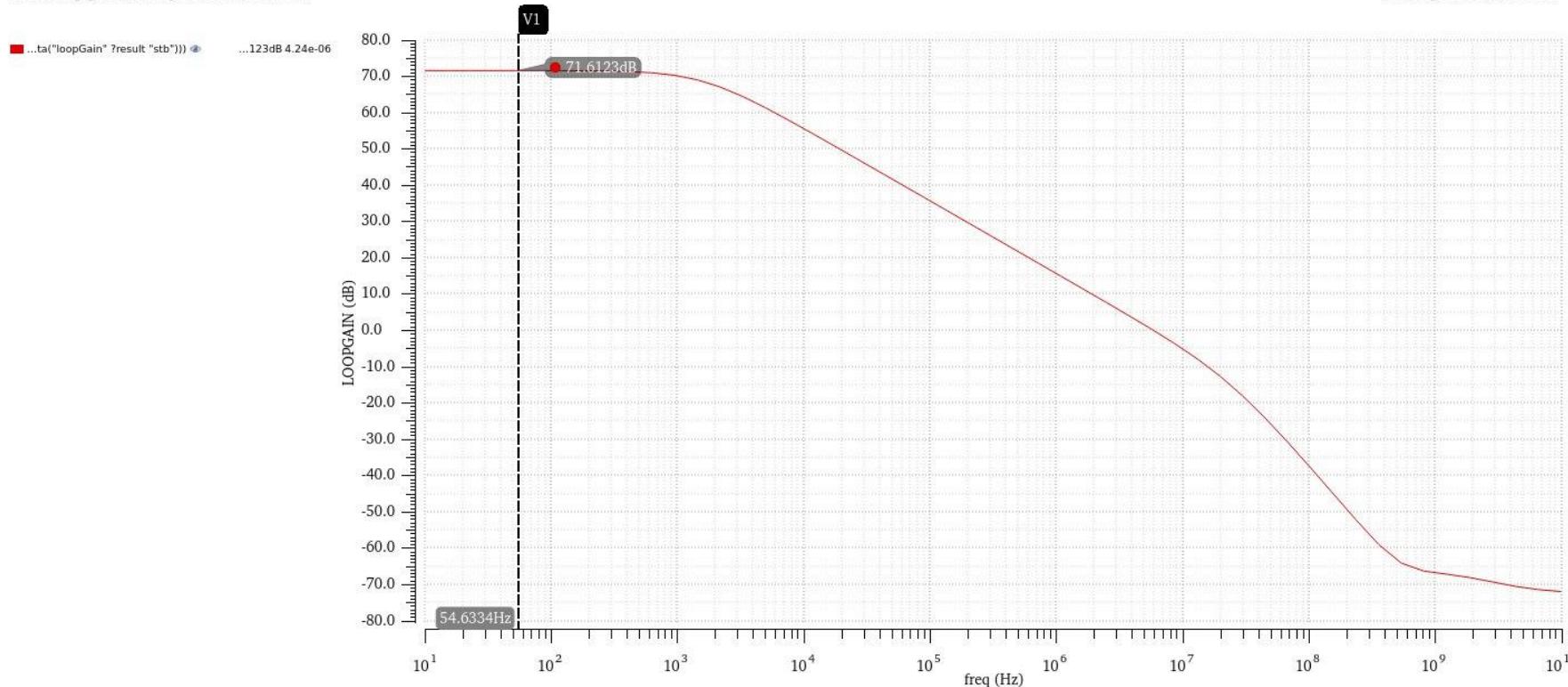
- ❑ OTA and the bias circuit with DC OP
- ❑ **Loop gain**
- ❑ Slew rate
- ❑ Settling time

Loop gain

□ Plot loop gain in dB and phase vs frequency.

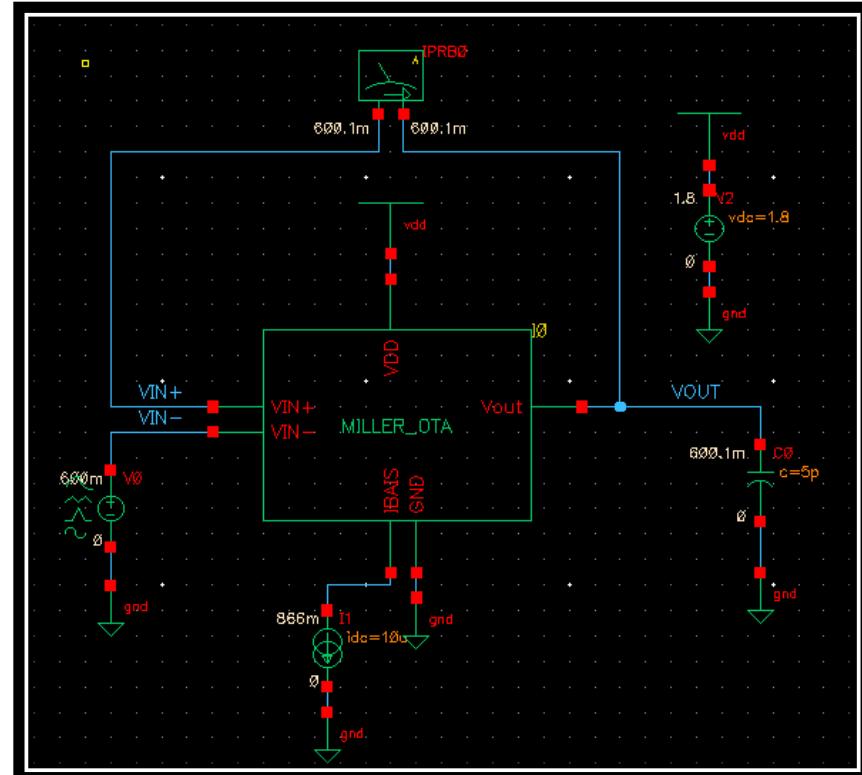
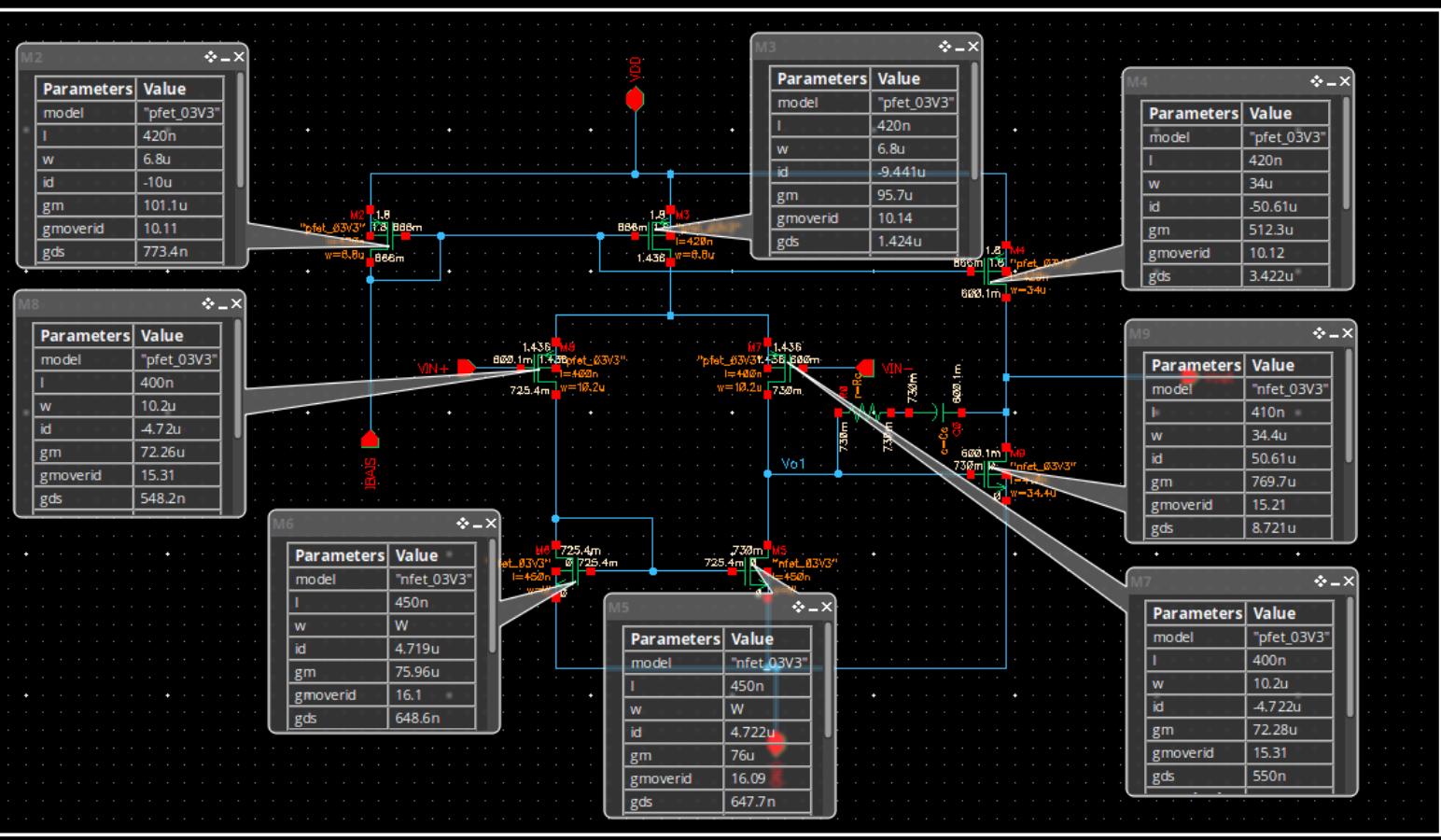
```
dB20(mag(getData("loopGain" ?result "stb")))
```

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Test	Output	Nominal	Spec	Weight	Pass/Fail
5T_OTA:MILLER_OTA_CL:1	AoI	3.809k	> 2000		pass
5T_OTA:MILLER_OTA_CL:1	fu	6.081M	> 5M		pass
5T_OTA:MILLER_OTA_CL:1	GBW	6.233M	> 5M		pass
5T_OTA:MILLER_OTA_CL:1	AoI_db	71.62	> 66		pass

OTA and the bias circuit with DC OP



Loop gain

- Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment

	Open loop	Closed loop	Closed loop Hand analysis
DC gain	3923	3809	3791
GBW	6.17 Mhz	6.23 Mhz	6.17
fu	6.03	6.08 Mhz	6.03

- Comment

➤ The gain changed as $V_{out,cm}$ changes giving diff. V_{ds} and g_{ds} , and as we see -ve feed back maintain f_u and GBW almost the same , but as we will see extended BW_{cl}

$$LG = A_{ol} * B = A_{ol1} * A_{ol2} * 1 = gm7(r_o7||r_o5) * (gm9 * (r_o9||r_o4)) = 3791$$

$$gm9 = 769 \text{ us}, r_o9 = 114k \Omega, r_o7 = 1.81M \Omega, r_o5 = 1.54M \Omega, gm7 = 72.28 \text{ us}, r_o4 = 292k \Omega$$

Loop gain

- Report PM. Compare with hand calculations. Comment.

	Sim	Hnad analysis
PM	75.3	76
5T OTA: MILLER OTA CL:1 getData("/phaseMargin" ?result ...	75.32 > 70	pass

$$let TF = \frac{Aol}{(1 + \frac{s}{w1})(1 + \frac{s}{w2})} = \frac{3809}{(1 + \frac{s}{w1})(1 + \frac{s}{w2})}$$

$$phase @ fu = 180 - 90 - \arctan\left(\frac{wu}{wp2}\right) = 90 - 14^\circ = 76^\circ$$

$$\omega_{p1} \approx \frac{1}{R_{out1}(G_{m2}R_{out2})C_C}$$
$$\omega_{p2} \approx \frac{G_{m2}}{C_1 + C_2} \approx \frac{G_{m2}}{C_L}$$

$$Rou1 = 0.825 M \Omega, Rout2 = 86 K \Omega$$
$$Cc = 1.8 p F, Gm2 = gm9 = 758 \mu s$$
$$Wu=6.08*2\pi=38.2$$

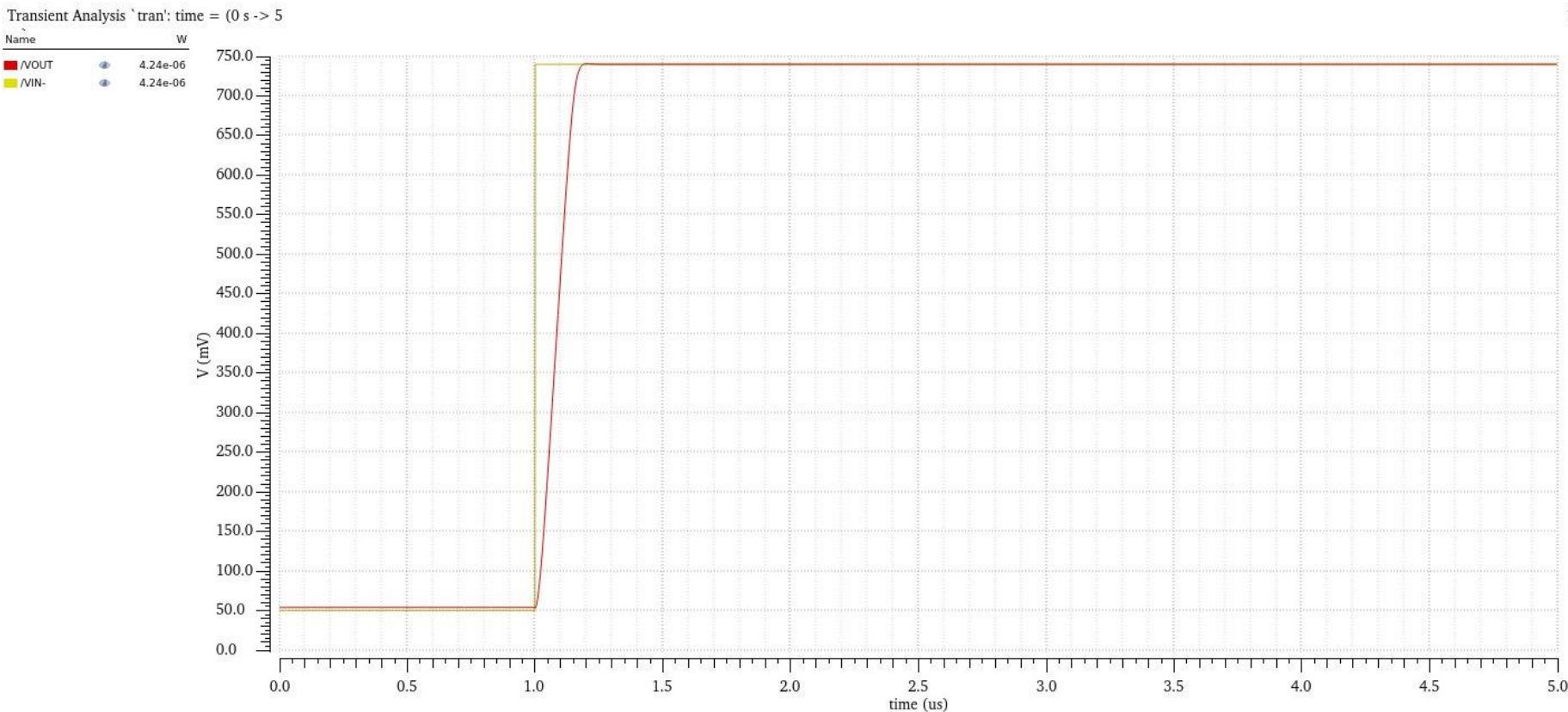
- making wu=4 Wpnd gave us good phase margin, making the system more stable

Closed-Loop OTA Simulation

- ❑ OTA and the bias circuit with DC OP
- ❑ Loop gain
- ❑ **Slew rate**
- ❑ Settling time

Slew rate

□ Report Vin and Vout overlaid.



□ Report the slew rate.

5T_OTA: MILLER_OTA_CL:1	slewRate(v"/VOUT" ?result "tran")	5.006M	> 5M	pass
5T_OTA: MILLER_OTA_CL:1	yMax(deriv(v"/VOUT" ?result "tran"))	5.32M	> 5M	pass

Slew rate

- Compare simulation results with hand calculations in a table.

$$SR = \frac{I_1}{C_c} = \frac{10u}{1.8P} = 5.5 M$$

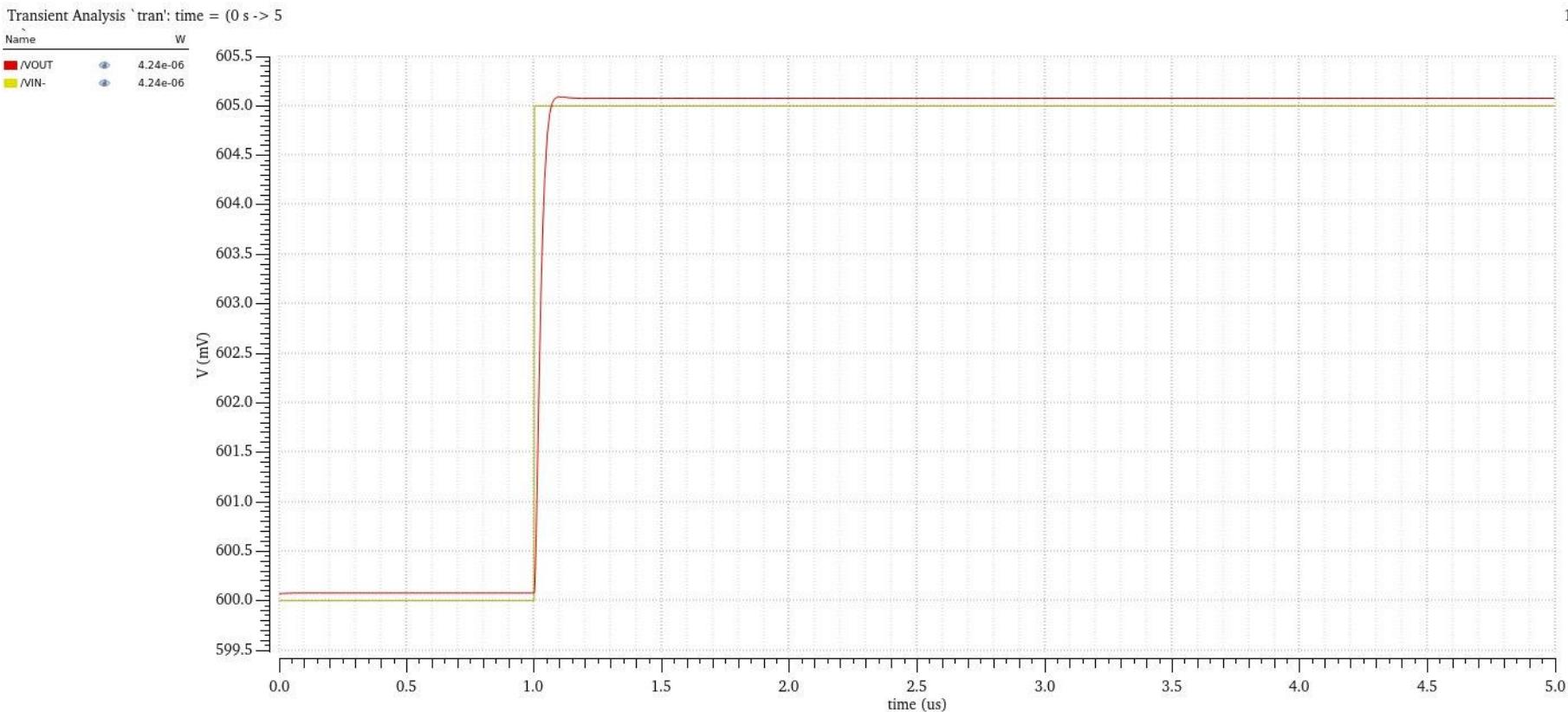
	Hand Analysis	simulation
SR	5.5 M	5M , 5.3M

Closed-Loop OTA Simulation

- OTA and the bias circuit with DC OP
- Loop gain
- Slew rate
- **Settling time**

Settling time

□ Calculate the output rise time from simulation.



5T_OTA: MILLER_OTA_CL:1 | `riseTime(v("VOUT")?result "tran..."` | 40.33n | < 70n | pass

Settling time

- Compare simulation results with hand calculations in a table

$$trise = 2.2\tau_{CL}$$

$$\tau_{CL} = \frac{1}{\omega_{p,CL}} = \frac{A_{CL}}{\omega_u}$$

	HA	Sim.
trise	57n s	40.3n s

$$trise = 2.2 * \frac{1}{\omega_u} = \frac{2.2}{2\pi * fu} = 70n\ s \text{ using the hand analysis fu}$$

$$trise = 2.2 * \frac{1}{\omega_u} = \frac{2.2}{2\pi * fu} = 57n\ s \text{ using the Simulation fu}$$

- Do you see any ringing? Why?

➤ Yes , because our PM lies between 72.4 and 76.3 which indicates that we have under damped response ($\zeta < 1$), that is because we didn't make $gm_2 = 11.11 gm_1$, but a little bit smaller, as our spec was more flexible

ω_p/ω_u	Q	ω_u/ω_u	Phase margin (°)
1	1	0.786	51.8
2	0.707	0.910	65.5
3	0.577	0.953	72.4
4	0.500	0.972	76.3

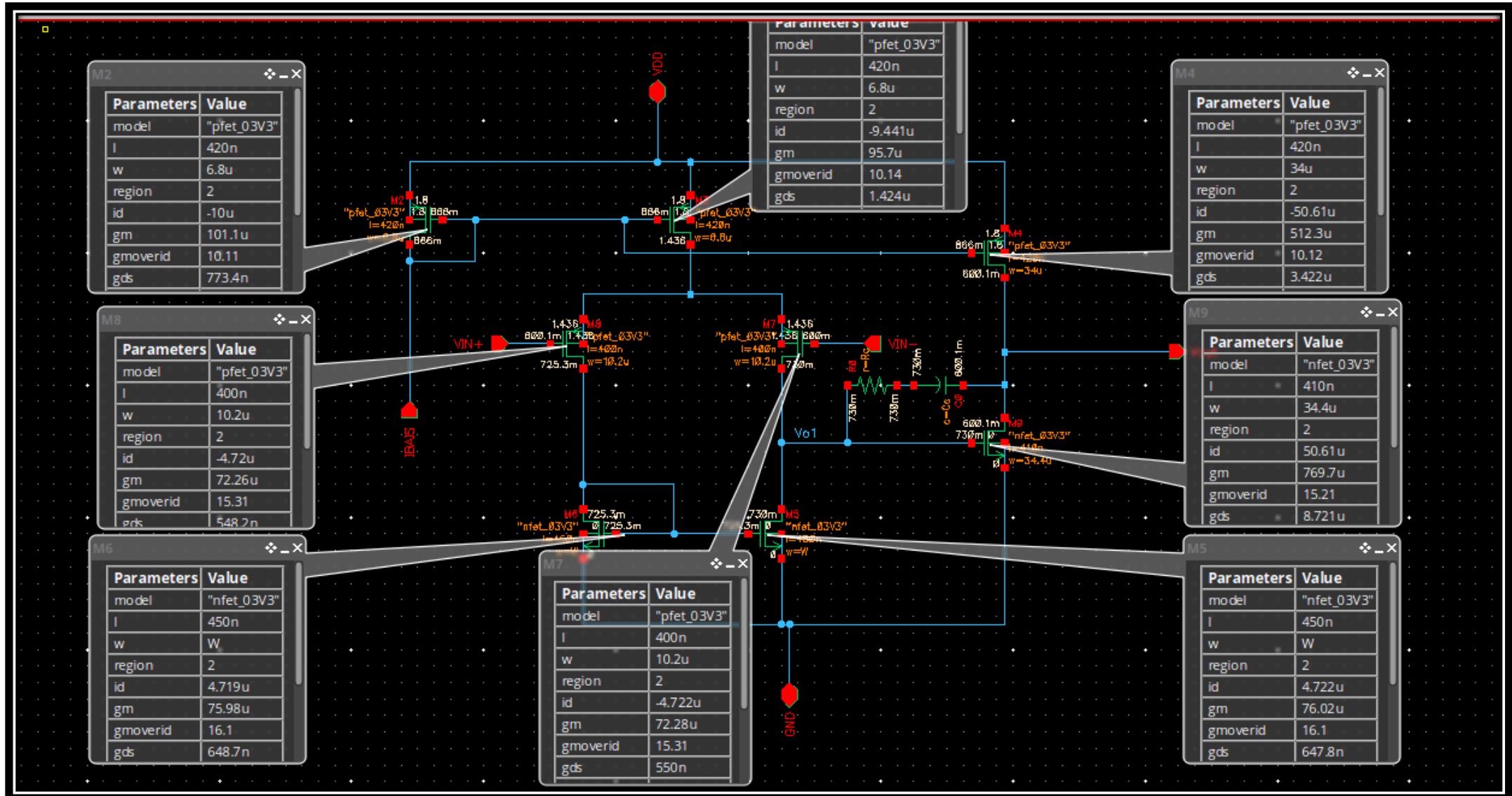
DC Closed Loop AC Open-Loop OTA Simulation

- ❑ the OTA and bias circuit with DC node voltages

- ❑ Diff small signal ccs
- ❑ CM small signal ccs
- ❑ CMRR
- ❑ Diff large signal ccs
- ❑ CM large signal ccs
- ❑ CM large signal ccs (GBW vs VICM)

the OTA and bias circuit with DC node voltages

□ OP



the OTA and bias circuit with DC node voltages

- Is the current (and gm) in the input pair exactly equal?
 - **no** , as $V_{ID} > 0 \Rightarrow$ current steering

- What is DC voltage at the output of the first stage? Why?
 - 725mv , Because V_{out1} follows Mirroring Node ,While Mirroring is the VGS of Cm load , **VGS=730 mv** , Well defind node

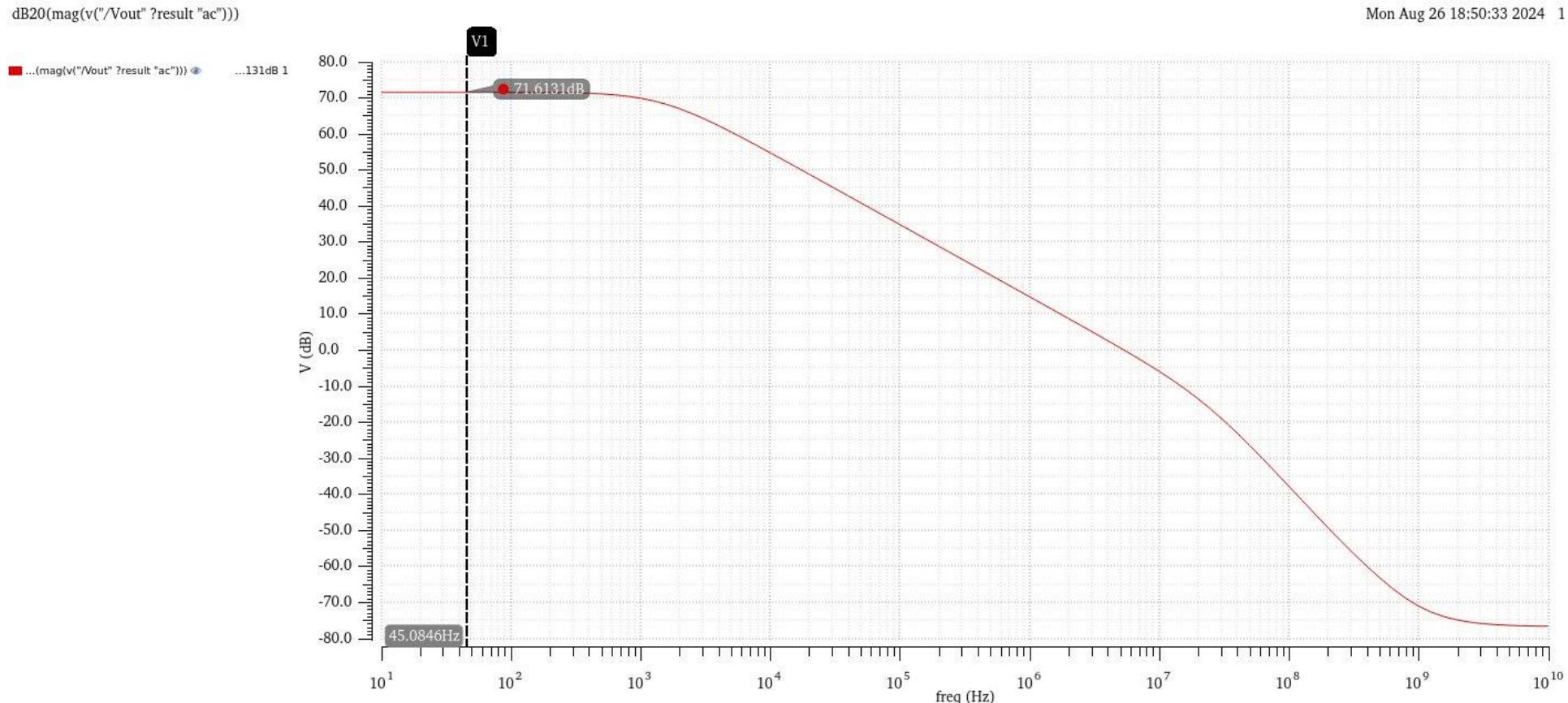
- What is DC voltage at the output of the second stage? Why?
 - **601 mv** , due to –ve feed back and that small error is due to non ideal feed back

DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs**
- CM small signal ccs
- CMRR
- Diff large signal ccs
- CM large signal ccs
- CM large signal ccs (GBW vs VICM)

Diff small signal ccs

- Plot diff gain (in dB) vs frequency.



- The margins we take gave bigger gain , as long we meet other specs no need for Tuning

Diff small signal ccs

- Plot diff gain (in dB) vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
5T_OTA:Miller_TB:1	/Vout	L			
5T_OTA:Miller_TB:1	fu	5.485M	> 5M		pass
5T_OTA:Miller_TB:1	A0I_dB	71.62	> 60		pass
5T_OTA:Miller_TB:1	AoI	3.809k	> 2000		pass

- The margins we take gave bigger gain , as long we meet other specs no need for Tuning
- If we aim to low power may be make tuning to remove excess gain

Diff small signal ccs

- Compare simulation results with hand calculations in a table.

$$Avd = Avd1 * Av2 = gm7(ro7||ro5) * (gm9 * (ro9||ro4)) = 3791$$

gm9 = 769 us , ro9 = 114.6 k Ω , ro7 = 1.81M Ω , ro5 = 1.54M Ω , gm7 = 72.28 us , ro4 = 292k Ω

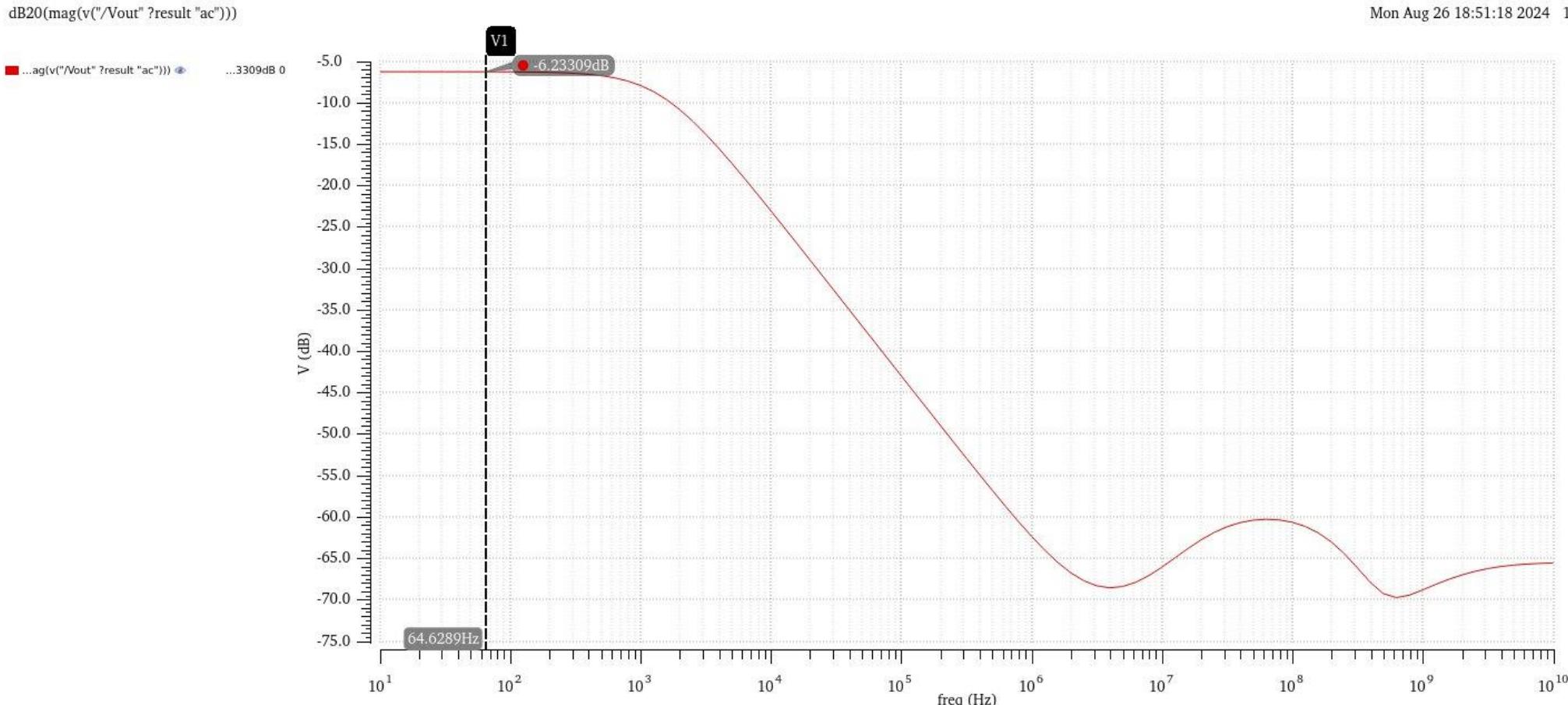
	Hand analysis	Simulation
Avd	3791	3809

DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs**
- CMRR
- Diff large signal ccs
- CM large signal ccs
- CM large signal ccs (GBW vs VICM)

CM small signal ccs

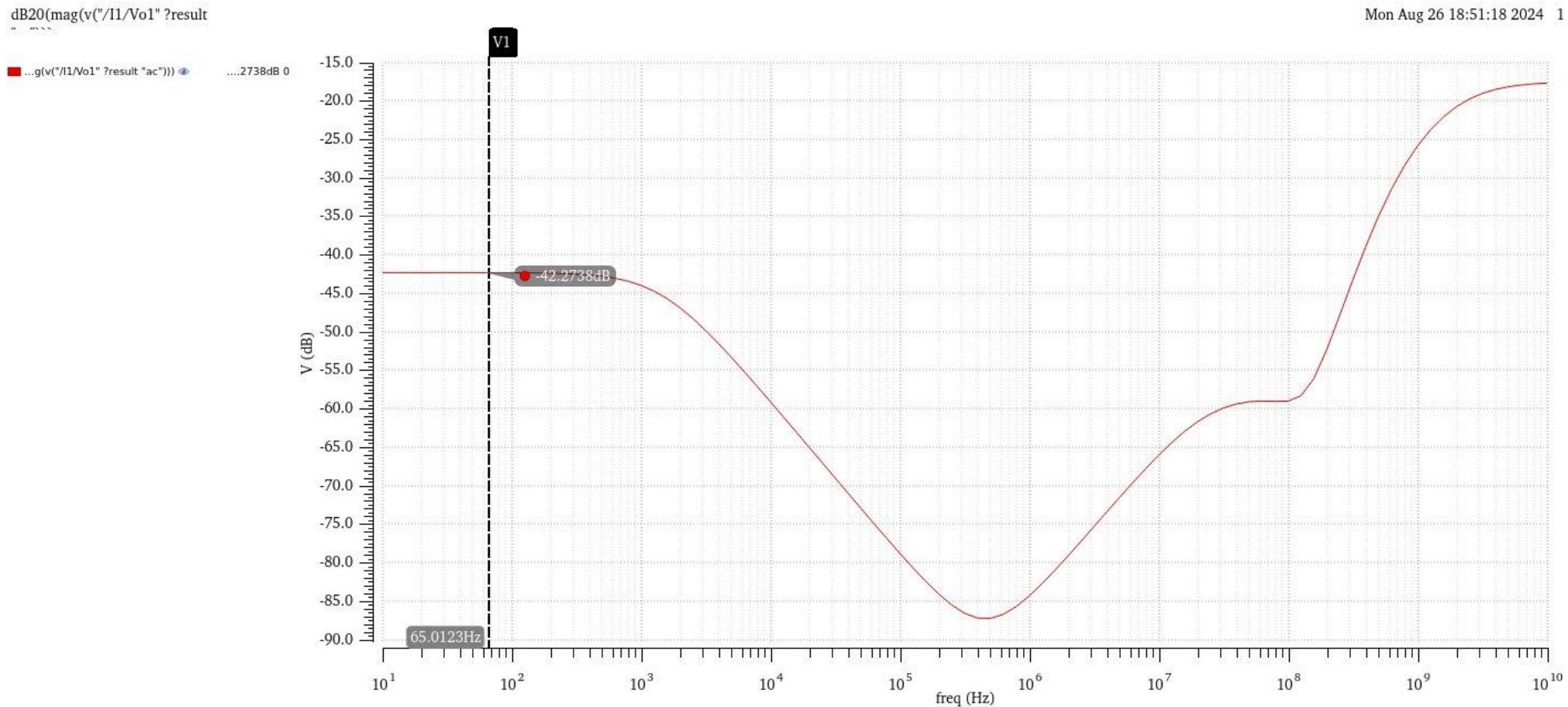
- Plot CM gain in dB vs frequency. **2 stages**



- Note that this is A_{vcm} of The entire 2 stages not the 1st stage only

CM small signal ccs

□ Plot CM gain in dB vs frequency. **1st stage only**



□ Note that this is Avcm 1st stage only

CM small signal ccs

- Compare simulation results with hand calculations in a table.

$$Avcm_{overall} = Avcm1 * Av2 = \frac{1}{2*gm6*ro3} * (gm9 * (ro9||ro4)) = 0.589$$

$$gm6 = 76 \text{ us}, ro3 = 704k \Omega, gm9 = 769 \text{ us}, ro9 = 114k \Omega, ro4 = 292k \Omega$$

	Hnad analysis	Simulation
Avcm	-4.6 dB	-6.23 dB

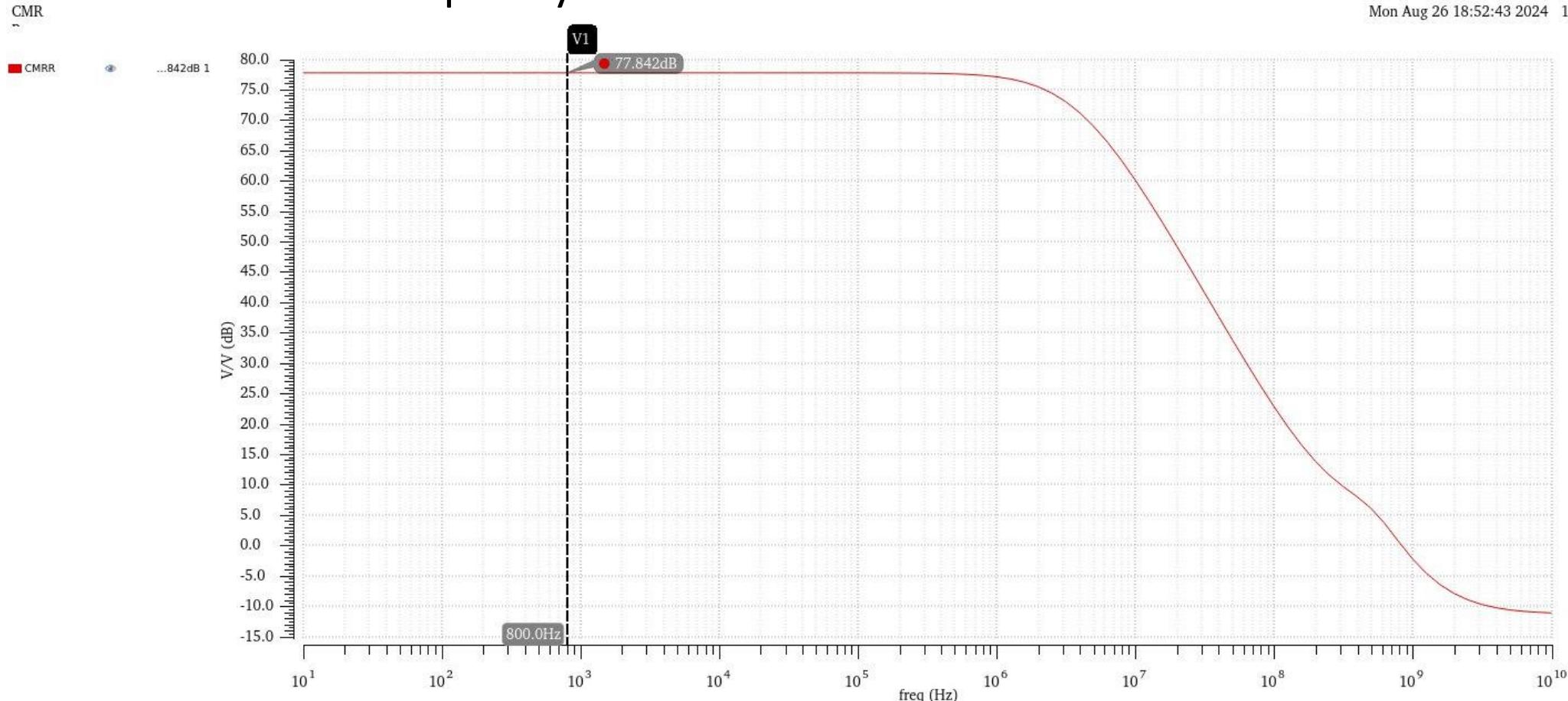
DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs
- **CMRR**
- Diff large signal ccs
- CM large signal ccs
- CM large signal ccs (GBW vs VICM)

CMRR

Plot CMRR in dB vs frequency.

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5T_OTA:Miller_TB:1	CMM_spec	77.84	> 74	pass
5T_OTA:Miller_TB:1	dvout	eval err		

CMRR

- Compare simulation results with hand calculations in a table.

$$Cmrr = \frac{Avd}{Acm} = (gm7 * (ro7||ro5)) * (2gm6 * r03)$$

$$ro7 = 1.81M \Omega , ro6 = 1.54M \Omega , gm7 = 72 \text{ us} , gm5,6 = 76 \text{ us} , ro3 = 704k \Omega$$

$$Cmrr = 76.2 \text{ dB}$$

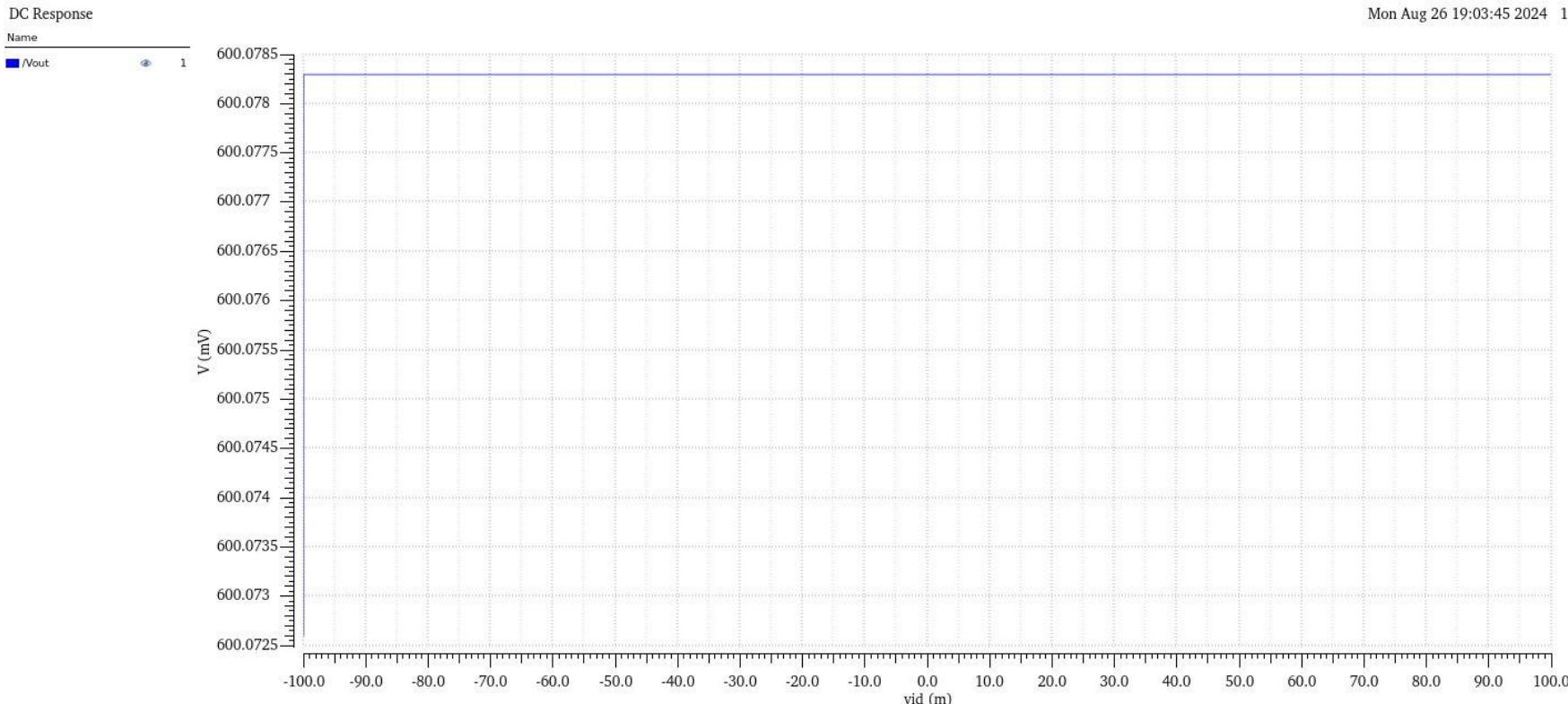
	Simulation	Hand analysis
$Cmrr$	76.17 dB	76.2 dB

DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs
- CMRR
- **Diff large signal ccs**
- CM large signal ccs
- CM large signal ccs (GBW vs VICM)

Diff large signal ccs

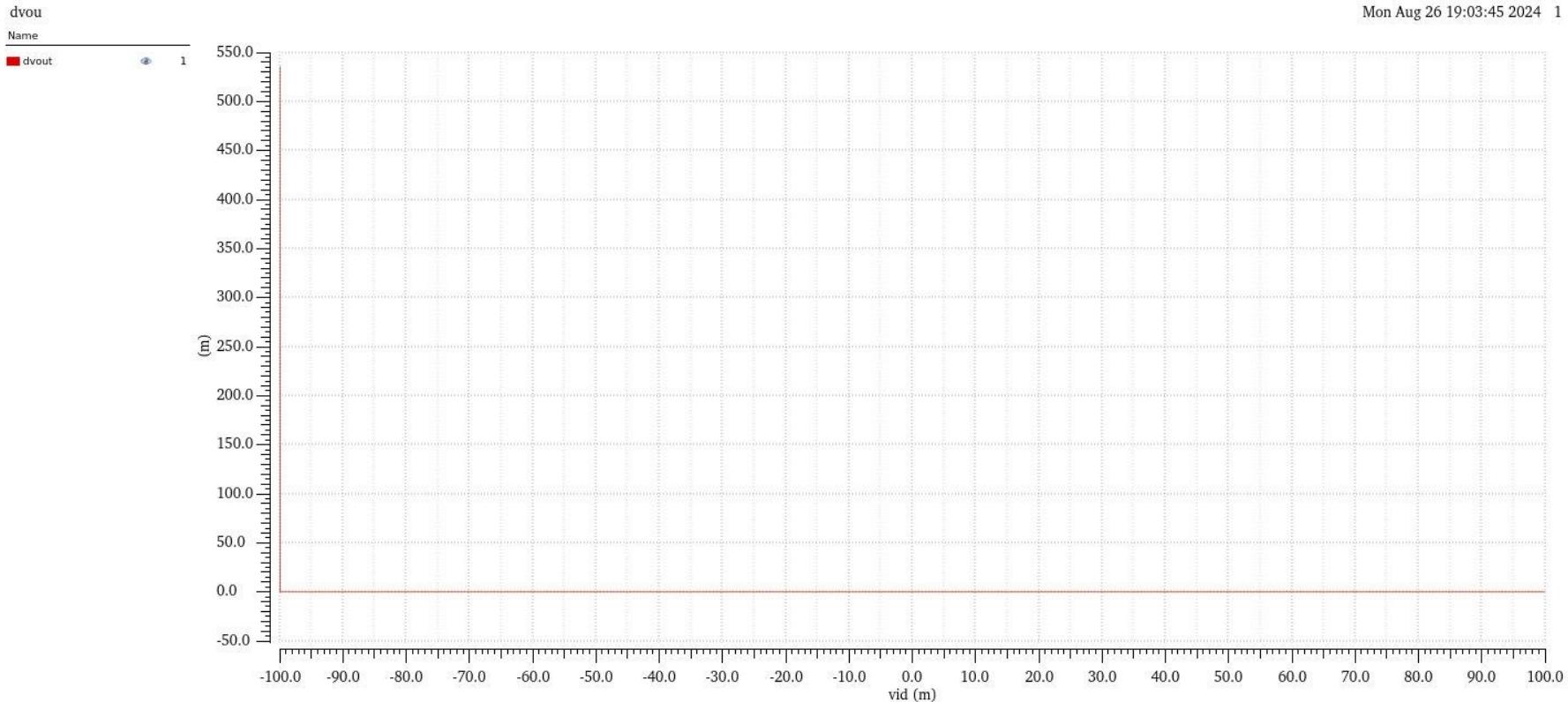
- ❑ Plot VOUT vs VID.



- ❑ what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.
 - 600mv , same as obtained from DC op sim, as we see Vout,cm is well defined .

Diff large signal ccs

- Plot the derivative of VOUT vs VID.



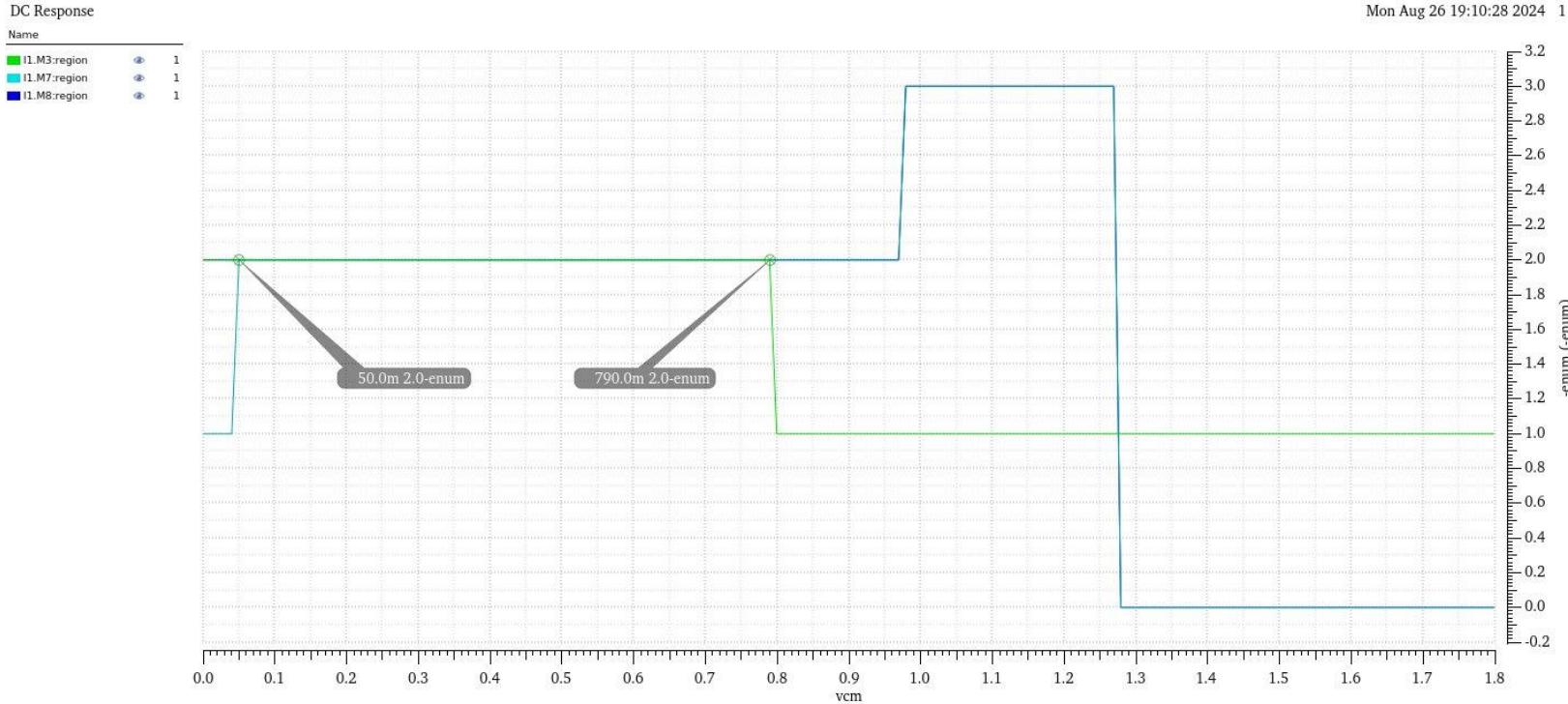
- due to switches trick , vid,LS has no effect on Cm level or operating point .

DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs
- CMRR
- Diff large signal ccs
- **CM large signal ccs**
- CM large signal ccs (GBW vs VICM)

CM large signal ccs

- Plot “region” OP parameter vs V_{CM} for the input pair and the tail current source



- Find the CM input range (CMIR). Compare with hand analysis in a table.

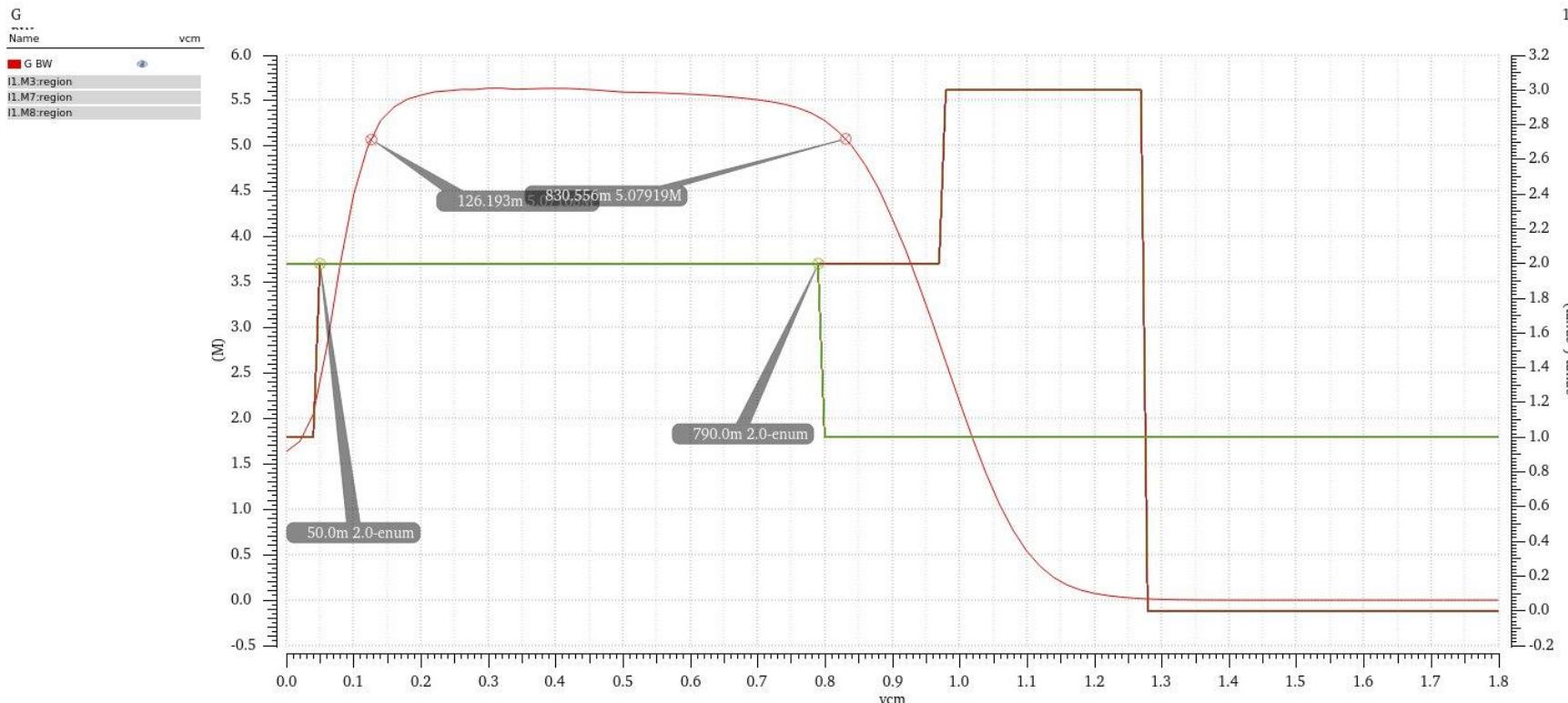
	Hand analysis	Simulation
High	850 mv	790 mv
Low	0	50 mv

DC Closed Loop AC Open-Loop OTA Simulation

- the OTA and bias circuit with DC node voltages
- Diff small signal ccs
- CM small signal ccs
- CMRR
- Diff large signal ccs
- CM large signal ccs
- **CM large signal ccs (GBW vs VICM)**

CM large signal ccs (GBW vs VICM)

- CM large signal ccs (GBW vs VICM)
- Calculate the input range as the range
- Range=704 mv



References

- ❑ Analog ic design by dr.hesham omran