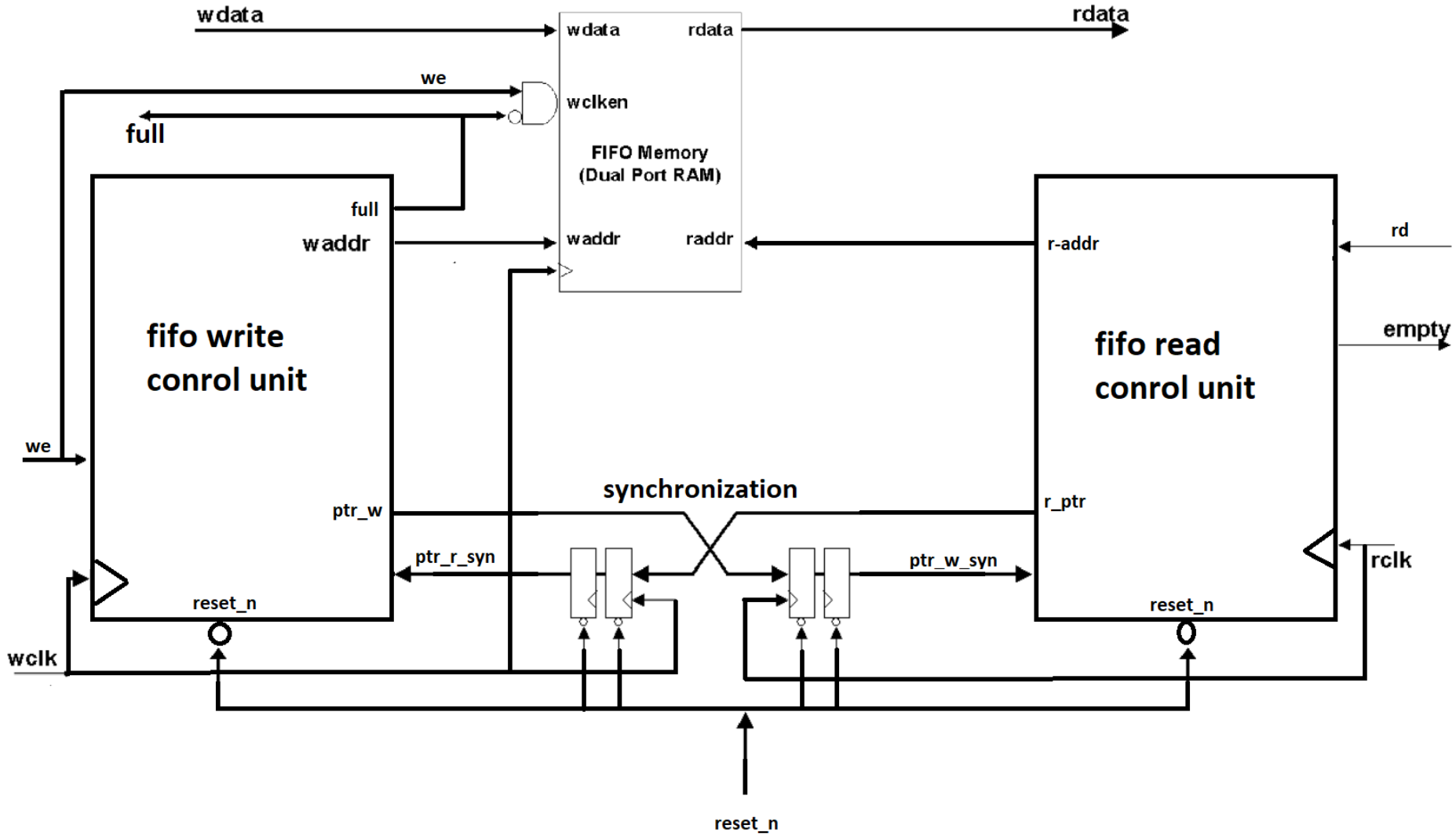
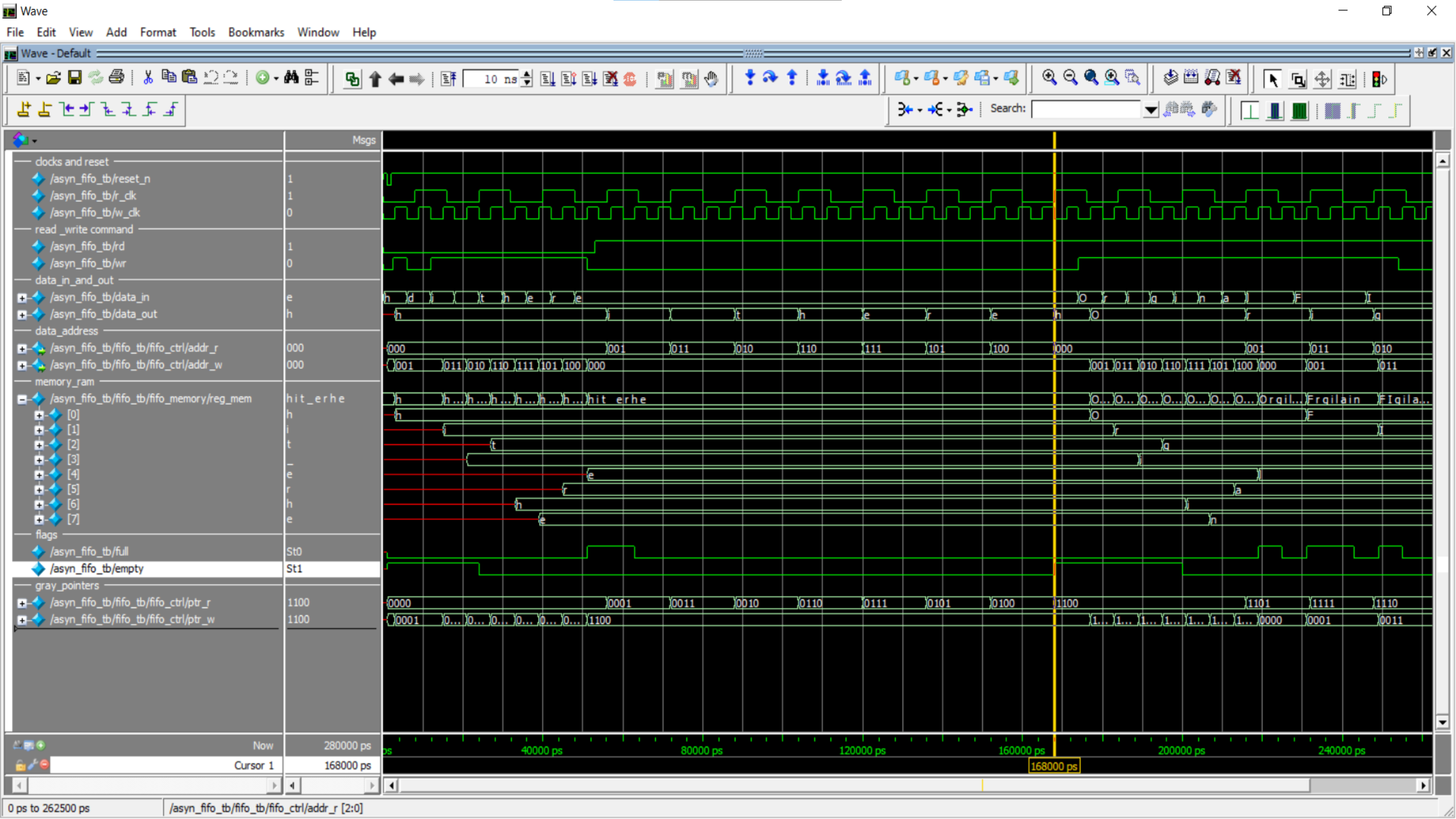
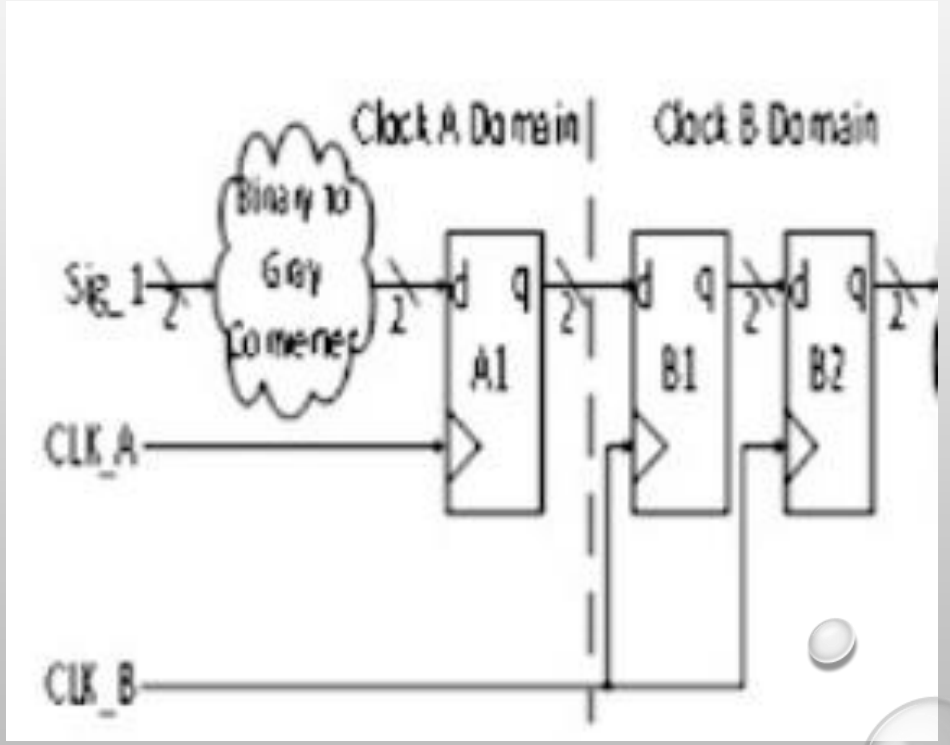
A N*B ASYNCHRONOUS FIFO WITH VERILOG HDL


wdata
wdata
rdata
rdata
we
wclken
full
FIFO Memory
(Dual Port RAM)
full
waddr
waddr
raddr
r-addr
rd
fifo write
conrol unit
fifo read
conrol unit
empty
we
synchronization
ptr_w
r_ptr
ptr_r_syn
ptr_w_syn
rclk
reset_n
reset_n
wclk
reset_n

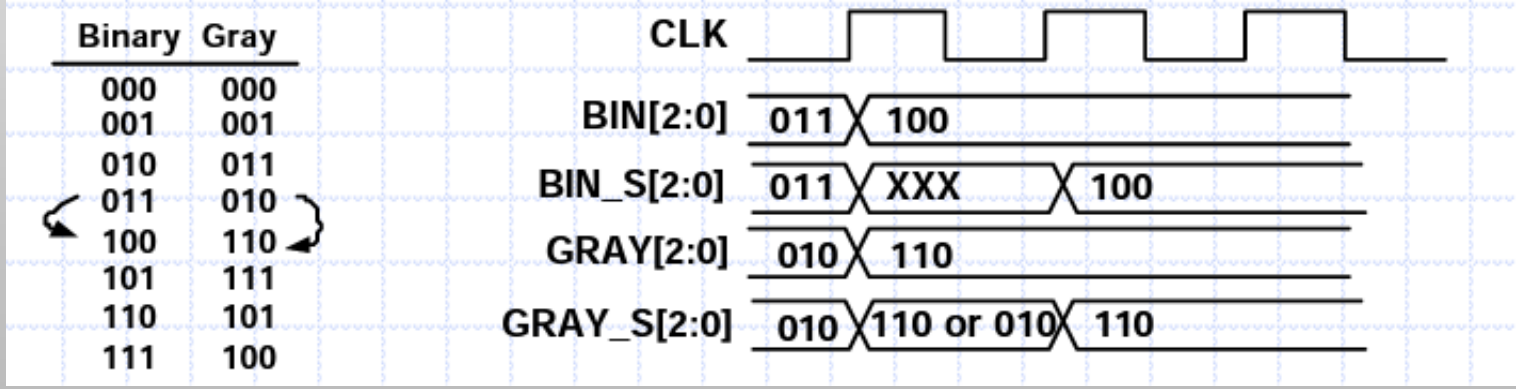

Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
clocks and reset
/asyn_fifo_tb/reset_n 1
/asyn_fifo_tb/r_clk 1
/asyn_fifo_tb/w_clk 0
read _write command
/asyn_fifo_tb/rd 1
/asyn_fifo_tb/wr 0
data_in_and_out
/asyn_fifo_tb/data_in e
/asyn_fifo_tb/data_out h
data_address
/asyn_fifo_tb/fifo_tb/fifo_ctrl/addr_r 000
/asyn_fifo_tb/fifo_tb/fifo_ctrl/addr_w 000
memory_ram
/asyn_fifo_tb/fifo_tb/fifo_memory/reg_mem hit_erhe
[0] h
[1] i
[2] t
[3] _
[4] e
[5] r
[6] h
[7] e
flags
/asyn_fifo_tb/full St0
/asyn_fifo_tb/empty St1
gray_pointers
/asyn_fifo_tb/fifo_tb/fifo_ctrl/ptr_r 1100
/asyn_fifo_tb/fifo_tb/fifo_ctrl/ptr_w 1100
Now 280000 ps
Cursor 1 168000 ps
40000 ps
80000 ps
120000 ps
160000 ps
200000 ps
240000 ps
168000 ps
0 ps to 262500 ps
/asyn_fifo_tb/fifo_tb/fifo_ctrl/addr_r [2:0]

WHY GRAY CODE

WHEN MULTI BIT SIGNALS ARE SYNCHRONIZED WITH 2 FLIP FLOP SYNCHRONIZER, EACH BIT IS SYNCHRONIZED USING SEPARATE 2-FF SYNCHRONIZER. METASTABILITY CAN CAUSE A FLIP FLOP TO SETTLE DOWN EITHER TO A TRUE VALUE OR A FALSE VALUE. SO, OUTPUT OF EVERY SYNCHRONIZER MAY NOT SETTLE TO CORRECT VALUE AT SAME CLOCK. THIS CAUSES DATA INCOHERENCY. IN ORDER TO SYNCHRONIZE MULTI BIT SIGNAL USING 2 FLIP FLOP SYNCHRONIZER METHOD, ONLY A SINGLE BIT CHANGE MUST BE GUARANTEED AT A PARTICULAR CLOCK CYCLE. THIS CAN BE ACHIEVED BY GRAY ENCODING.



- FOR EXAMPLE, IN ASYNCHRONOUS FIFO DESIGN, WHEN WE SYNCHRONIZE READ POINTER VALUE AFTER CONVERTING TO GRAY VALUE IN WRITE CLOCK DOMAIN USING 2-FF SYNCHRONIZER, THERE IS POSSIBILITY OF METASTABILITY. AS THERE IS ONLY ONE BIT CHANGE IN THE GRAY ENCODING SO EVEN IF THERE IS METASTABILITY WHEN CLOCK CROSSING, THE GRAY COUNTER VALUE WILL BE PREVIOUS VALUE. FOR EXAMPLE, READ POINTER (GRAY COUNTER) VALUE IS CHANGING FROM 010 TO 110 AND SYNCHRONIZED WITH WRITE CLOCK THEN DUE TO METASTABILITY (IF IT OCCURS) POSSIBILITY IS READ POINTER REMAINS 011



WHY DUAL GRAY COUNTER

WE USE N+1 BIT TO A N BIT FIFO ADDRESS

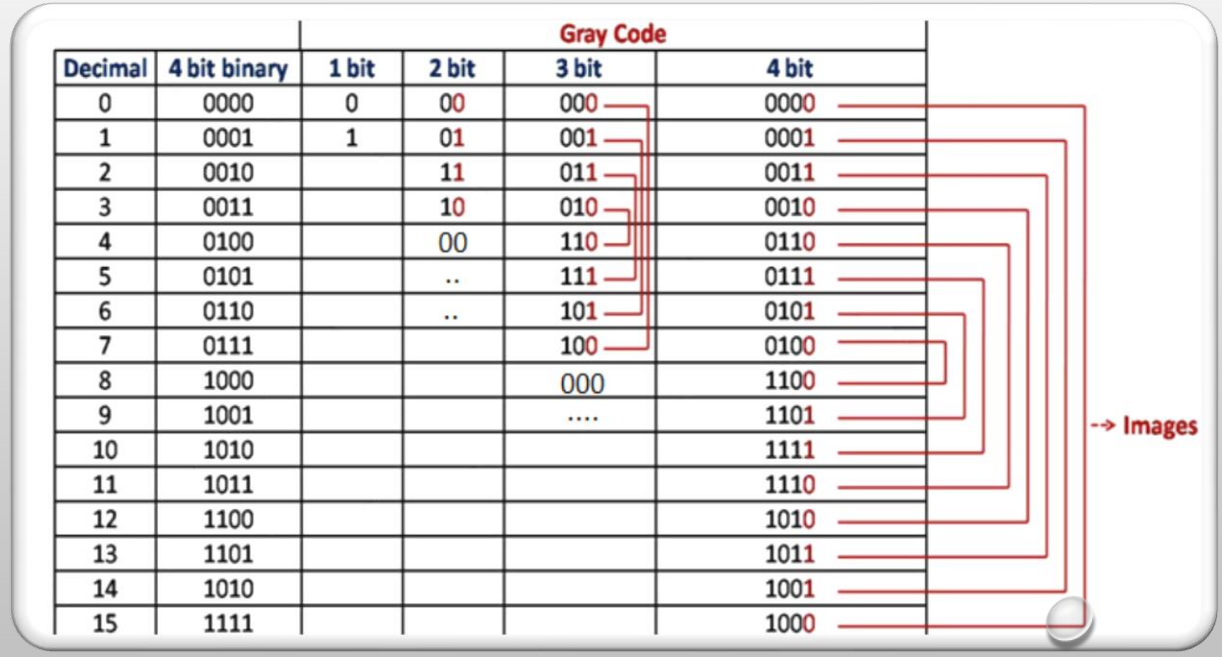
WHY? THAT'S BECAUSE WE NEED THE MSB TO FULL AND EMPTY FLAG –EXPLAINED IN

CODE-.

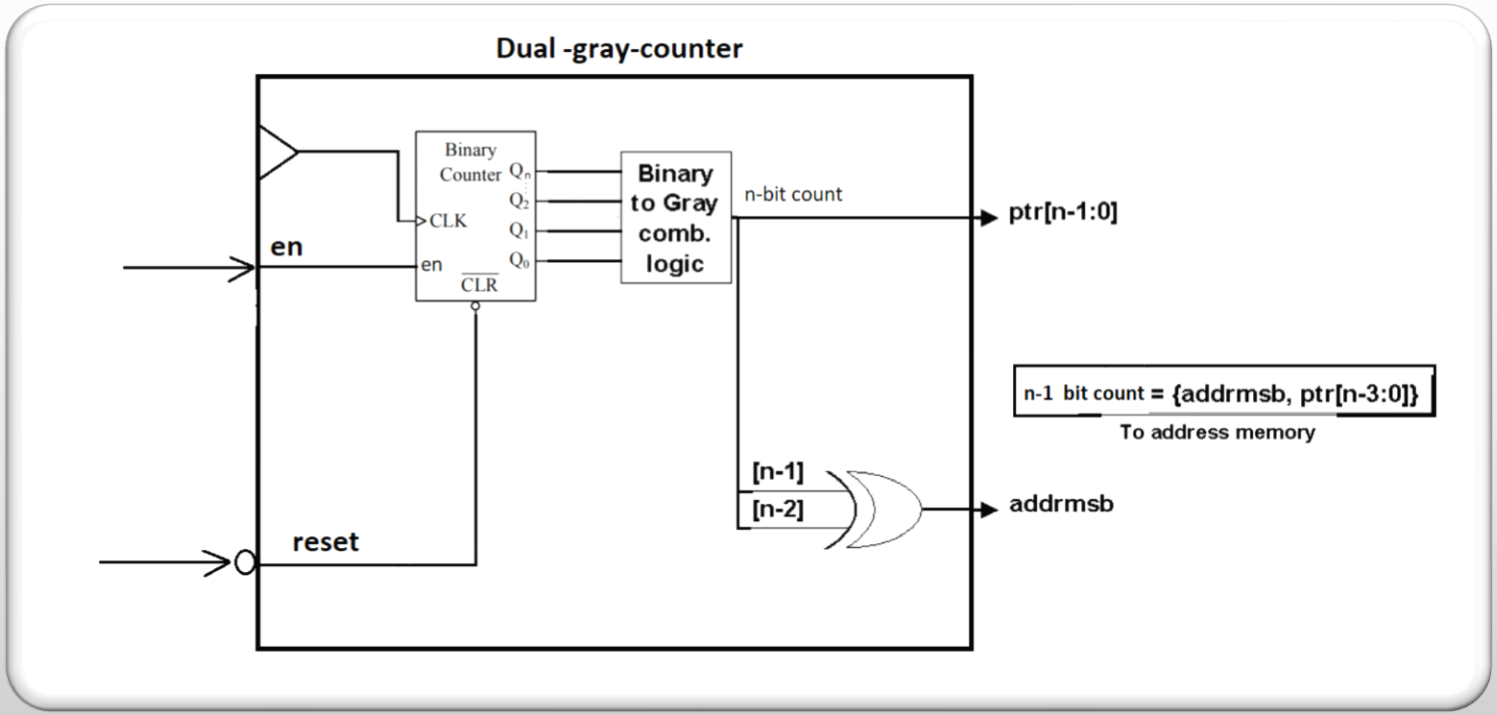
SO WHY DUAL COUNTER ?,CAN'T WE JUST

USE THE LAST N BITS AS AN ADDRESS?

ACTUALLY, WE CAN'T AND THE REASON OF THAT IS THE IMAGE OR MIRROR FEATURE WILL CAUSE MY DATA TO BE OVERWRITTEN OR READ FALSE DATA

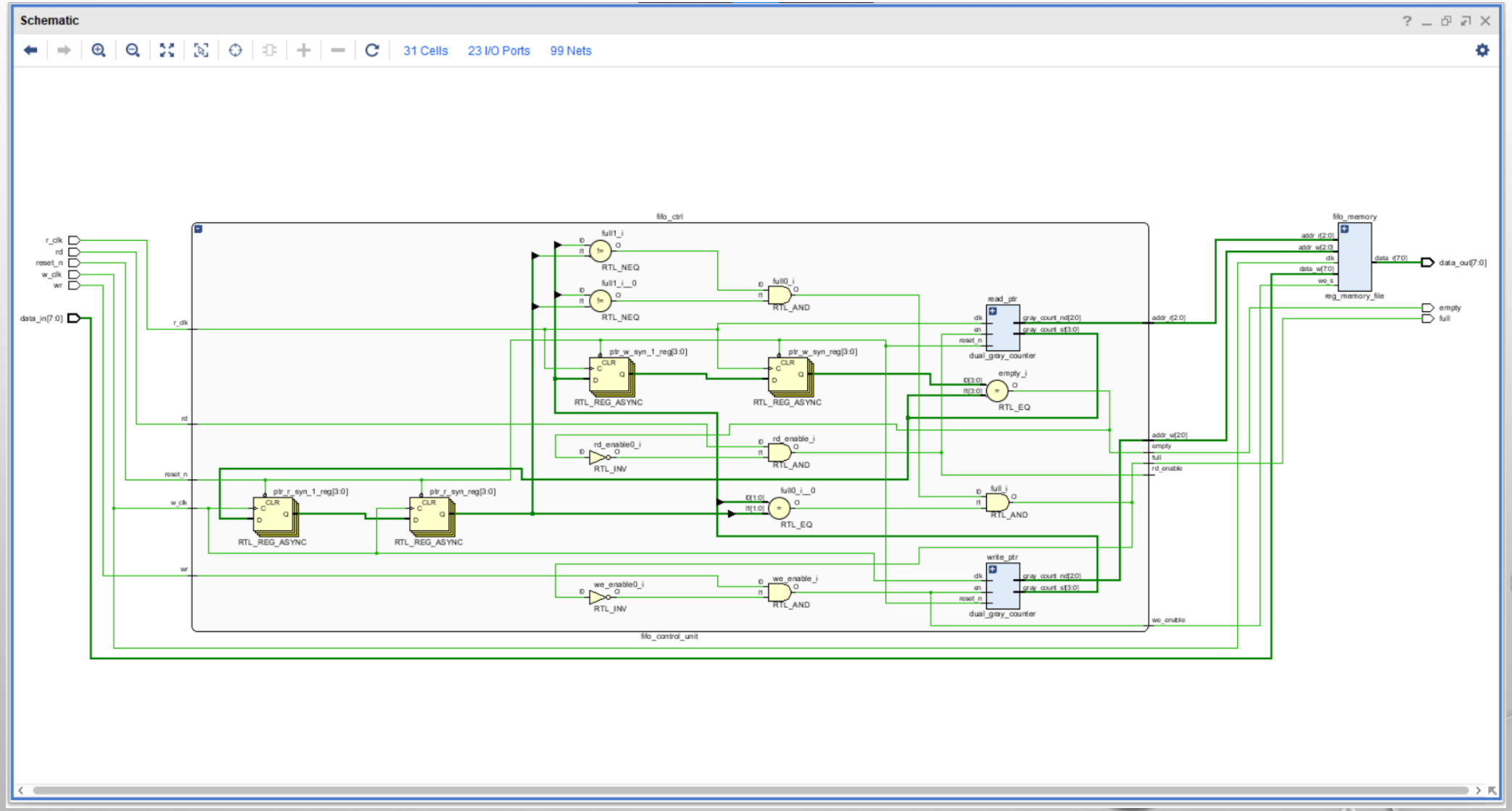


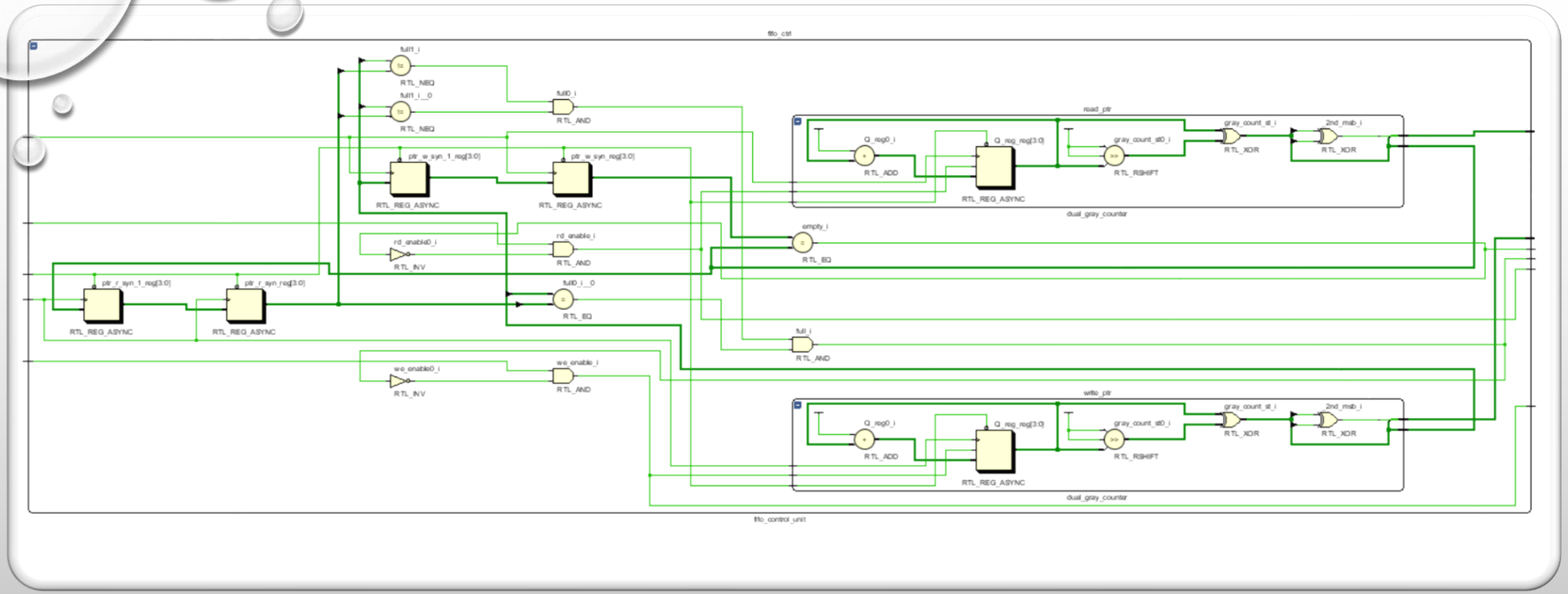
		Gray Code			
Decimal	4 bit binary	1 bit	2 bit	3 bit	4 bit
0	0000	0	00	000	0000
1	0001	1	01	001	0001
2	0010		11	011	0011
3	0011		10	010	0010
4	0100		00	110	0110
5	0101		..	111	0111
6	0110		..	101	0101
7	0111			100	0100
8	1000			000	1100
9	1001			....	1101
10	1010				1111
11	1011				1110
12	1100				1010
13	1101				1011
14	1010				1001
15	1111				1000



HOW WE GENERATE GRAY ADDRESS AND POINTER

VIVADO SCHEMATIC





CONTROL UNIT SCHEMATIC

THANK YOU

DON’T FORGET TO CHECK THE HDL AND GIVE A REVIEW .

LINK TO HDL:

HTTPS://GITHUB.COM/MOHAMED-ABDULRAHMAN5/ASYNCROUNUS_FIFO_BUFFER.GIT

DESIGNER : ENG. MOHAMED ABDULRAHMAN.

REFERENCES:

CLIFFORD E. CUMMINGS, SUNBURST DESIGN, INC

SYNCHRONIZATION IN DIGITAL LOGIC CIRCUITS RYAN DONOHUE