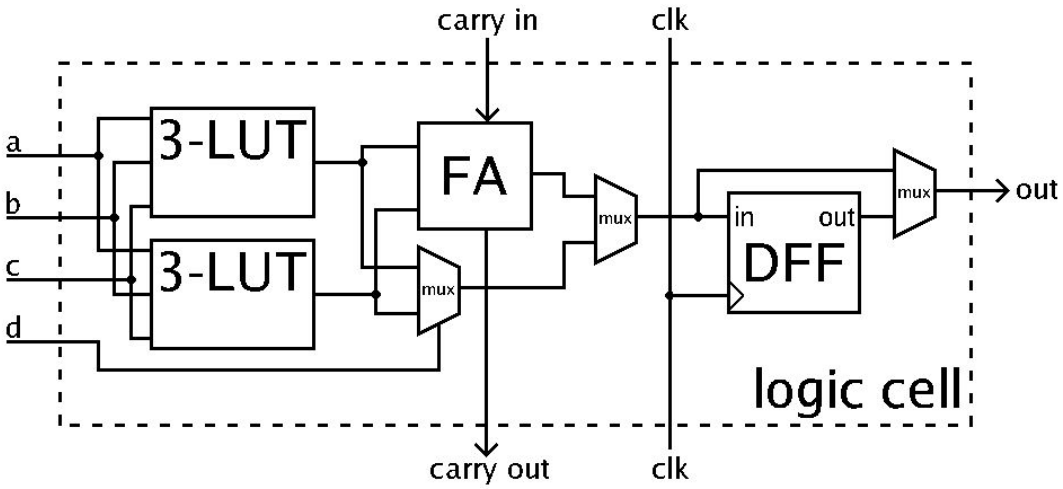
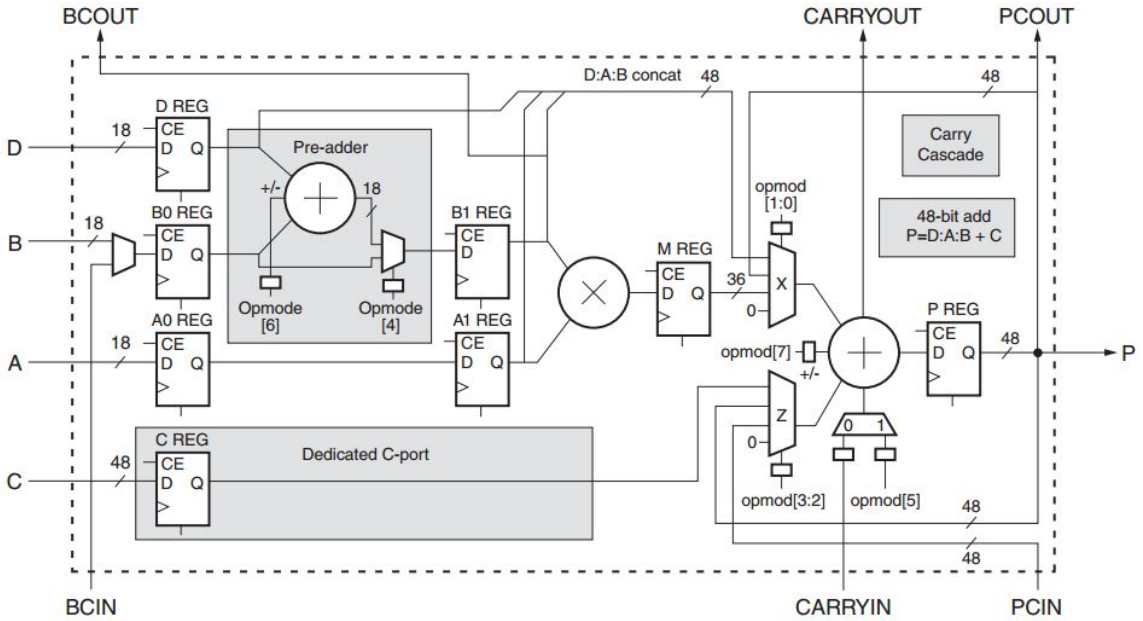
FPGA Contents

1- Programmable Logic (+Routing)



FPGA Contents

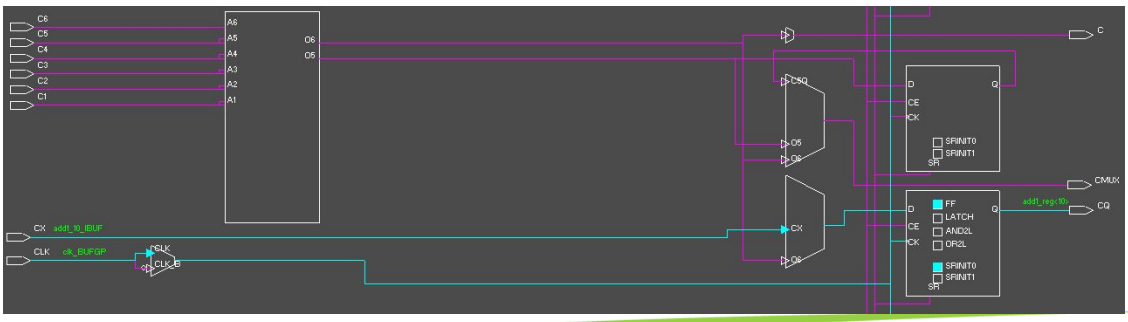
2- DSP Blocks



April 2020 I VHDL II

FPGA Contents: Exercise

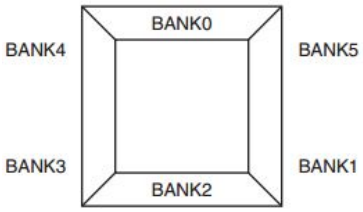
- Open your last project using Xilinx ISE
- PAR > View/Edit Routed Design (FPGA Editor)
- Identify:
  a. IOB of any pin
  b. Trace its route till its register
  c. Double click to view CLBs



FPGA Contents

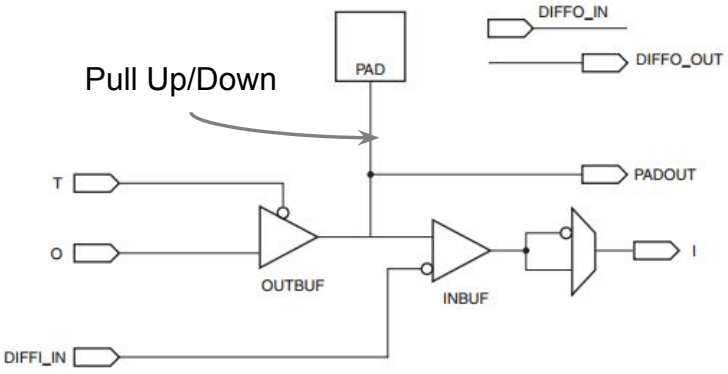
3- IO Pads

1. Single-Ended / Differential
2. Drive strength (Fan-out)
3. Slew rate
4. On-chip termination



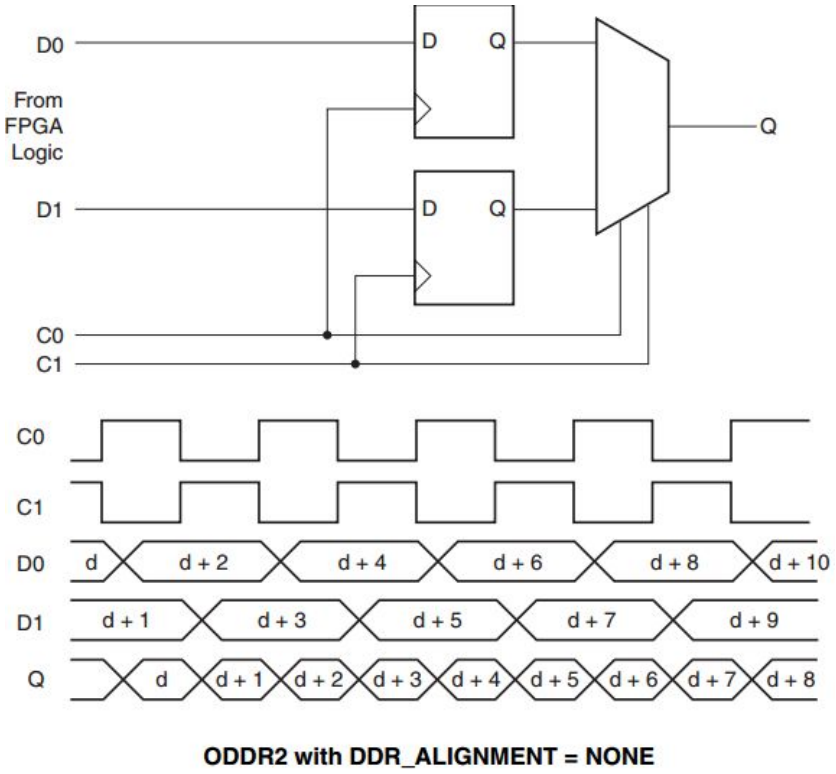
Xilinx Primitives [Single Ended]

1. IBUF (input buffer)
2. IBUFG (clock input buffer)
3. OBUF (output buffer)
4. OBUFT (3-state output buffer)
5. IOBUF (input/output buffer)



FPGA Contents

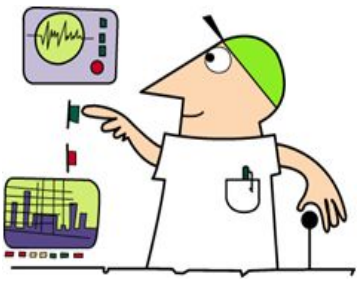
Many useful Blocks/Cells ..



ODDR2 with DDR_ALIGNMENT = NONE

FPGA Contents

- Low static and dynamic power (clock gating?)
- Multi-voltage, multi-standard IOs
- High-speed MGT serial transceivers
- Integrated Endpoint (PCIe)
- Integrated Memory Controllers
- Block RAM
- Clock Management
- Design Security



Lab #2

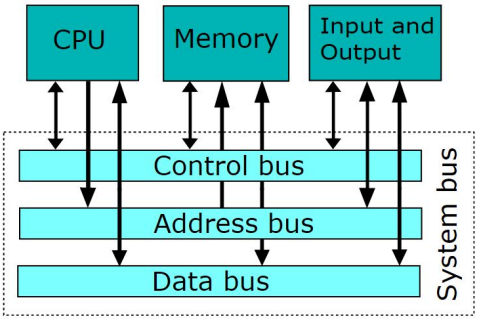
- Write a VHDL module to generate 2x and 0.5x of a given clock using PLL_BASE (xilinx primitive)
- Constrain the resulting clocks to IO pins, reimplement

```
pll_base_inst : PLL_BASE
generic map (
  BANDWIDTH => "OPTIMIZED",
  CLK_FEEDBACK => "CLKFBOUT",
  COMPENSATION => "SYSTEM_SYNCHRONOUS",
  DIVCLK_DIVIDE => a,
  CLKFBOUT_MULT => b,                  CLKFBOUT =>,
  CLKFBOUT_PHASE => 0.000,             CLKOUT0 =>,
  CLKOUT0_DIVIDE => c,                 CLKOUT1 =>,
  CLKOUT0_PHASE => 0.000,              CLKOUT2 =>,
  CLKOUT0_DUTY_CYCLE => 0.500,         CLKOUT3 =>,
  CLKOUT1_DIVIDE => d,                 CLKOUT4 =>,
  CLKOUT1_PHASE => 0.000,              CLKOUT5 =>,
  CLKOUT1_DUTY_CYCLE => 0.500,         LOCKED =>,
  CLKIN_PERIOD => e,                   RST => ,
  REF_JITTER => 0.010                  CLKFBIN =>,
  ) port map (                         CLKIN =>
       ..
```


Jump high: Computer Buses

Gen1: Single System Bus

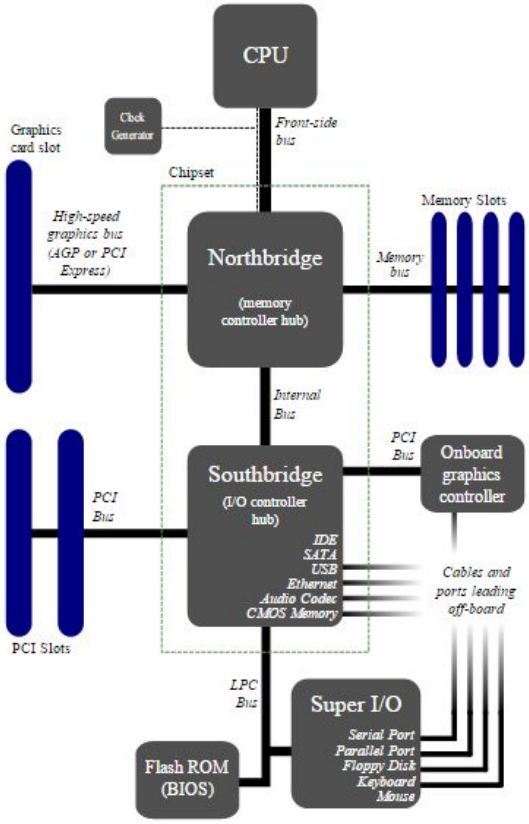
- Integrated
- Limit CPU Speed Evolution
- Configure using Jumpers:
  - Memory space
  - Interrupt Number and priority
- Good for embedded?



Jump high: Computer Buses

Gen2: Internal/External

- Decoupled fast CPUs
- AGP: Graphics cards
- Plug-n-Play
- 8bit → 64-bit PCI
- Multi-Gbps as in PCIe



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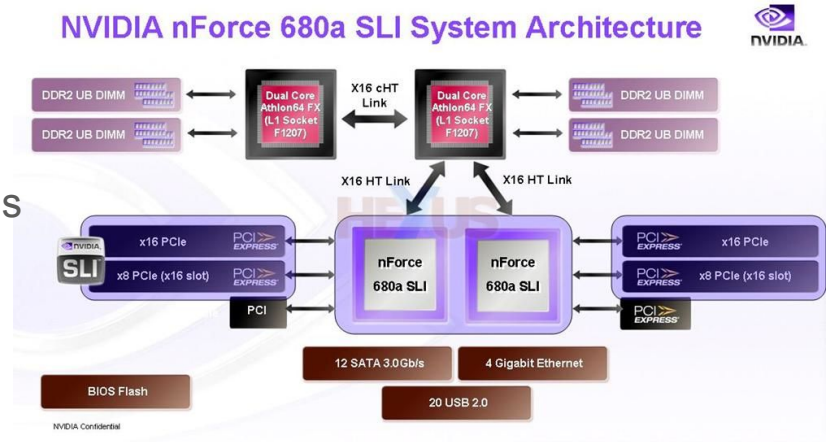
Jump high: Computer Buses

Gen3: Bus of Everything

- Emerged since 2001
- HyperTransport, InfiniBand
- Physical form can be flexible
- Packet oriented, SW overheads
- Replaces:
  - Front-side bus
  - Multi-core interconnect
  - Co-processor interconnect
  - Pluggable Cards slots
  - Routers for networking!



Valeo