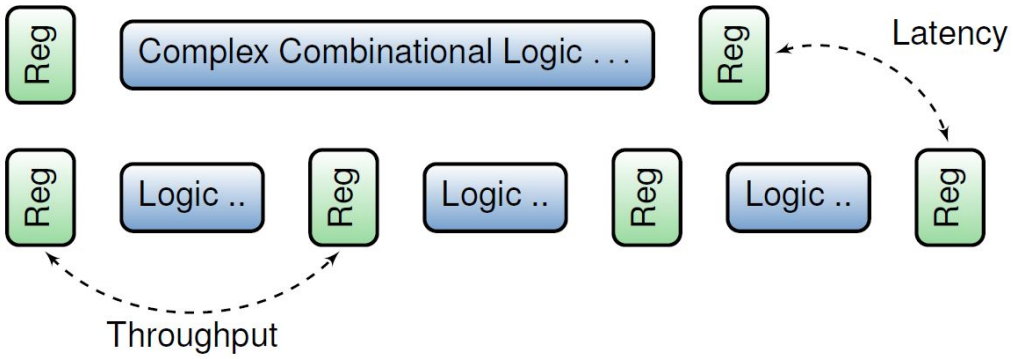
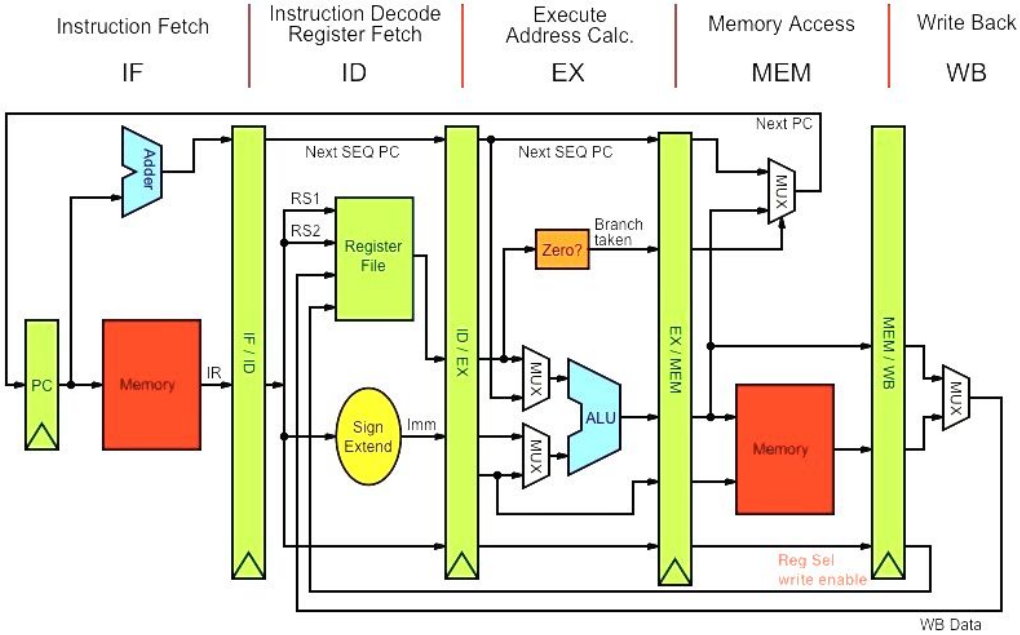
Pipelines



- Area?
- Power?
- Optimal number of stages?
- Automatic Register Balancing

Pipelines

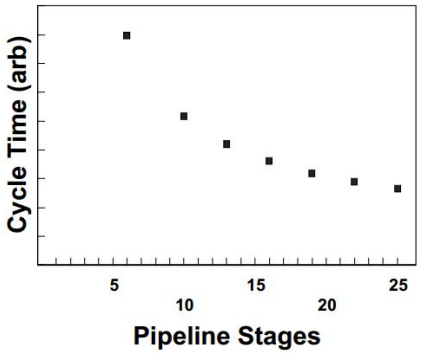
- Does **Feedback** break the pipe?

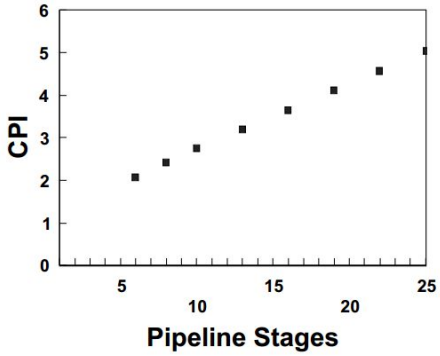


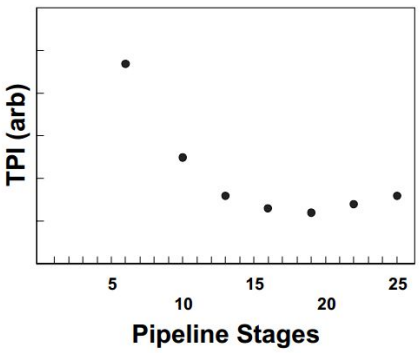
Lab #1

1. Write a vhdl module that adds 4 x 18bit registered inputs, and deliver the result at the clock positive edge
2. Write a TB to check results
3. Analyse
   a. RTL Schematics
   b. Technology Schematics
   c. Post PAR static timing
4. Add pipeline stages, calculate on 2 steps
5. Do steps 2~3
6. ~~Add 3 shift registers at output~~
7. ~~Do steps 2~3~~
8. ~~Enable register balancing~~
9. ~~Do steps 2~3~~

Pipelines

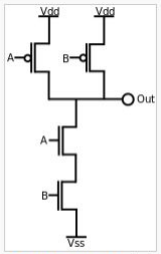






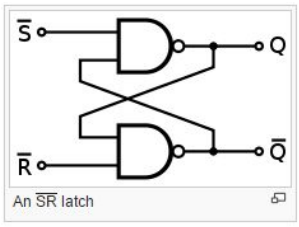
- CPU: Who breaks the pipeline?
- What sets the limits to other digital designs?

Pipelines: Latches



CMOS NAND gate

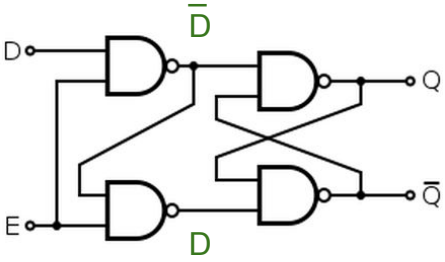
INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0



An $\overline{SR}$ latch

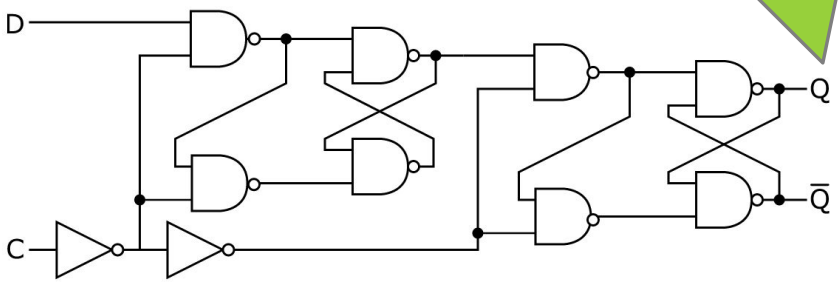
$\overline{SR}$ latch operation		
$\overline{S}$	$\overline{R}$	Action
0	0	not allowed
0	1	Q = 1
1	0	Q = 0
1	1	No Change

anim



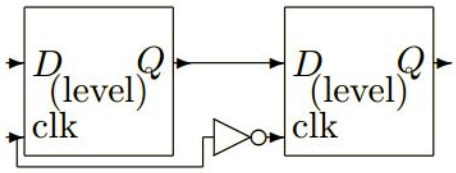
Latch:
- IO Ports
- Incomplete statements!

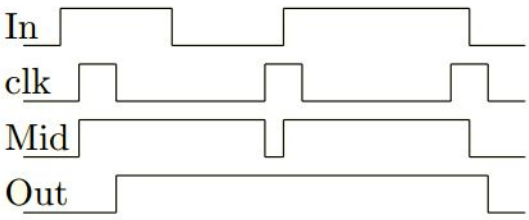
MS Edge D-Flip Flop:
- Registers
- Negative edge?

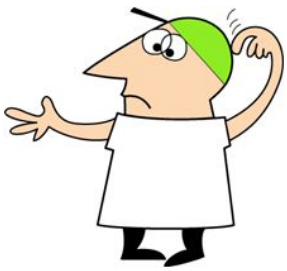


Why latches have poor timing?

Pipelines: Latches





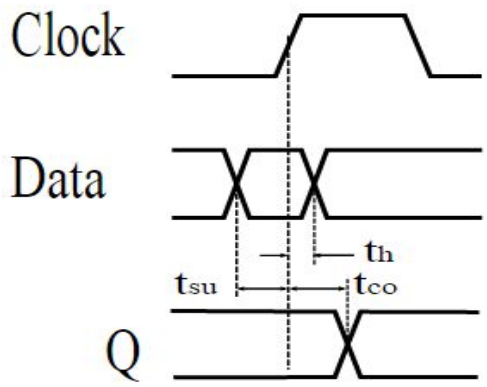


Pipelines: Latches

- Setup Time
- Hold time
- Clock-to-Output time

Maximum Combinational Delay

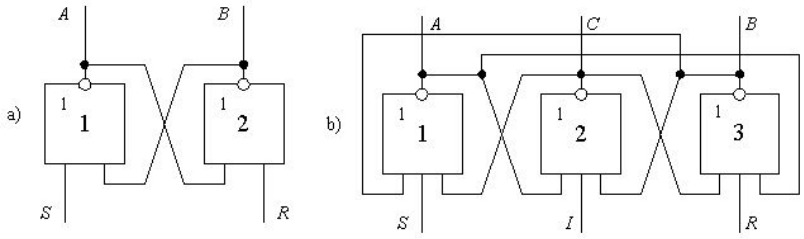
$$\frac{T_{clk} - T_{co} - T_{su}}{1/F_{max}}$$

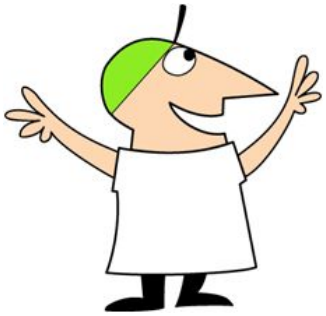


- Metastability:
  - Respect T_{su} and T_h
  - Practical range?
  - System inputs?
- In a shift register, Can $T_{co} < T_h$?

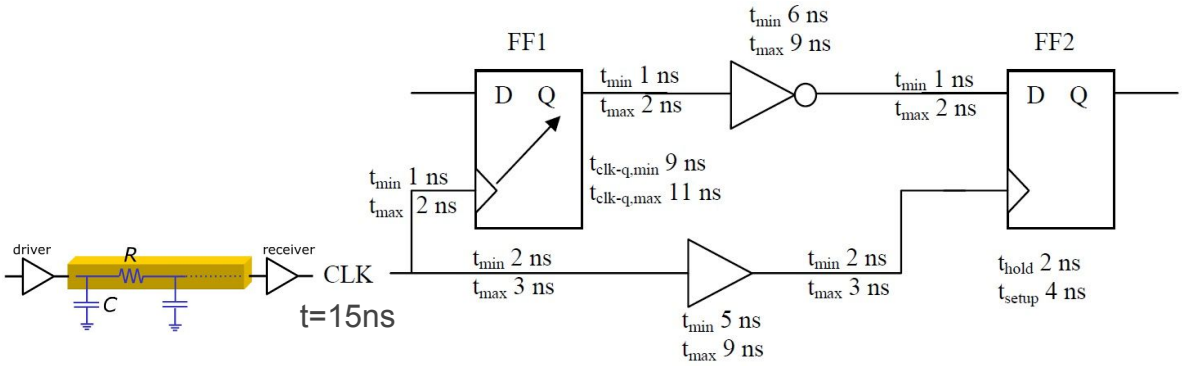
Pipelines: Out-of-the-box!

- Multi-valued Logic
- Wave pipelining!





Static Timing Analysis: Setup/Hold Violation?



Hold Analysis: Will new data overwrite the old at FF2?

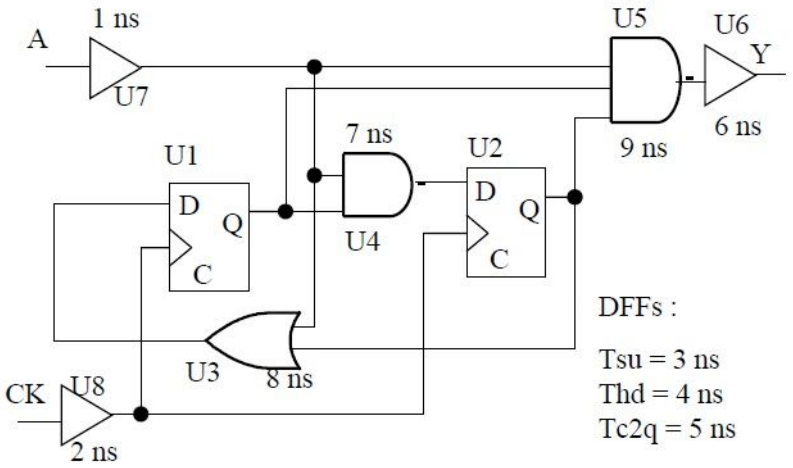
- Min Data Delay
- Max Clock Delay
- Tclk-Td = 18-17 = +ve slack

Setup Analysis: Will data miss the sampling edge at FF2?

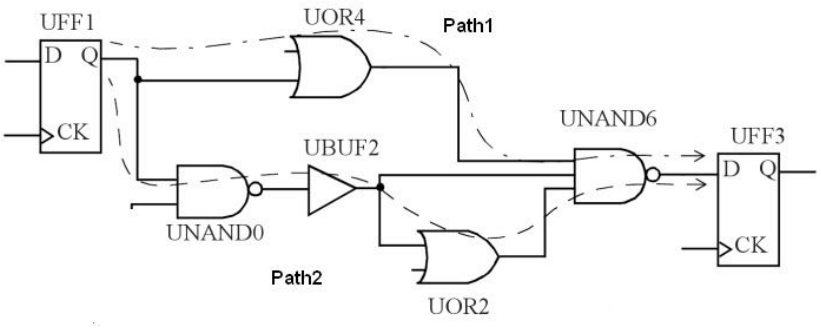
- Max Data Delay
- Min Clock Delay
- Tclk-Td = 20-26 = -ve slack

Static Timing Analysis

1. Reg-to-Reg delay [16ns]
   a. Possibilities?
2. Input Setup time [12-2ns]
   a. Tsu+Max.Td-Min.Tck
3. Input Hold time [-2ns]
   a. Thd+(Max.Tck-MinTd)
4. Clock-to-Output delay [22ns]
   a. Critical path?
5. Pin-to-Pin Combinational delay [16ns]
6. Max Clock frequency?
   a. 1/Max(Reg2Reg, Clk2Out, Pin2I



Static Timing Analysis



- Multiple Paths => Min, Max
- Backtrace method
- Combinational loops?
- System: Where to optimize?