Information Technology Institute

Digital IC Design

Presented by:

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Subject: Lab\_2 verilog

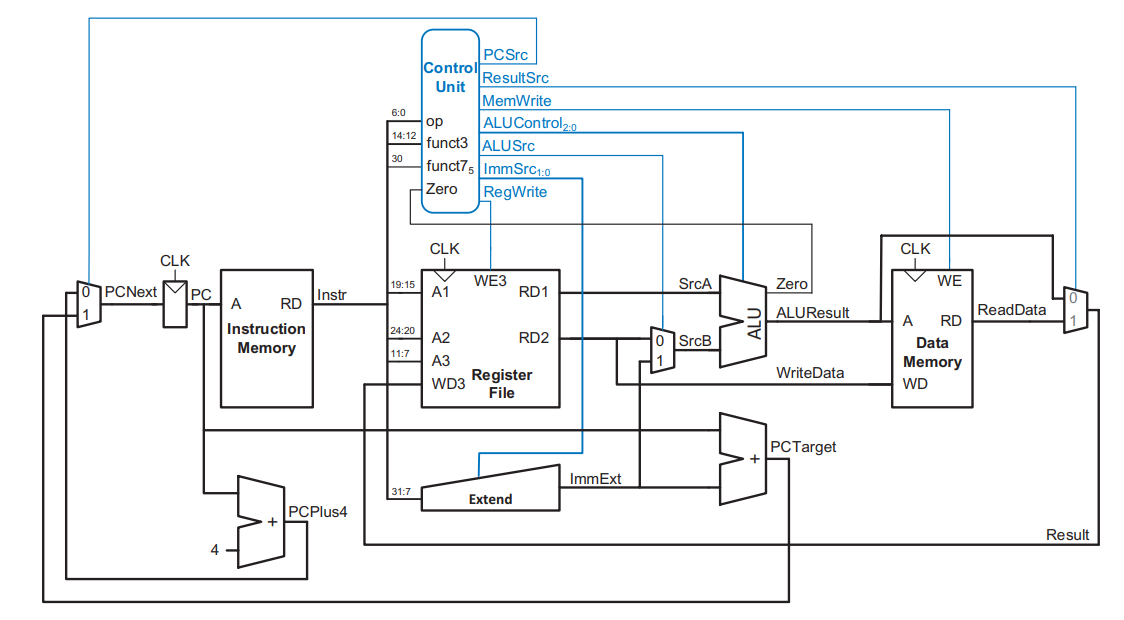
"RISC\_V single cycle Processor"

Under supervising of:

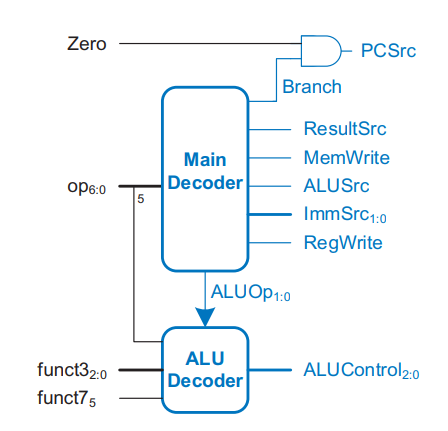
Eng. Rawan Naguib

●RISC\_V Single Cycle Processor Description :

» The single-cycle datapath, adding one piece at a time to the state elements from RISC\_V single cycle system Figure . The new connections are emphasized in black (or blue, for new control signals), whereas the hardware that has already been studied is shown in gray. The example instruction being executed is shown at the bottom of each figure. The program counter contains the address of the instruction to execute. The first step is to read this instruction from instruction memory. RISC\_V single cycle system Figure shows that the PC is simply connected to the address input of the instruction memory. The instruction memory reads out, or fetches, the 32-bit instruction, labeled Instr. In our sample program from RISC\_V single cycle system Figure, PC is 0x1000. (Note that this is a 32-bit processor, so PC is really 0x00001000, but we omit leading zeros to avoid cluttering the figure.)

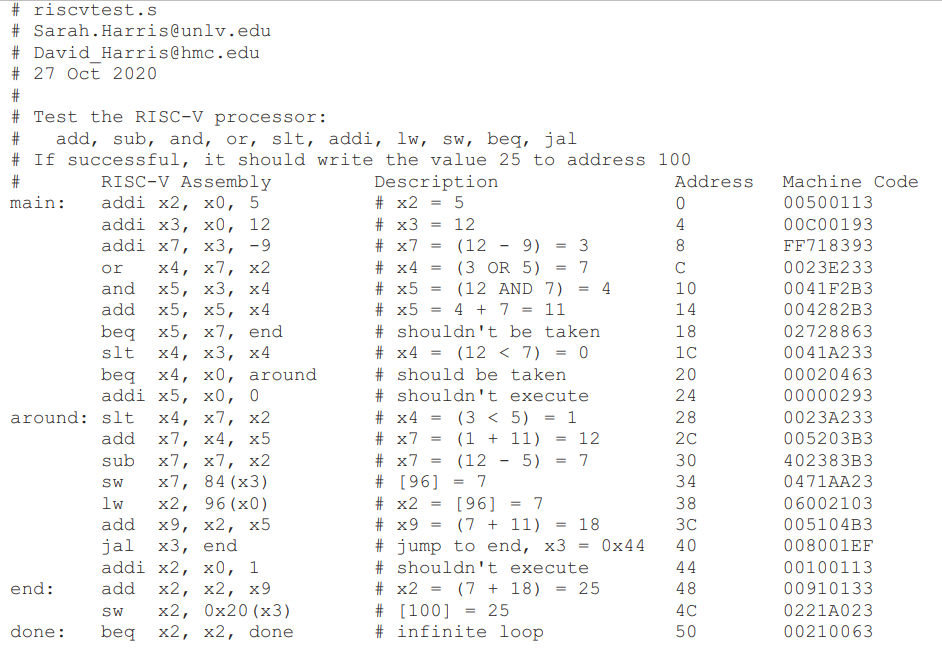


===========RISC\_V single cycle system Figure==========



===========RISC\_V single cycle control unit===========

●what I need in testbench :



●Simulation Result :

