Placement And Routing

By: Ahmed Elgammal

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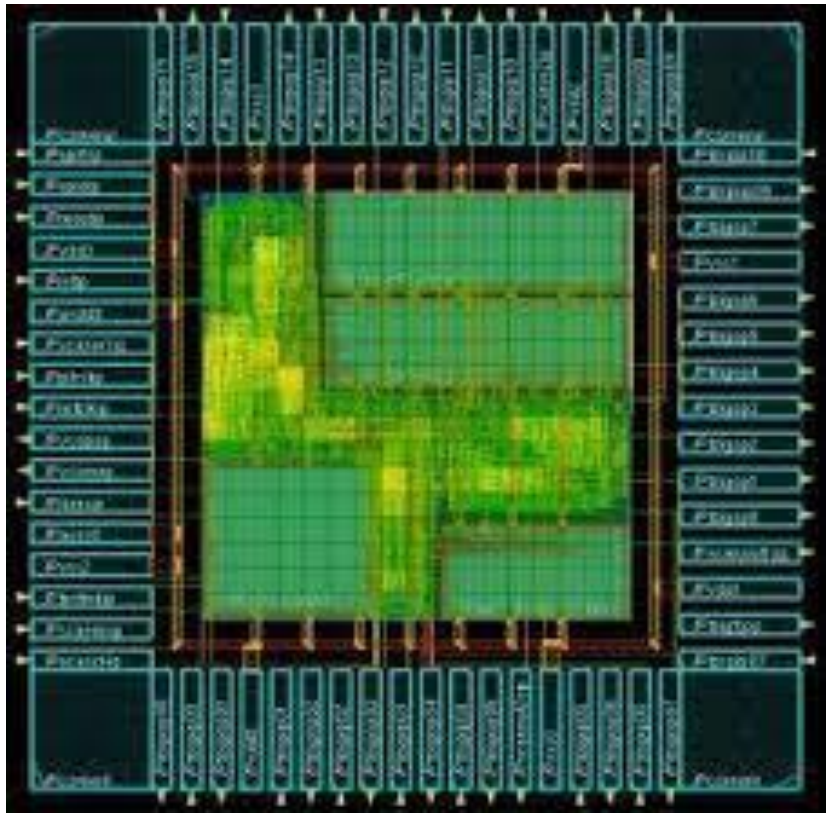
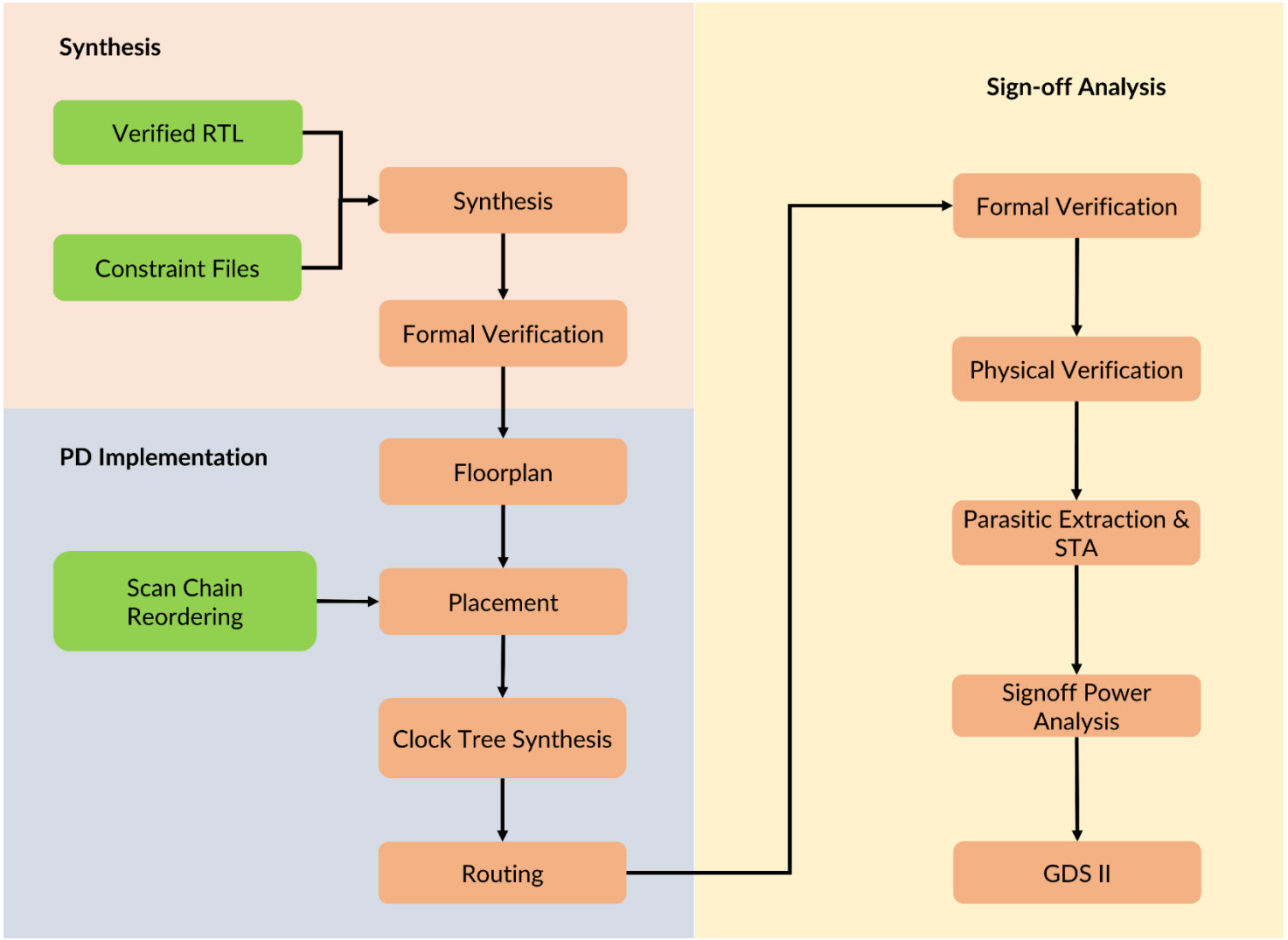


ASIC Flow



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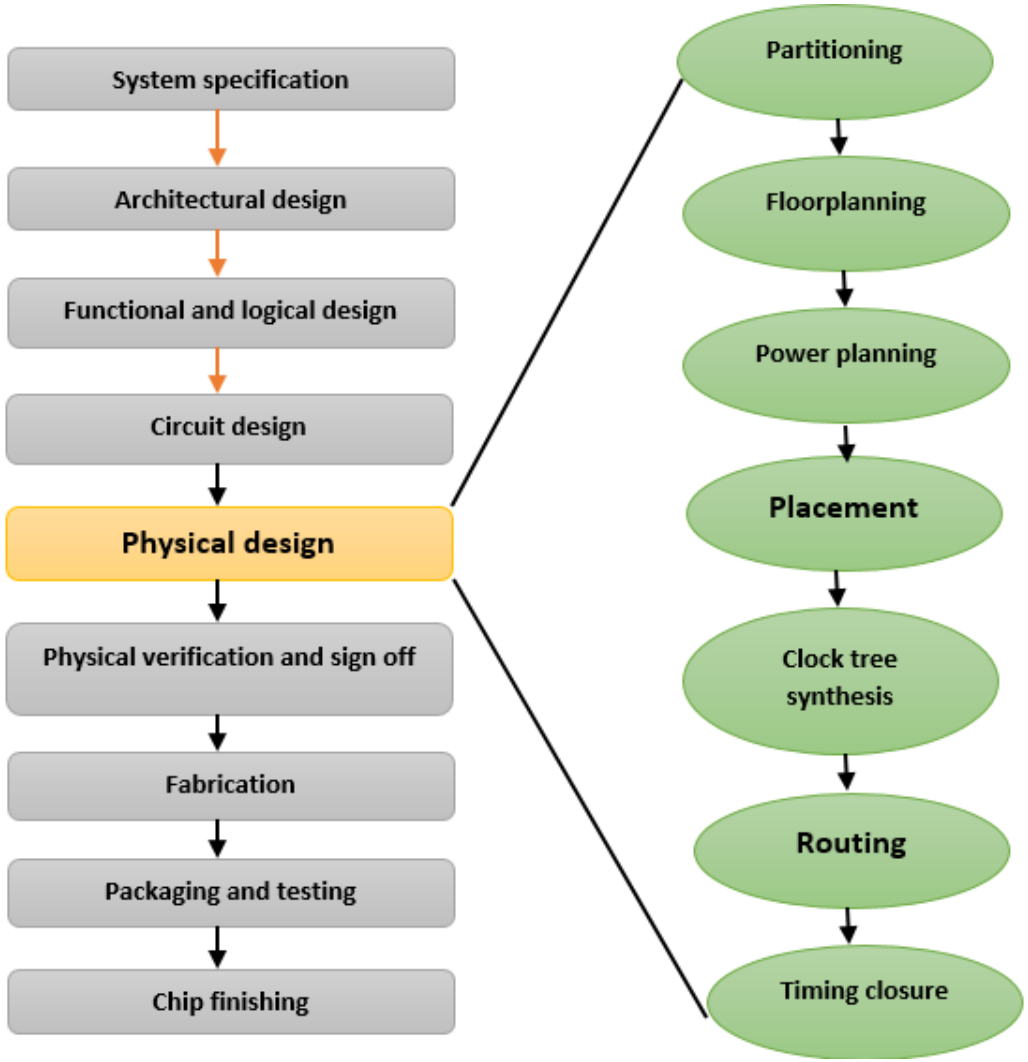
Physical design Steps



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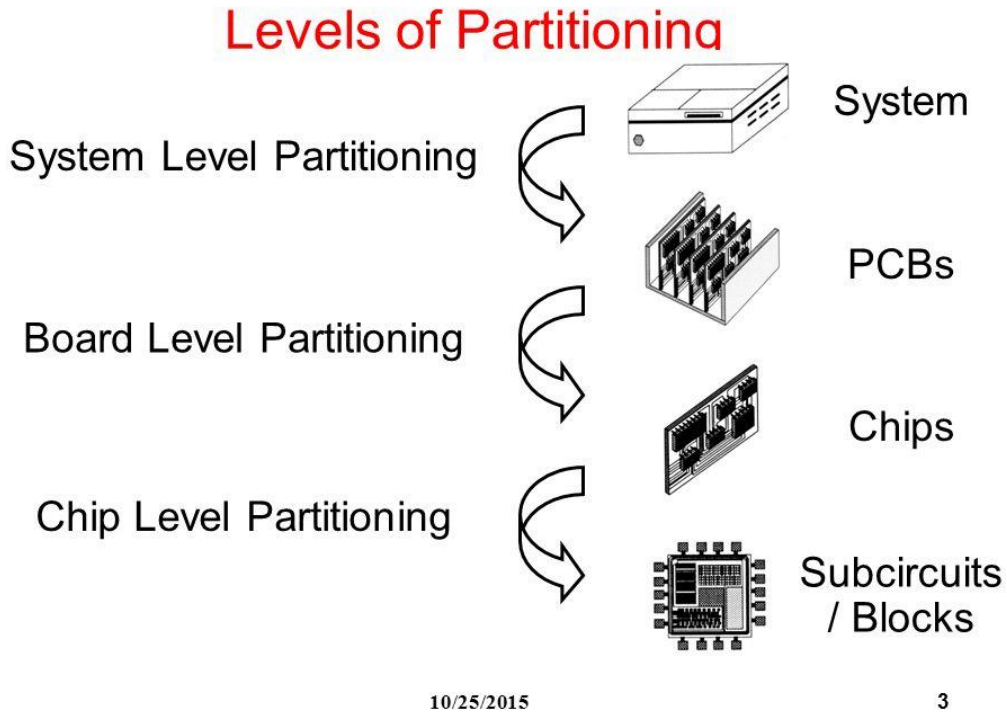
Partitioning

Physical design Steps

1. Partitioning:

is a preliminary step in the PnR flow that divides the design into manageable blocks or modules based on functionality, hierarchy, or timing constraints. It enables parallel processing during subsequent steps and facilitates easier placement and routing.

There are various factors to consider when determining the partitioning strategy, (size , complexity, performance requirements, power considerations, and physical constraints).



Floor Planning

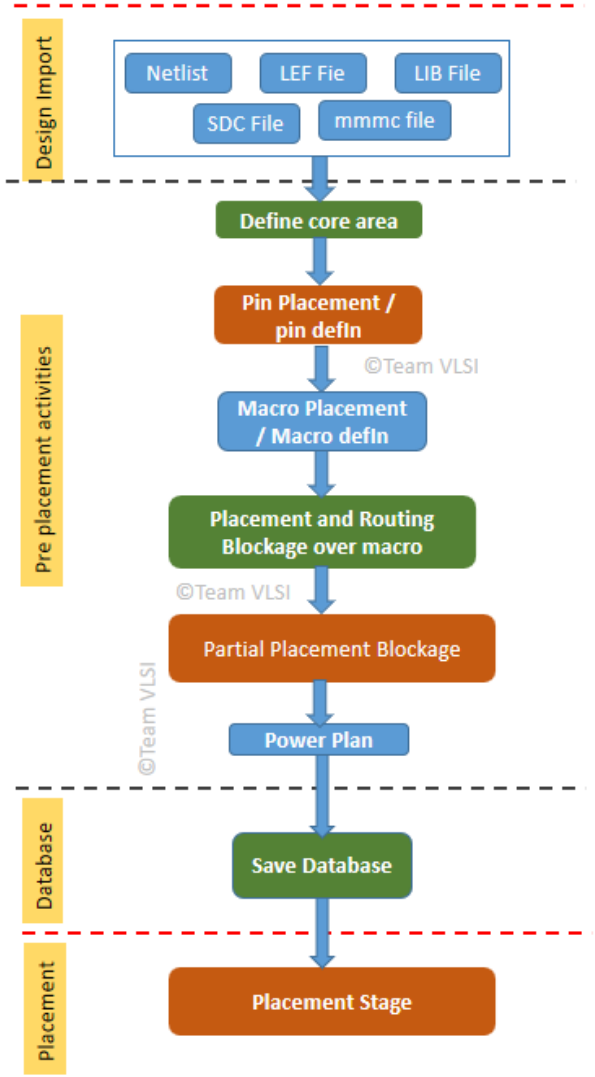
Physical design Steps

2. Floor planning:

defining the overall chip's top-level structure and organizing the different functional blocks.

- **Objectives of Floor Planning:**
  - 1-Minmize the area
  - 2-Minmize Timing
  - 3-Reduce wire length
  - 4-Better Routing
  - 5-Reduce IR

- **Floorplan Outputs :**
  - 1-IO port placed
  - 2-cell row created
  - 3-Macro placement
  - 4-Core boundary and area
  - 5-Floor planning def



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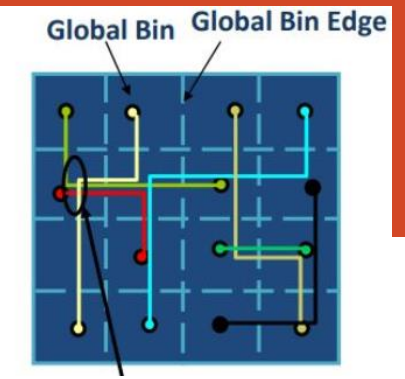
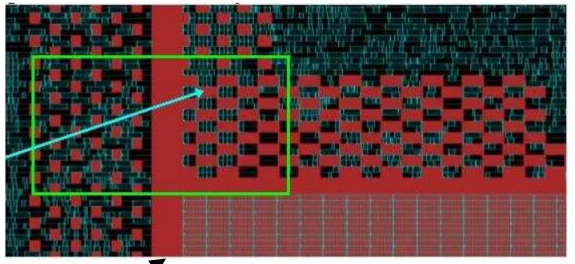
Floor planning:



***Congestion* :**

If the number of required routing resources are more than the number of available routing tracks, and in placement happen because of overlapping between std cells

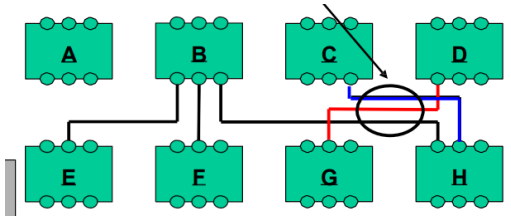


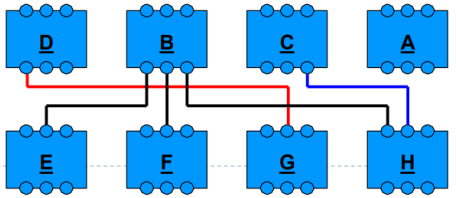
Causes of Congestion

-Missing Placement Blockages
-Inefficient floorplan
-Placing macros in the middle of floorplan etc.)
-Floorplan the macros without giving routing space for interconnection betweenmacros
-High Cell Density (High local utilization)
-Placement of standard cells near macros
-High pin density on one edge of block
-Too many buffers added for optimization
-No proper logic optimization
-Very Robust Power network
-High via density due to dense power mesh

Fix of Congestion

-Add placement blockages in channels and around macro corners
-Review the macro placement
-Reduce local cell density using density screens
- Checkerboard Blockage
-Reordering scan chain to reduce congestion





Floor planning:

***Core Boundary*:**

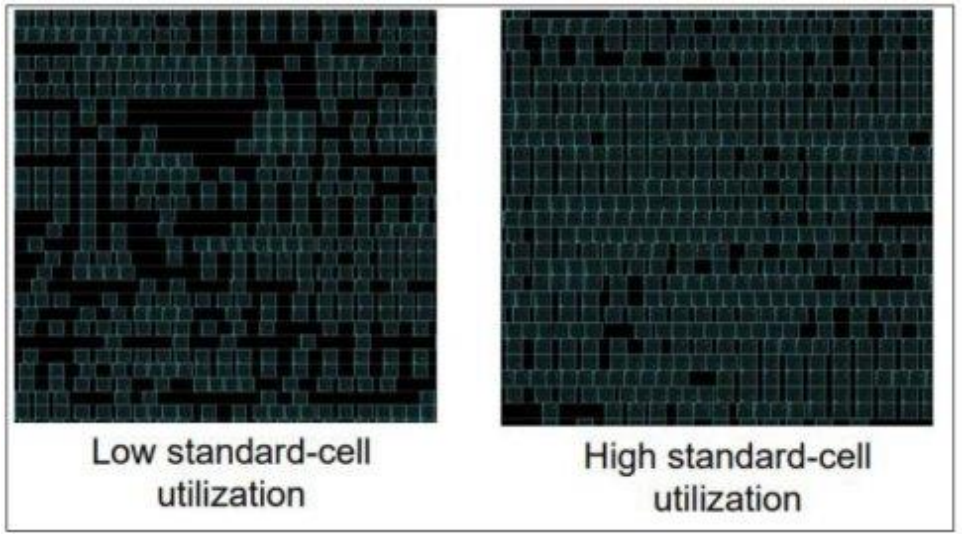
1-Core utilization:

Utilization will define the area occupied by the standard cells, macros, and other cells.

Range Utilization : min **25%** : max **75%**

2-Aspect ratio:

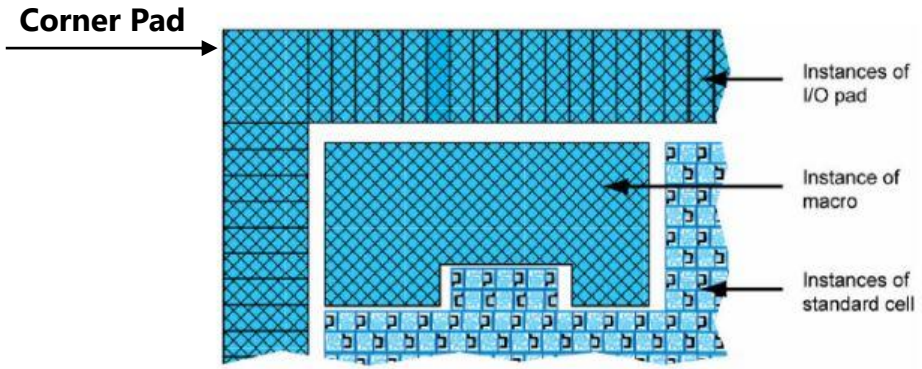
This is the ratio of height divided by width and determines whether you get a square or rectangular floorplan.

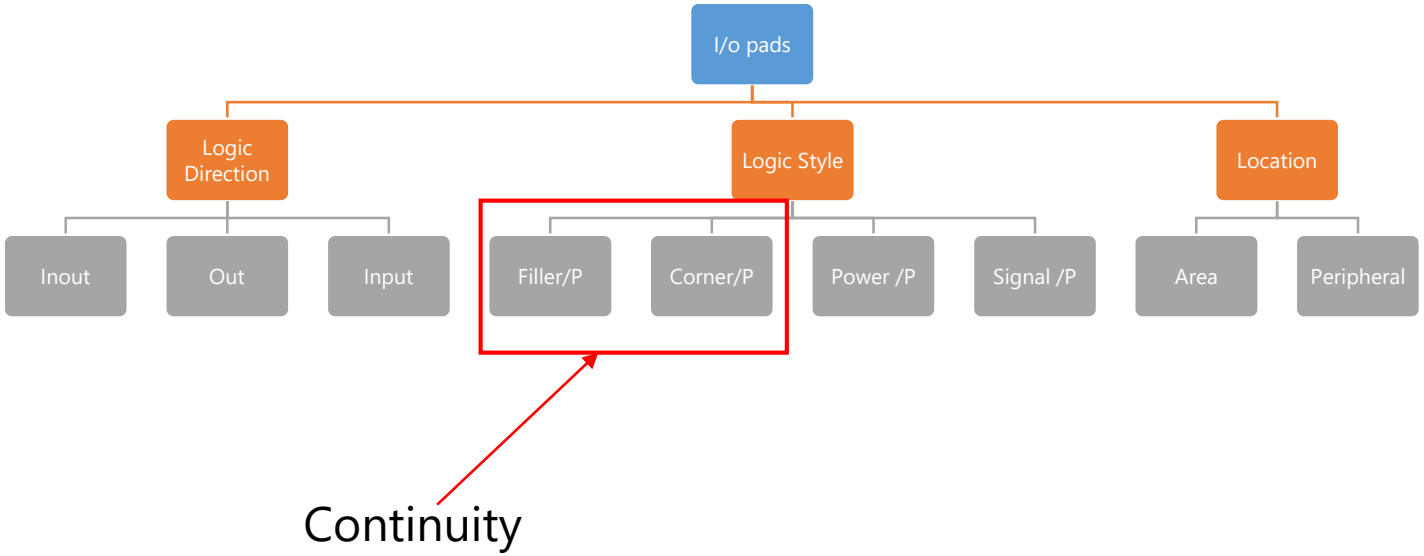


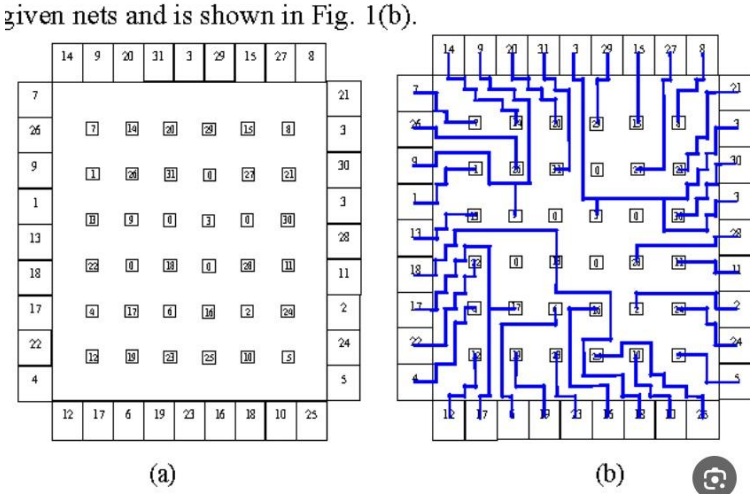
Floor planning:

***Pin placement* :**

Pads are generally arranged around the chip perimeter in a "pad frame". Pad frame will have a signal ring of pads in smaller designs.







Floor planning:

***Macro placement* :**

Important Step to get good Floor planning , Should follow this Techniques:

1-All macros should be placed at the boundaries.

2. Check the orientation and pin direction of all macros, all pins should point towards the core logic.

3. Spacing between macros should be sufficient for routing and power grid.

4. Good congestion and QoR results.

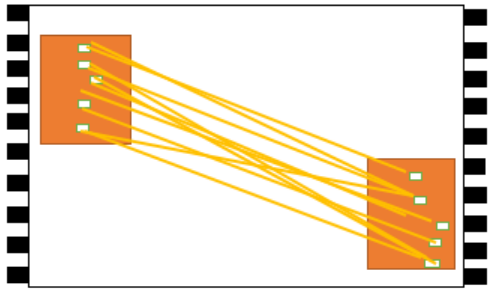


Fig a: macro to macro fly lines

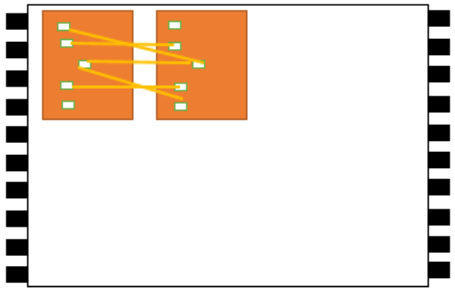
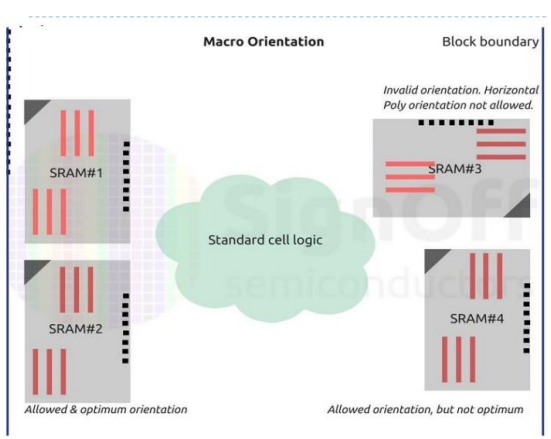
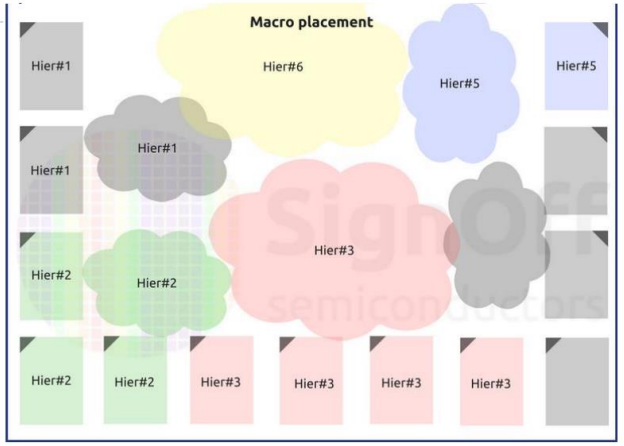


fig b: macros placed near to each other





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Floor planning:

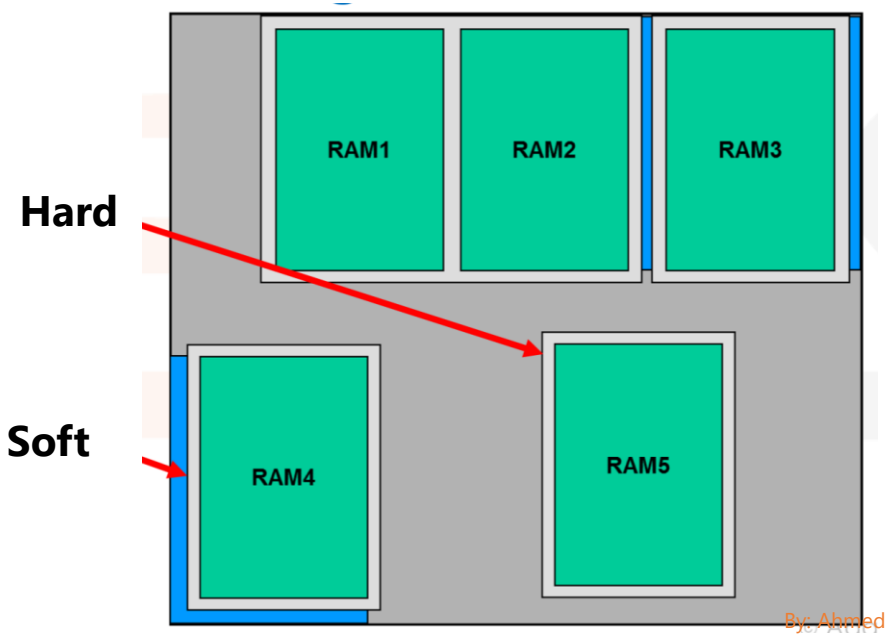
Blockage (Placement & Routing) :

it is Specific location where Placing of cells or wire are blocked , act as guidelines for tool (by avoiding put std cell in the blocked area).

- **Hard** — No cells can placed inside
- **Soft** — Only buffered can be Placed
- **Partial** — Can block std cell as per "percentage value "

Note :Halo like soft can be placed buffered in this area, it should be clear of Std cells .

Halo around Macro



Power Planning

Power planning:

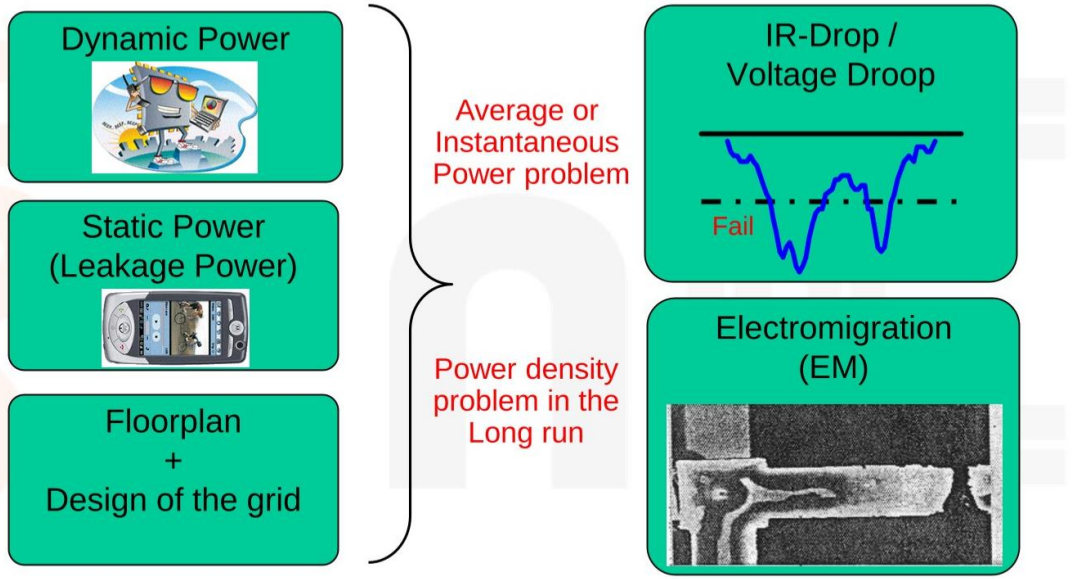
3.Power Planning :

it's important for ,how will deliver power to the design's standard cells!

-Why is it importance?

All analysis it depended on all Std cells supplied with ideal voltage.

If the actual circuit supply is different significantly, cell operation will be different than the behavior characterized in the .libs, which will cause all types of timing violations!

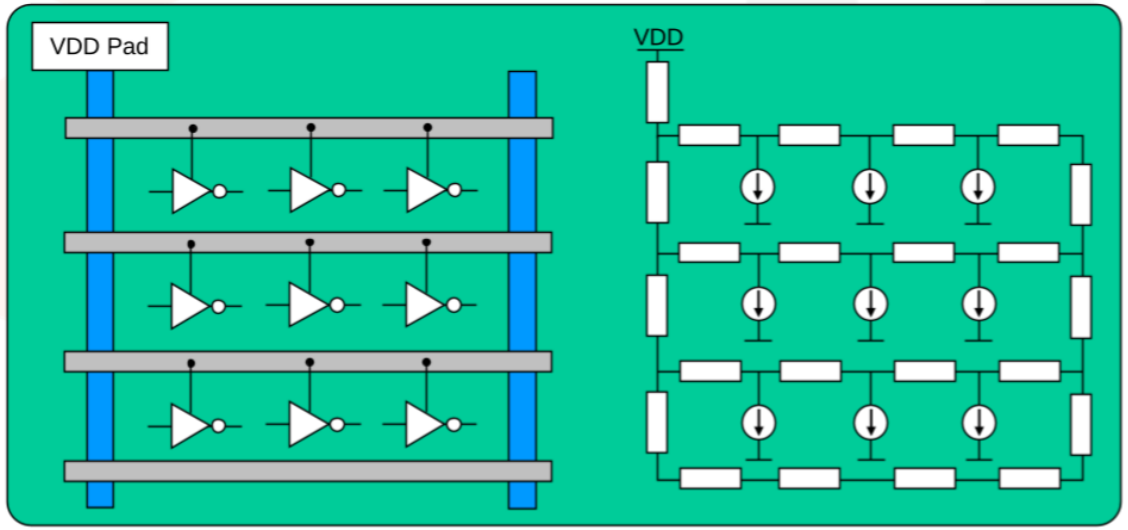


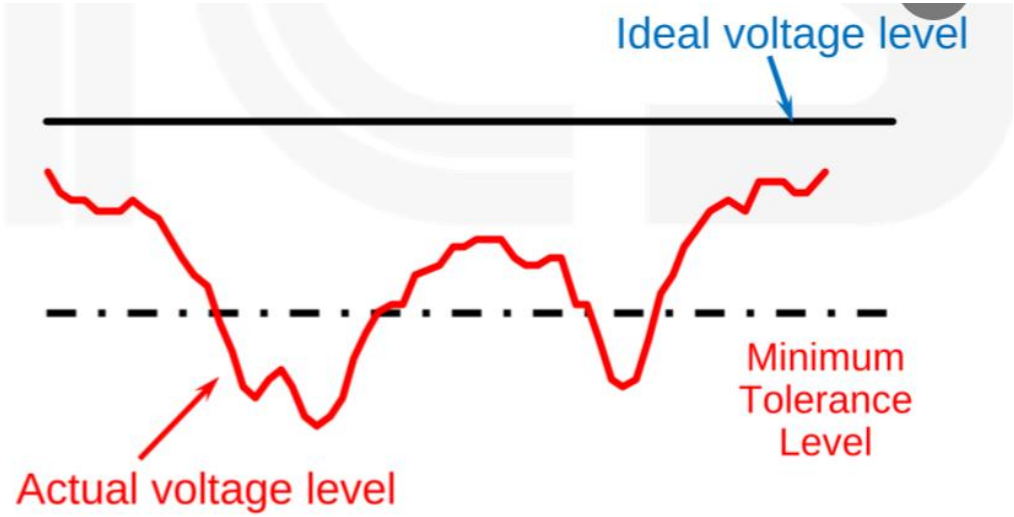
Power planning:

IR Drop:

The drop in supply voltage over the length of the supply line

- A resistance matrix of the power grid is constructed
- The matrix is solved for the current at each node, to determine the IR-drop.





Power planning:

Electromigration (EM) :

Electromigration refers to the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor.

-Problems results EM :

- Open : void on a single wire.
- Short : bridging between to wires.
- EM can cause performance degradation.

Power planning:

Power Networking :

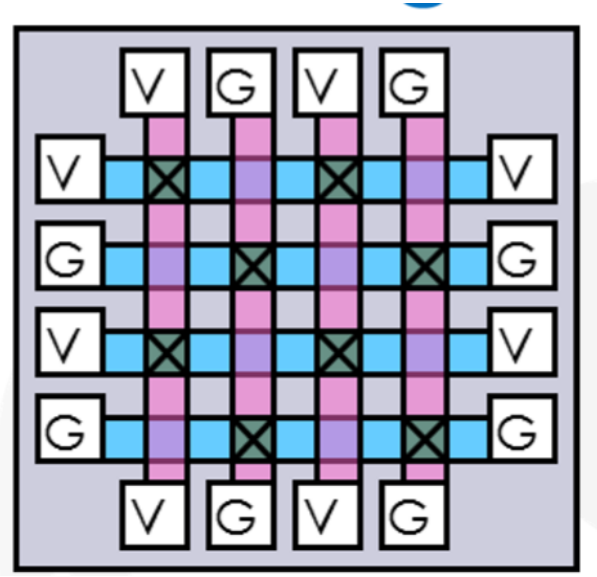
Power network finctions:

-Carry current from pads to transistor on chip.

-Maintain stable voltage with low noise .

-Provide average and peak power demands.

-Avoid EM .



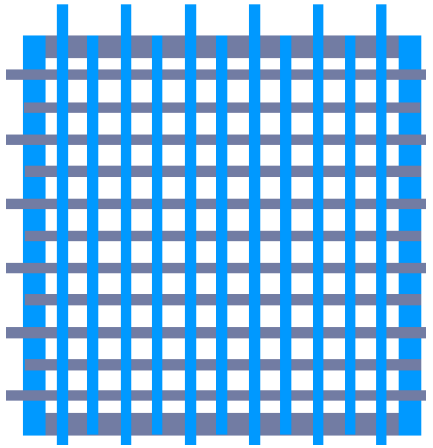
More (Wider) Power Lines:

- Less Static (IR) drop
- Less Dynamic (dI/dt) drop
- Less Electromigration

Trade off

More (Wider) Power Lines:

- Fewer (signal) routing resources (i.e., higher congestion)



Placement

Placement :

4.Placement :

Placement is the process of placing the standard cells inside the core boundary in an optimal location.

The objectives:

1-Provide legal location of entire netlist
2- Avoiding routing congestion to routing.
3- Minimize wire length
4- Minimize Power consumption
5- Minimize Timing delays

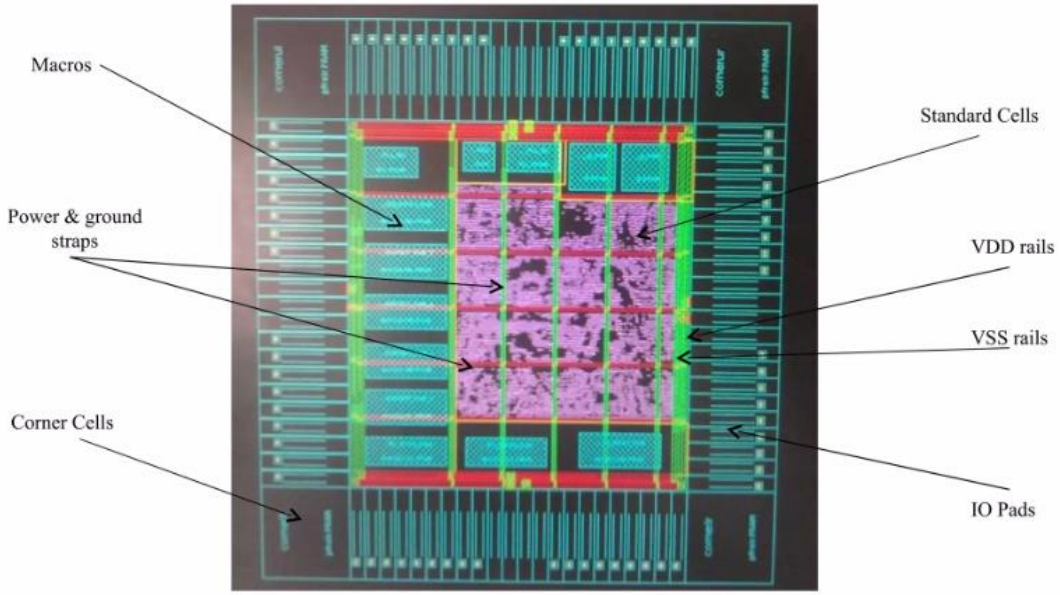


Figure 2 Chip level placement

- **Placements Outputs :**
  1-Reports (Congestion, Timing)
  2-Design with all std cells placed in core area .
  3-Placement def .

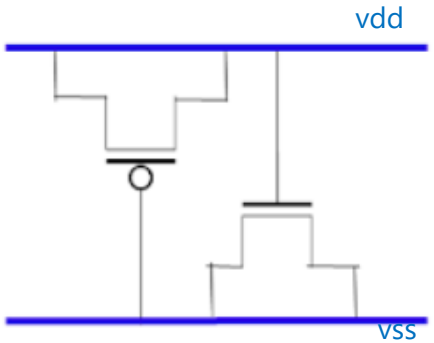
Placement :

Physical-Only Cells (Well Taps, End Caps) :

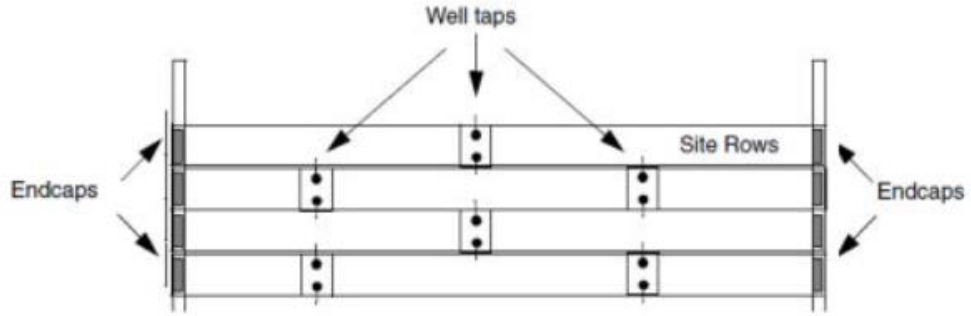
- End Caps protect the gate of a standard cell placed near the boundary from damage during manufacturing.also prevents DRC violations by satisfying Well tie-off requirements for core rows.
- Well Taps help to tie Substrate and N-wells to VDD and VSS levels and thus prevent Latch-up.

Special Cells (Decap Cells):

- Decaps for avoiding Instantaneous Voltage Drop (IVD)
- Decaps is used to fill empty spaces at chip-finishing stage, with the good impact of stabilizing voltage.



Decap celll



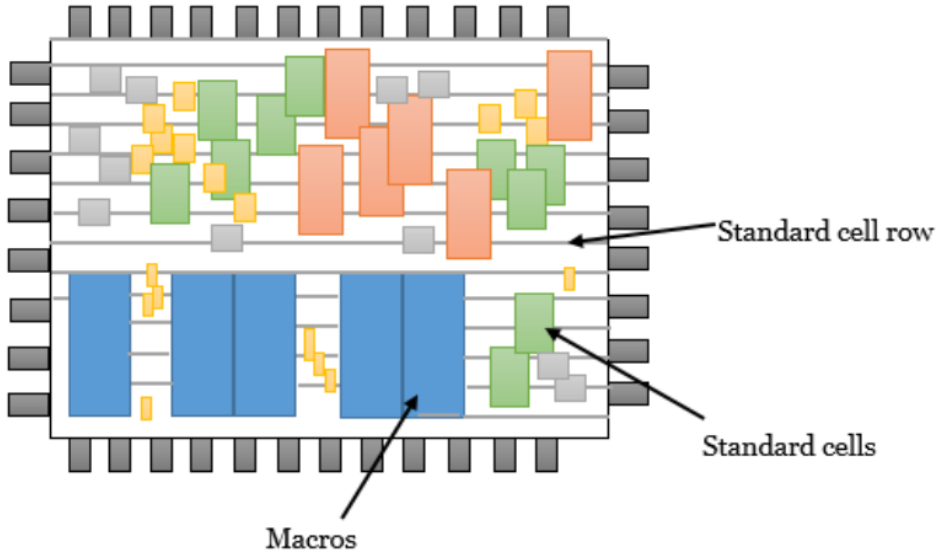
Placement :

Placement stages :

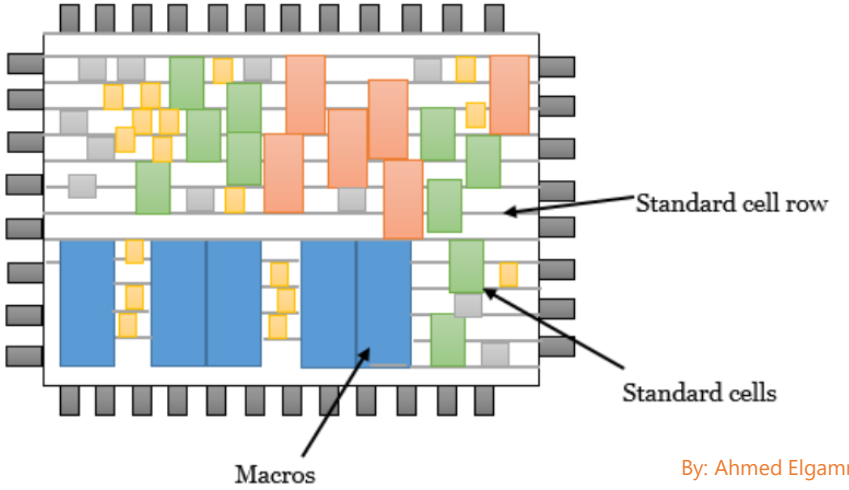
Task during placement:

1-HFNS
2-Scan Chain Reordering
3-insert Tie cell

Global/Coarse Placement



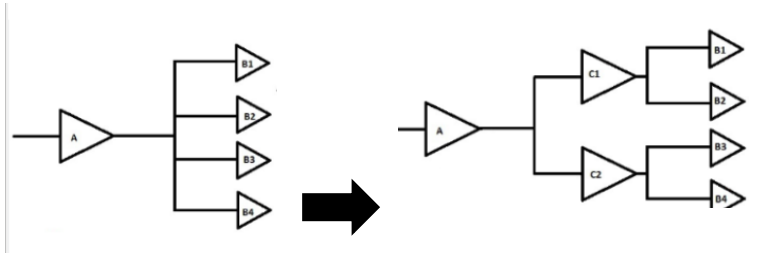
Detailed Placement/ legalization



Placement :

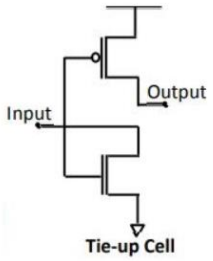
High Fanout Nets Synthesis :

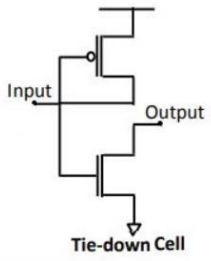
High Fanout Net Synthesis (HFNS) is the process of buffering the High Fanout Nets to balance the load.

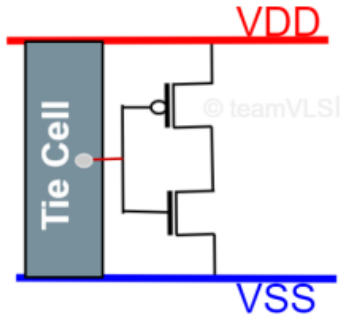


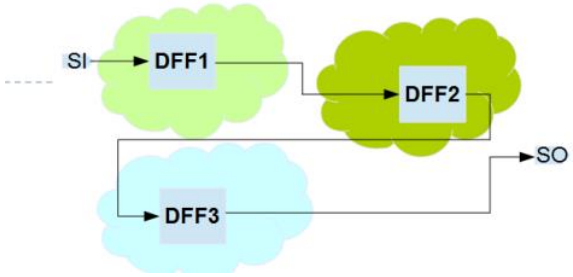
Scan-chain reordering:

It's the process of reconnecting the scan chains in a design to optimize for routing by reordering the scan connection which improve timing and congestion.

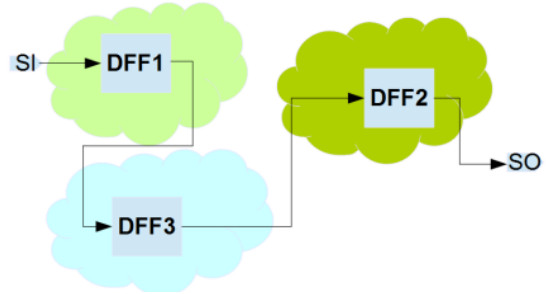








Before



After

Tie-cell insertion :

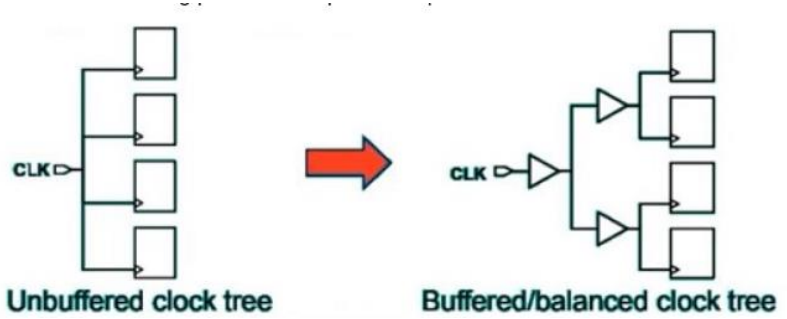
- To avoid damaging the gate oxide under the poly gate

CTS

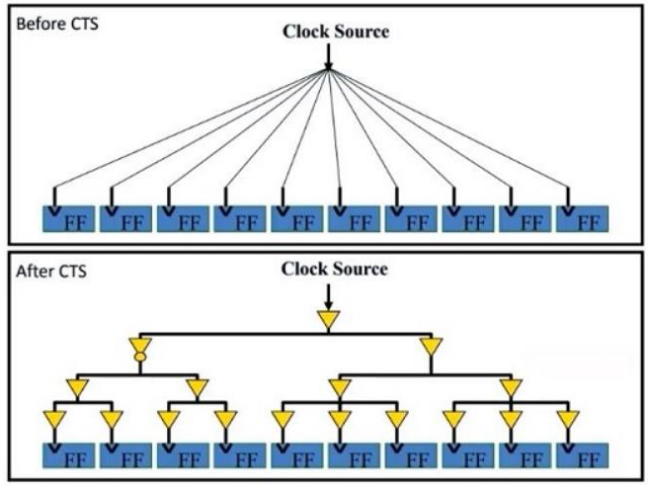
Clock Tree Synthesis

CTS :

The technique of balancing the clock delay to all clock inputs by inserting buffers/inverters along the clock routes of an ASIC design



- **CTS Objective :**
  1-Clock Signal Distribution "Balanced"
  2-Clock Skew Minimization
  3-Clock Tree Power Optimization
  4-Timing Closure
  5-Crosstalk Mitigation



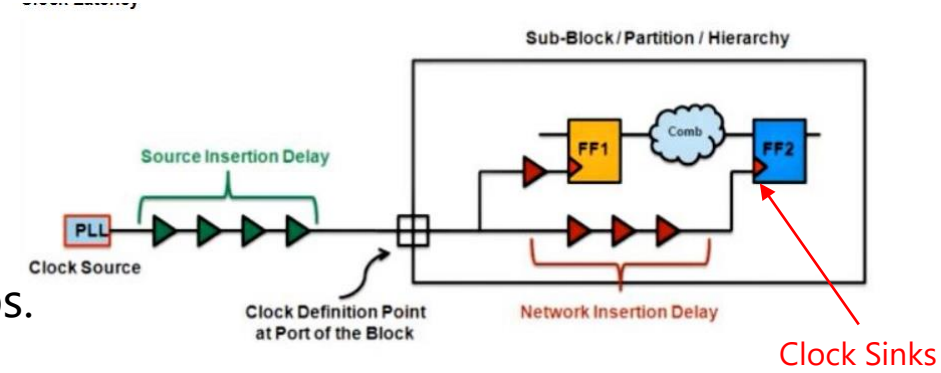
- **CTS Outputs :**
  1-Report (Timing – Congestion – Skew-insertion delay)
  2-CTS def file

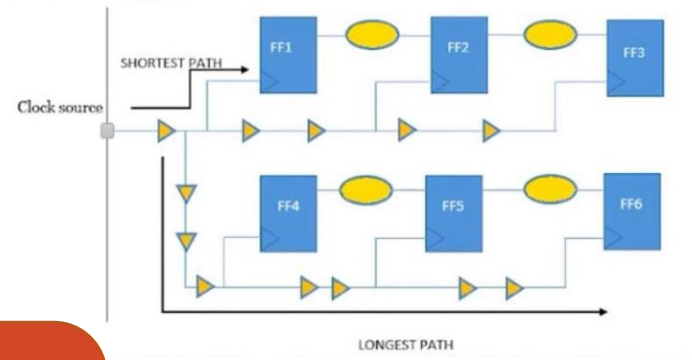
Clock Tree Synthesis_ *Terminology*

1-Insertion delay : It is the delay from the clock definition point to the clock pin of the register.

2-local skew : Local skew is the difference in the arrival of clock signal at the clock pin of related flops.

3-Global skew : Difference between max insertion delay and Min insertion delay.





NOTE: There are different between clock buffer and normal buffer

1-Clock buffer have equal rise time and fall time, therefore pulse width violation is avoided.

2-Clock buffers are usually designed such that an input signal with 50% duty cycle produces an output with 50% duty cycle.

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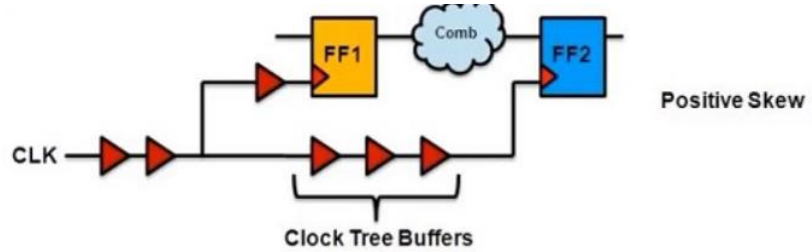
Clock Tree Synthesis

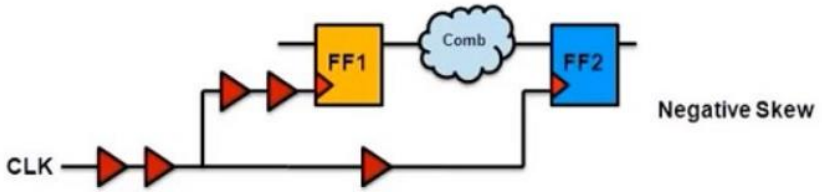
Positive Skew:

If capture clock comes late than launch clock then.



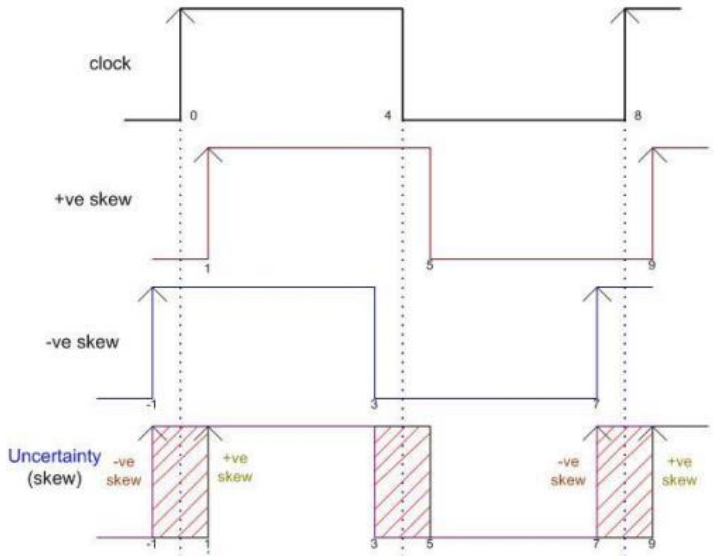
Negative Skew:

If capture clock comes early than launch clock it



Uncertainty Clock:

uncertainty is the time difference between the arrivals of clock signals at registers in one clock domain or between domains.



Setup equation: **Max**

$$T_{c2q} + T_{comb} + T_{setup} \leq T_{clk} + T_{skew}$$

Hold equation: **Min**

$$T_{c2q} + T_{comb} \geq T_{hold} + T_{skew}$$

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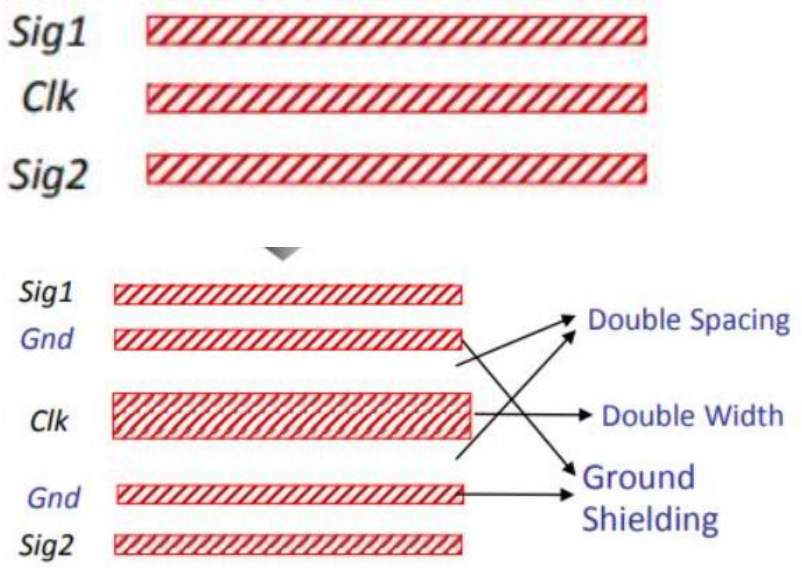
Clock Tree Synthesis

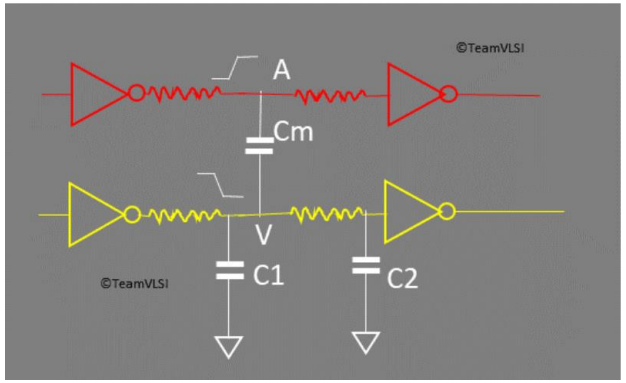
Non-Default Clock Routing:

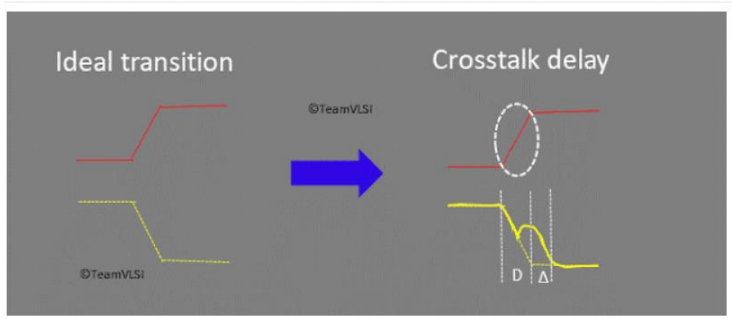
NDR are often used to “harden” the clock, make the clock routes less sensitive to Cross .

Crosstalk Delay

Crosstalk delay occurs when both aggressor and victim nets switch together.







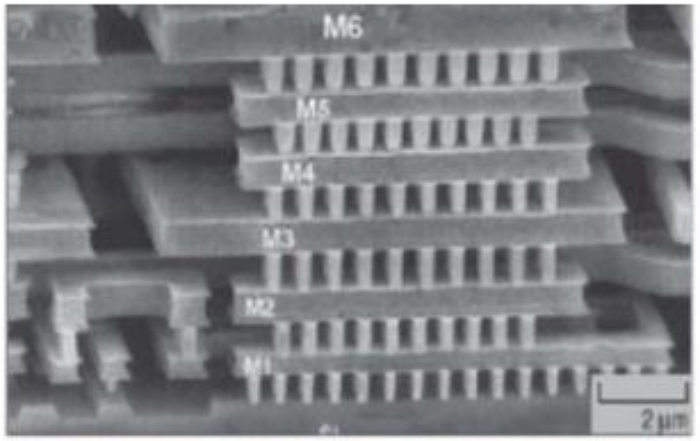
Routing

Routing

Routing:

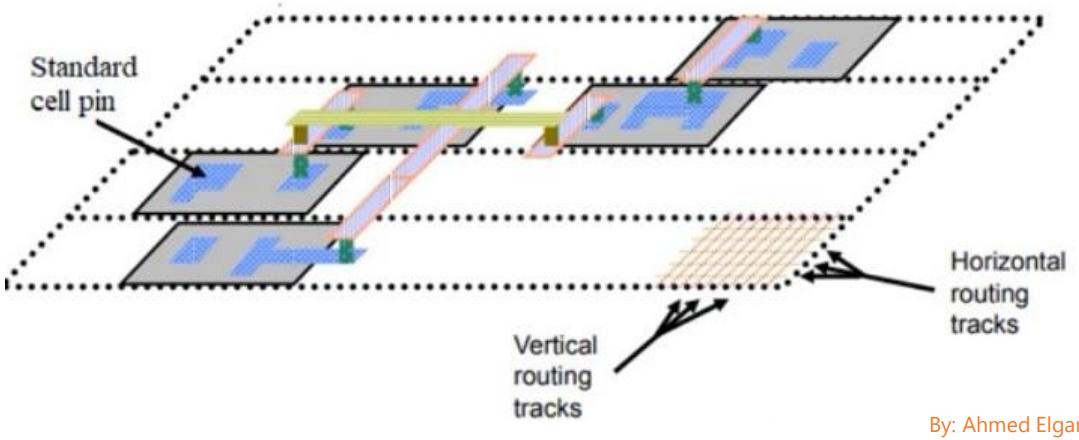
creates physical connections to all clock and signal pins through metal interconnects

- Routed paths must meet setup and hold timing, max cap/trans, and clock skew requirements
- Metal traces must meet physical DRC requirements



Multi-level Interconnection (MLI) Technology Layer stacks

Routing Flow

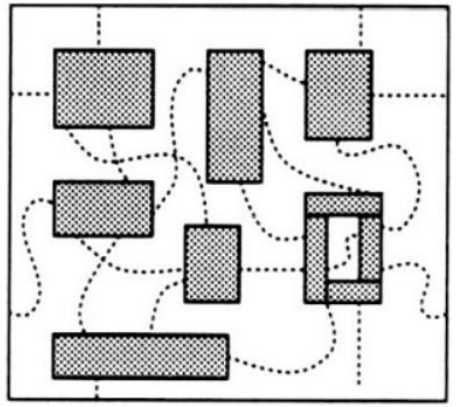


By: Ahmed Elgammal

Routing

Global Routing:

1- Avoid congested while minimizing detours
2- Avoid Blockage
3-Don't take consider DRC
4-identifying Routable path shortest

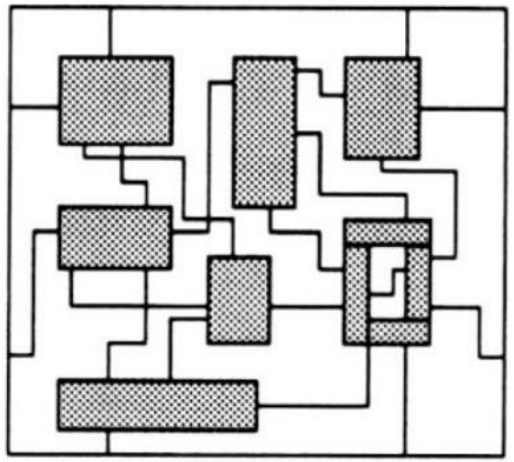


Global Routing

Track Assignment (TA):

1- Assigns each net to a specific track and lays down the actual metal trace
2- Make long, straight traces
3-Reduce n.of Via
3-Don't Check DRC

Detailed Routing



Detailed Routing

Detailed Routing

1-The detailed router uses the routing plan laid by the router during the Global Routing and Track Assignment and lays actually metal to logically connect pins with nets and other pins in the design.
2-Solve violations DRC and meet timing

Each Inputs for each step in flow

Floor Planning	Power Planning	Placement	CTS	Routing
• Technology file (.tf) • Netlist • SDC • Library files (.lib & .lef) • TLU+	• Netlist & SDC • Jib .lef • tech file • Tlu+ file • UPF	• Technology file (.tf) • Netlist • SDC • Library files (.lib & .lef) •TLU+ file • Floorplan & Powerplan DEF file	• Technology file (.tf) • Netlist • SDC • Library files (.lib & .lef) • TLU+ file • Placement DEF file	• Netlist • All cells & ports should be legally placed • CTS DEF file • NDRs • Routing blockages • Technology data

Thanks