SPYGLASS Lab

A-Linting

1- Mention the major violations linting tool can detect.

2- Mention the error appeared after running linting goals for these codes and mention how will you fix them

a-
```
always @ (*)
a = a & b;
```

b-
```
always @ (posedge clk)
if (a > b)
    c <= a;
```

c-
```
always @ (posedge clk)
if (a > b)
c <= a;
c <= b;
else
c <= c;
```

d-
```
wire [3:0] a;
wire [7:0] b;
assign a = b;
```

e-
```
 input A;
 input B;
 output C;

 assign C = A;
```

f-
```
A = 32'bx;
```

g-
```
reg [1:0] v;
case (v)
    00: x = 1
    10: x = 0
endcase
```

h-
```
assign out = en ? in : out;
or
assign a = en ? z : c;
assign z = en ? a : y;
```

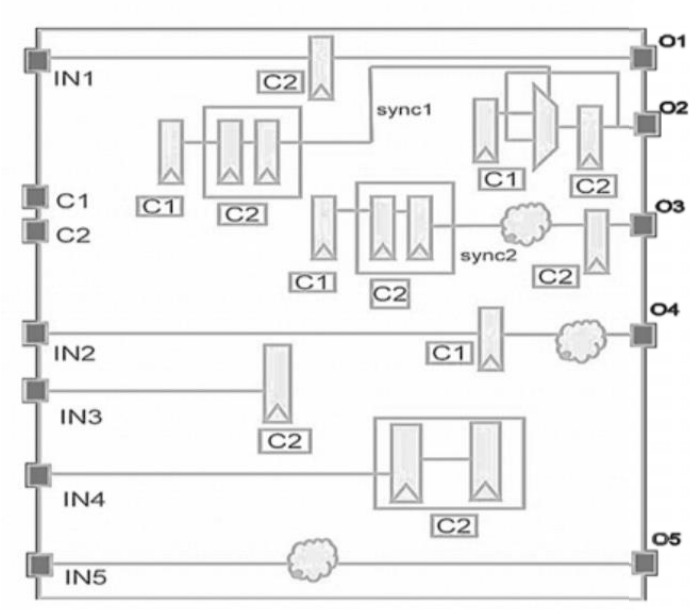
i- for this especially code insert modularity schematic for this design code before fixing code and illustrate ur answer

```
always @(posedge clk or posedge rst)
    begin
    if(rst)
        out1 <= 0;
    else
        out1 <= in;
    end
always@(posedge clk)
    begin
    if(rst)
        out2 <= 0;
    else
        out2 <= in;
end
```

3- Run your previous RISCV design code on spyglass and mention the errors got appeared and fix them

B-CDC

1- Mention at least 3 CDC problems and their solutions.
2- Are synchronous clock domain crossings safe?
3- Do metastability problems depend on the frequency of the destination clock?
4- Can static timing tool like Synopsys Prime Time detect asynchronous clock domain crossings?
5- Name the two key problems caused by asynchronous cl k oc d i oma n crossings
6- Do metastability problems depend on the frequency of the destination clock? mention why if(yes or no).
7- Write .sgdc file for this rtl diagram



8- Which signals need to be constrained by Sgdc?

9- Write a rtl code for this architecture and it's SGDC file and run it to spyglass with fixing errors will appear