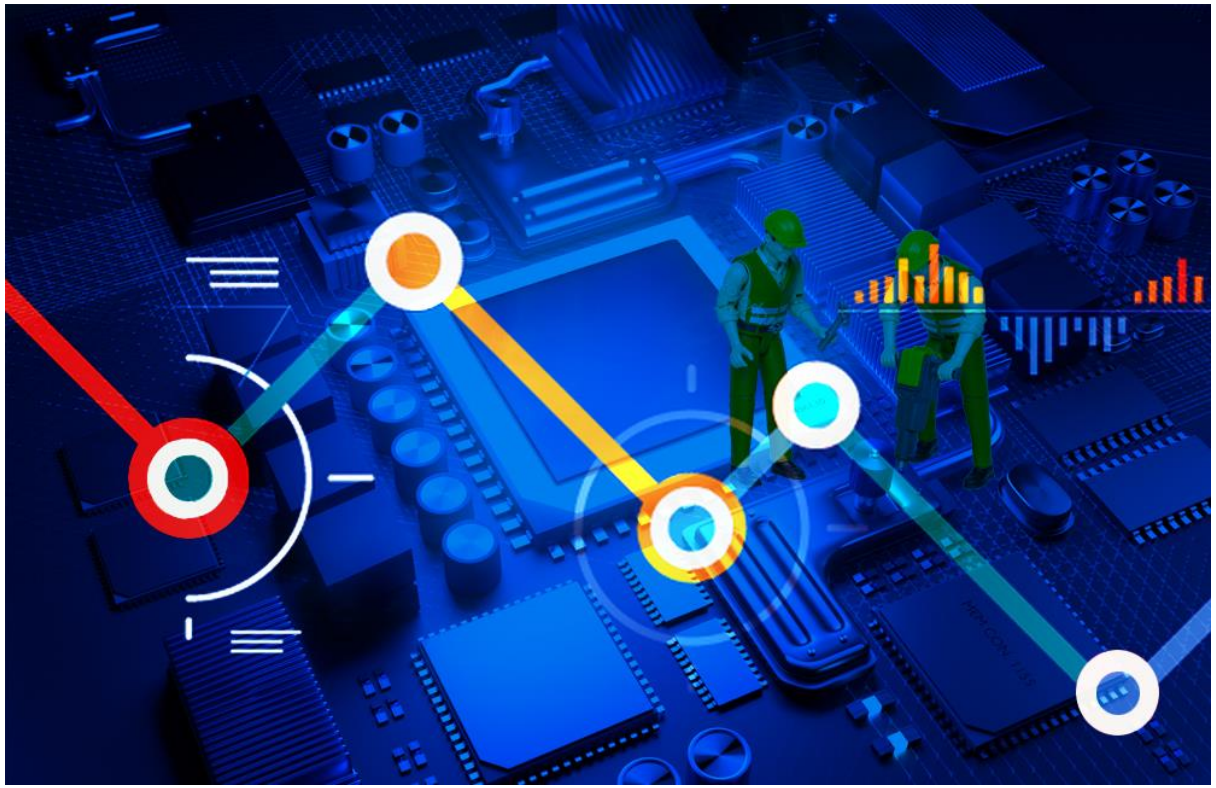
Design For Testability

DFT

Ahmed Elgammal

Agenda

1. What DFT
2. Tools
3. Observability & Controllability
4. Physical defects
5. DFT Challenges
6. Fault Models
7. Stuck At Model
8. Scan insertion
9. Lockup latch
10. Stuck at Speed
11. ATPG
12. Fault Classes
13. Calculated Coverage



DFT

What DFT ?

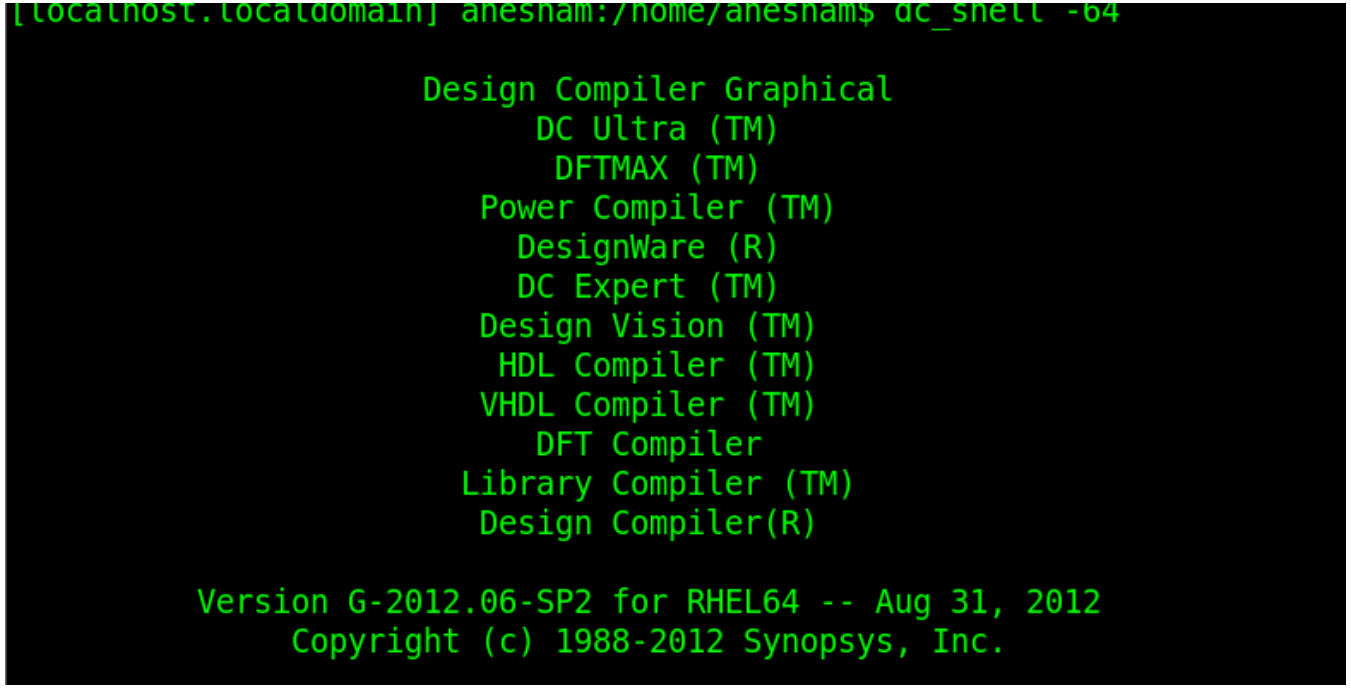
Design for Testability (DFT) is an approach that aims to make digital circuits easier to test during the manufacturing and debugging process by adding incorporating additional circuitry and design features such as scan chains, built-in self-test (BIST) circuits, and boundary scan cells into the chip design to facilitate testing.

Why DFT ?

Design for testability in VLSI design is essential to ensure that the fabricated chips are free from any kind of manufacturing defects and reduces the overall test time , the cost of testing, and debugging.

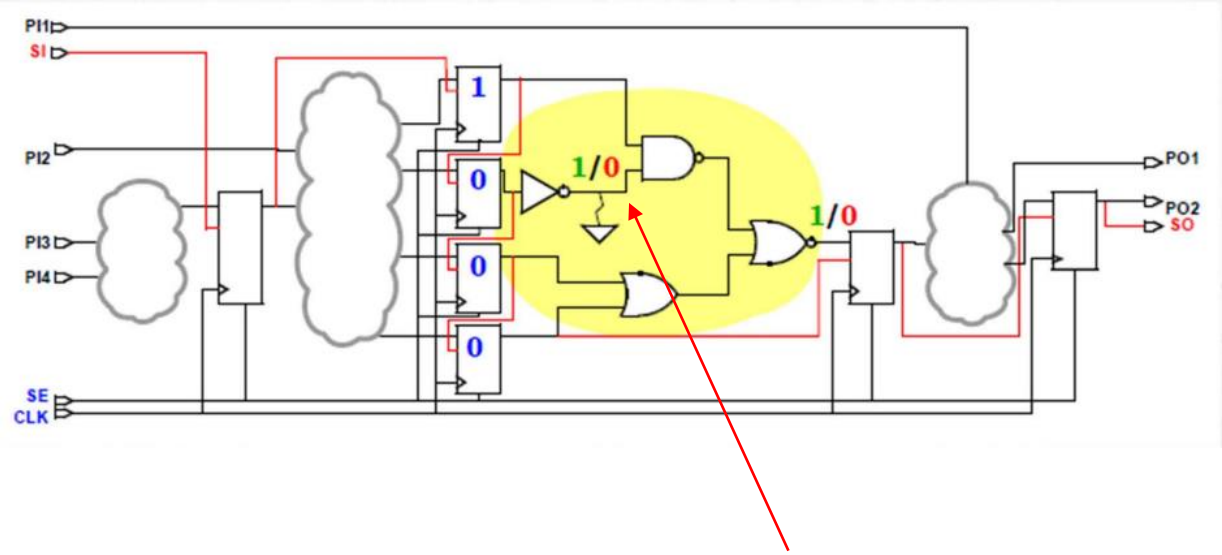
Tools

- **Synopsys**
  - DFT Compiler (TM)
  - Tetra Max
- **Mentor**
  - Tessent Scan
  - Tessent FastScan



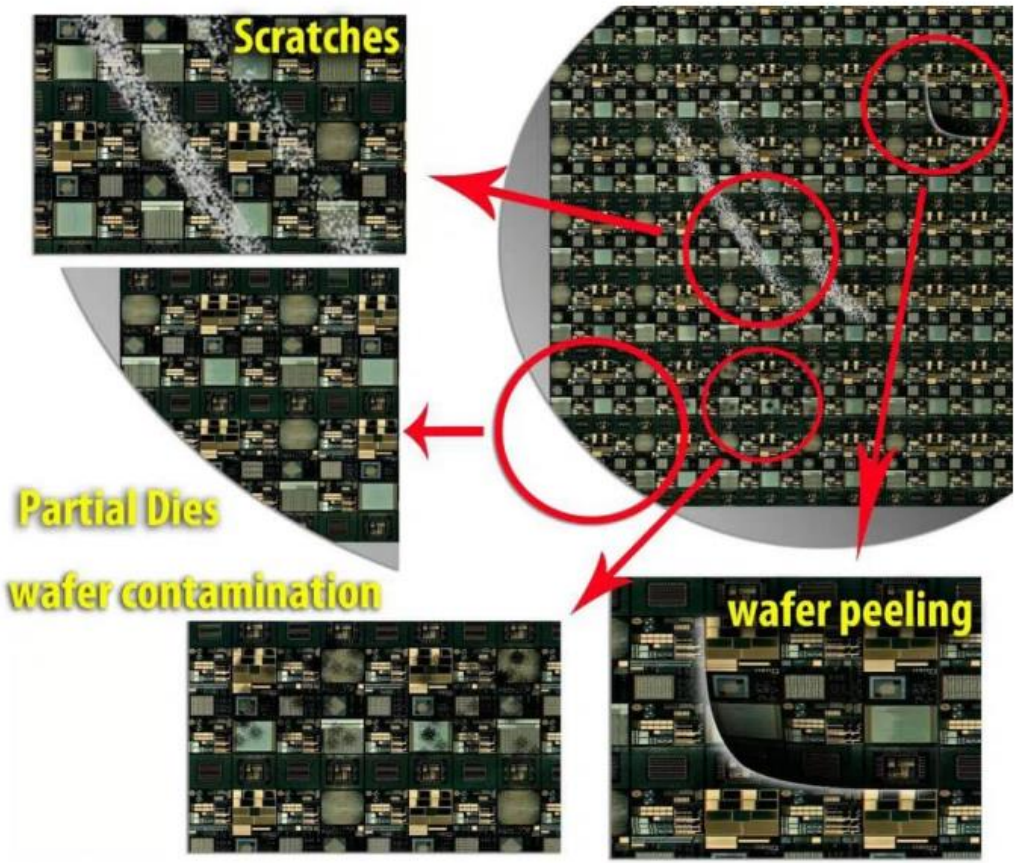
Terminology

- **Observability**
  - Reflect the difficulty of propagation the logic value of the signal line to outputs.
- **Controllability**
  - Reflect the difficulty of setting a signal line to a required logic value from primary inputs.



Physical defects

- **Problems manufacturing**
  - Scratch
  - Partial die
  - Wafer peeling
  - Wafer Contamination
- **Physical Defects**
  - Short & Open circuit
  - Bridging



DFT Challenges

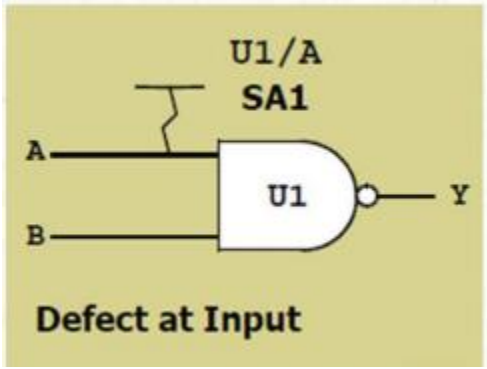
- **DFT Challenges**
  - Internal nets
  - IO number
  - Sequential Circuits
  - Test Circuit area
  - High Coverage

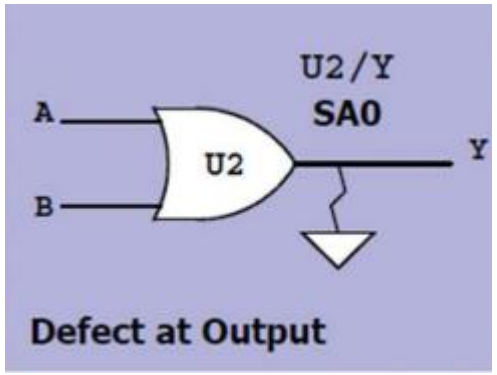
Fault Models

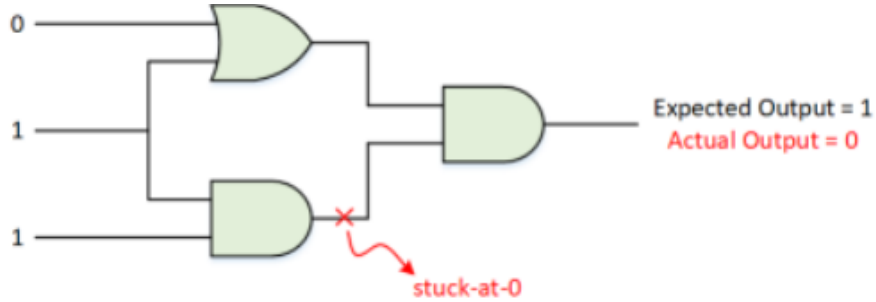
- **Fault Model**
  - Stuck At
  - AT-Speed
  - Quiescent Current
  - Bridge

Stuck AT

- **Stuck At**
  - This is the most common fault model used in industry. It models manufacturing defects which occurs when a circuit node is shorted to VDD (stuck-at-1 fault) or GND (stuck-at-0 fault) permanently

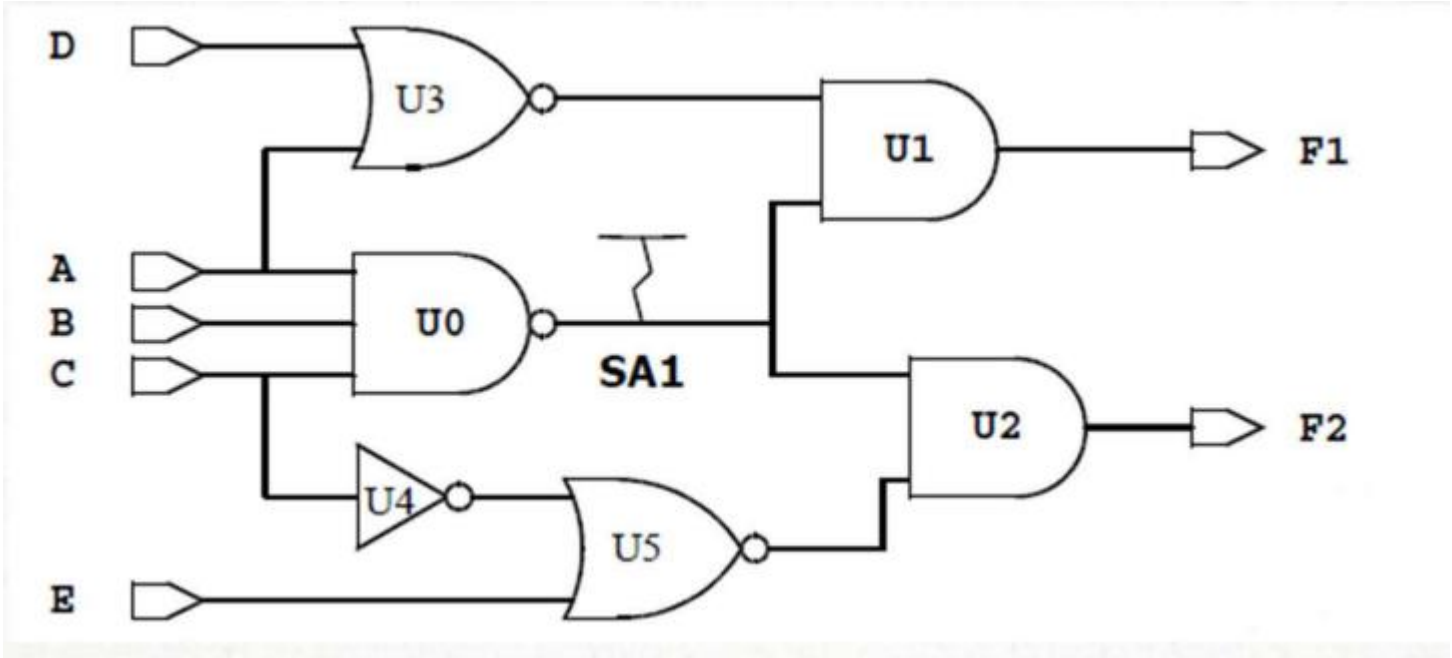






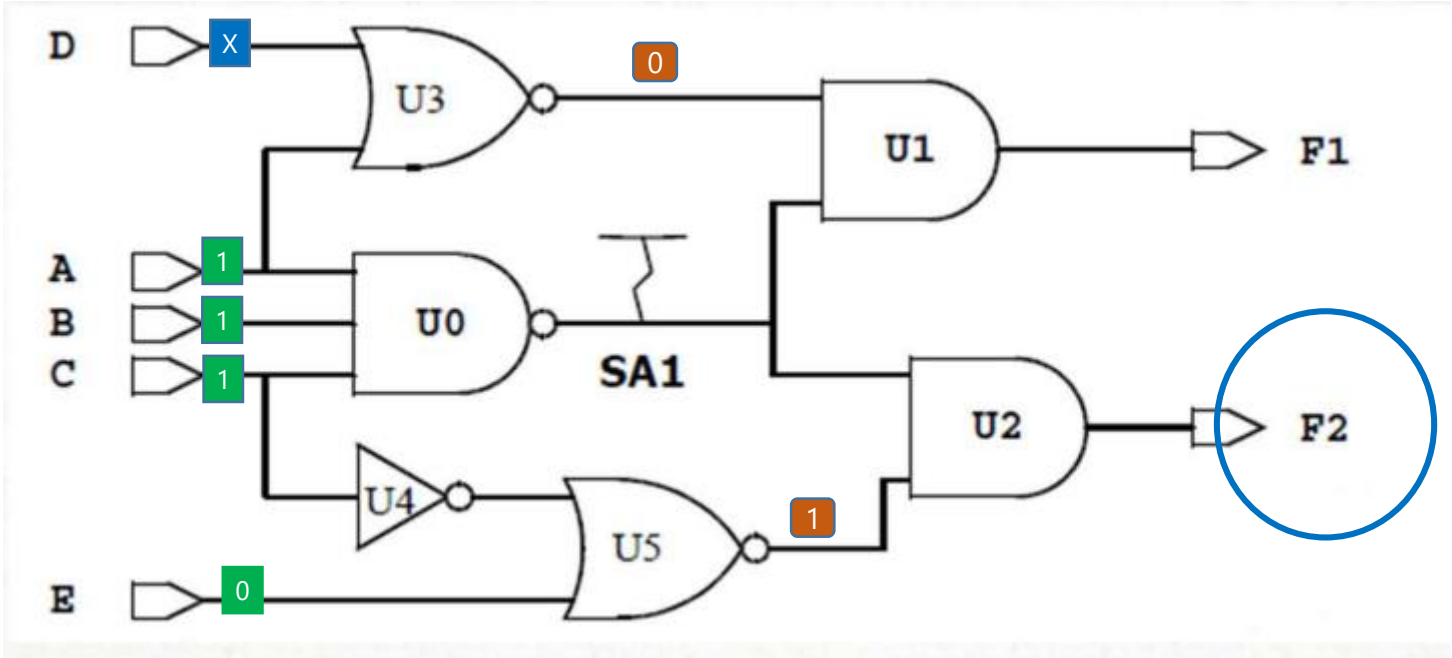
Example

- **EX**



Example

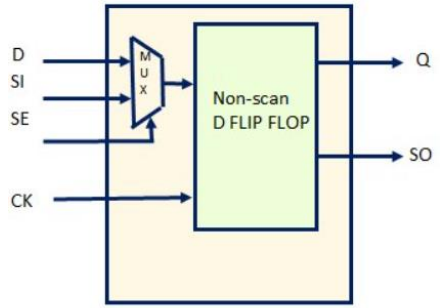
- **EX**

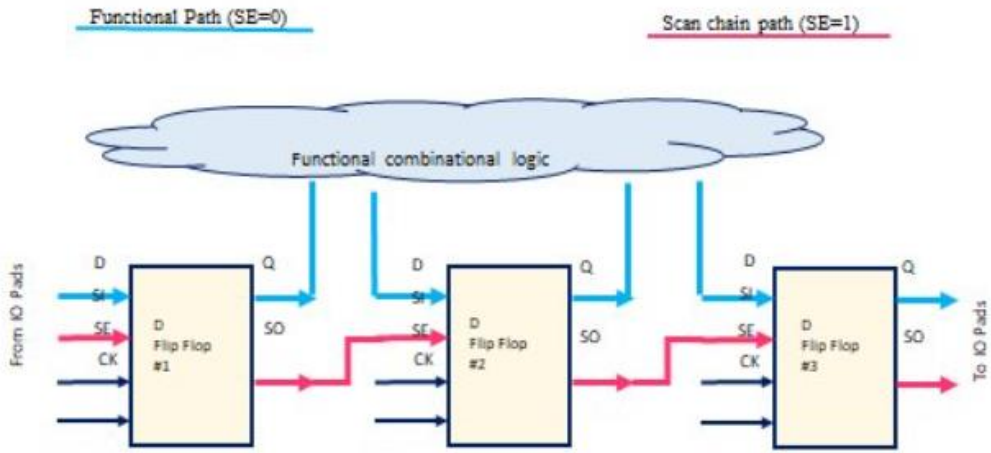


Expected Output =0
Actual Output =1

Scan Chain

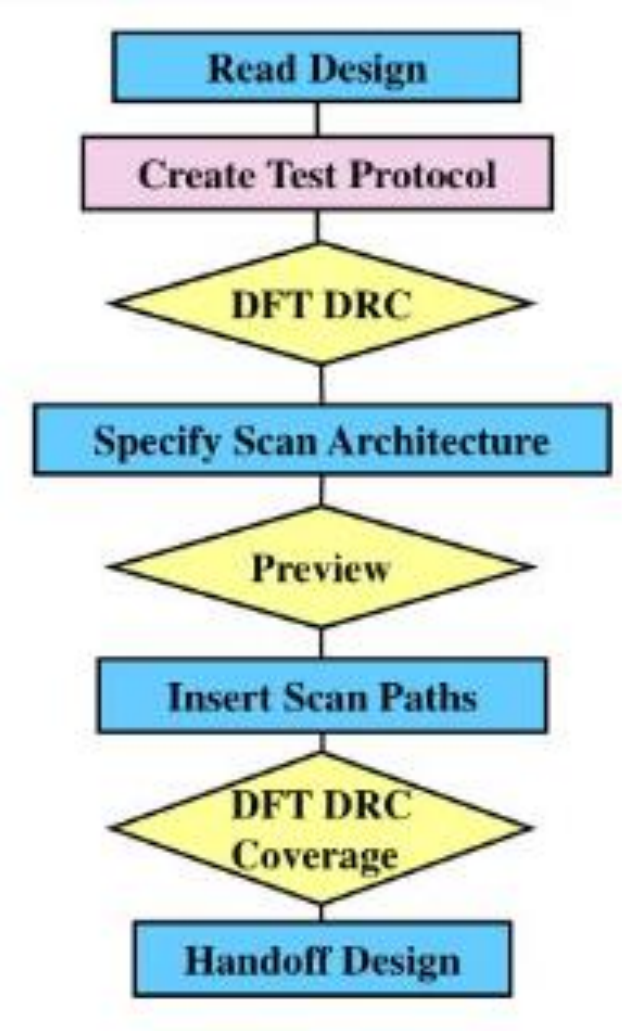
- **Scan Chain**
  - All the flip-flops present in the design are replaced with the scan flip-flops (for a full scan design). The scan flip-flops are connected together in form of a chain – scan chain.
  - Scan chain acts as a shift register when the design is in test timing mode; SE (test enable signal) is active. The first flip-flop of the scan chain is connected to the scan input port and the last flop the scan chain is connected to the scan output port.





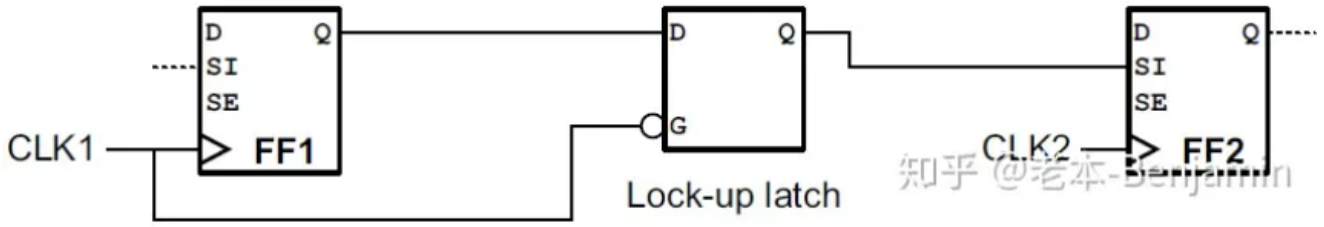
Scan Chain **Flow**

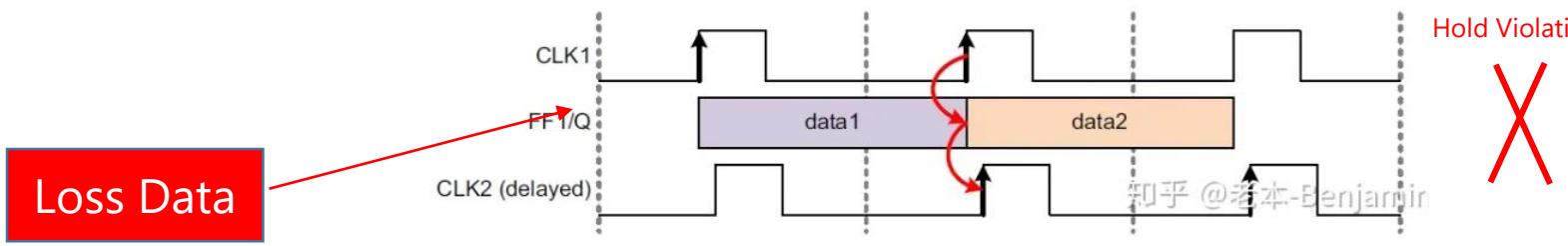
```
set test_default_scan_style
read_verilog ../source/johnson_dft.v

read_sdc ../source/johnson.sdc

create_clock clk -period 1000
set_input_delay 250 SCANINPORT -clock clk
set_input_delay 150 SE -clock clk

set_dft_signal -view exist -type ScanClock -timing {45 55} -port clk

set_dft_signal -view exist -type Reset -active 1 -port r
set_dft_signal -view exist -type ScanEnable -active 1 -port SE
report_dft_signal -view exist

create_test_protocol
dft_drc

compile -scan
link

set_dft_insertion_configuration -preserve_design_name true

set_dft_signal -view spec -port SCANINPORT -type ScanDataIn
set_dft_signal -view spec -port SCANOUTPORT -type ScanDataOut
set_scan_configuration -chain_count 1

preview_dft
insert_dft

write_test_protocol -out ../results/johnson_dft.spf
```

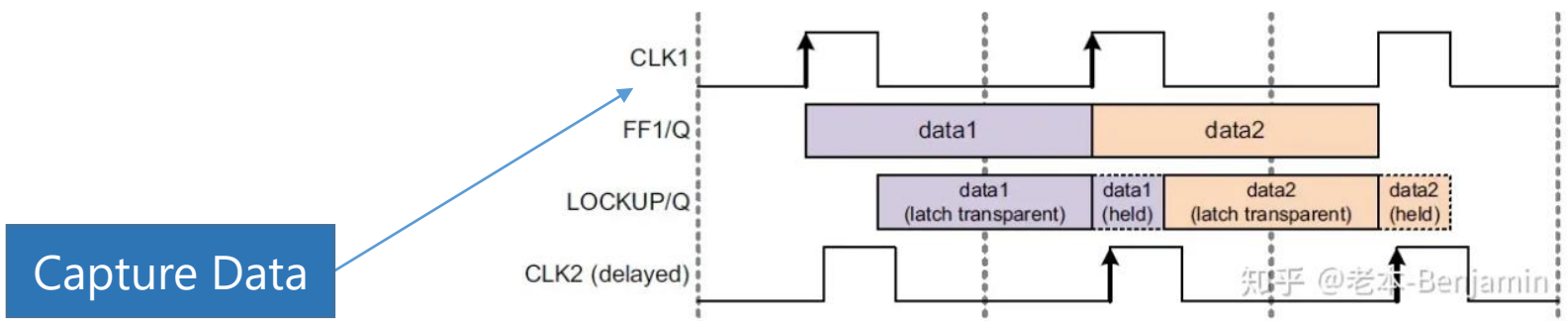


Lockup Latch

- The lockup latch is just like a transparent latch, which is placed at that point, where clock skew is maximum. To reduce the clock skew and follow the hold time constraints





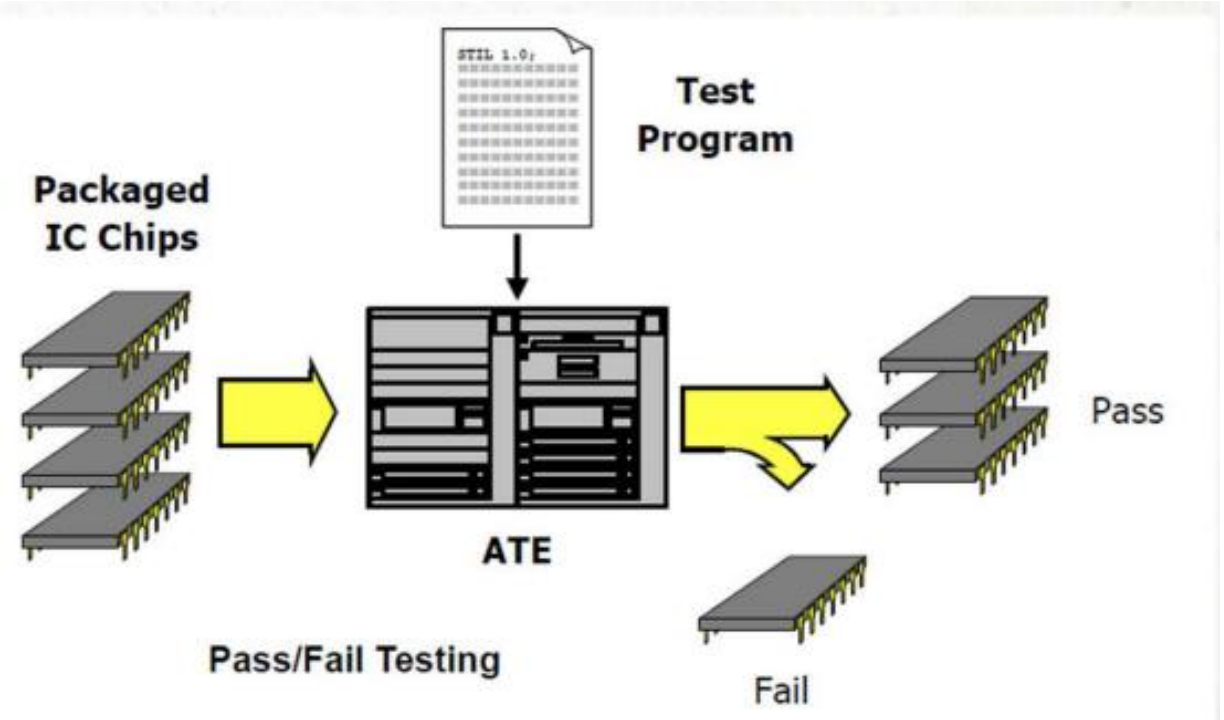


Stuck At-Speed

- Manufacturing defects that prevents the device from operation at-speed
- Under slow conditions it operates as expected

Automatic Test Pattern Generation (ATPG)

- **ATPG** : generate Automated by tool (Tetra Max)
- ATE : Automatic Test Equipment



Fault Classes

- **DT- Detected**
  - DS : detected by simulation
  - DI : detected by implication
- **PD- Possibly Detected**
  - PT : Possible testable
  - PU : Possible untestable
- **UN- undetectable**
  - UU : undetectable unused
  - UB : undetectable blocked
  - UR : undetectable redudant
- **ND – Not Detected**
  - NC: Not controlled
  - NO : Not Observed
- **AU - ATPG_UNTESTABLE**

Coverage

$$\text{Test Coverage} = \frac{DT + (PT * posdet\_credit)}{all\ faults - (UD + (AU * au\_credit))}$$

$$\text{Fault Coverage} = \frac{DT + (PT * posdet\_credit)}{all\ faults}$$

posdet_credit = 50% by default

au_credit = 0% by default

Thanks