VHDL Design Lab #1

Objective: In this lab, you will design and implement three different solutions for a given problem using VHDL. These solutions will be implemented with three different architectures: behavioral, dataflow, and structural. Additionally, each solution will have its own test bench, with three different types of test benches in total.

Problem Statement: Implement a 4-bit binary adder-subtractor circuit using VHDL. The circuit should have two 4-bit inputs (A and B) and a mode input (M) to select between addition (M=0) and subtraction (M=1). The output should be a 4-bit result (S) and a carry-out (Cout).

Requirements:

Implement three different solutions for the problem using VHDL, one for each architecture: behavioral, dataflow, and structural.

Each solution should have its own test bench, with three different types of test benches in total.

- -The first test bench should use 'asserts' to verify the correctness of the design.
- -The second test bench should read test cases from a file, and compare the output to expected results.
- -The third test bench should compare the outputs of the different architecture implementations to each other.

Use a configuration to decide which architecture to use for each solution.

Deliverables:

- 1- VHDL code for each of the three solutions (behavioral, dataflow, and structural)
- 2- Test bench code for each solution, including the three types of test benches described above
- 3- A report documenting your design and implementation choices, and the results of each test bench. Make sure to include comparisons between the different architecture implementations.

Grading:

Correctness of each solution (40%)

Correctness of each test bench (30%)

Proper use of configurations (10%)

Quality and clarity of report (20%)

Submission:

Submit your VHDL code and test bench code as separate files, along with your report in PDF format.

Make sure to include your name and student ID in the report and code files.

Good luck with your lab, and feel free to reach out if you have any questions or need further assistance.