

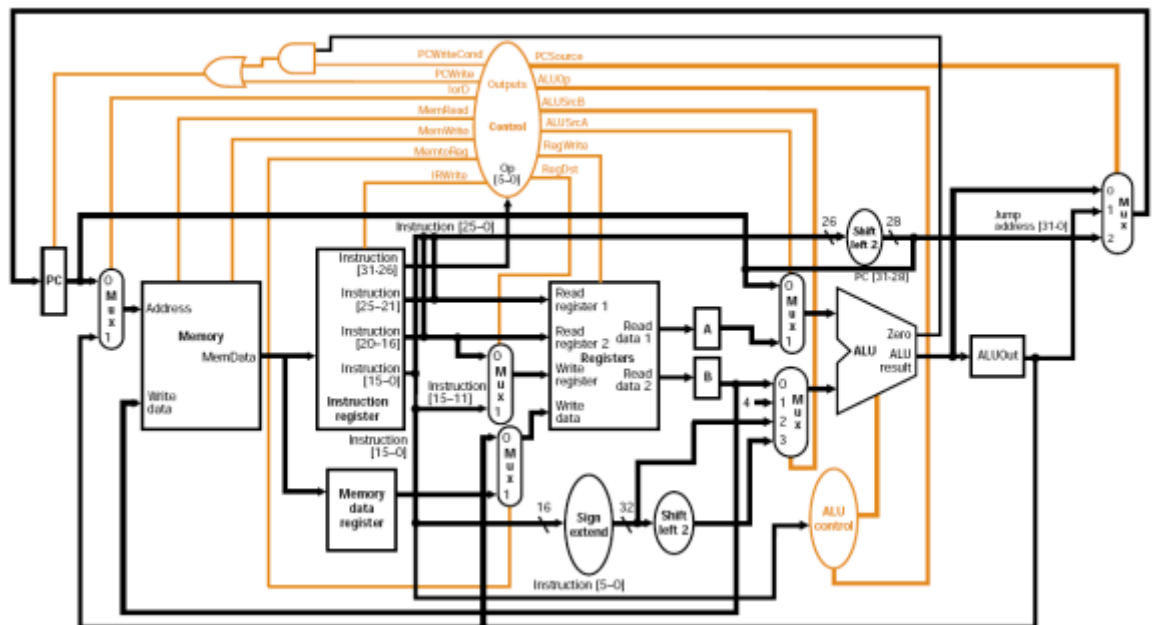


Course **CSE 226: Hardware Design** **PROJECT**

No.	Name	Academic number	Task completed
1			
2			
3			

Part 1 – Implement a multi cycle processor that implement MIPS ISA 32 bit processor. (15 Mark)

- Using (VHDL) in the implementation
- Implement the Datapath and the control unit
- Simulate your design for different input



1 Mark will be deducted for each day of delay.

Submission Date:

The due date is W13.

The presentation day after week 13.

Report (3 Mark) and Prestation content (2 Mark)

- The report should be written as a **Complete Report**. It must contain the following:



كلية الهندسة - جامعة الزقازيق

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Cover Page

Table of Contents

1. The assignment Aim
2. The Problem Solution.
 2. 1. Inputs and Outputs
3. Implementation
 - 3.2 Give the Schematic diagram using Active HDL
 - 3.3 Simulate result
4. References

- Write your work, and name, ID, and email for each student in the coverpage.
- The file should be in word document format (.docx) or (.pdf) . As well as the presentation in PPT.
- You request to describe your design in report, include the design, code and simulation shown the inputs and outputs signals.
- The report includes all your references