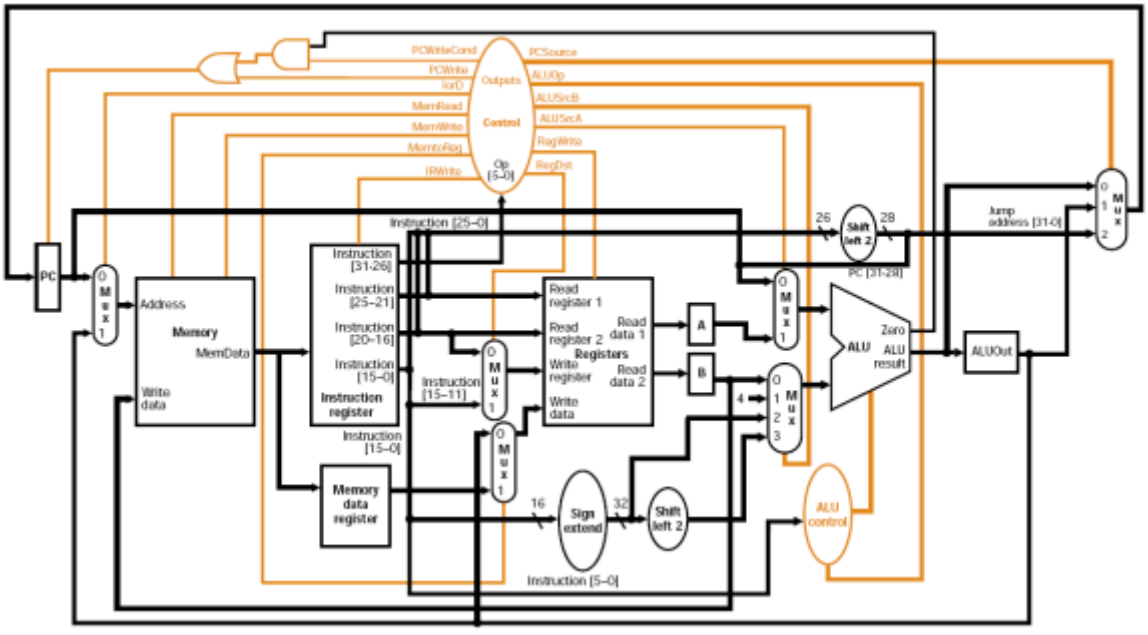
Course *CSE 226: Hardware Design*
PROJECT

No.	Name	Academic number	Task completed
1			
2			
3			

Part 1 – Implement a multi cycle processor that implement MIPS ISA 32 bit processor. (15 Mark)

- Using (VHDL) in the implementation
- Implement the Datapath and the control unit
- Simulate your design for different input



1 Mark will be deducted for each day of delay.

Submission Date:
The due date is W13.
The presentation day after week 13.

Report (3 Mark) and Prestation content (2 Mark)

- The report should be written as a **Complete Report**. **It must contain the following:**

- Write your work, and name, ID, and email for each student in the coverpage.
- The file should be in word document format (.docx) or (.pdf) . As well as the presentation in PPT.
- You request to describe your design in report, include the design, code and simulation shown the inputs and outputs signals.
- The report includes all your references