Tx TLP Scenario (gen1/2):

1- Link layer sends the TLP on 64x8 (512 bits) to LPIF Tx control & data flow module and the position of the starting symbol and the ending symbol of the packet.

2- LPIF Tx control & data flow module inserts the starting and ending symbol on their position and stores the packet in the FIFO.

3- LPIF Tx control & data flow module sends the stored data to the mux with width equals the number of lanes x pipe width (16 lanes x 32 bits).

4- The mux selects between the LPIF Tx control & data flow module input and the OS generator depending on the TX LTSSM selector and passes it to the lane management control.

5- The lane management control stripes the bytes on the pipe lanes (eg. 16 lanes) and passes them to the scrambler.

6- The scrambler passes the reserved symbols and scrambles the rest of the data.

7- The pipe Tx data block asserts the Tx data valid.