

## Analytical methods



\*

hyperperiod.

$$* \text{CPU load} = \frac{\text{time of execution}}{\text{time-free}} \times 100$$

\* schedulability : no missing of deadline  
VRM / time demand  
analysts

التاريخ:

الموضوع:

① hyperperiod : 100

every 100ms all task at the same execution time

$$② \text{CPU load} = \frac{(1 \times 2) + (1 \times 2) + 1 + (1 \times 5) + (5 \times 10) + 12}{100} \times 100$$

$$\text{CPU load} = 72\%$$

Rate monotonic utilization =  $URM$

$$U = \sum_{i=1}^n \frac{C_i}{P_i} \leq n(2^{\frac{1}{n}} - 1)$$

$$U = \frac{1}{50} + \frac{1}{50} + \frac{1}{100} + \frac{1}{20} + \frac{5}{10} + \frac{12}{100} = 0.72$$

$$URM = 6 \times (2^{\frac{1}{6}} - 1) = 0.73$$

$$U \leq URM$$

System guaranteed schedulable

Time demand analysis

$$w_i(t) = e_i + \sum_{k=1}^{i-1} \left\lceil \frac{t}{P_k} \right\rceil e_k$$

time demand < time provided.

$$w_1(10) = 5 + 0 = 5 \text{ schedulable}$$

$$w_2(20) = 1 + \left(\frac{20}{10}\right) 5 = 11 \quad //$$

$$w_3(50) = 1 + \left(\frac{50}{50}\right) 11 + \left(\frac{50}{10}\right) 5 = 27 \text{ schedulable}$$

$$w_4(50) = \quad // \quad // \quad //$$

$$w_5(100) = 1 + \left(\frac{100}{50}\right) + \left(\frac{100}{50}\right) + \left(\frac{100}{100}\right) 12 +$$

$$\left(\frac{100}{10}\right) 5 + \left(\frac{100}{20}\right) 1 = 72$$

schedulable

$$w_6(100) = 12 + \left(\frac{100}{50}\right) + \left(\frac{100}{50}\right) + \left(\frac{100}{100}\right)$$

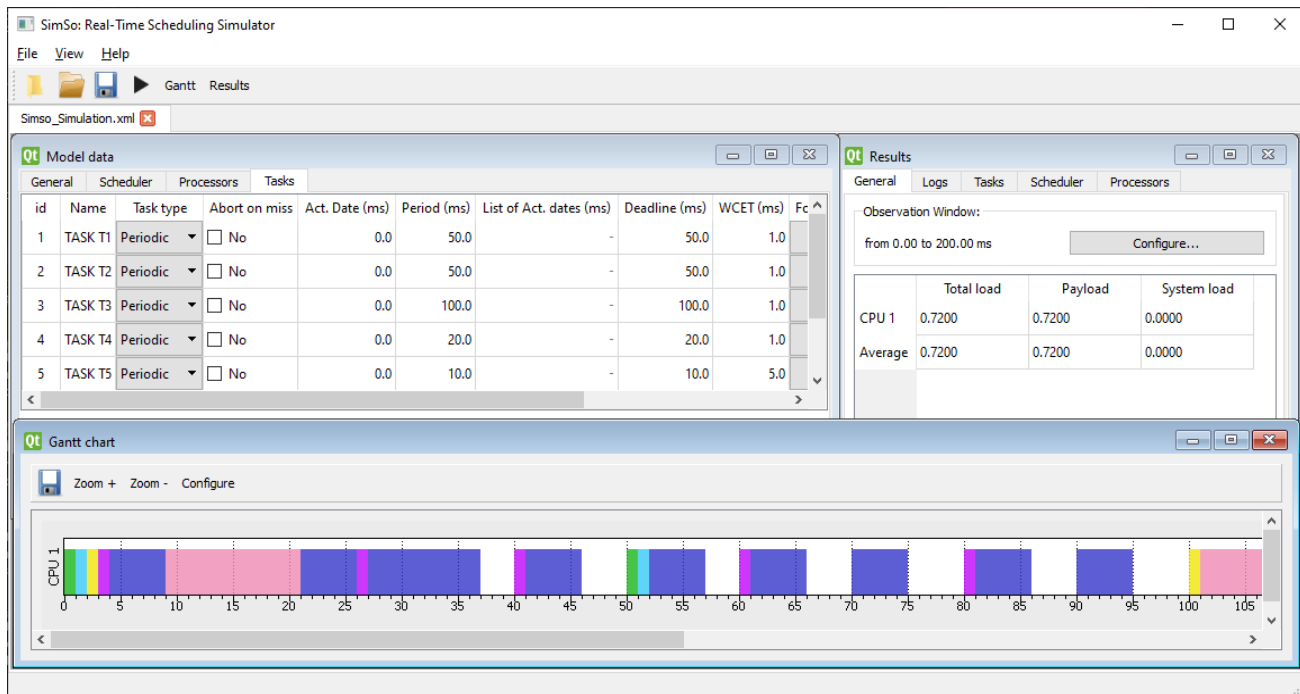
$$+ \left(\frac{100}{10}\right) 5 + \left(\frac{100}{20}\right) 1 = 72$$

schedulable

No task misses the deadline

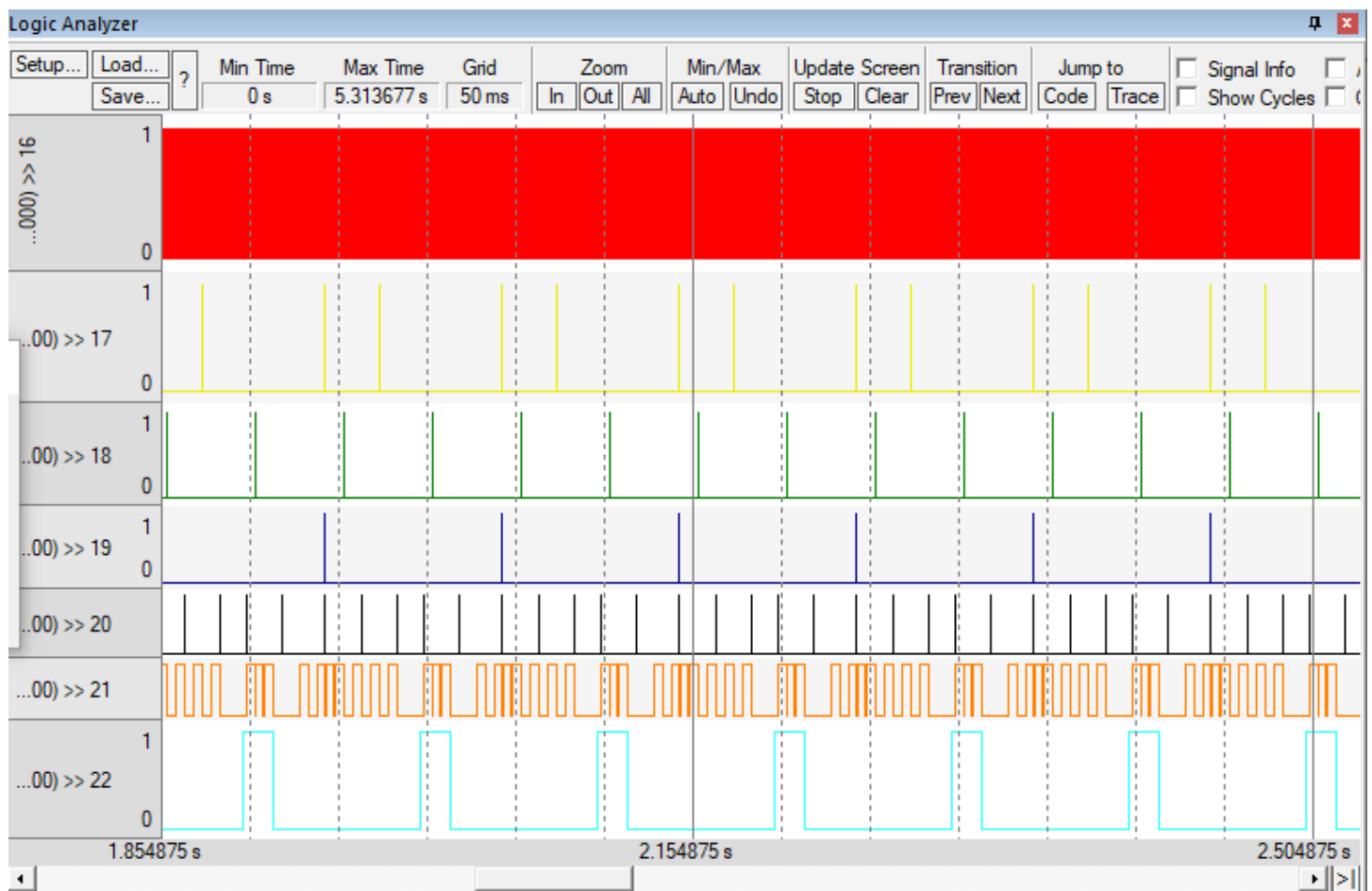
System is schedulable

## Offline Simso:



## Online Simulator:

Logic analyzer **Using trace macros and GPIOs**



## Data watching using **timer 1** and **trace macros**

Watch 1			⌵
Name	Value	Type	
system_Time	0x0004DBD5	uint	
CPU_load	72	uint	
TASK_5_timeTotal	0x0002121A	uint	
TASK_6_timeTotal	0x00016F44	uint	
missA	0x00000001	uint	
missB	0x00000000	uint	
<Enter expression>			

UART #2		
L		
oad_2_ 2984	9%	
Periodi 2645	7%	
Uart_Re 4738	14%	
Button_ 7957	24%	
rt_Re 4738	14%	
H		
P		
eriodi 2645	7%	
Uart_Re 5061	14%	
Load_2_ 2984	8%	
Button_ 1228	3%	
rt_Re 4738	14%	
H		

**Results indicate a successful implementation**