# Computer Architecture

## Lab # 02 : Reorder Buffer

**Section # 7**

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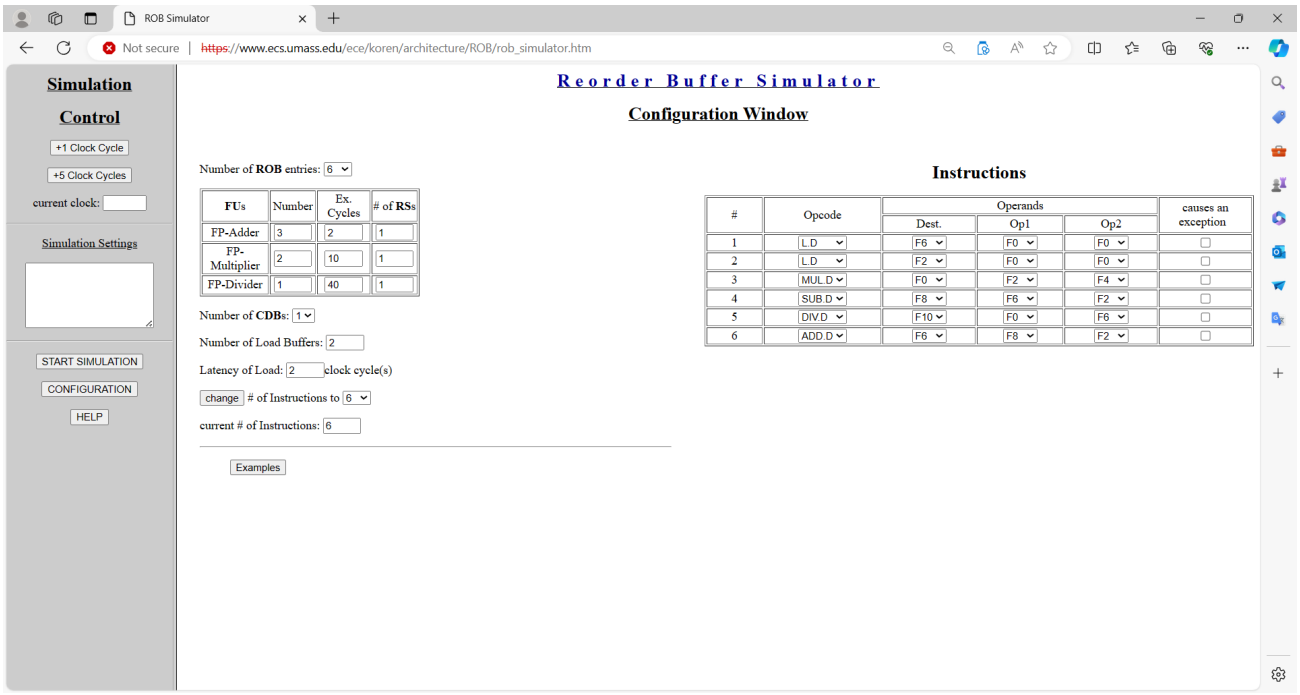
**It is required to come up with two different instruction sets (of no less than 5 instructions each):**

## Part 1

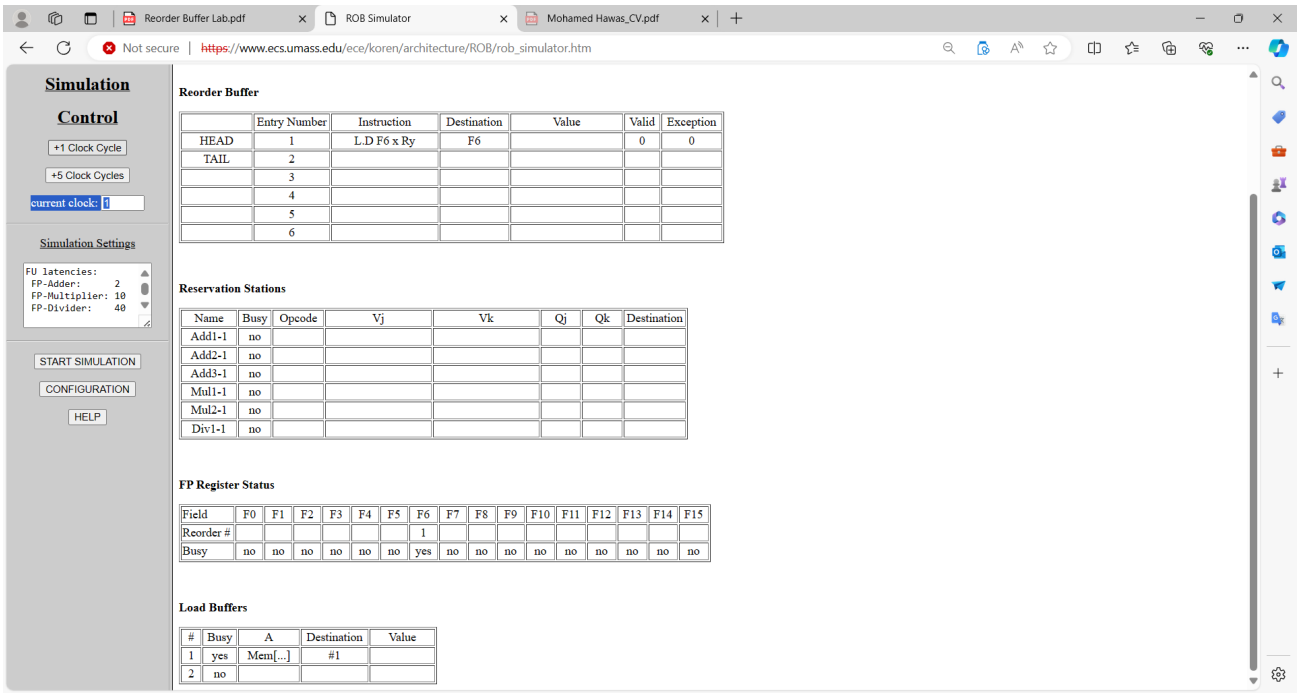
One that shows the strengths of the reorder buffer technique. That is, show how it could enable multiple, simultaneous execution of different instructions on different functional units.

**Solution.**

- Configuration



- **Cycle : 01**



Reorder Buffer Lab.pdf | ROB Simulator | Mohamed Hawas_CV.pdf

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 1

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | | 0 | 0 |
| TAIL | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

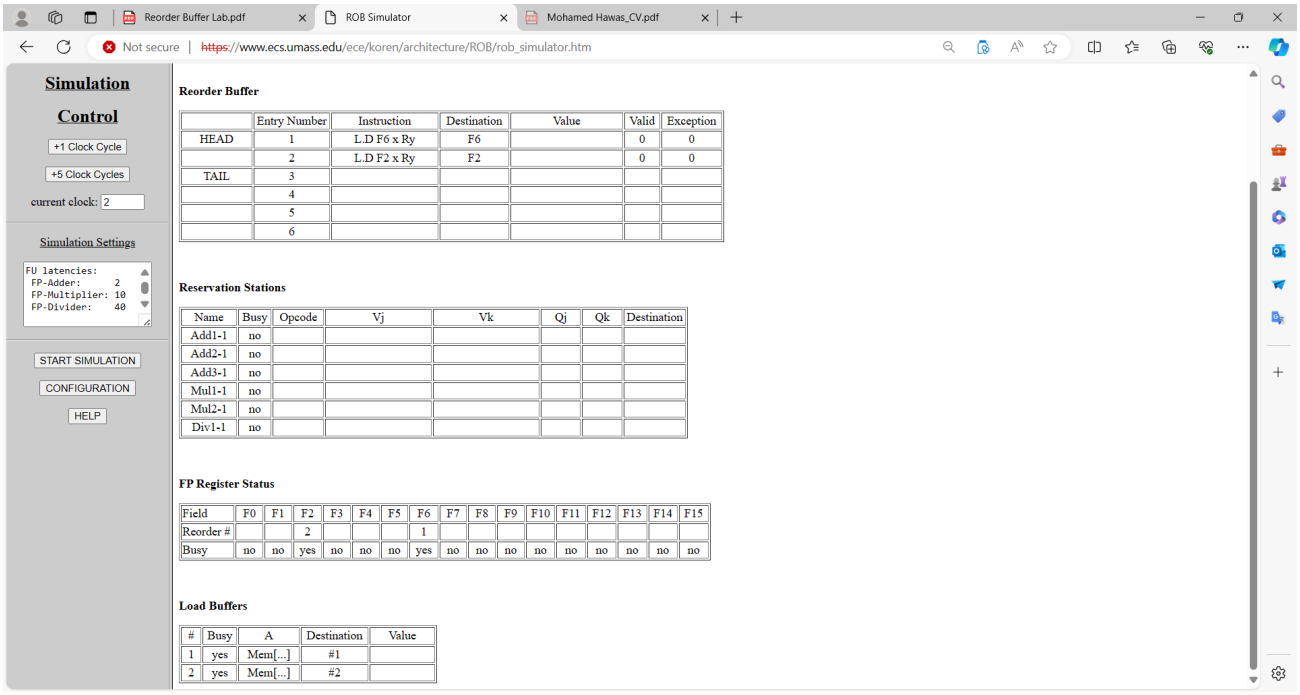
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 1 | | | | | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #1 | |
| 2 | no | | | |

- **Cycle : 02**



Reorder Buffer Lab.pdf | ROB Simulator | Mohamed Hawas_CV.pdf

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 2

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | | 0 | 0 |
| | 2 | L.D F2 x Ry | F2 | | 0 | 0 |
| TAIL | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

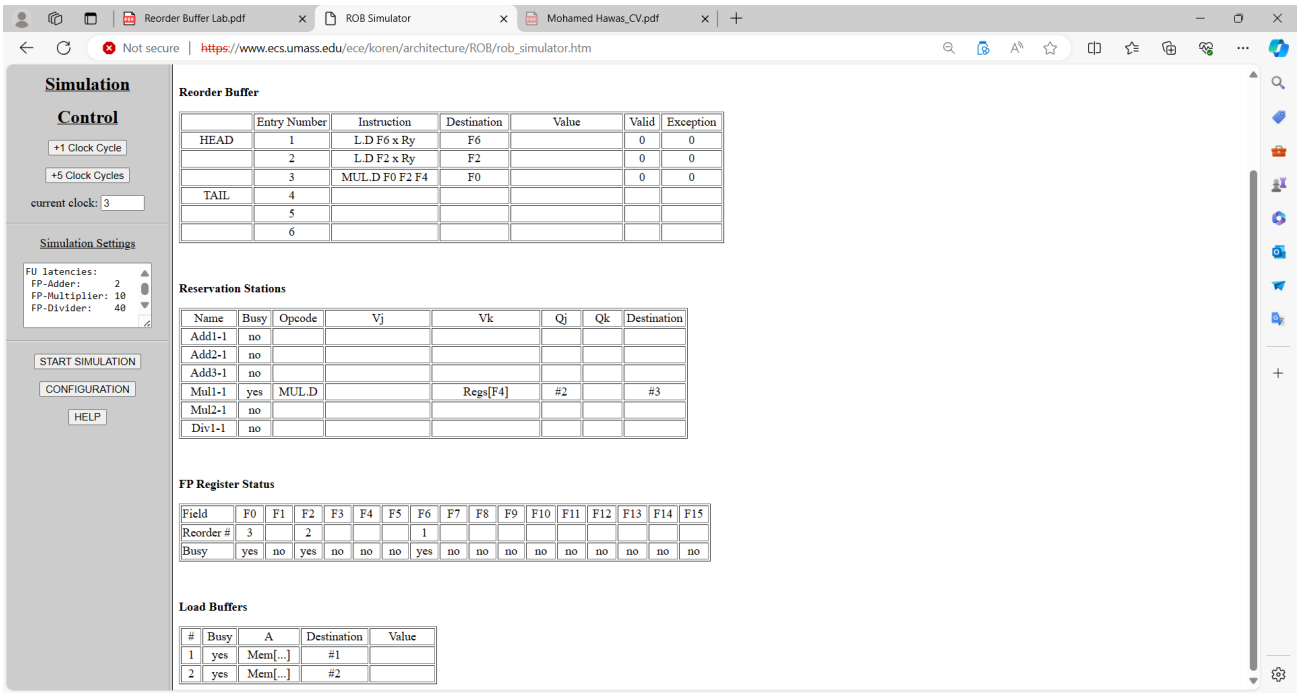
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | 2 | | | | 1 | | | | | | | | | |
| Busy | no | no | yes | no | no | no | yes | no | no | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #1 | |
| 2 | yes | Mem[...] | #2 | |

- **Cycle : 03**



Reorder Buffer Lab.pdf | ROB Simulator | Mohamed Hawas_CV.pdf

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 3

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | | 0 | 0 |
| | 2 | L.D F2 x Ry | F2 | | 0 | 0 |
| | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| TAIL | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | | Regs[F4] | #2 | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

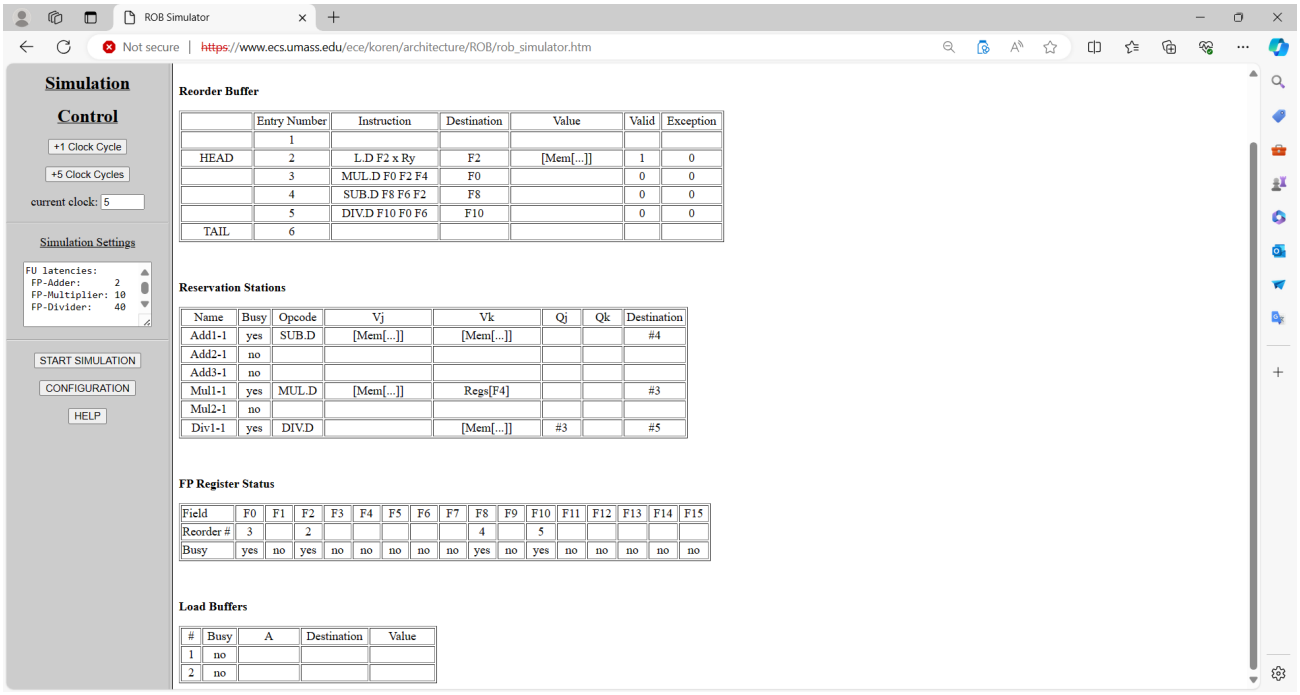
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | 2 | | | | 1 | | | | | | | | | |
| Busy | yes | no | yes | no | no | no | yes | no | no | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #1 | |
| 2 | yes | Mem[...] | #2 | |

- **Cycle : 05**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 5

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| HEAD | 2 | L.D F2 x Ry | F2 | [Mem[...]] | 1 | 0 |
| | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | | 0 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| TAIL | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | SUB.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | [Mem[...]] | Regs[F4] | | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | | [Mem[...]] | #3 | | #5 |

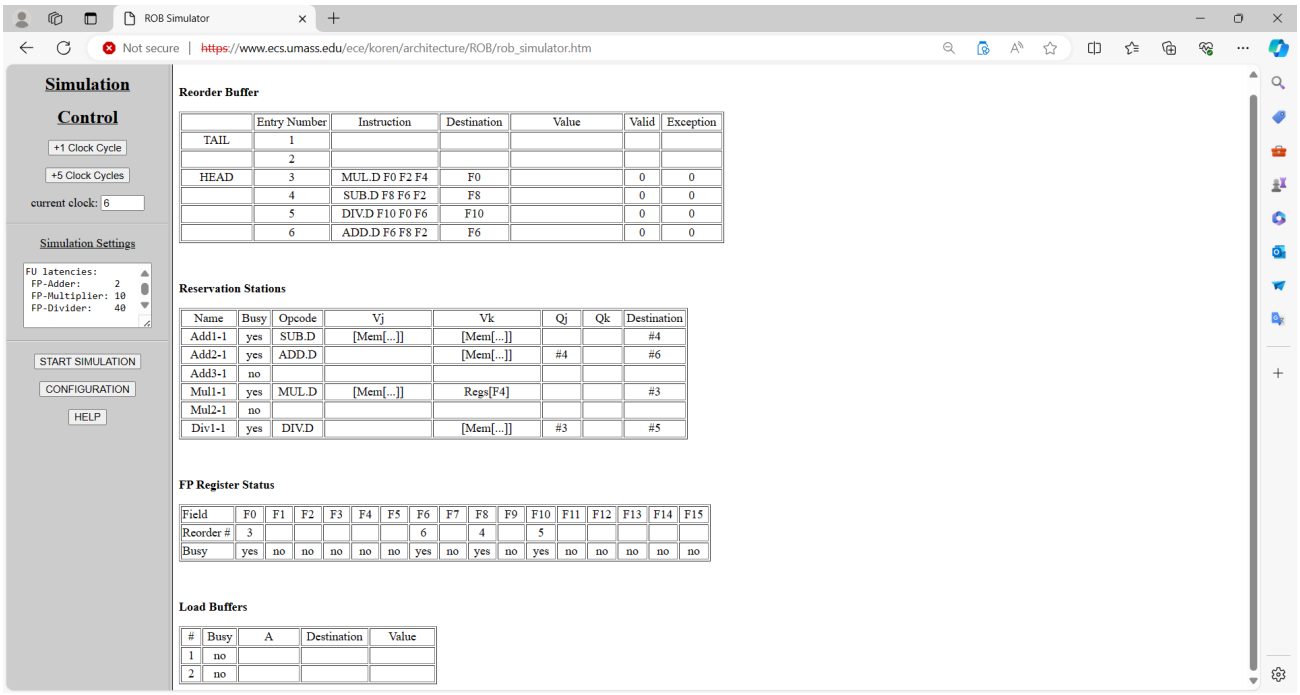
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | 2 | | | | | | 4 | | 5 | | | | | |
| Busy | yes | no | yes | no | no | no | no | no | yes | no | yes | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 06**



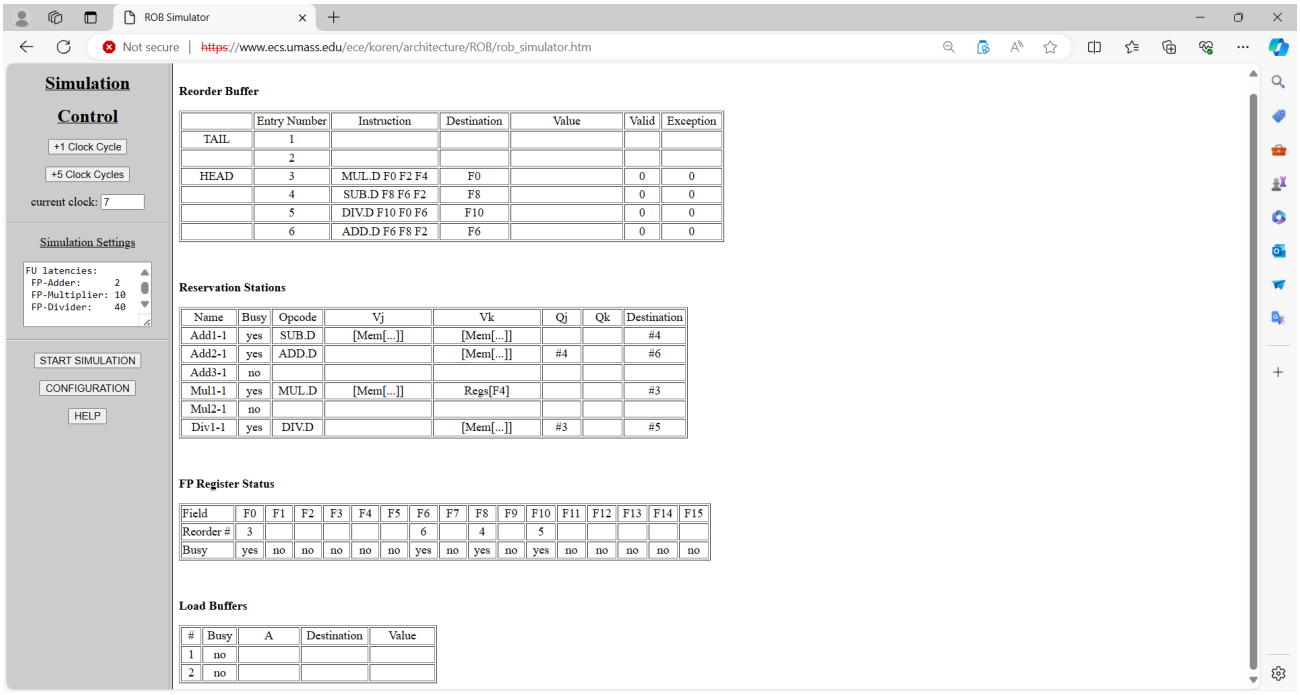

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | | 0 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | | 0 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | SUB.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Add2-1 | yes | ADD.D | | [Mem[...]] | #4 | | #6 |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | [Mem[...]] | Regs[F4] | | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | | [Mem[...]] | #3 | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | yes | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 07**



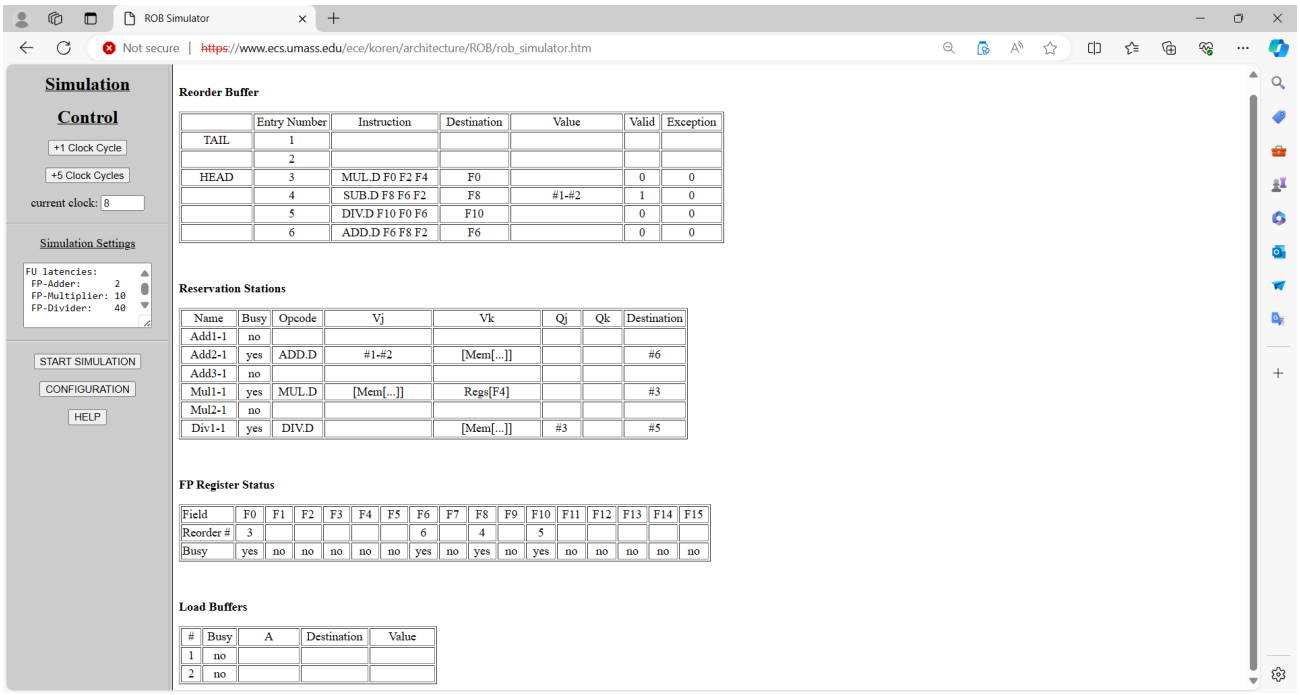

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | | 0 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | | 0 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | SUB.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Add2-1 | yes | ADD.D | | [Mem[...]] | #4 | | #6 |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | [Mem[...]] | Regs[F4] | | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | | [Mem[...]] | #3 | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | yes | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 08**



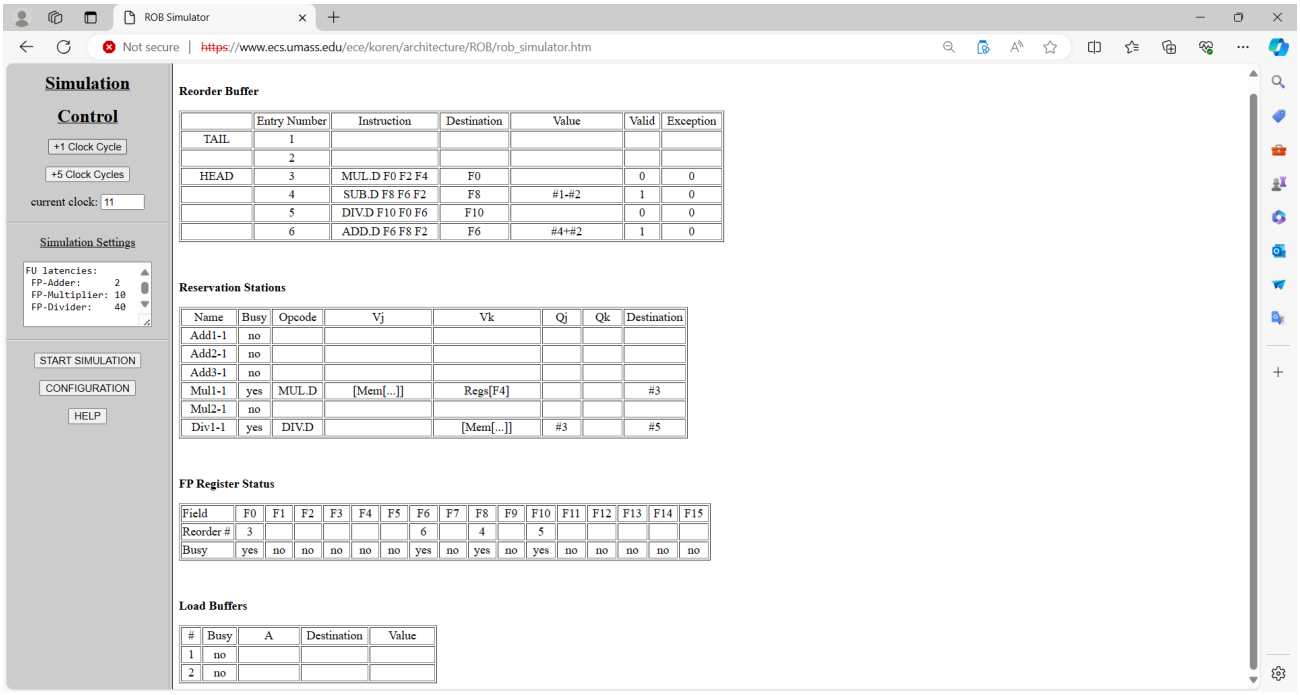

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | #1-#2 | 1 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | | 0 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | yes | ADD.D | #1-#2 | [Mem[...]] | | | #6 |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | [Mem[...]] | Regs[F4] | | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | | [Mem[...]] | #3 | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | yes | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 11**



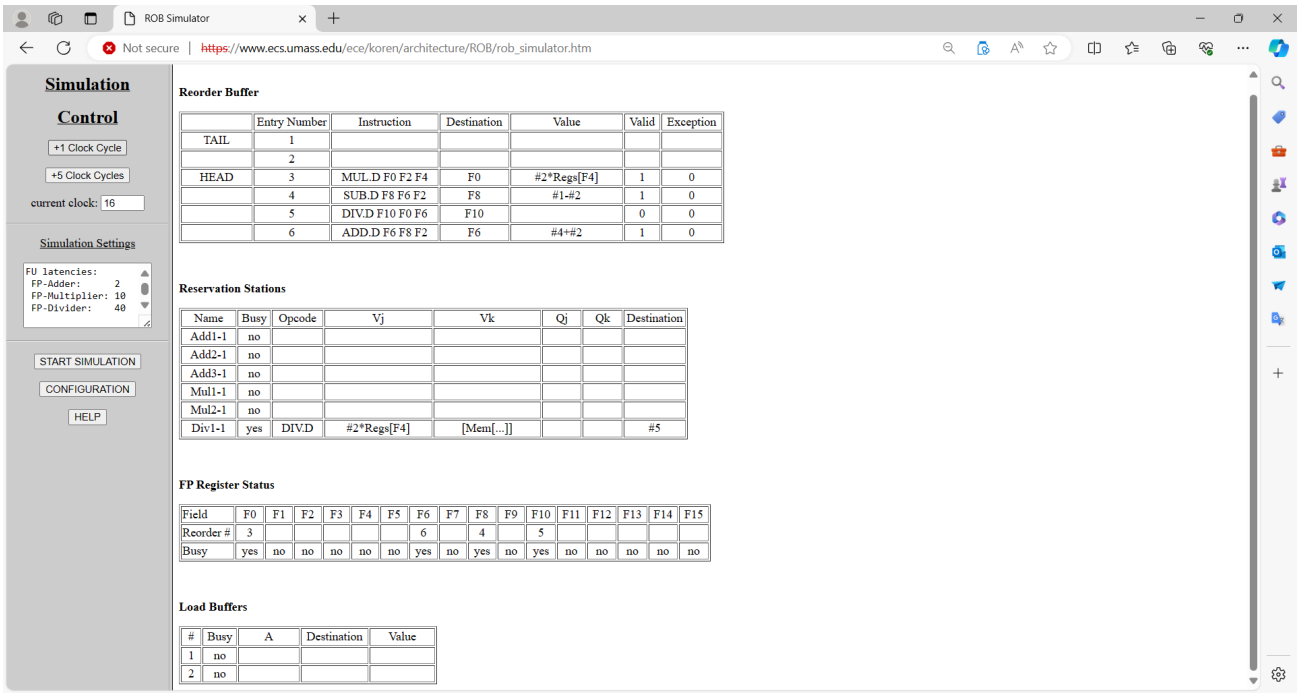

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | MUL.D F0 F2 F4 | F0 | | 0 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | #1-#2 | 1 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | yes | MUL.D | [Mem[...]] | Regs[F4] | | | #3 |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | | [Mem[...]] | #3 | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | yes | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 16**



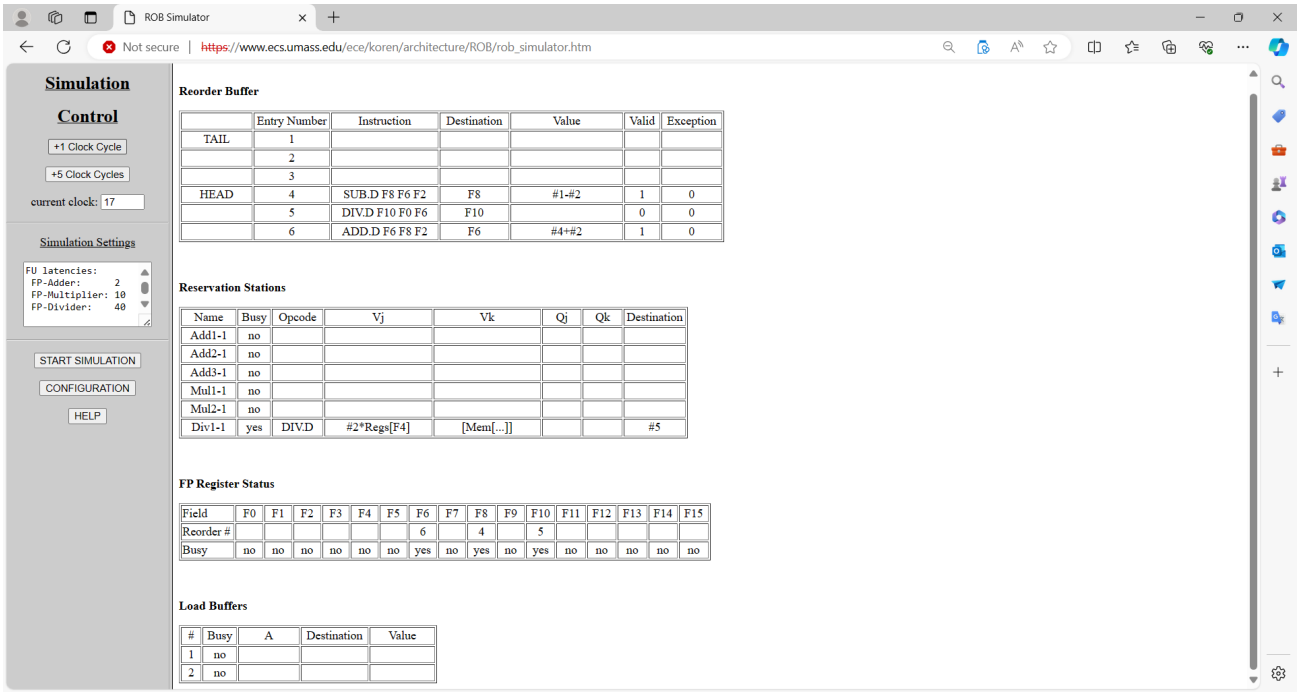

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | MUL.D F0 F2 F4 | F0 | #2*Regs[F4] | 1 | 0 |
| | 4 | SUB.D F8 F6 F2 | F8 | #1-#2 | 1 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | #2*Regs[F4] | [Mem[...]] | | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | yes | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 17**



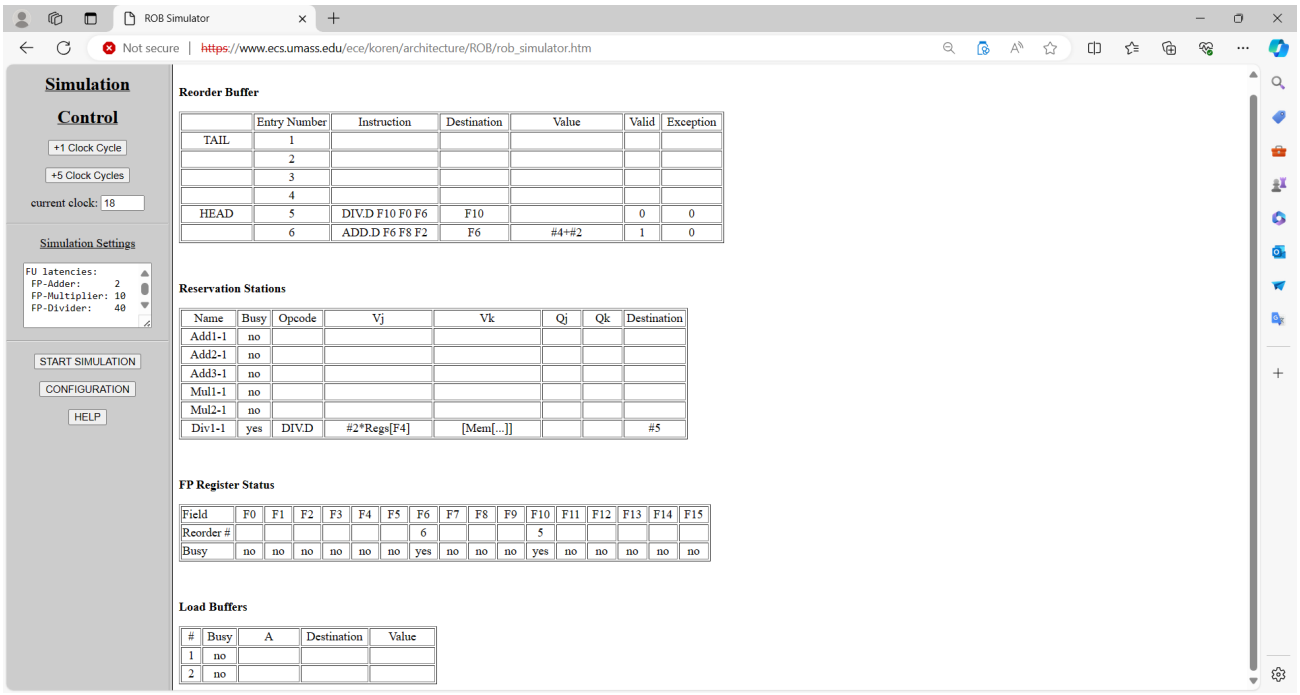

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| HEAD | 4 | SUB.D F8 F6 F2 | F8 | #1-#2 | 1 | 0 |
| | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | #2*Regs[F4] | [Mem[...]] | | | #5 |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | 4 | | 5 | | | | | |
| Busy | no | no | no | no | no | no | yes | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 18**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 18

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| HEAD | 5 | DIV.D F10 F0 F6 | F10 | | 0 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | yes | DIV.D | #2*Regs[F4] | [Mem[...]] | | | #5 |

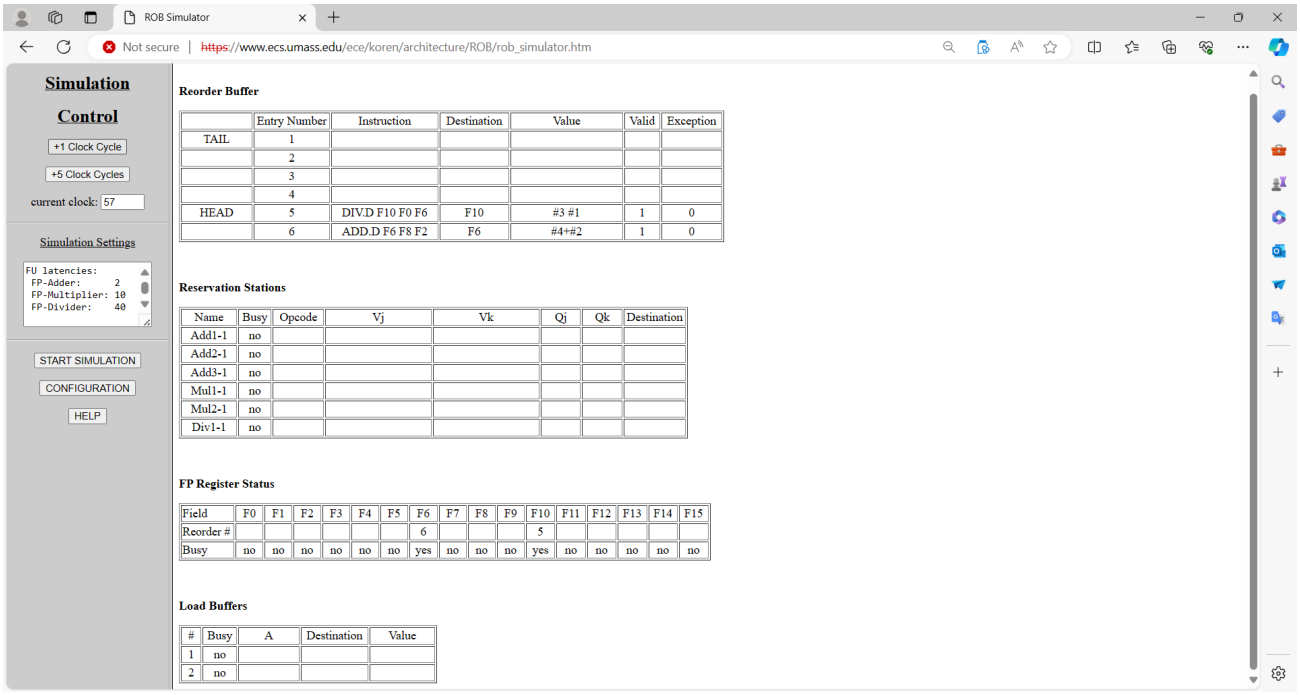
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | | | 5 | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | yes | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 57**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 57

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| HEAD | 5 | DIV.D F10 F0 F6 | F10 | #3 #1 | 1 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

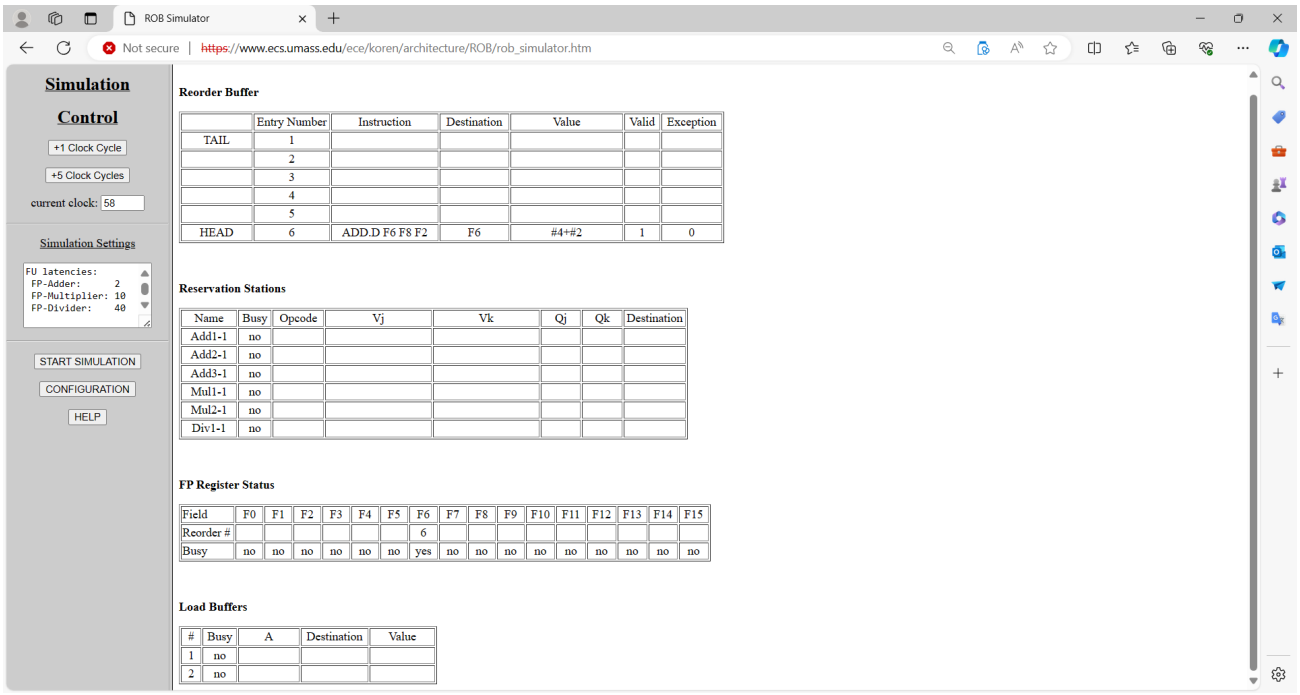
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | | | 5 | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | yes | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Last Cycle : 58**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 58

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| HEAD | 6 | ADD.D F6 F8 F2 | F6 | #4+#2 | 1 | 0 |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

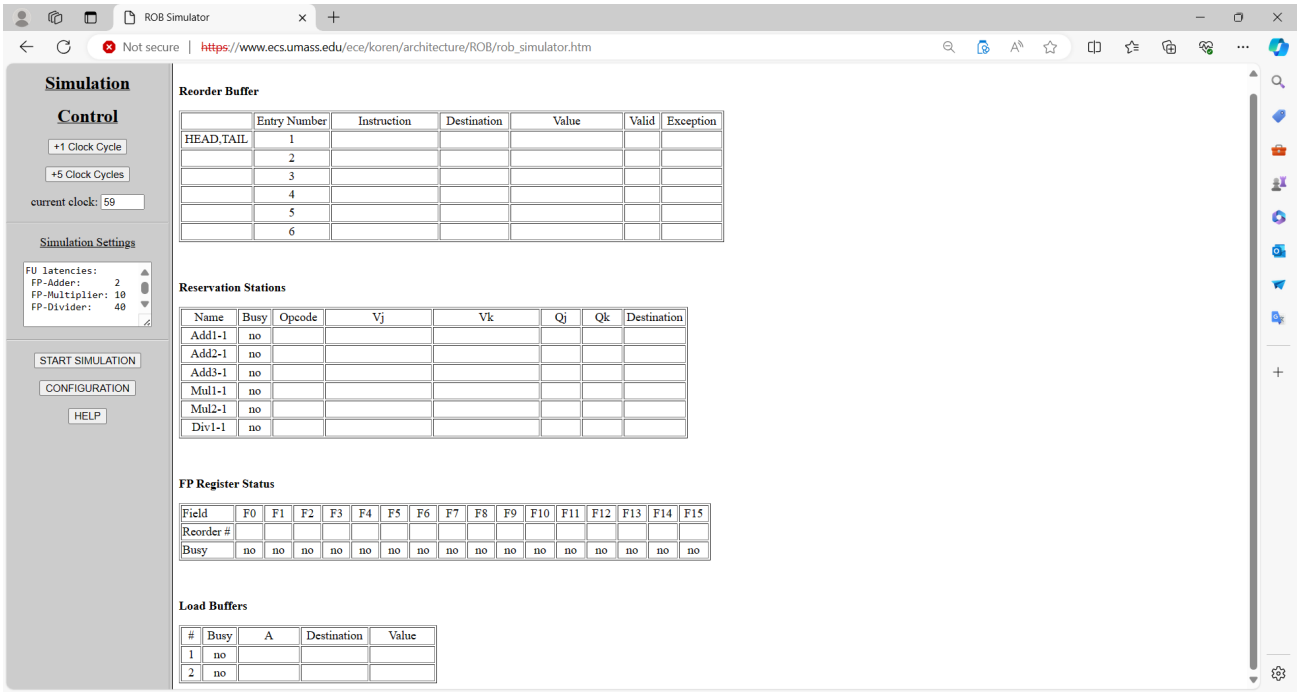
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | | | | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 59**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 59

Simulation Settings

```
FU latencies:
 FP-Adder:      2
 FP-Multiplier: 10
 FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD,TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Add2-1 | no | | | | | | |
| Add3-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Mul2-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | | | | | | | | | | |
| Busy | no | no | no | no | no | no | no | no | no | no | no | no | no | no | no | no |

**Load Buffers**

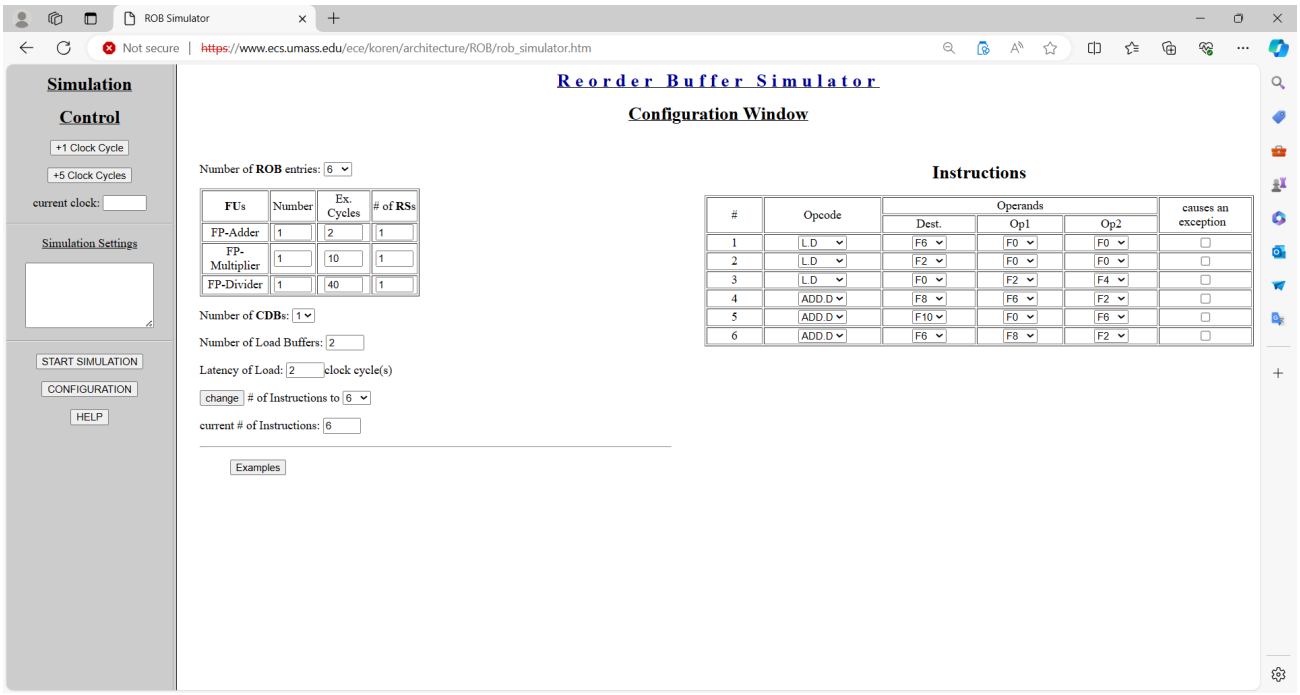
| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

## Part 2

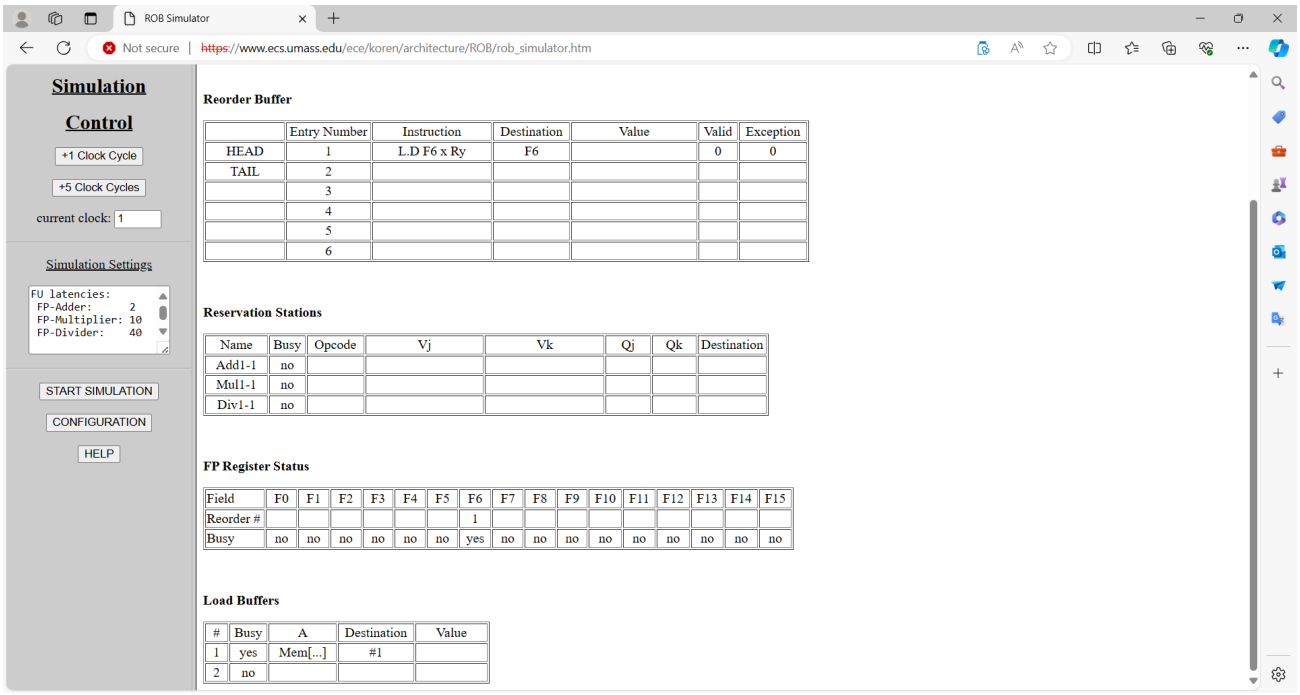
One where the reorder buffer does not help. For example, where the instructions go to the same functional unit.

### Solution.

- Configuration



- **Cycle : 01**



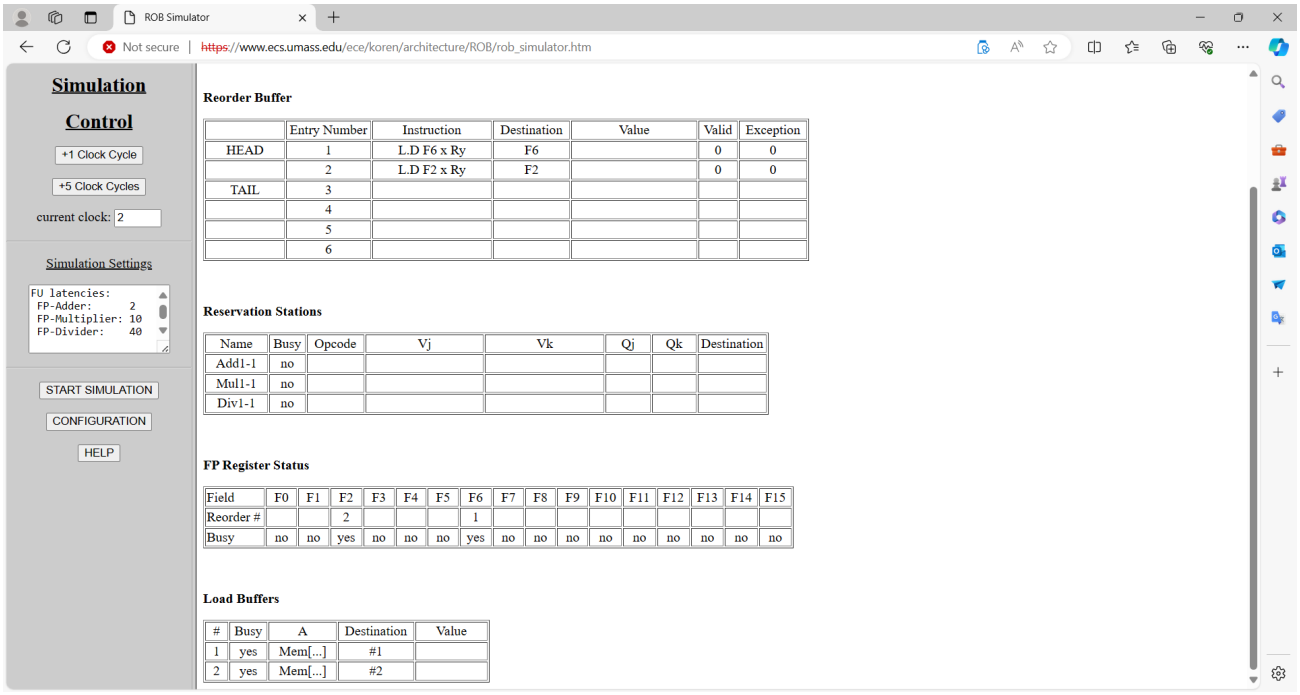

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | | 0 | 0 |
| TAIL | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 1 | | | | | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | no | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #1 | |
| 2 | no | | | |

- **Cycle : 02**



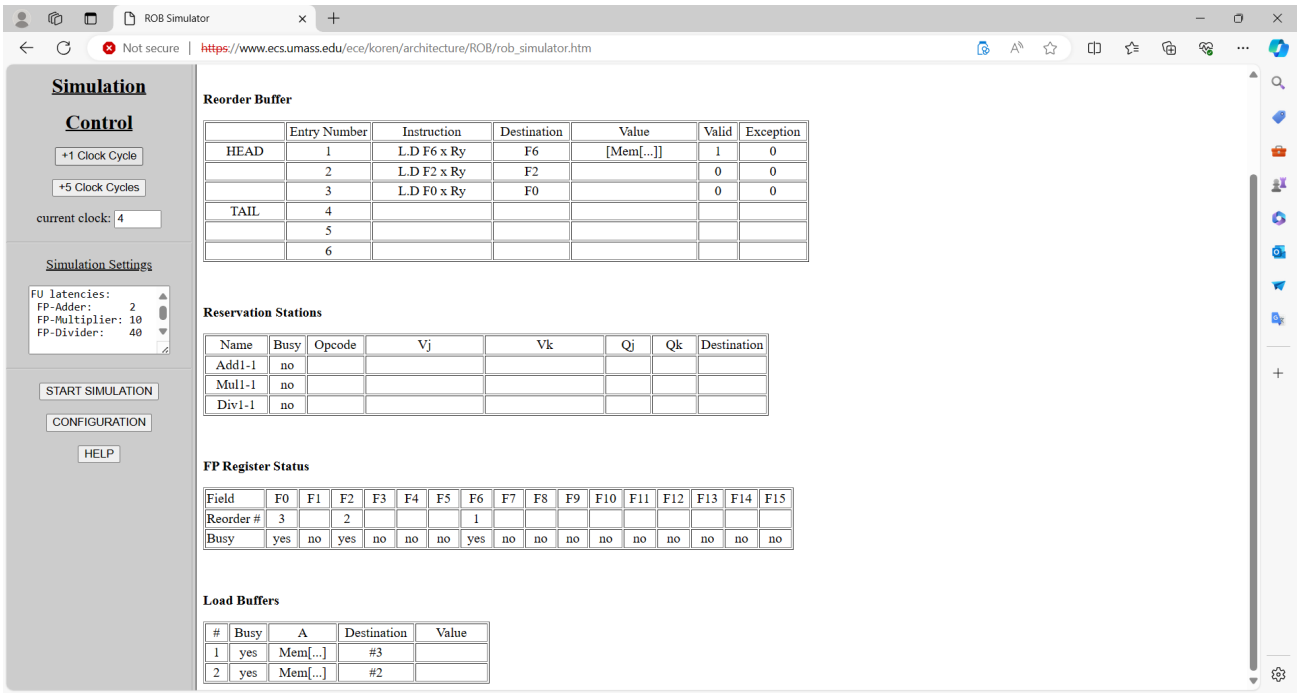

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | | 0 | 0 |
| | 2 | L.D F2 x Ry | F2 | | 0 | 0 |
| TAIL | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | 2 | | | | 1 | | | | | | | | | |
| Busy | no | no | yes | no | no | no | yes | no | no | no | no | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #1 | |
| 2 | yes | Mem[...] | #2 | |

- **Cycle : 04**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 4

Simulation Settings

```
FU latencies:
FP-Adder:       2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| HEAD | 1 | L.D F6 x Ry | F6 | [Mem[...]] | 1 | 0 |
| | 2 | L.D F2 x Ry | F2 | | 0 | 0 |
| | 3 | L.D F0 x Ry | F0 | | 0 | 0 |
| TAIL | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | no | | | | | | |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

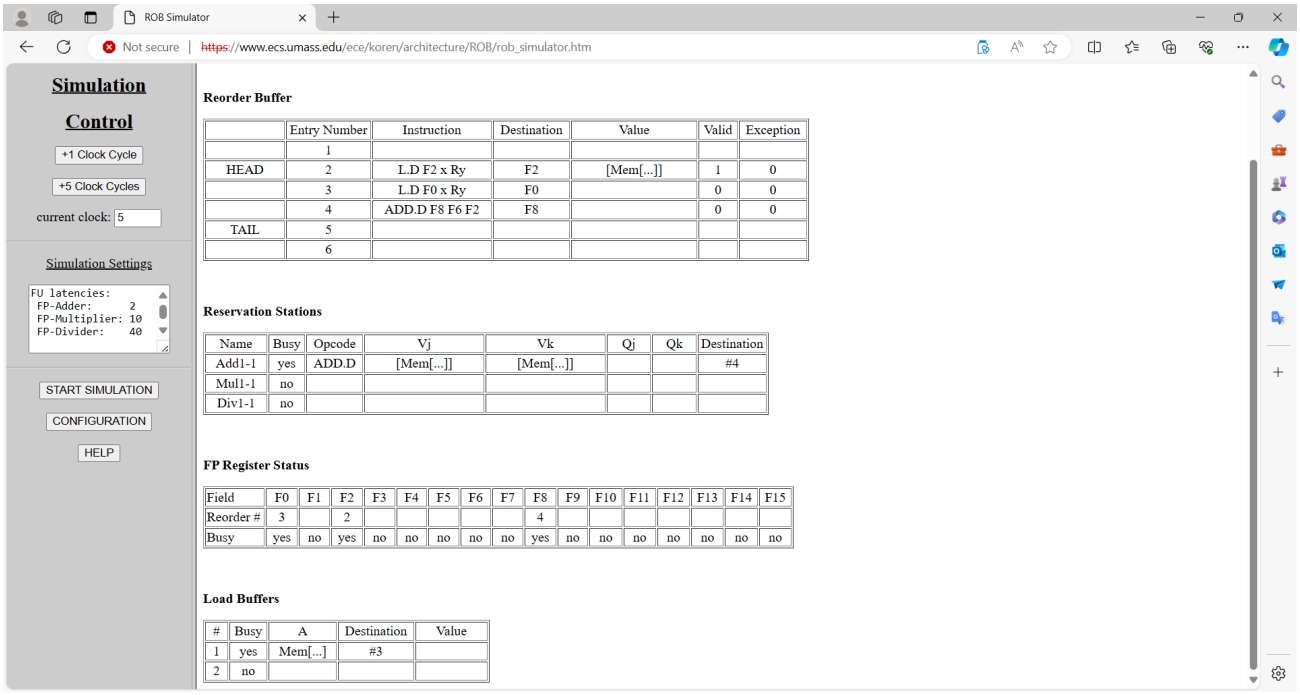
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | 2 | | | | 1 | | | | | | | | | |
| Busy | yes | no | yes | no | no | no | yes | no | no | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #3 | |
| 2 | yes | Mem[...] | #2 | |

- **Cycle : 05**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 5

Simulation Settings

```
FU latencies:
FP-Adder:       2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| HEAD | 2 | L.D F2 x Ry | F2 | [Mem[...]] | 1 | 0 |
| | 3 | L.D F0 x Ry | F0 | | 0 | 0 |
| | 4 | ADD.D F8 F6 F2 | F8 | | 0 | 0 |
| TAIL | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

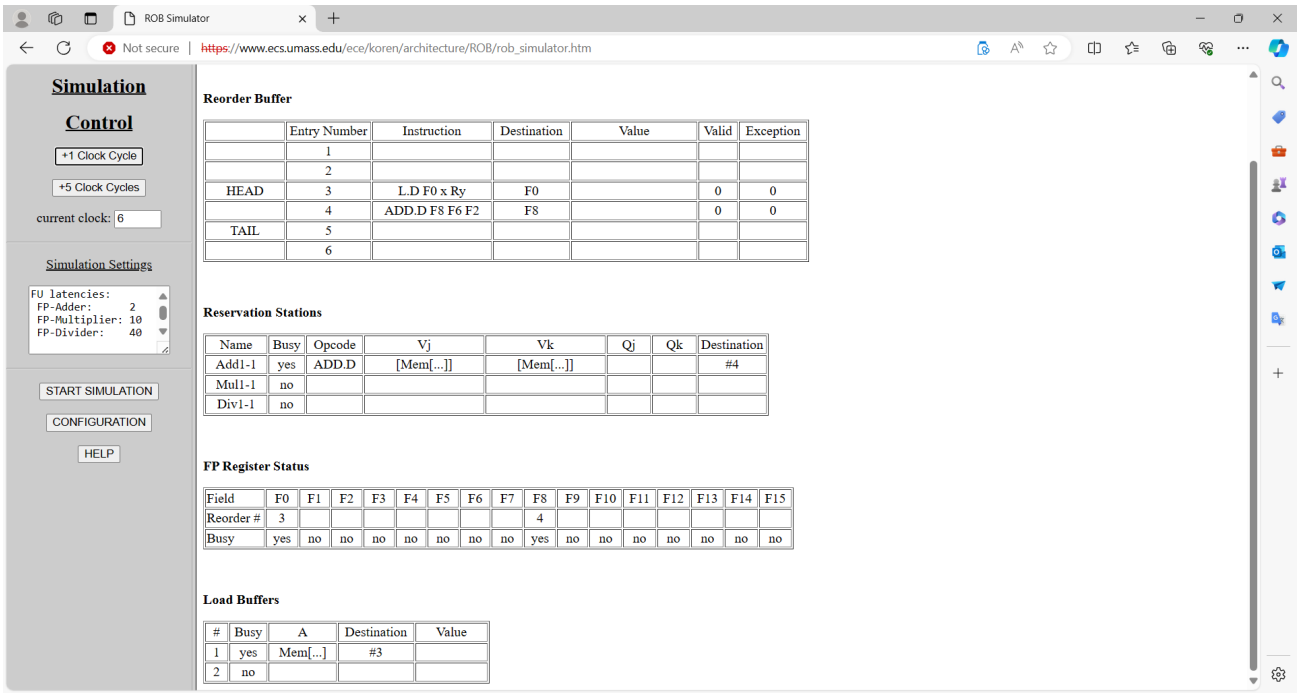
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | 2 | | | | | | 4 | | | | | | | |
| Busy | yes | no | yes | no | no | no | no | no | yes | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #3 | |
| 2 | no | | | |

- **Cycle : 06**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 6

Simulation Settings

```
FU latencies:
FP-Adder:       2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | L.D F0 x Ry | F0 | | 0 | 0 |
| | 4 | ADD.D F8 F6 F2 | F8 | | 0 | 0 |
| TAIL | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

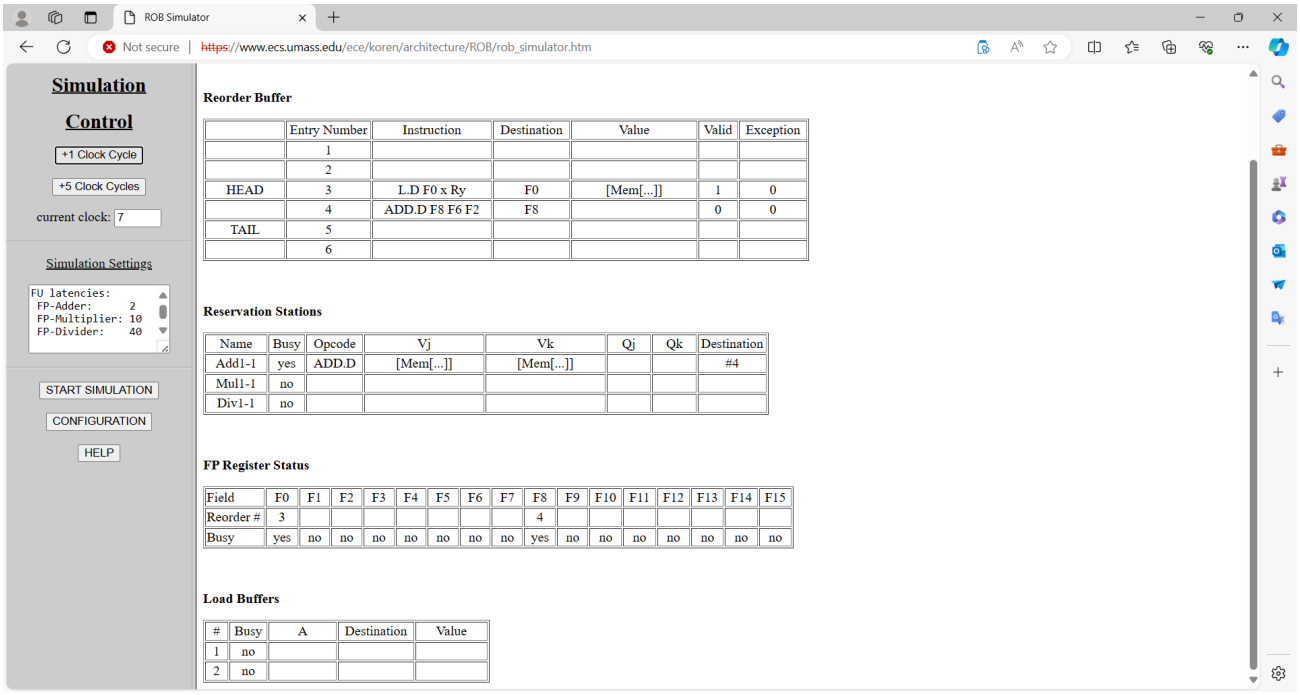
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | | | 4 | | | | | | | |
| Busy | yes | no | no | no | no | no | no | no | yes | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | yes | Mem[...] | #3 | |
| 2 | no | | | |

- **Cycle : 07**



ROB Simulator

Not secure | https://www.ecs.umass.edu/ece/koren/architecture/ROB/rob_simulator.htm

**Simulation Control**

+1 Clock Cycle

+5 Clock Cycles

current clock: 7

Simulation Settings

```
FU latencies:
FP-Adder:       2
FP-Multiplier: 10
FP-Divider:    40
```

START SIMULATION

CONFIGURATION

HELP

**Reorder Buffer**

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| HEAD | 3 | L.D F0 x Ry | F0 | [Mem[...]] | 1 | 0 |
| | 4 | ADD.D F8 F6 F2 | F8 | | 0 | 0 |
| TAIL | 5 | | | | | |
| | 6 | | | | | |

**Reservation Stations**

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | [Mem[...]] | [Mem[...]] | | | #4 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

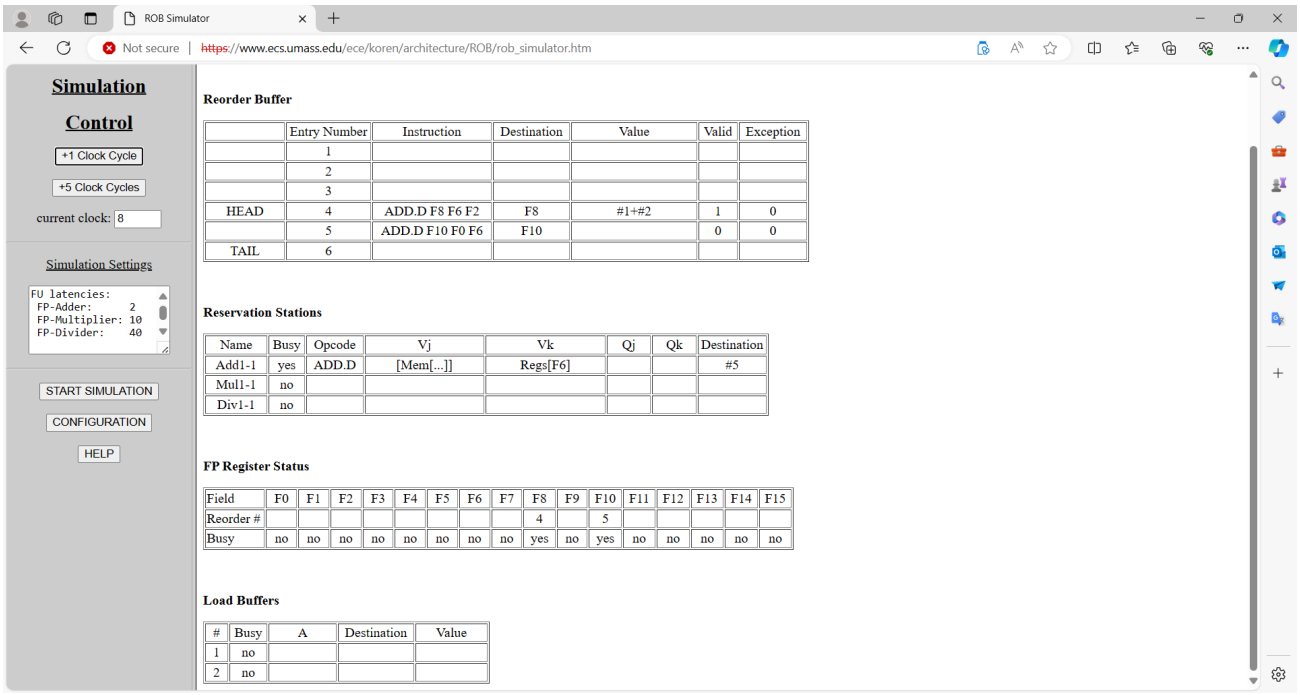
**FP Register Status**

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | 3 | | | | | | | | 4 | | | | | | | |
| Busy | yes | no | no | no | no | no | no | no | yes | no | no | no | no | no | no | no |

**Load Buffers**

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 08**



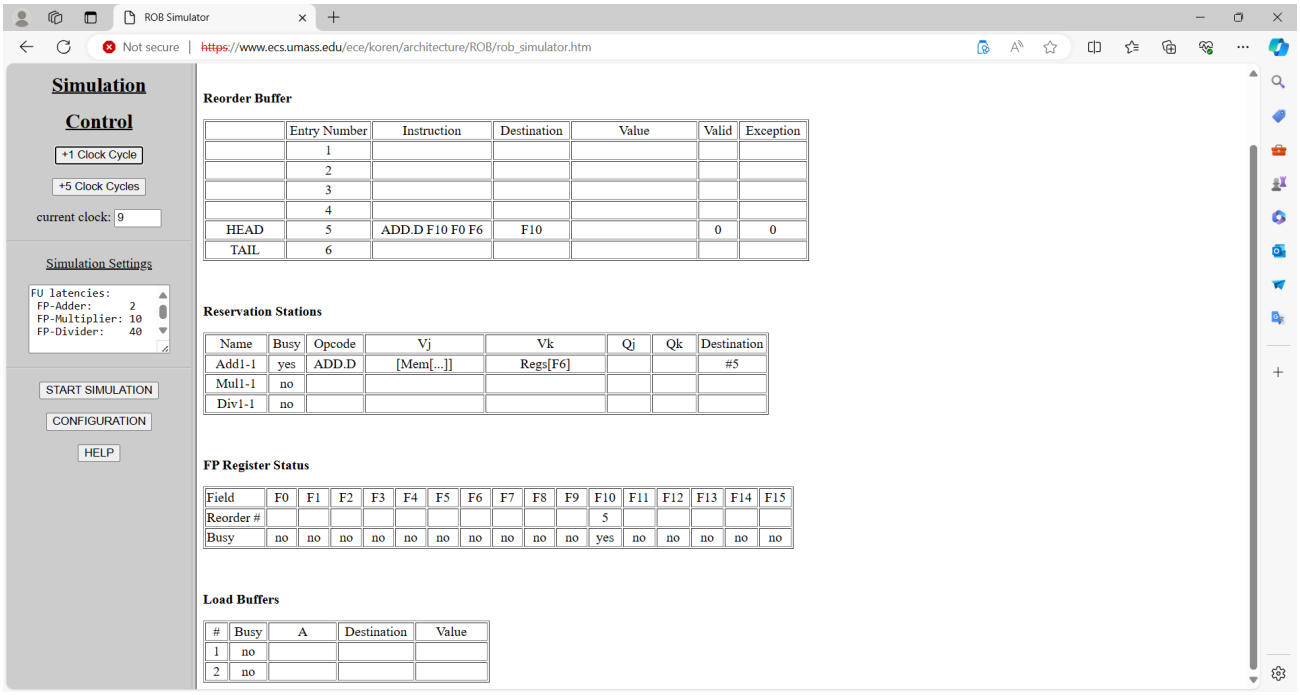

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| HEAD | 4 | ADD.D F8 F6 F2 | F8 | #1+#2 | 1 | 0 |
| | 5 | ADD.D F10 F0 F6 | F10 | | 0 | 0 |
| TAIL | 6 | | | | | |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | [Mem[...]] | Regs[F6] | | | #5 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | | | 4 | | 5 | | | | | |
| Busy | no | no | no | no | no | no | no | no | yes | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 9**



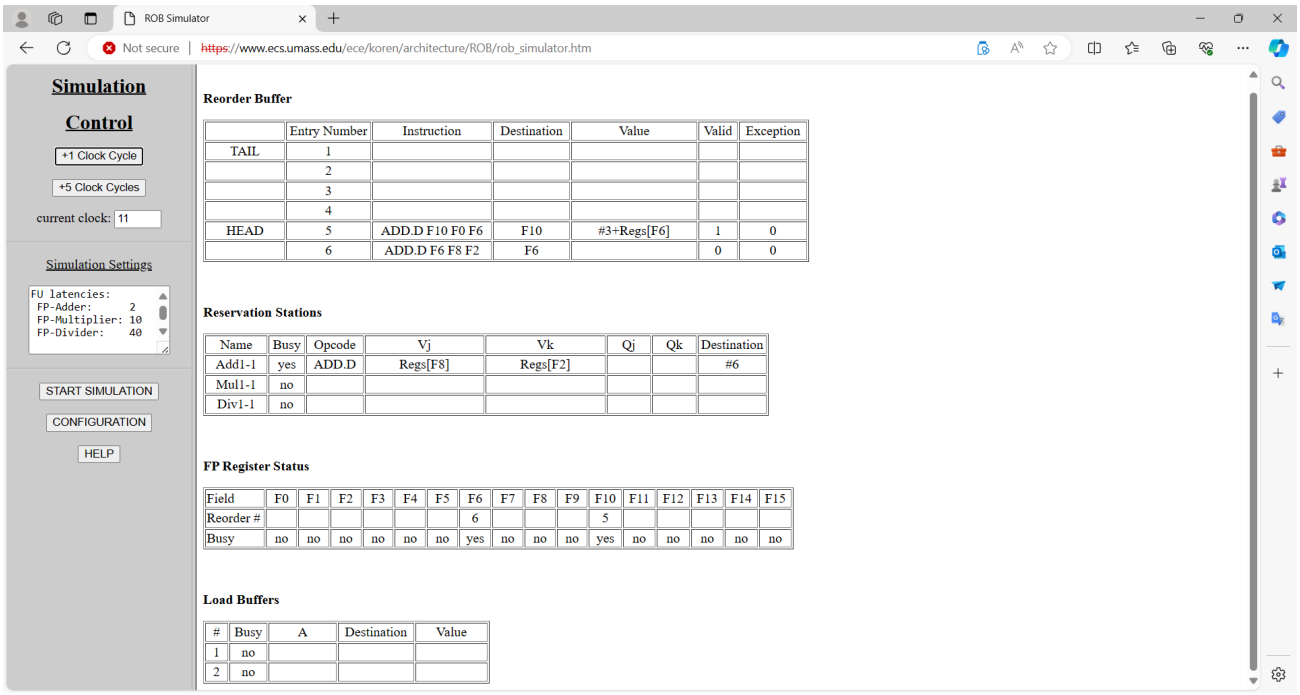

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| HEAD | 5 | ADD.D F10 F0 F6 | F10 | | 0 | 0 |
| TAIL | 6 | | | | | |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | [Mem[...]] | Regs[F6] | | | #5 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | | | | | 5 | | | | | |
| Busy | no | no | no | no | no | no | no | no | no | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 11**



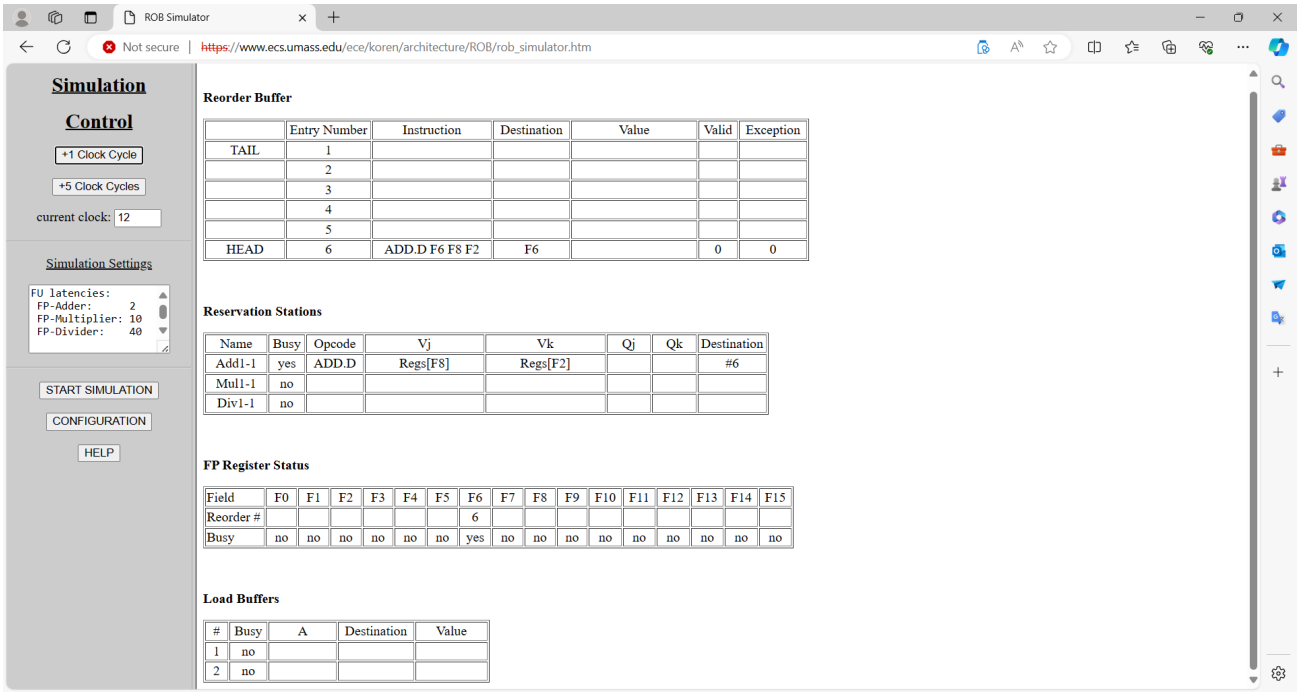

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| HEAD | 5 | ADD.D F10 F0 F6 | F10 | #3+Regs[F6] | 1 | 0 |
| | 6 | ADD.D F6 F8 F2 | F6 | | 0 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | Regs[F8] | Regs[F2] | | | #6 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | | | 5 | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | yes | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Cycle : 12**



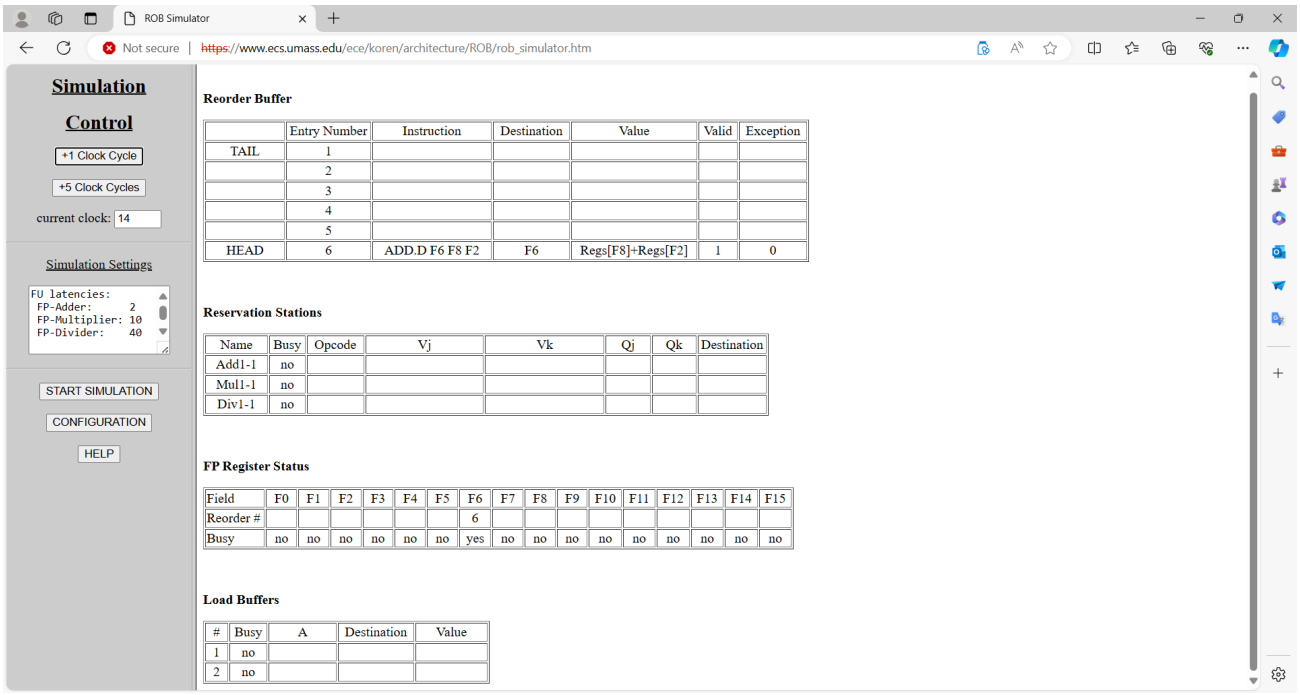

| | Entry Number | Instruction | Destination | Value | Valid | Exception |
|---|---|---|---|---|---|---|
| TAIL | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | | | | | |
| HEAD | 6 | ADD.D F6 F8 F2 | F6 | | 0 | 0 |

| Name | Busy | Opcode | Vj | Vk | Qj | Qk | Destination |
|---|---|---|---|---|---|---|---|
| Add1-1 | yes | ADD.D | Regs[F8] | Regs[F2] | | | #6 |
| Mul1-1 | no | | | | | | |
| Div1-1 | no | | | | | | |

| Field | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 | F14 | F15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reorder # | | | | | | | 6 | | | | | | | | | |
| Busy | no | no | no | no | no | no | yes | no | no | no | no | no | no | no | no | no |

| # | Busy | A | Destination | Value |
|---|---|---|---|---|
| 1 | no | | | |
| 2 | no | | | |

- **Last Cycle : 14**




- **Cycle : 15**