



Register File Implementation

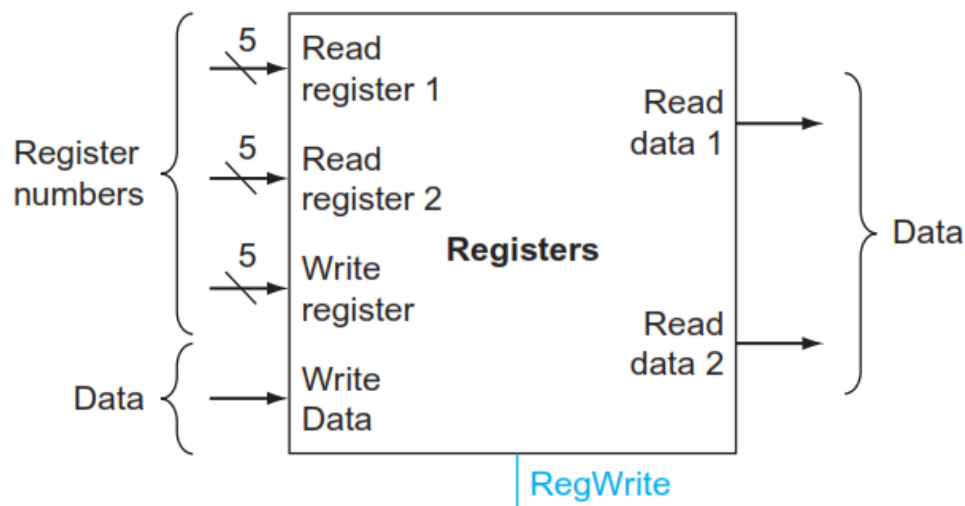
In this lab, you will implement the register file using VHDL. The register file consists of 32 registers.

The input to the register file includes:

- 3 register numbers: 2 numbers for read registers and 1 number for the write register. Each number consists of 5 bits to index 1 of the 32 registers.
- Data to be written consisting of 32 bits.
- RegWrite control line to enable writing to the register file.
- Clock such that data is written in the first half cycle, while the data is read in the second half cycle.

The output of the register file includes:

- 2 data outputs of the 2 read registers specified where each output consists of 32 bits.



Environment

You can install [ModelSim](#) to use it for compilation and simulation. In case there is another tool that you prefer, feel free to use it.

Submission

- You will submit a report including the code and screenshots of the simulation during multiple clock cycles. Also, you should add in the report a link to your code.
- Your work must include testbench code that covers different cases (ex: Set RegWrite to one/zero, write and read in the same register in the same clock cycle).
- You are allowed to work in pairs.