Alexandria University *Faculty of Engineering* *Computer and Systems Engineering Dept.*		*Computer Architecture* *Spring 2024* *Assigned: 17 April 2024* *Due: 23 April 2024*

Reorder Buffer

Overview

In this assignment, you will use a Reorder Buffer simulator to come up with different instruction sets that cause different behaviours. The purpose of the lab is to make you more aware of the pros and cons of the reorder buffers. You are provided with a working version of the simulator, and your job is to simulate exactly 2 scenarios. One where the reorder buffer is better than the non-reorder buffer architectures and another where it introduces a problem.

Background

In this assignment, you'll use the simulator provided by the link below:

ROB Simulator

The simulator runs a sequence of instructions on the reorder buffer architecture and shows the following values at each step:

- **Reorder Buffer**
- **Reservation Stations**
- **FP Register Status**
- **Load Buffers**

Requirements

It is required to come up with two different instruction sets (**of no less than 5 instructions each**):

1) One that shows the strengths of the reorder buffer technique. That is, show how it could enable multiple, simultaneous execution of different instructions on different functional units.
2) One where the reorder buffer does not help. For example, where the instructions go to the same functional unit.

Required

- You are required to show the values of **Reorder Buffer**, **Reservation Stations, FP Register Status, and Load Buffers** after each change in the hardware (cycles where the nothing changes in the register are not required)

- Mention the number of cycles taken to execute the instruction set using Reorder Buffer by simulation.

Submission Instructions

- You are allowed to work in pairs.
- Please submit a report including the results for the simulation as described above with your name(s) as well as your student ID(s).
- No late submission will be accepted unless there is a valid documented excuse.