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SSE

TP1 : Modélisation << Concurrent >>

Affectations simultanées de signaux << concurent Signal Assignements >> avec des opérateurs logiques :

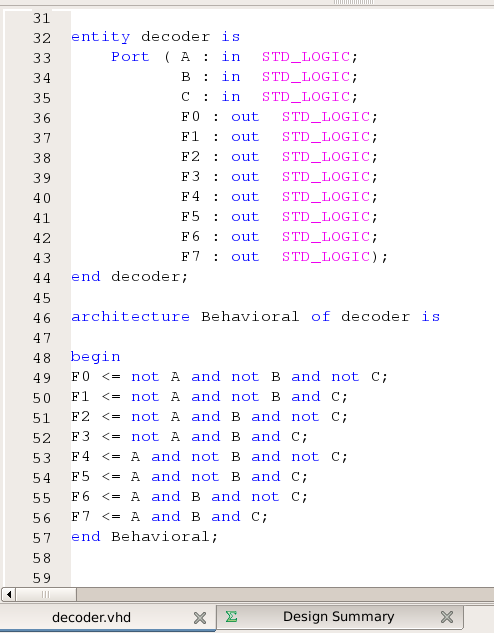
Exercice 1 : Décodeur 3-to-8 :

1. Les équations de sortie F0-F7 :

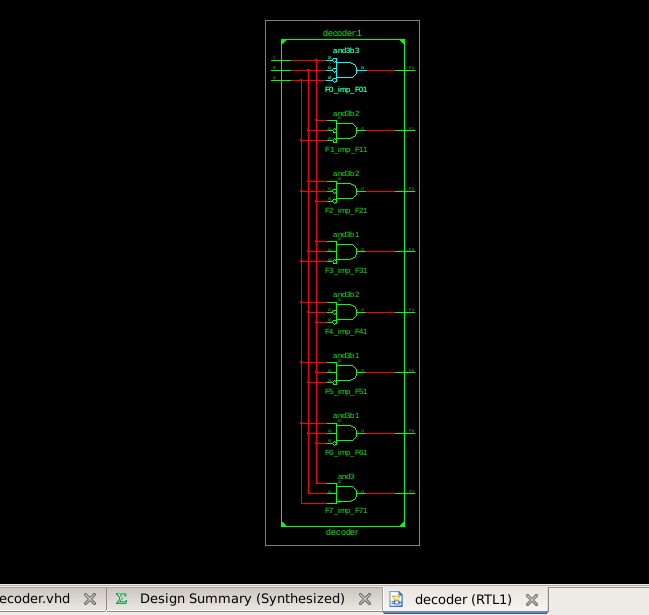
F0 = not A & not B & not C; F1 = not A & not B & C; F2 = not A & B & not C; F3 = not A & B & C;

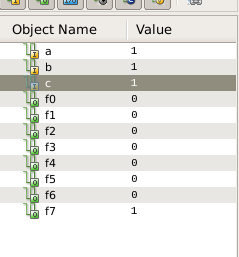
F4 = A & not B & not C; F5 = A & not B & C; F6 = A & B & not C; F7 = A & B & C;

1. Modélisation VHDL du Décodeur 3-to-8 à l’aide des opérateurs logiques :



1. Vérification des résultats à l’aide de Isim :





Exercice 2 : Décodeur d’affichage à 7 segments :

1. Les équations Fa…Fb :

Fa = not A and not B and not C or not A and B and not C or not A and B and C or A and not B and C or A and B and not C or A and B and C;

Fb = not A and not B and not C or not A and B and not C or not A and B and C or A and B and not C or A and not B and not C or A and B and C;

Fc = not A and not B and not C or not A and not B and C or not A and B and C or A and not B and not C or A and not B and C or A and B and not C or A and B and C;

Fd = not A and not B and not C or not A and B and not C or not A and B and C or A and not B and C or A and B and not C;

Fe = not A and not B and not C or not A and B and not C or A and B and not C;

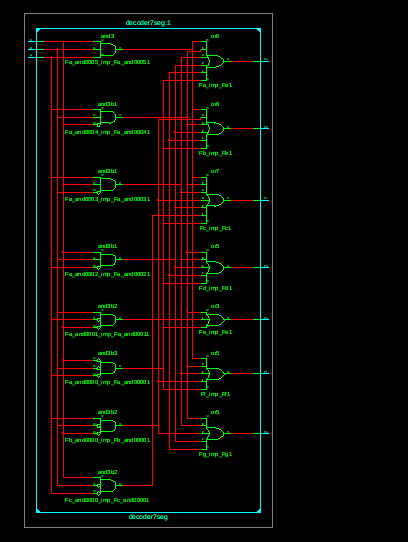
Ff = not A and not B and not C or A and not B and not C or A and not B and C or A and B and not C or A and B and C;

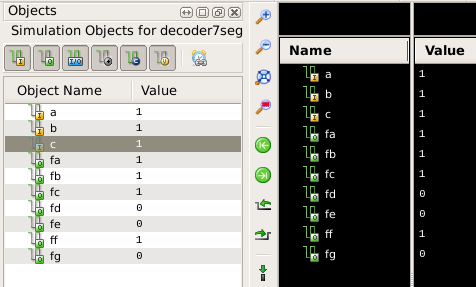
Fg = not A and B and not C or not A and B and C or A and not B and not C or A and not B and C or A and B and not C;

1. Modélisation VHDL du decoder 7 segments à l’aide des opérateurs logiques :



1. Vérification des résultats à l’aide de Isim :





Affectations conditionnelles de signaux :

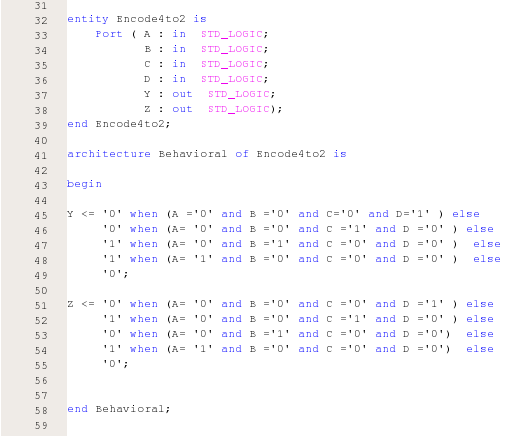
Exercice 1 :

1. Les équations de sorties Y et Z :

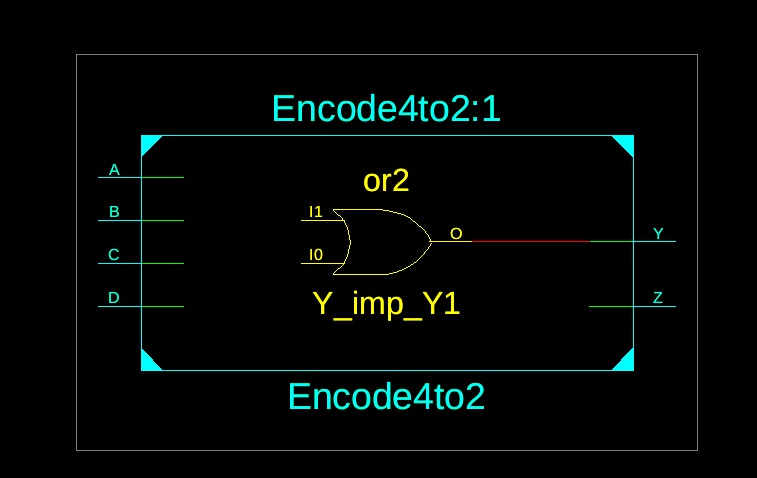
Y = not A and B and not C and not D or A and not B and not C and not D;

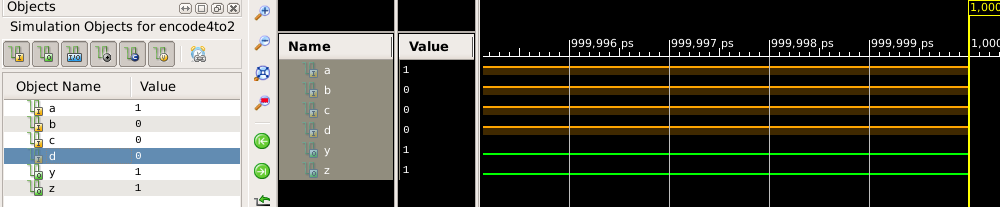
Z = not A and not B and C and not D or A and not B and not C and not D;

1. Modélisation VHDL de l’encodeur 4-to-2 :



1. Vérification des résultats :





Affectations sélectionnées de signaux :

Exercice1 :

1. L’équation de F :

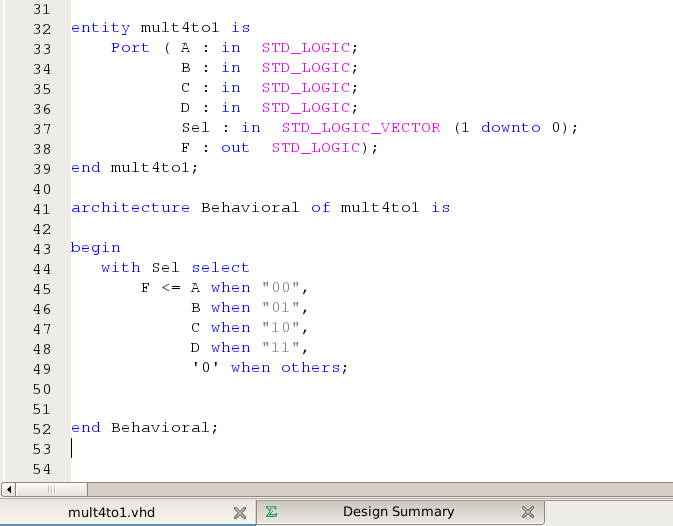
F = not sel1 and not sel0 and A

Or not sel1 and sel0 and B

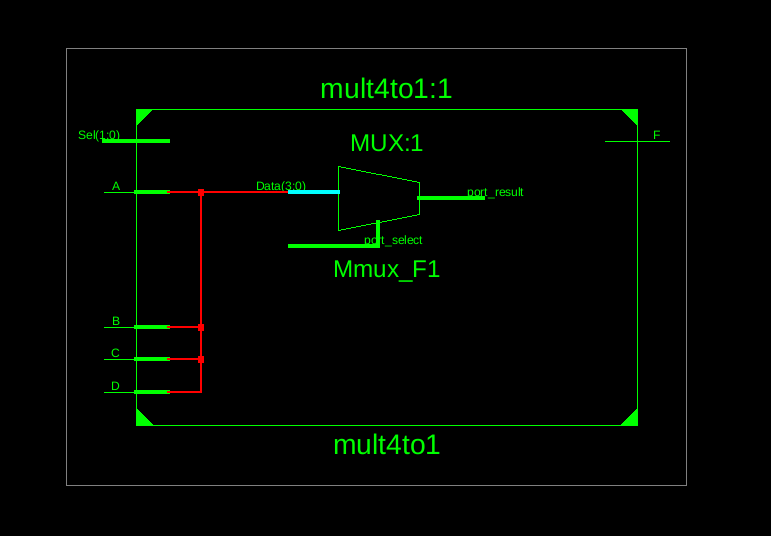
Or sel1 and not sel0 and C

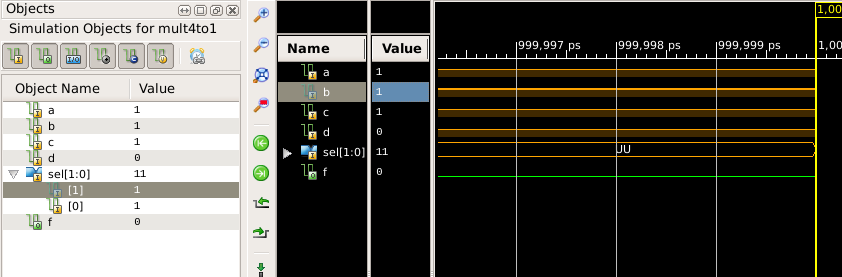
Or sel1 and sel0 and D;

1. Modélisation VHDL:



1. Vérification des résultats:





Exercice 2:

1. Les équations de sortie de F :

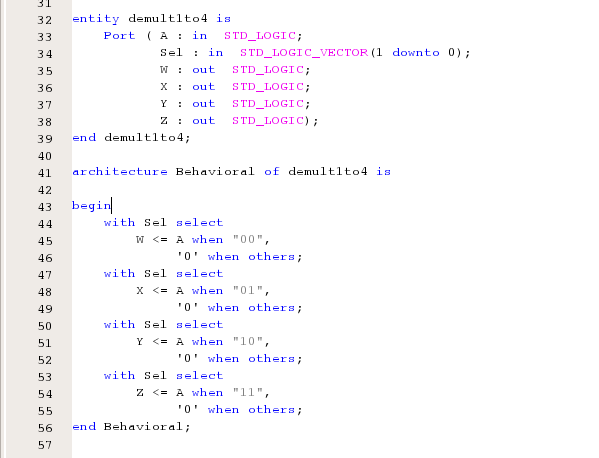
W = not sel1 and not sel0 and A;

X = not sel1 and sel0 and A;

Y = sel1 and not sel0 and A;

Z = sel1 and sel0 and A;

1. Modélisation VHDL :



1. Vérification des résultats :

