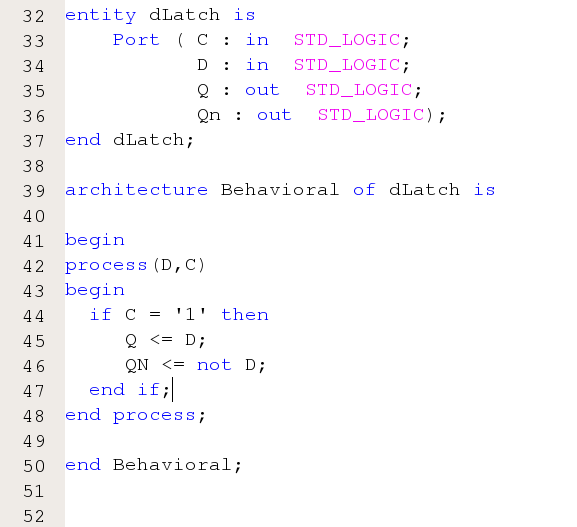
Mohamed Manessouri  
SSE

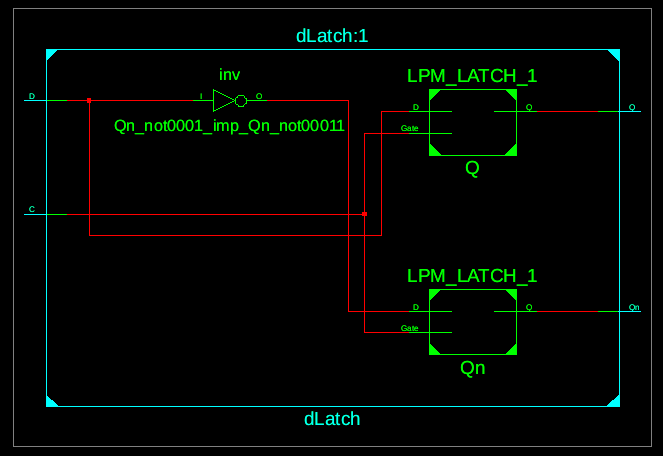
**Tp5 : Modélisation Séquentielle**

**Stockage et registre**

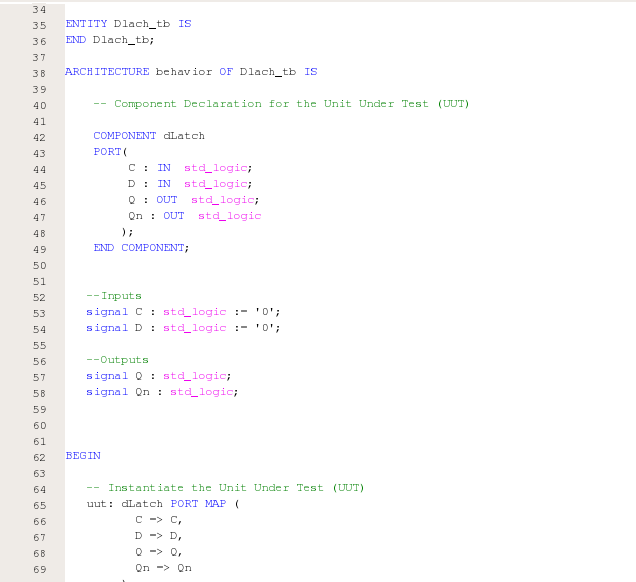
**Exercice 1 :**

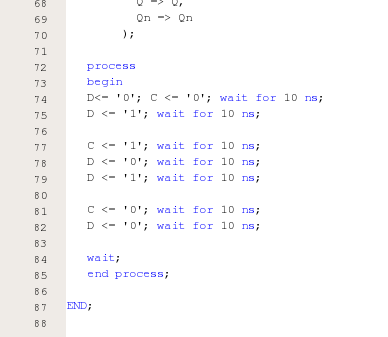
1. Modèle VHDL modélisant les types de bascule D et test bench :

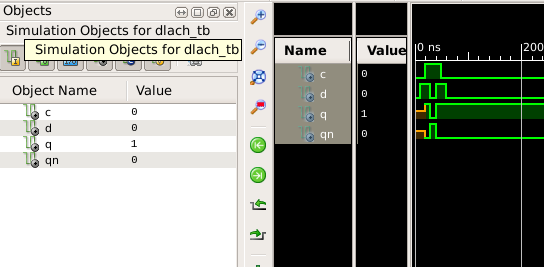
D\_Latch ****



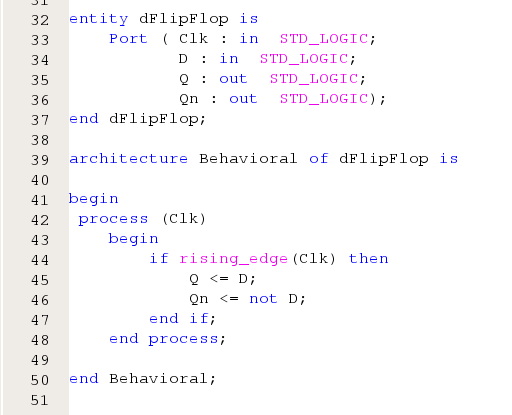
Test bench pour D\_lach:



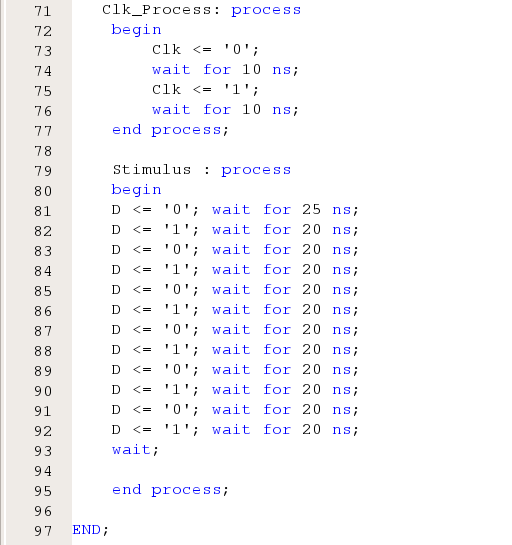


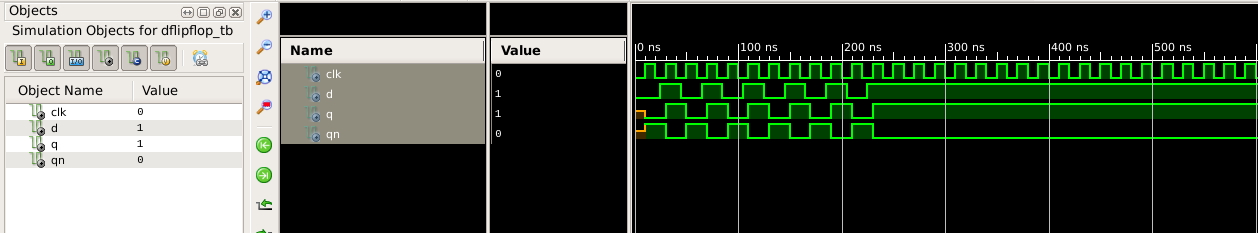


D\_Flip\_Flop

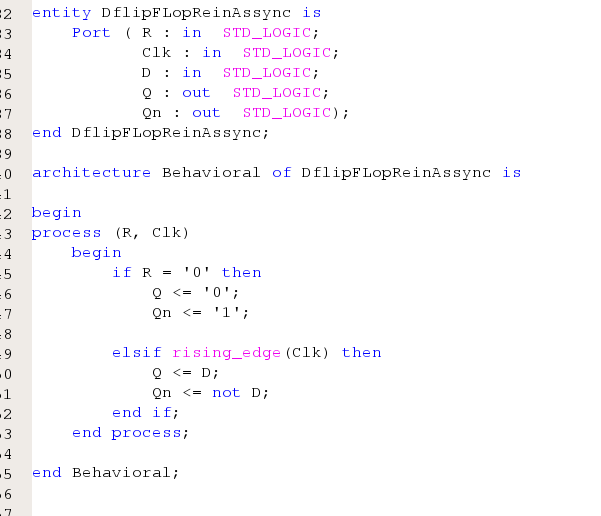


Testbench pour D\_Flip\_Flop:

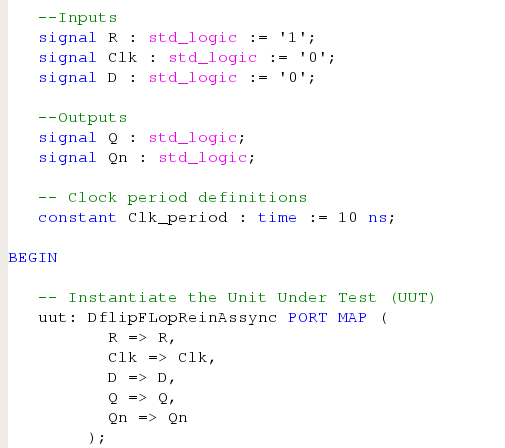
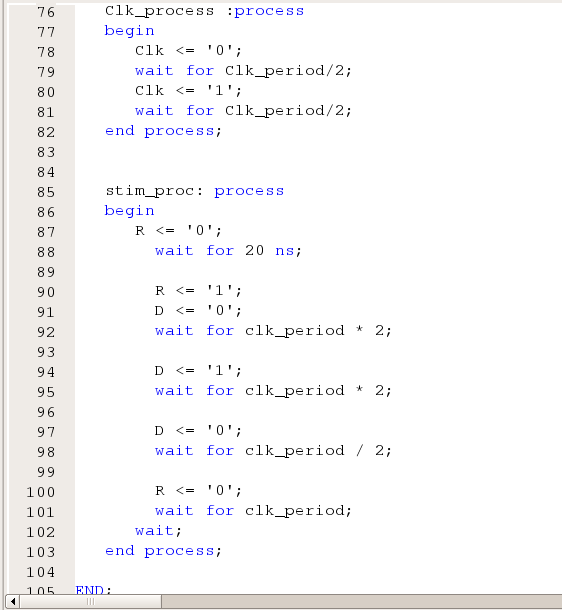


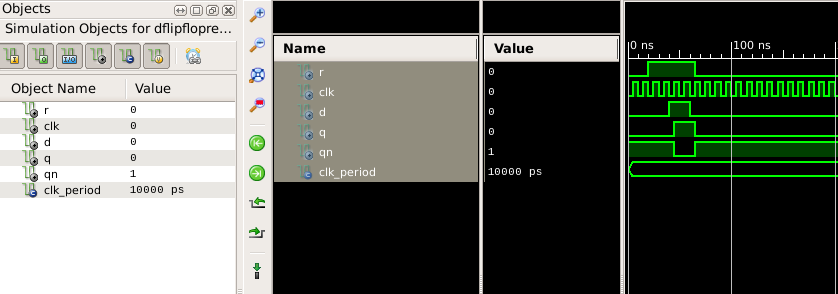


D\_Flip\_Flop avec réinitialisations asynchrones

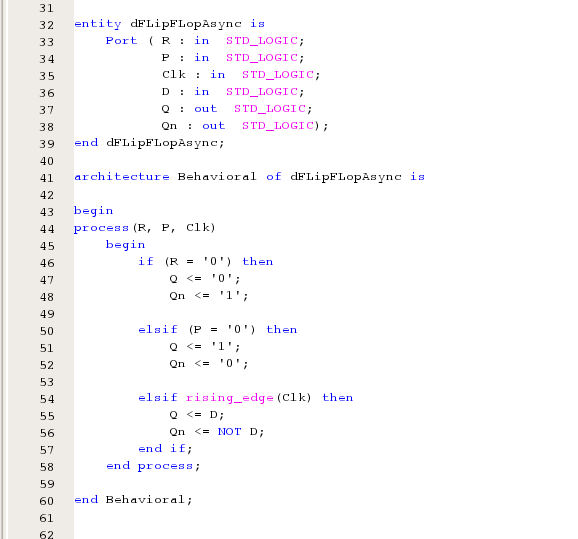


Test Bench pour D\_Flip\_Flop avec réinitialisations asynchrones

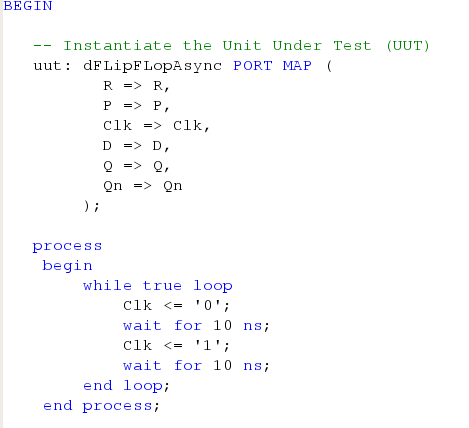
 

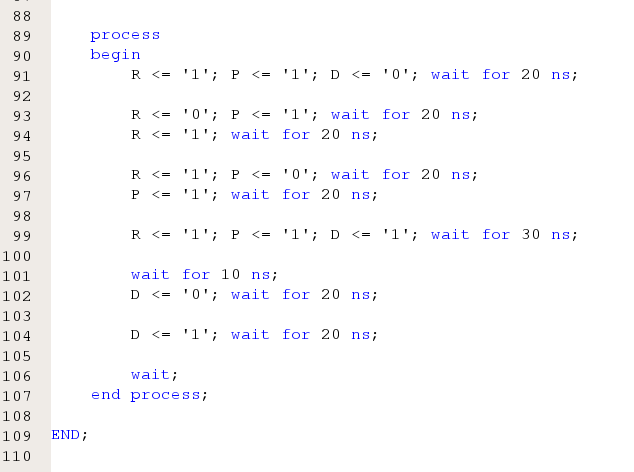


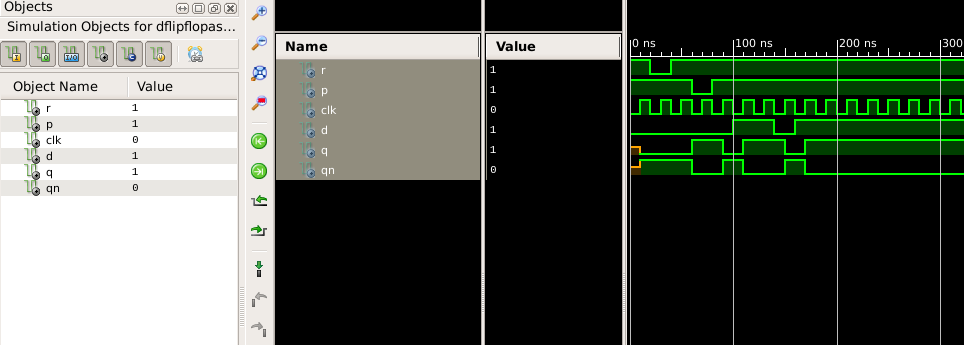
D\_Flip\_Flop avec Asynchrones Reset and Preset



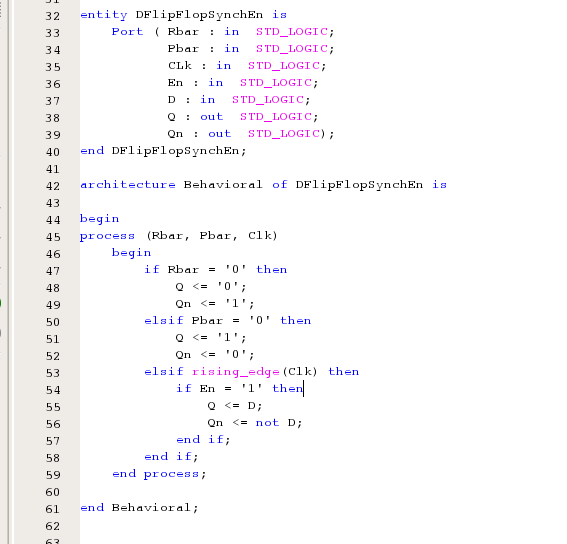
Test bench pour D\_Flip\_Flop avec Asynchrones Reset and Preset



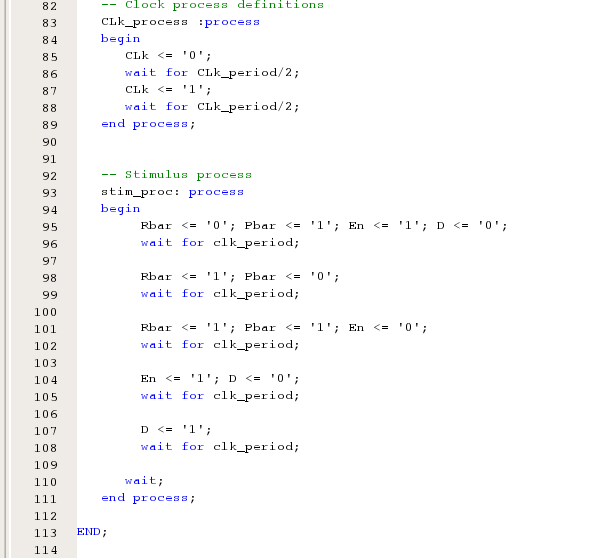


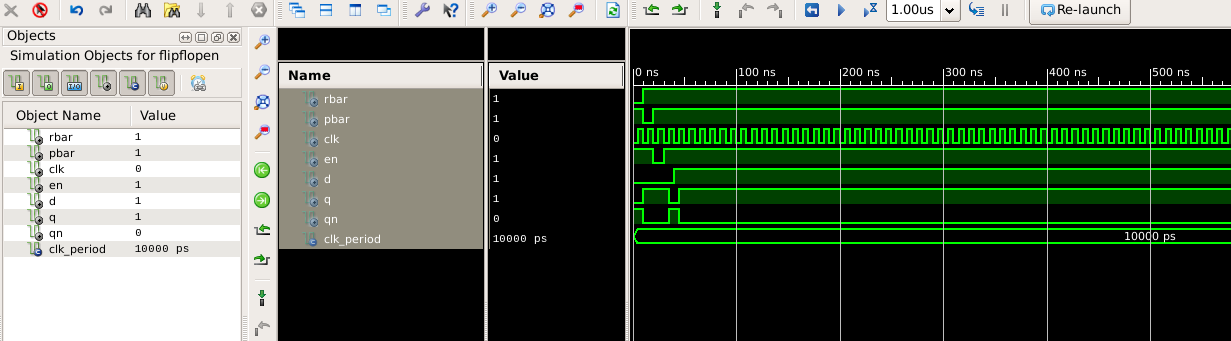


D\_Flip\_Flop avec Synchrone Enable



Testbench pour D\_Flip\_Flop avec Synchrone Enable

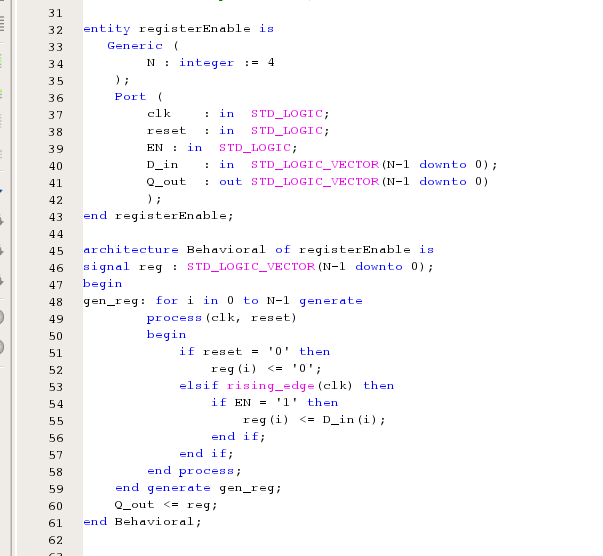




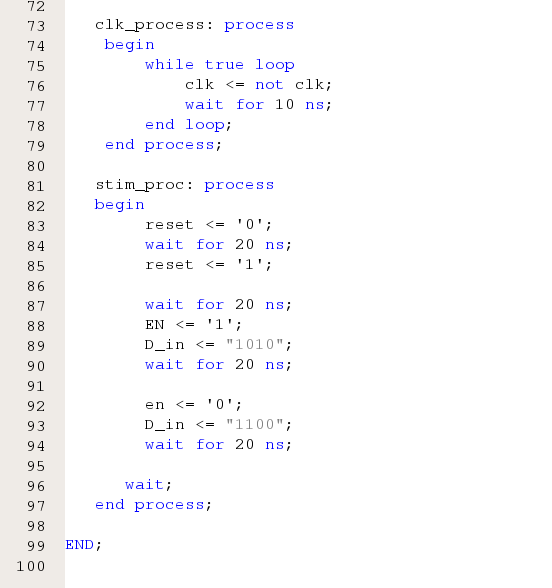
**Exercice 2:**

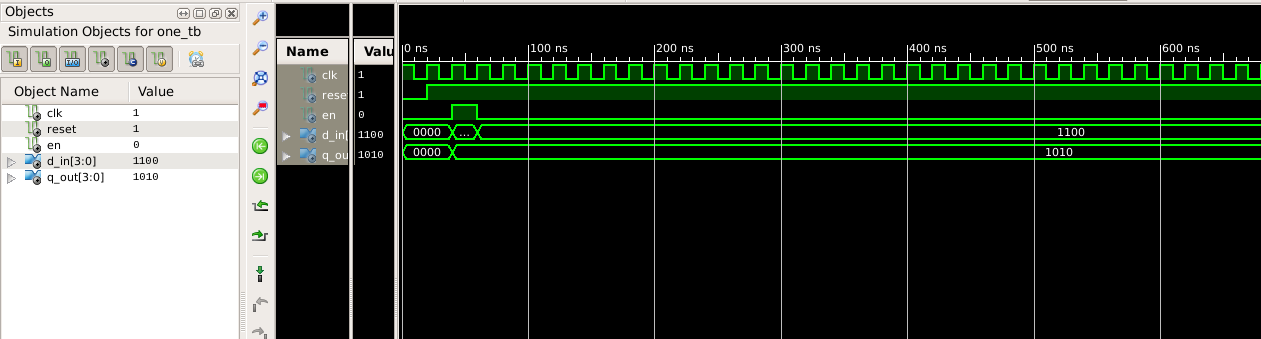
1. Register avec Enables 4 bits

Modèle VHDL avec generate

****

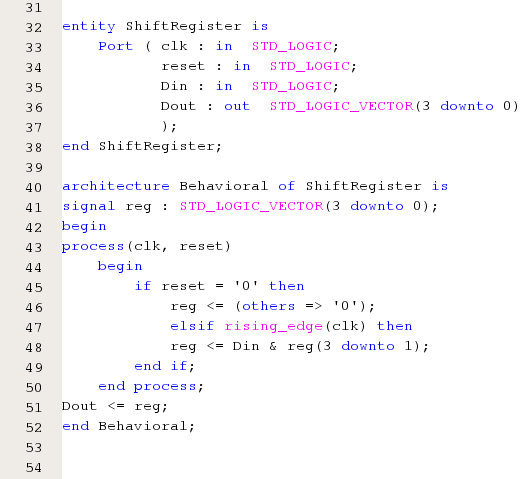
Test bench:

****

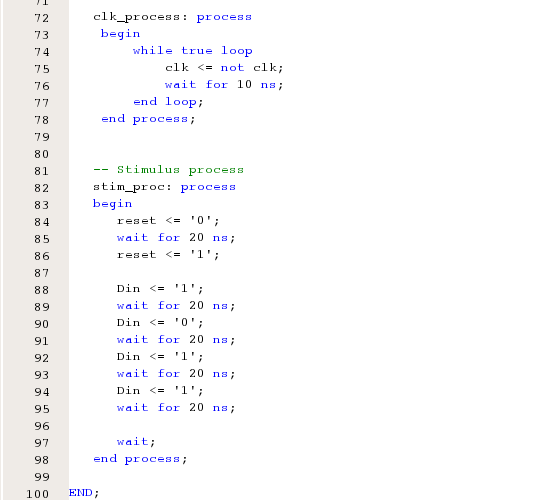
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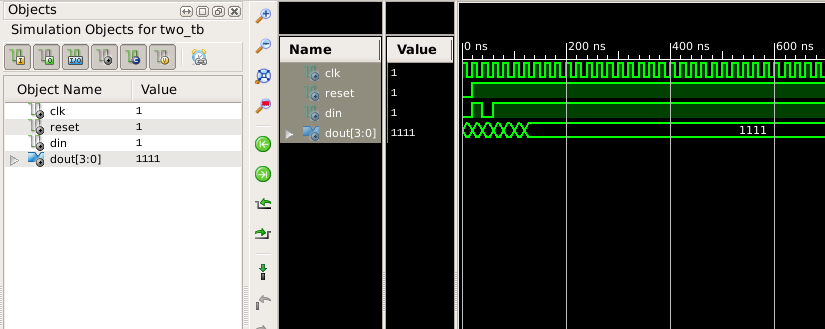
1. Shift Registers:

Modèle VHDL:



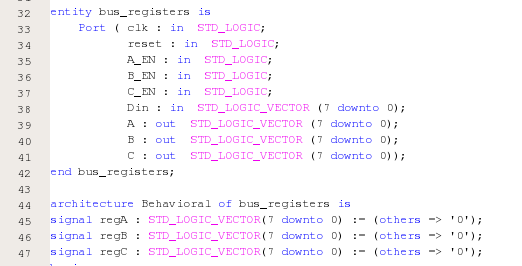
Test Bench:

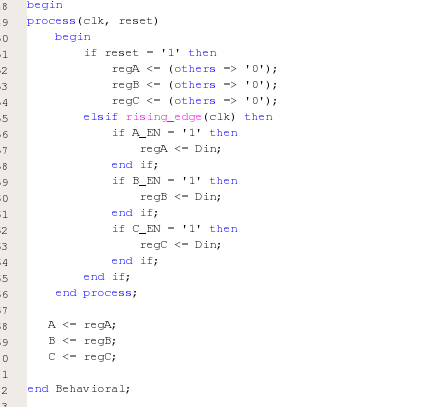




1. Registres sur un Bus de données

Modèle VHDL :





Test Bench :

