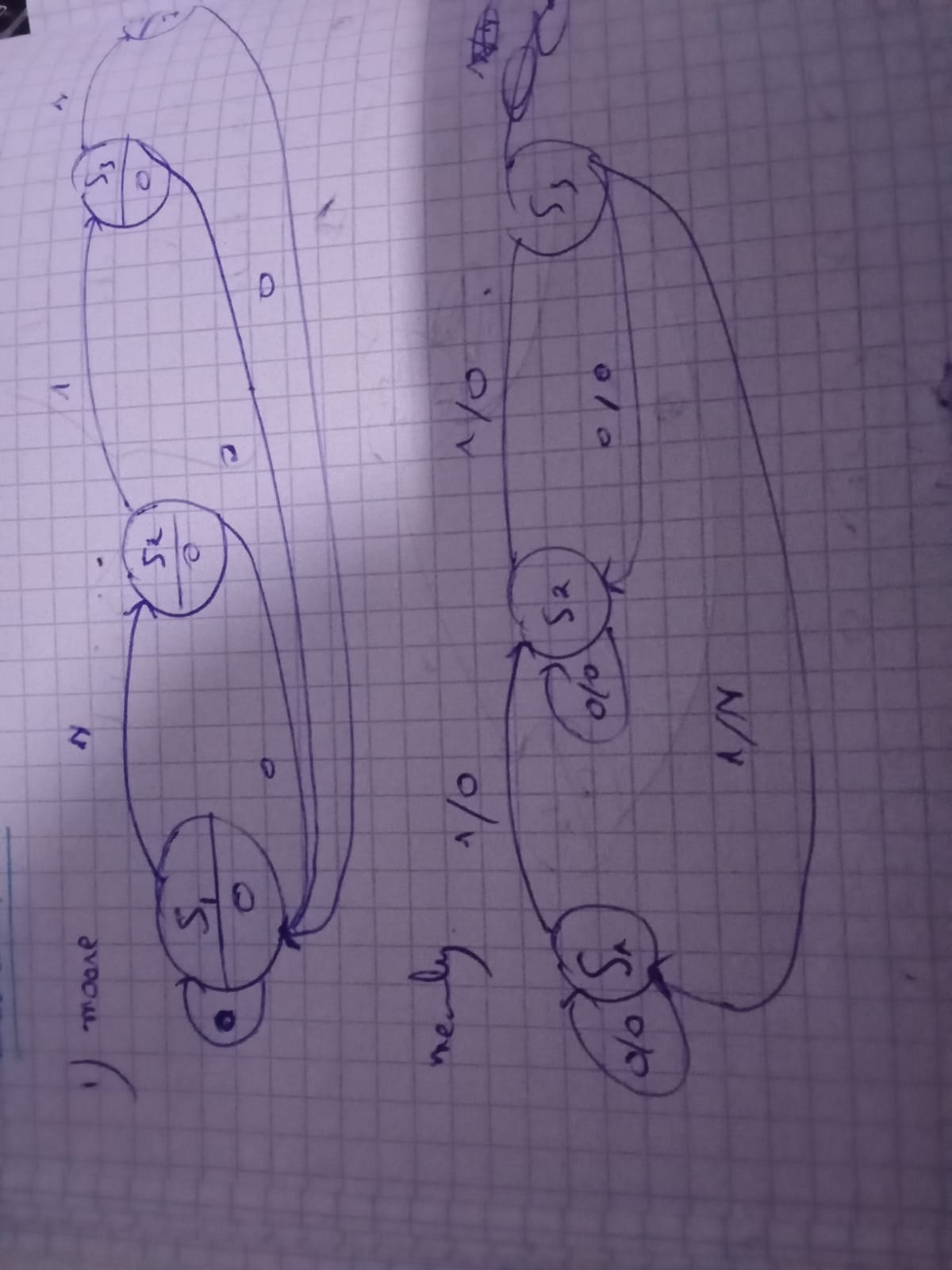
Mohamed Manessouri  
SSE  
  
 **Tp6 : Modélisation de machines à états finis**

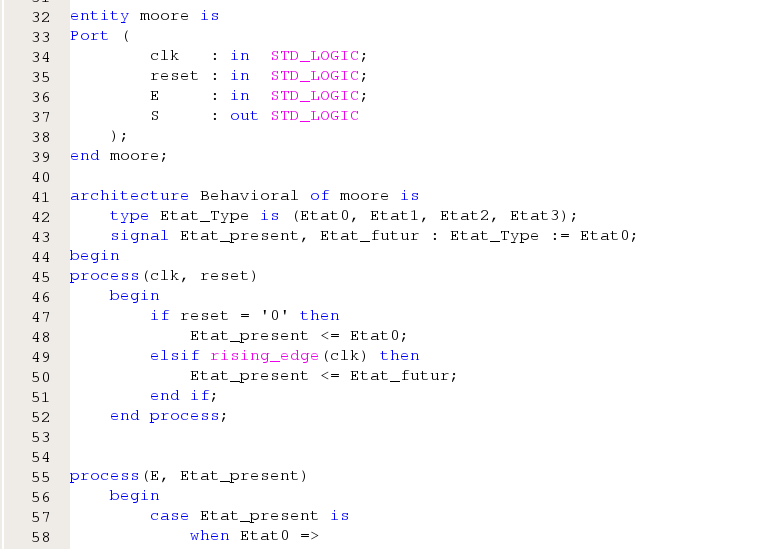
**Exercice 1 :**

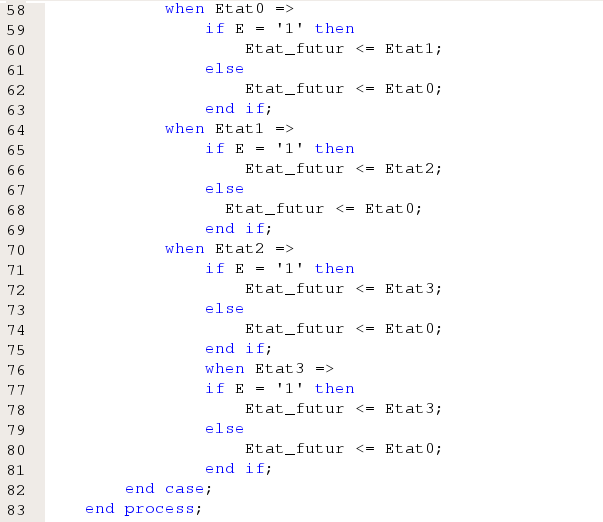


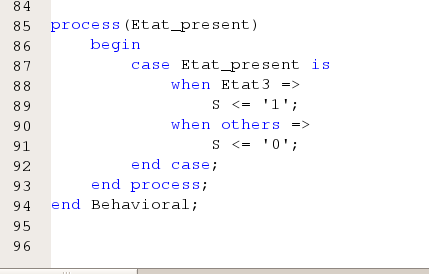
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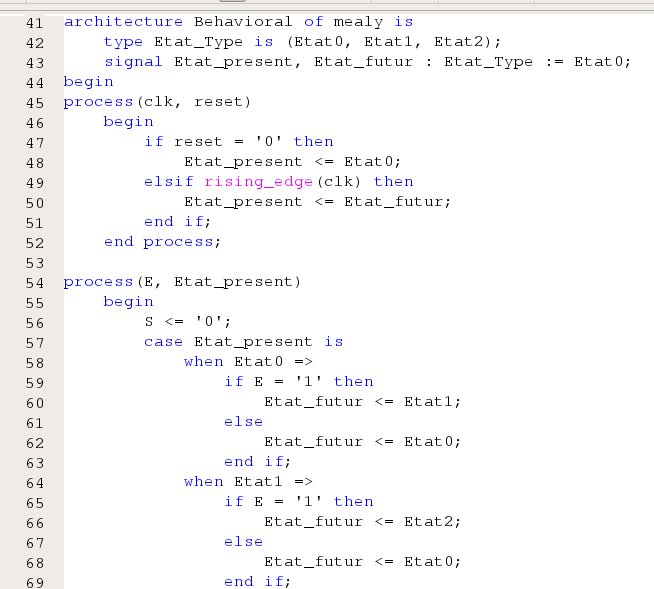
**Moore.vhdl**

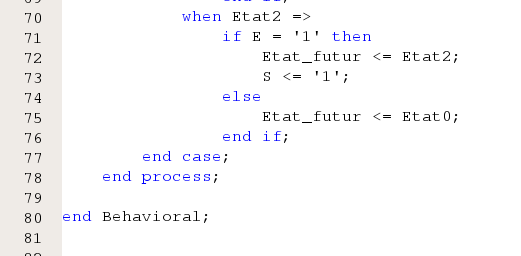
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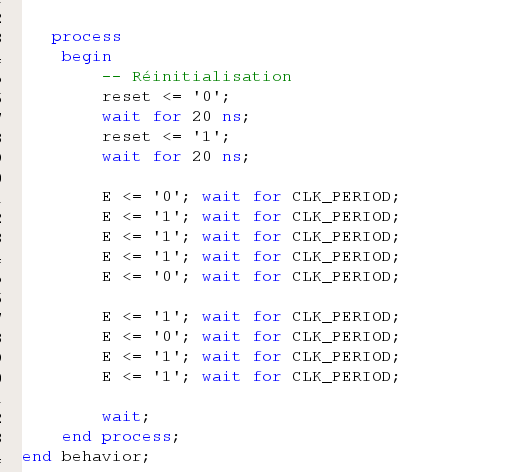
**Mealy.vhdl**

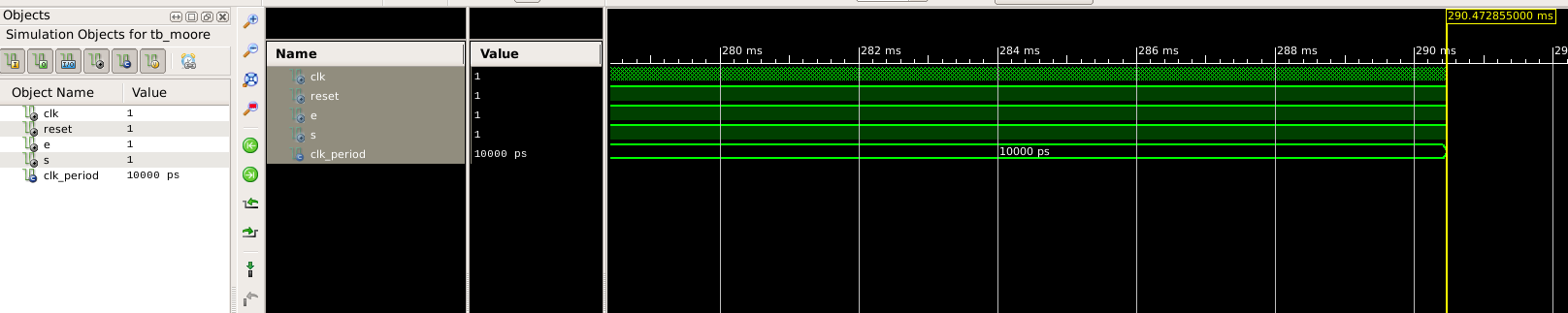
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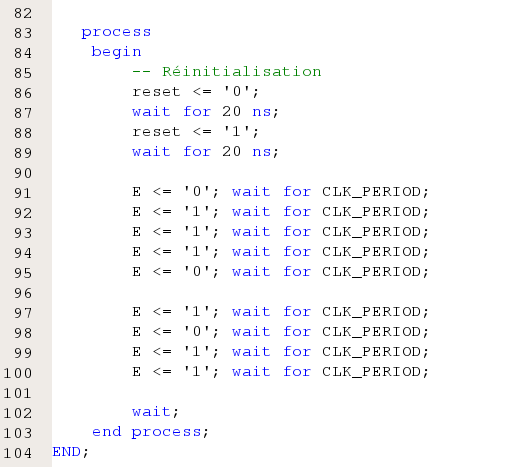
1. **Test Bench :**

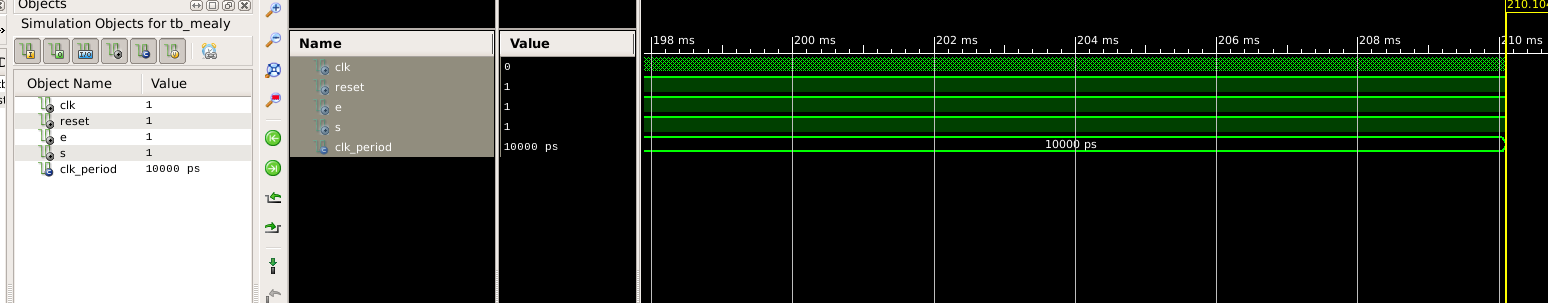
**Tb\_moore.vhdl**

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**Tb\_mealy.vhdl**

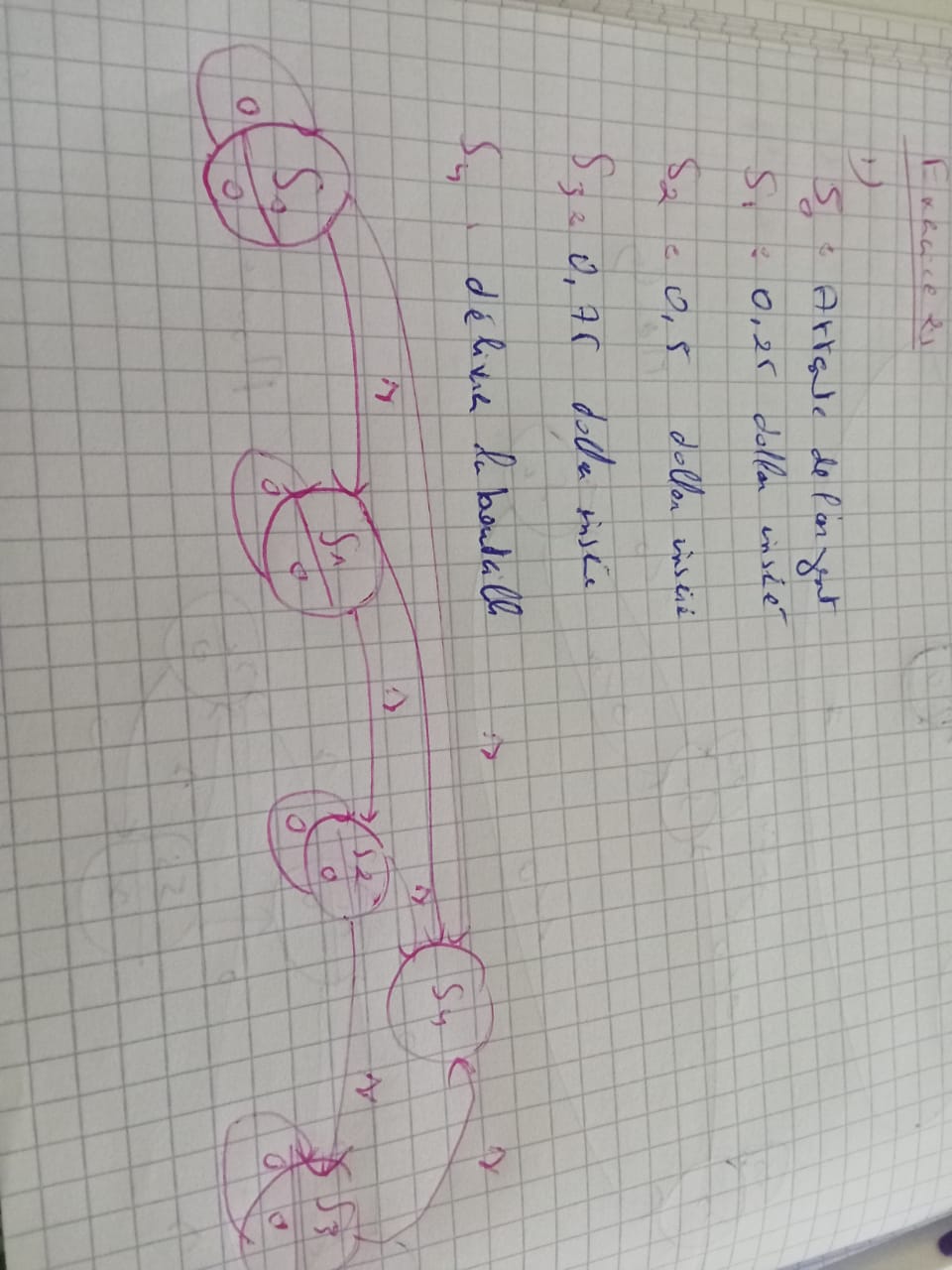
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1. Les sorties d'une machine de **Mealy** dépendent des entrées et changent immédiatement (asynchrone), tandis que celles d'une machine de **Moore** dépendent uniquement de l'état présent et changent sur un front d'horloge (synchrone).

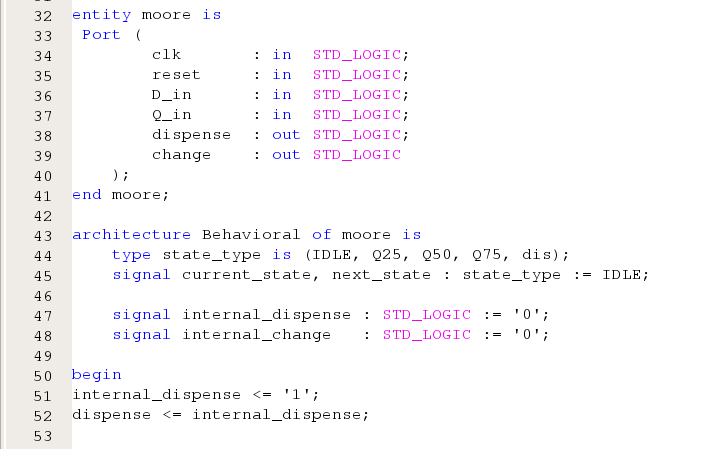
**Exercice 2 :**

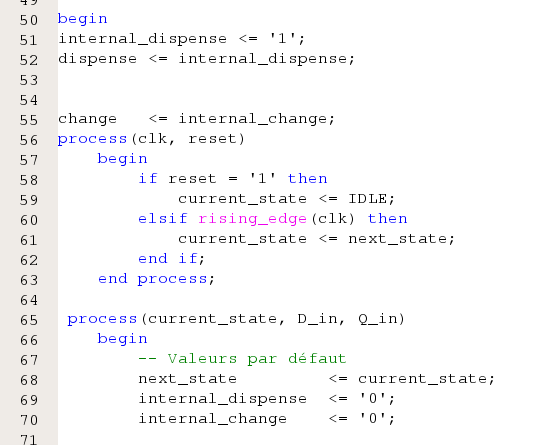


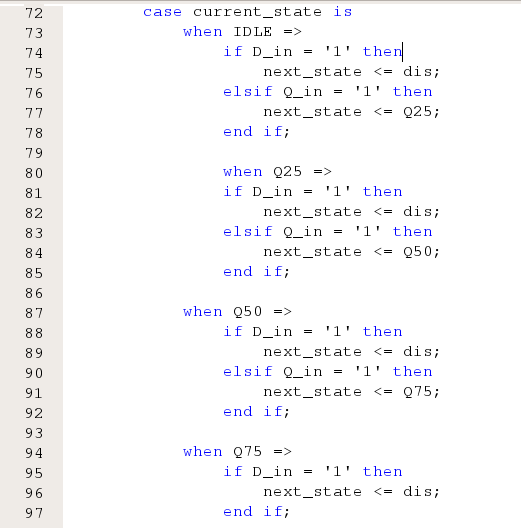
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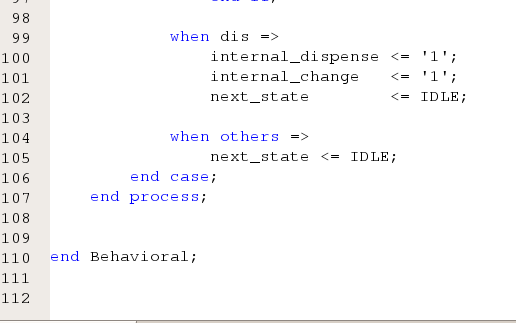


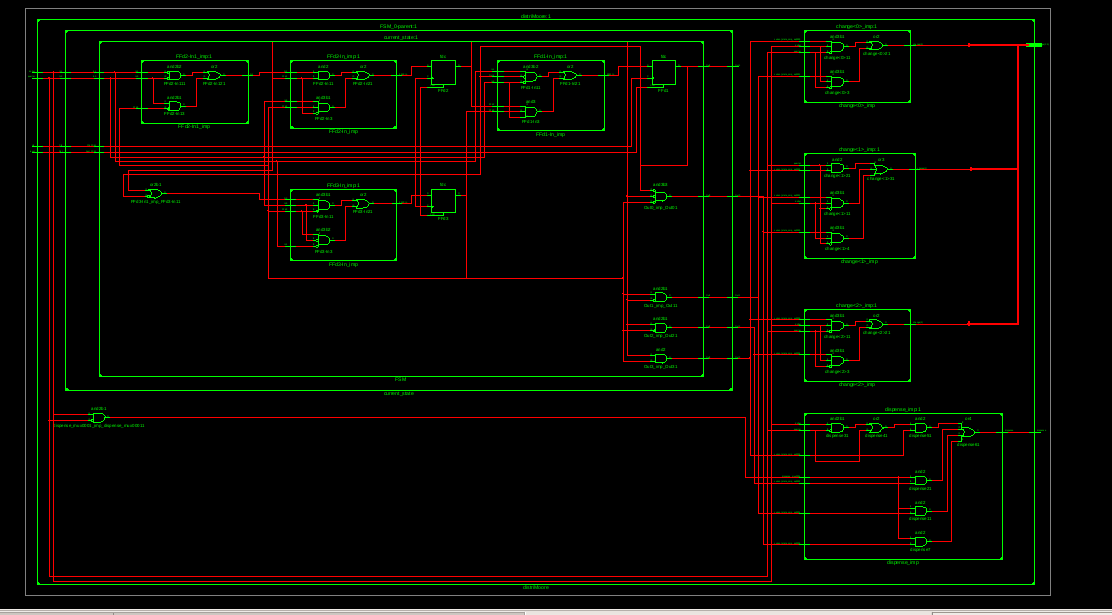
**Moore.vhdl**

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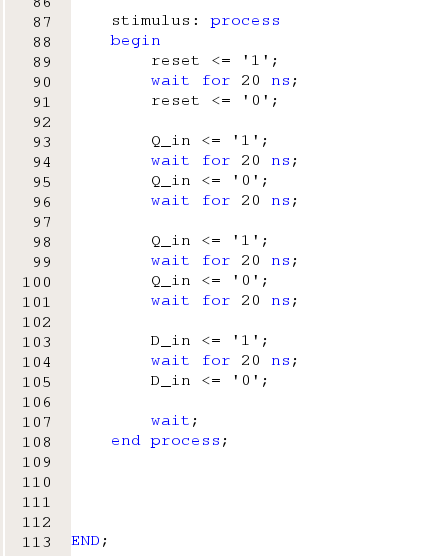
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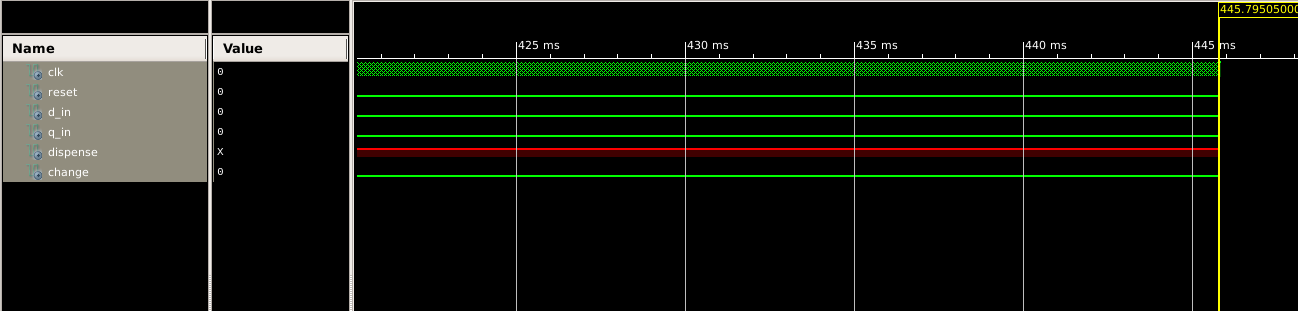
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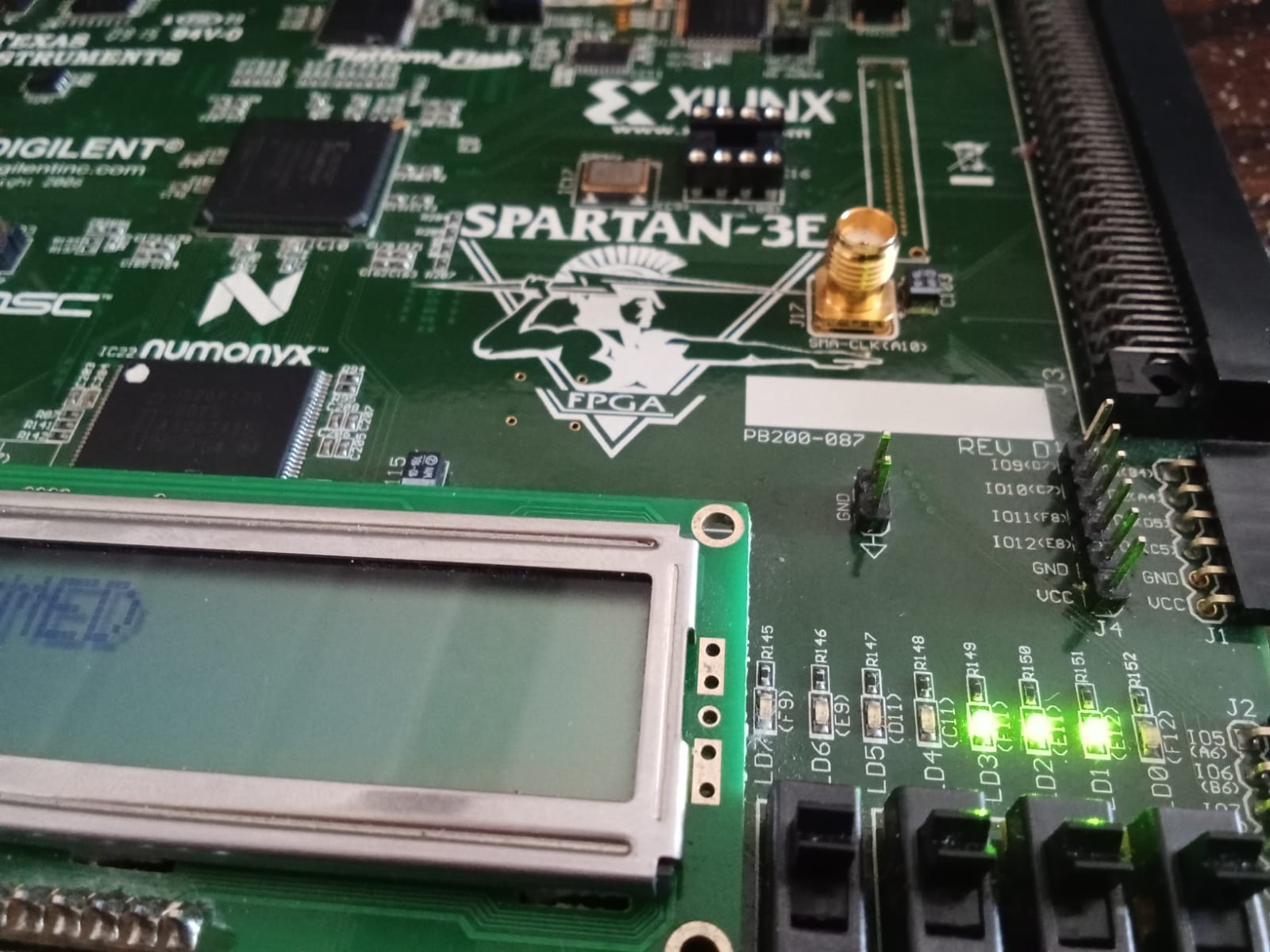
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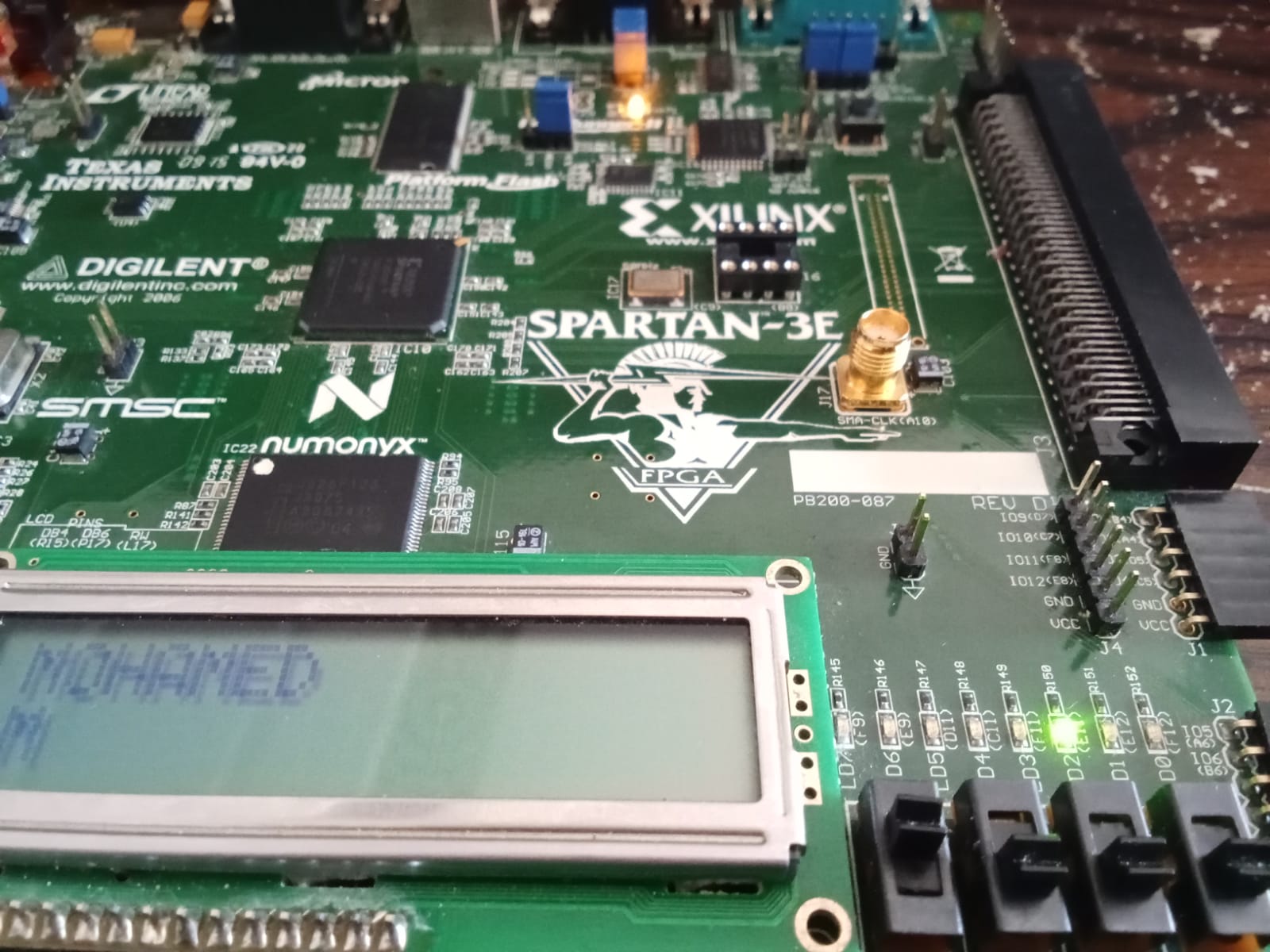
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1. **Test Bench :**

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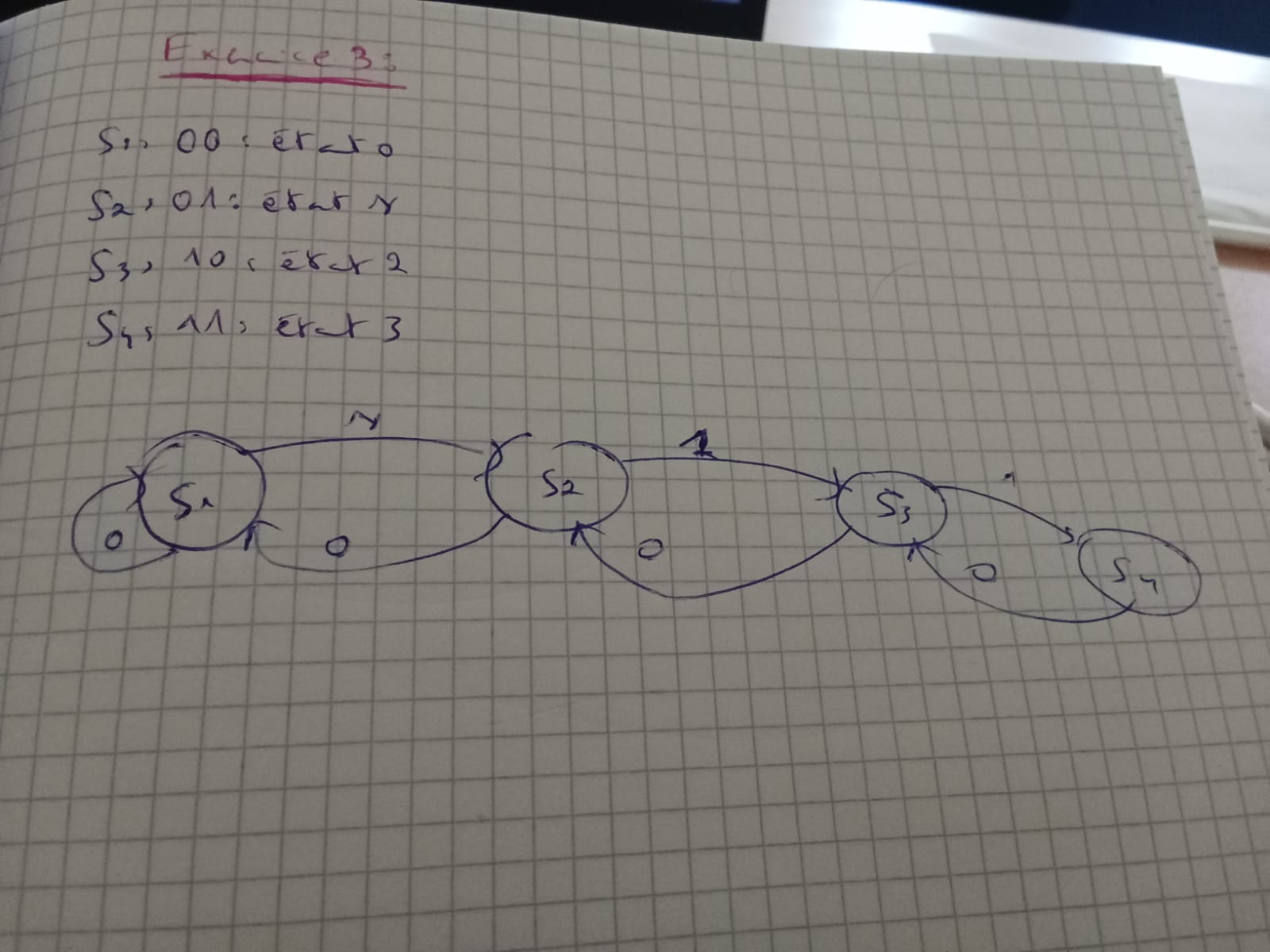
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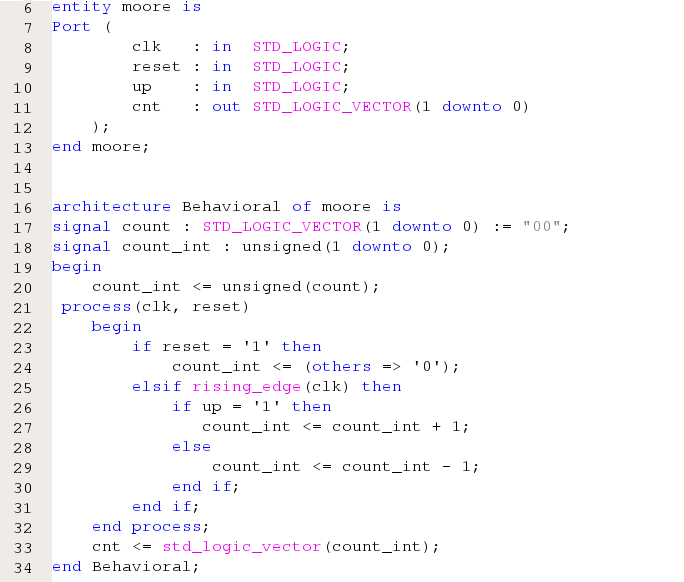
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**Exercice 3 :**

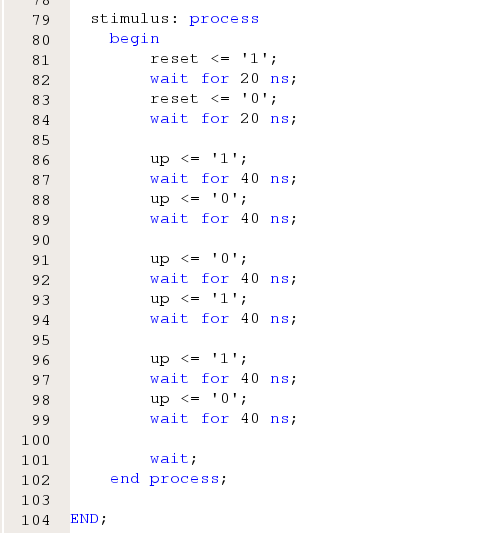


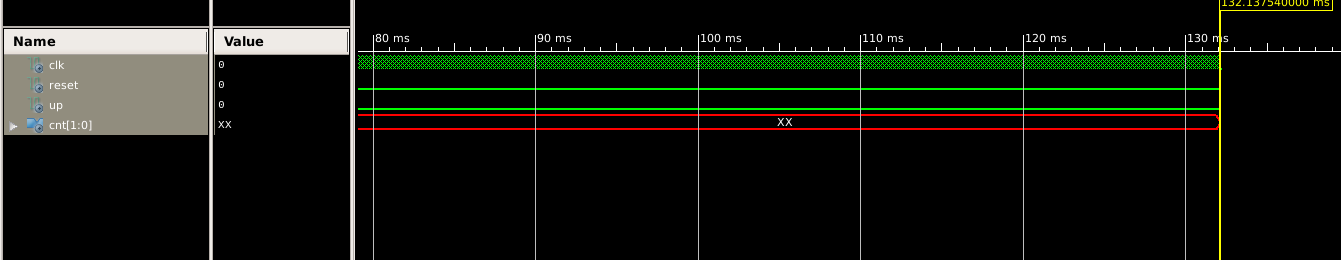
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1. **Test Bench :**

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