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AMBA

AHB_lite

Protocol:

AMBA AHB-Lite addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation.

AHB-Lite implements the features required for high-performance, high clock frequency systems including:

• burst transfers

• single-clock edge operation

• non-tristate implementation

• wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

Figure 1-1 shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master

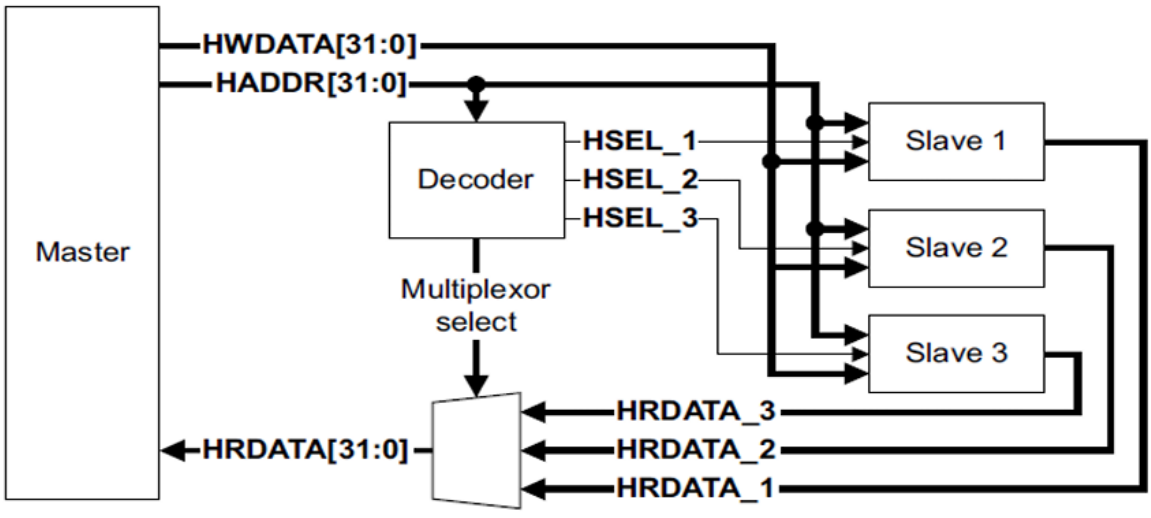
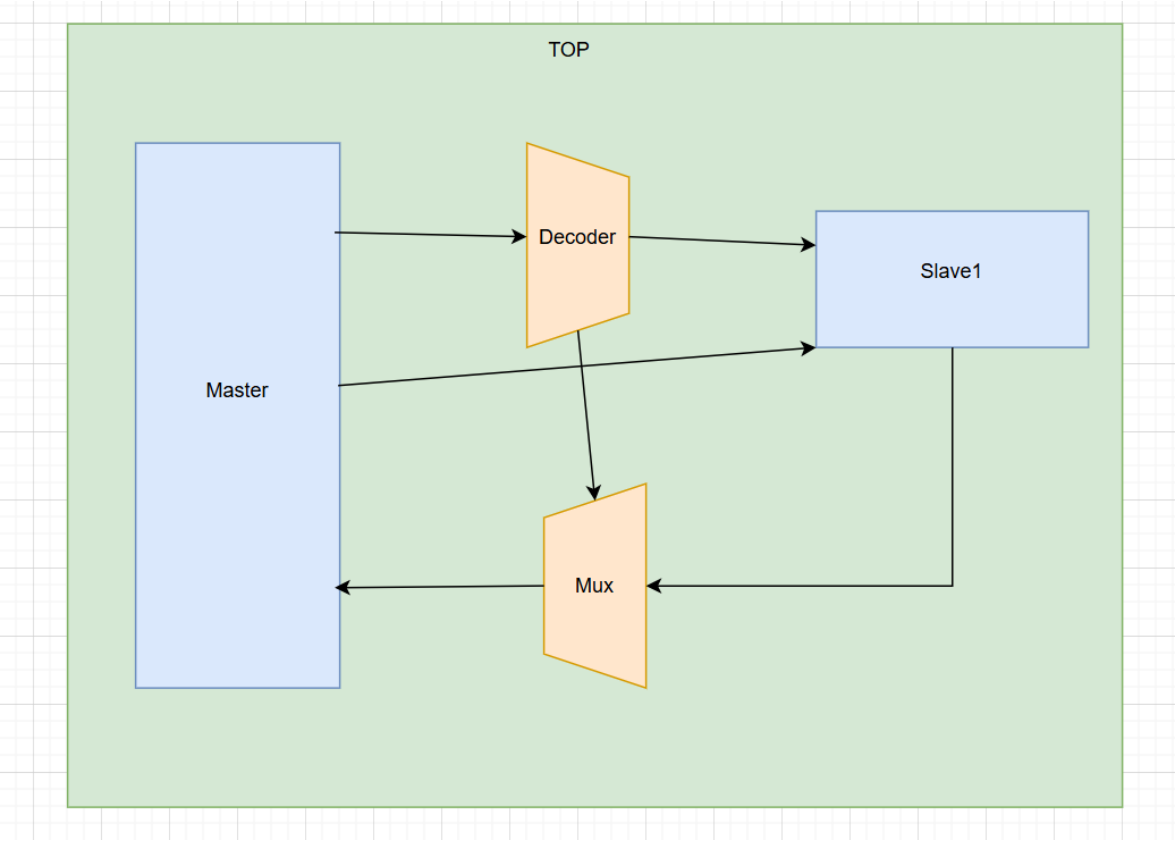


Figure 1-1 AHB-Lite block diagram

The implemented design using draw.io



I made only one slave we can add more later and chosed the slave to be memory.

Master

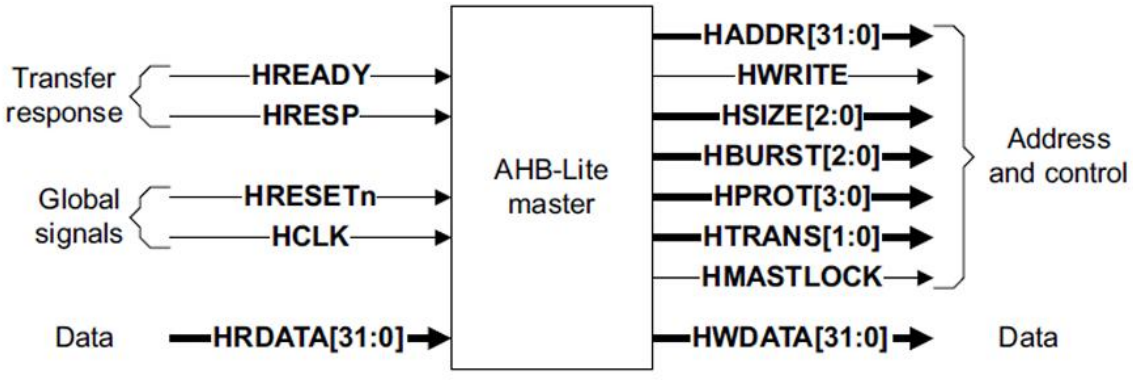
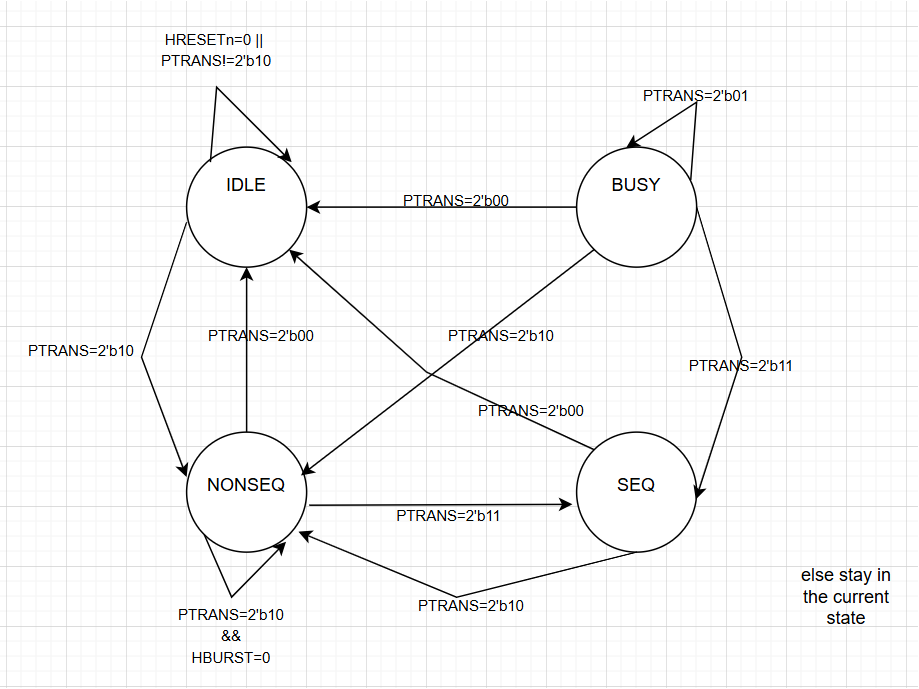


Figure 1-2 Master interface

The FSM of master



Slave

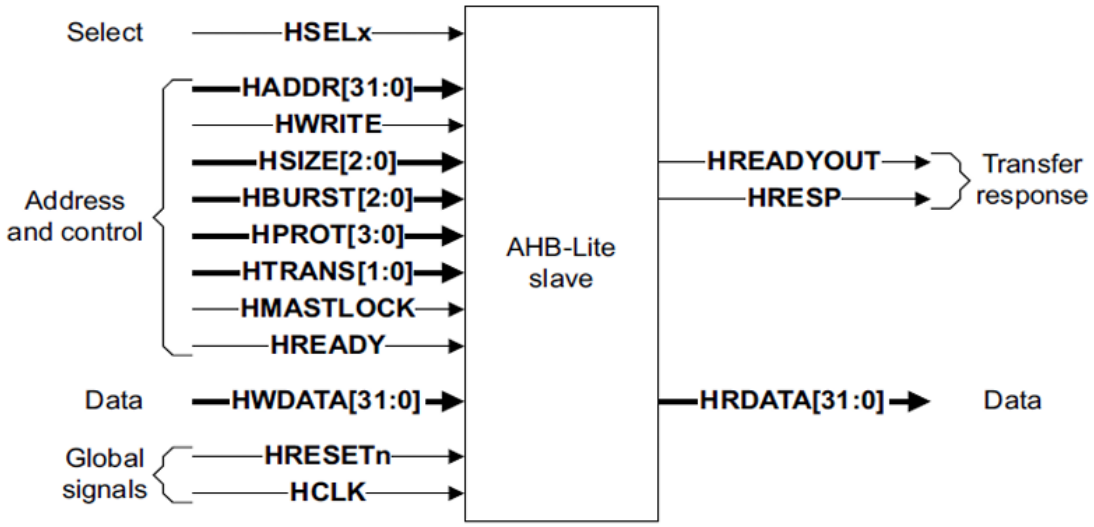


Figure 1-3 Slave interface

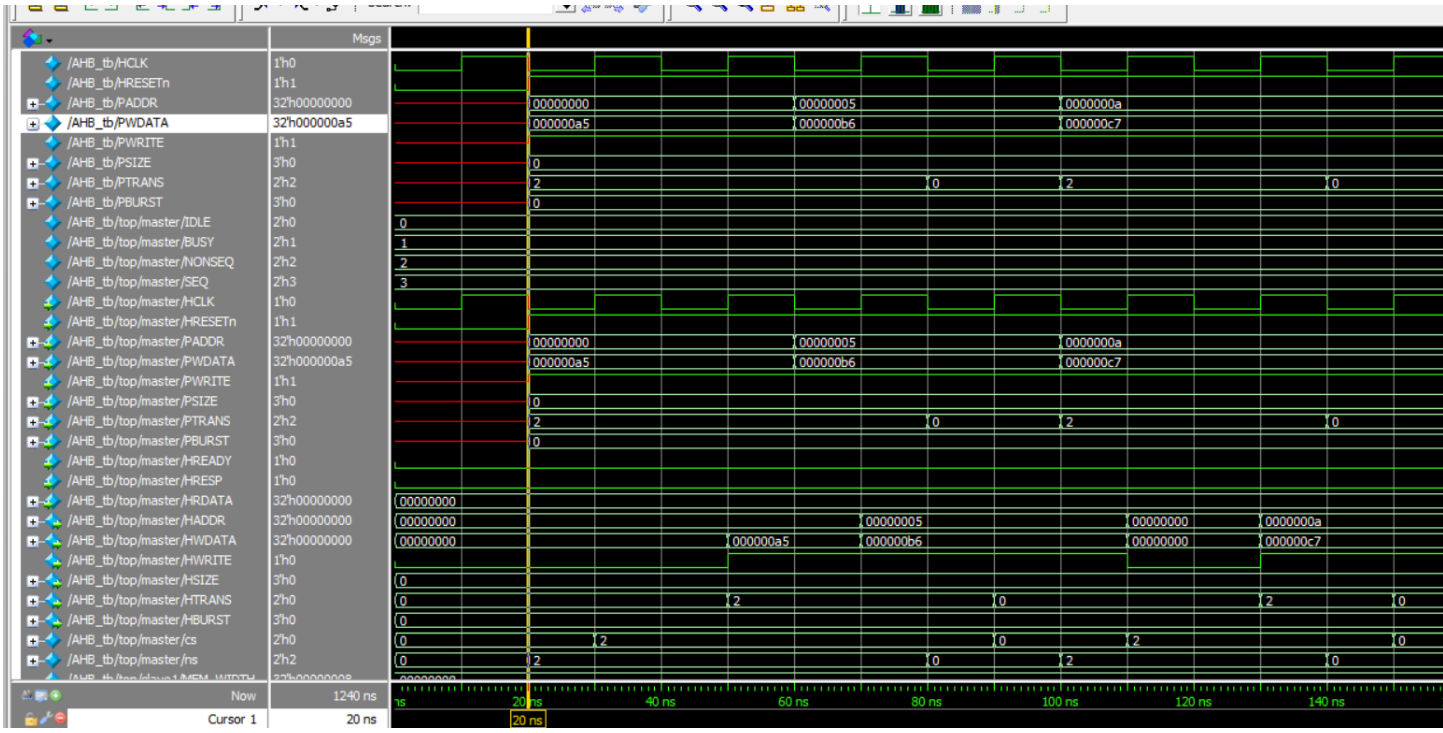
We only covered the **HBURST** signal to be single or incr.

And the **HSIZE** to be only byte or halfword or word. if more than word we should take it 2 times ex if 64 bit is inserted we can take it into 2 32-bit word.

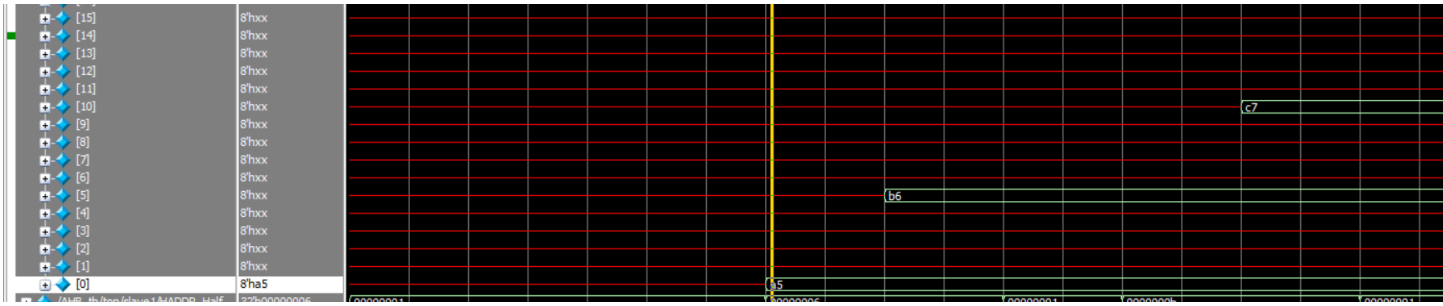
We did not cover the **HPROT** or **HMASTLOCK** signals.

simulated result in QUESTASIM

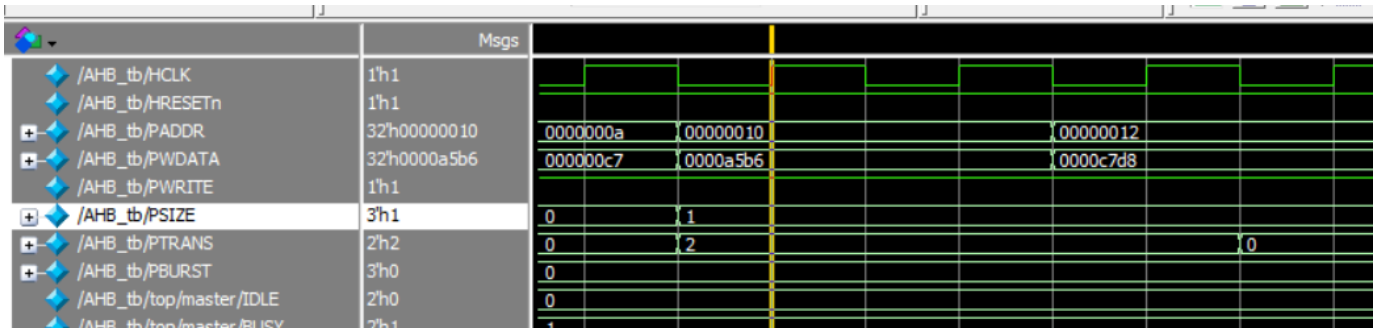
first we need to write a one byte using single HBURST in several locations



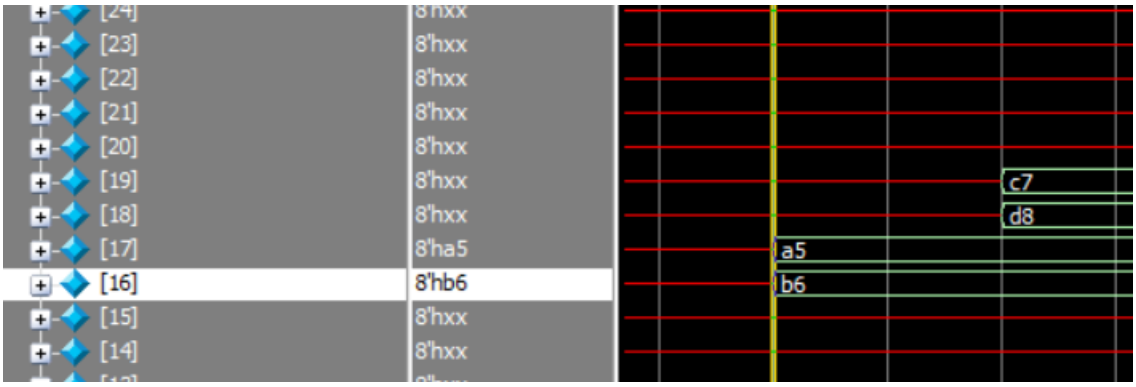
Here is the memory we wrote a5,b6,c7



Now we will write 16-bit in several address so the psize will be 1 now

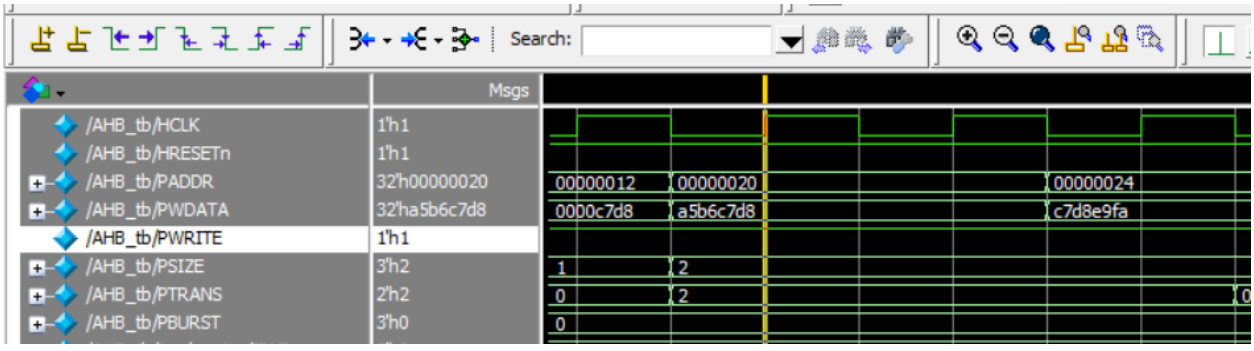


the memory

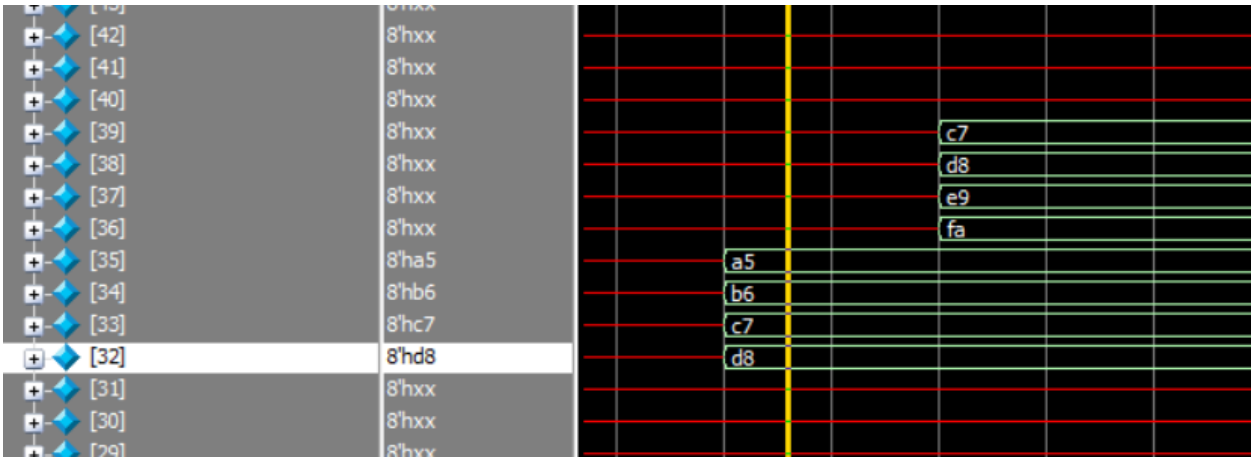


We made the memory sized 8 so it can be flexible to write 8 or 16 or 32 bit . so here we write halfword a5b6 so it written in 2 address location.

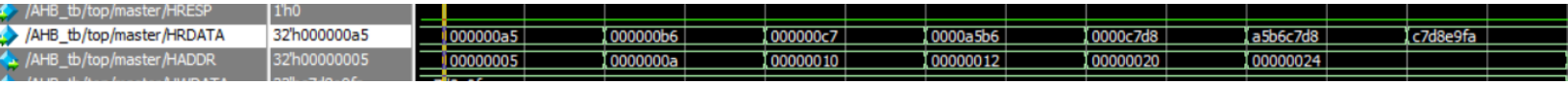
Now lets try to write a whole word using single HBURST so now the PSIZE is 2



Memory



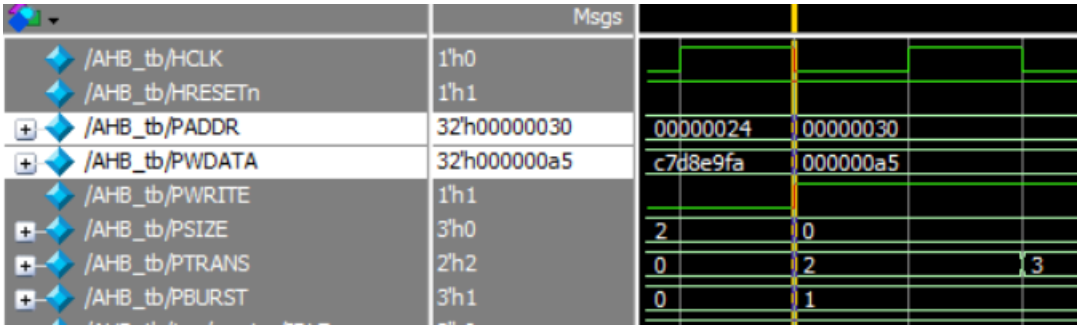
Now we will read what we wrote from the same address



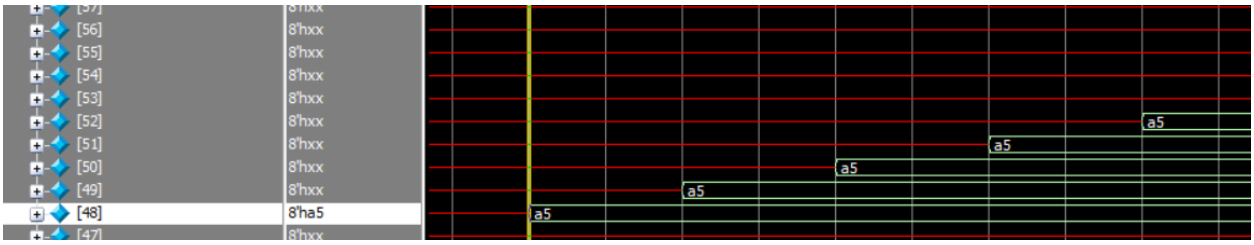
In addr=0 we read a5 and addr=5 we read b6 and so on

Now test the incr BURST

Write 8-bit in 5 seq address starting from 0x30 and HBURST=1

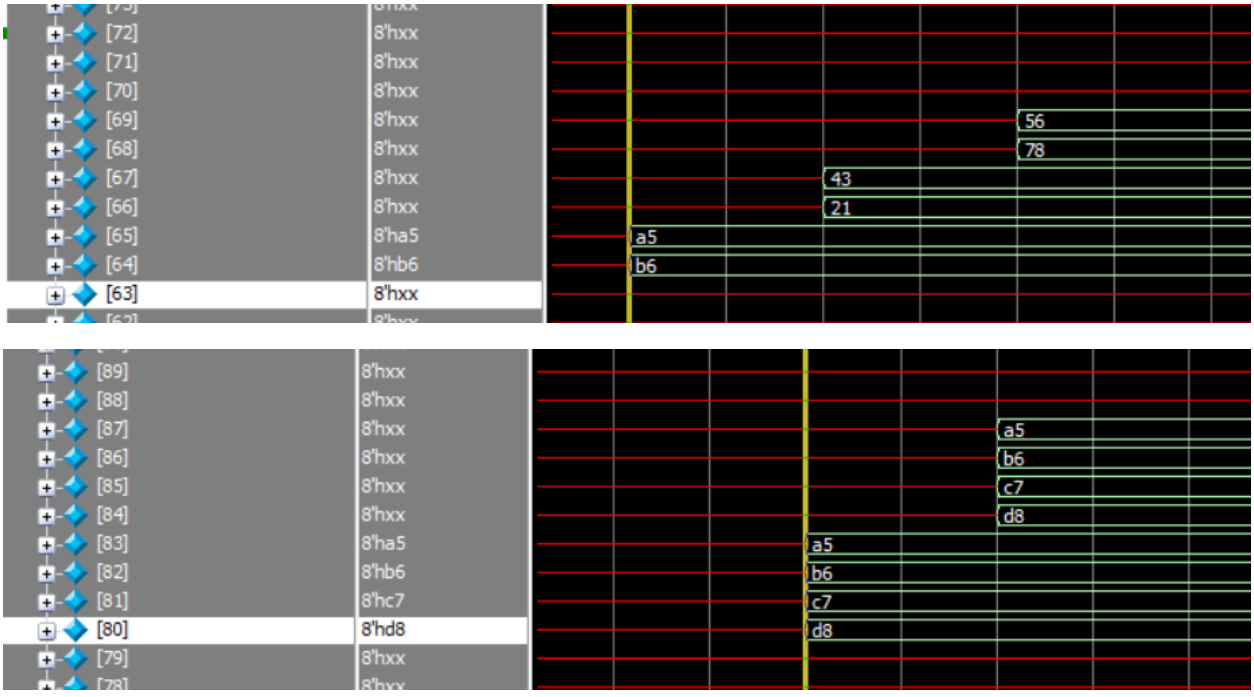


Expecting in memory it will write the a5 in address 0x30 and the next 4 addresses



Also make the same thing in 16-bit and 32-bit word

Memory for 16 and 32



And the same for reading.

SUPERVISOR

ENG. Fatma Ali