

FFT Project

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Introduction – Design Phases



- System modeling using MATLAB.
- RTL design.
- RTL verification.
- ASIC implementation using (OpenLane).
- We will go through the System modeling and RTL design, simple RTL verification, start of the ASIC.

Overview of FFT



- It's "fast fourier transform" an algorithm that computes the discrete fourier transform "DFT" of a sequence, or its inverse.
- A fourier transform converts a signal from its original domain to a representation in the frequency domain and vice versa.
- FFT manages to reduce the complexity of computing the DFT from O(n^2) to O(nxlog n) where n is the data size.
- we will implement 8-point FFT.
- Architecture used is iterative (one butterfly reused across time steps), and in-place (reuse the same memory for updates).
- The input/outputs is bit-reversed
- Radix-2 mean the input size N must be of power 2.
- the algorithm recursively splits the signal into even and odd indexed parts ,compute FFT of both , and combines using twiddle factors.

Overview of butterfly



• We can replace the 2-point DFT with a butterfly

Figure 4-3. FFT implementation of an 8-point DFT as two 4-point DFTs and four 2-point DFTs.

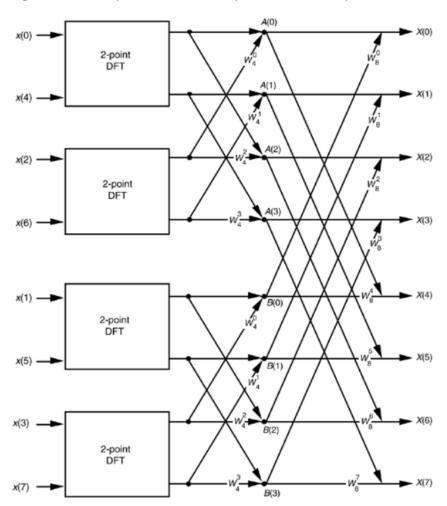
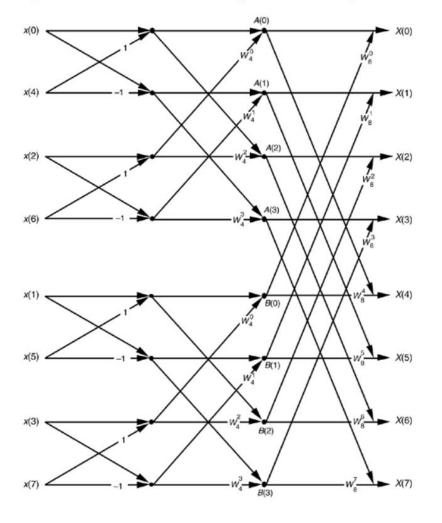


Figure 4-5. Full decimation-in-time FFT implementation of an 8-point DFT.



Overview of Twiddle Factor



•
$$W_N^m = e^{-j2pi(m/N)}$$

$$X(m) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi nm/N}.$$

$$X(m) = \sum_{n=0}^{(N/2)-1} x(2n)e^{-j2\pi(2n)m/N} + \sum_{n=0}^{(N/2)-1} x(2n+1)e^{-j2\pi(2n+1)m/N}.$$

$$X(m) = \sum_{n=0}^{(N/2)-1} x(2n)e^{-j2\pi(2n)m/N} + e^{-j2\pi m/N} \sum_{n=0}^{(N/2)-1} x(2n+1)e^{-j2\pi(2n)m/N}.$$

$$X(m) = \sum_{n=0}^{(N/2)-1} x(2n)W_N^{2nm} + W_N^m \sum_{n=0}^{(N/2)-1} x(2n+1)W_N^{2nm}.$$

<u>DERIVATION OF THE RADIX-2 FFT ALGORITHM | Chapter Four.</u> <u>The Fast Fourier Transform</u>

Here, we consider about the property of the twiddle factor. The twiddle factor has the periodic property as be shown in equation (2.2)

$$\begin{pmatrix} W_N^{k+N} = W_N^k \\ W_N^{k+\frac{N}{2}} = -W_N^k \end{pmatrix}$$

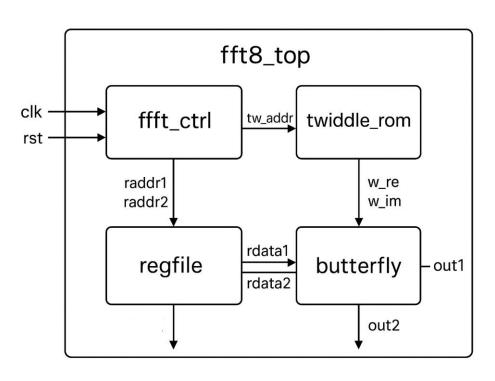
Block diagram

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

- N=8, W=12, F=8
- fft_ctrl is FSM that control the flow of the design
- butterfly block of the 2-point DFT
- -twiddle_rom contain twiddles factor values -regfile have the mem that store the input and rewrite the out

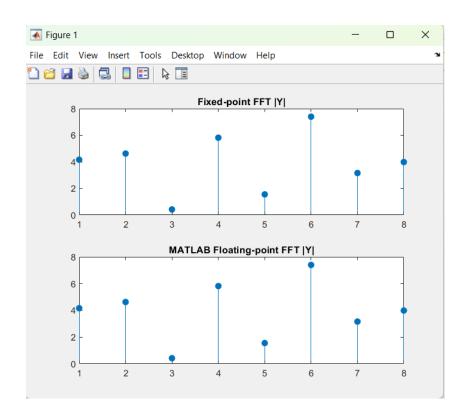
values



MATLAB

```
>> test fft_prepared_fixpt
 Max real: 1.438, Min real: -2.944
 Max imag: 0.628, Min imag: -0.865
 Fixed-point error norm = 2.686e-03
 SQNR vs MATLAB FFT = 73.340 dB
 Fixed-point output min: 0.422, max: 7.396
 Fixed-point input samples:
   Columns 1 through 6
   1.0938 - 0.7695i 1.1094 + 0.3711i -0.8633 - 0.2266i 0.0781 + 1.1172i -1.2148 - 1.0898i -1.1133 + 0.0312i
   Columns 7 through 8
   -0.0078 + 0.5508i 1.5312 + 1.1016i
          DataTypeMode: Fixed-point: binary point scaling
            Signedness: Signed
            WordLength: 12
        FractionLength: 8
 Stored integers (hex):
 X[1] re=118 im=F3B
 X[2] re=11C im=05F
 X[3] re=F23 im=FC6
 X[4] re=014 im=11E
 X[5] re=EC9 im=EE9
 X[6] re=EE3 im=008
 X[7] re=FFE im=08D
fx X[8] re=188 im=11A
 Fixed-point FFT output samples:
   Columns 1 through 6
    Columns 7 through 8
    2.5664 - 3.7969i 5.4336 + 0.2383i
          DataTypeMode: Fixed-point: binary point scaling
            Signedness: Signed
            WordLength: 12
         FractionLength: 8
  Stored integers (hex):
  Y[1] re=09D im=116
  Y[2] re=462 im=0DC
  Y[3] re=EEF im=F6E
  Y[4] re=0BD im=EB1
  Y[5] re=D67 im=BD8
  Y[6] re=EAE im=17E
  Y[7] re=291 im=C34
 Y[8] re=56F im=03D
```

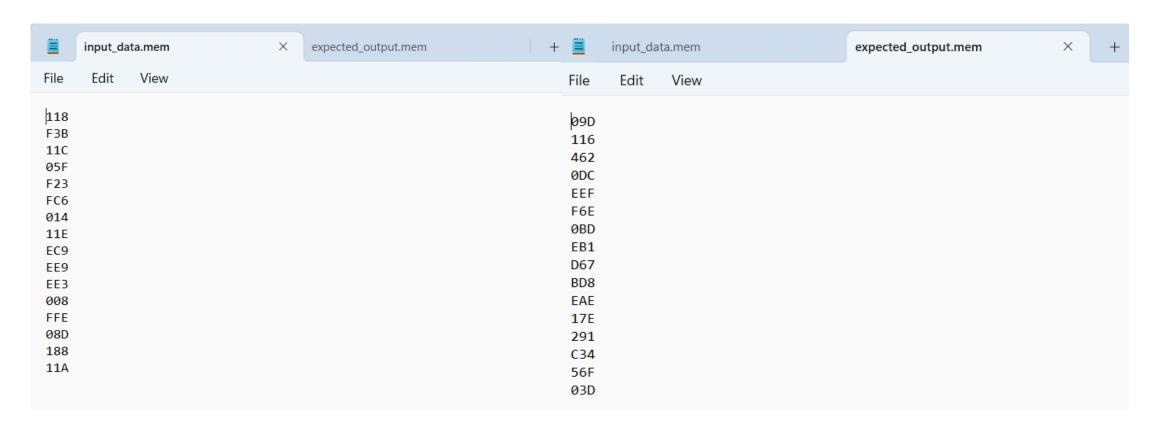




Input/output files



They will be sent to the testbench



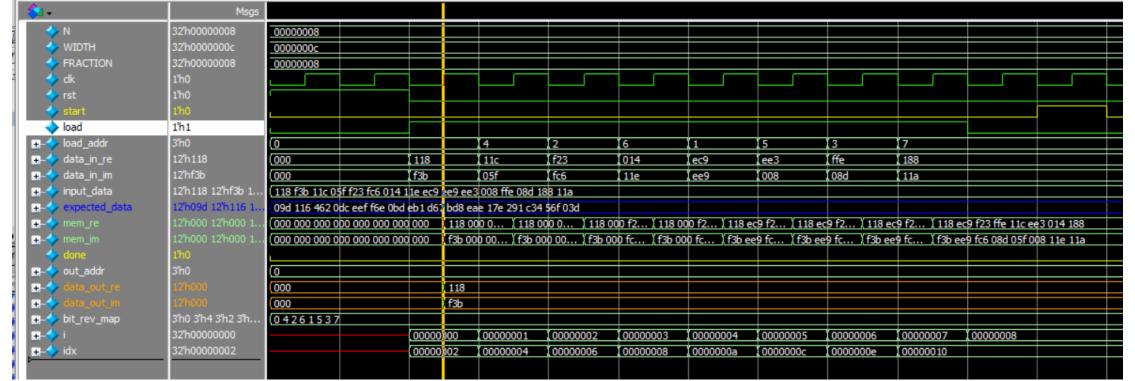
Questasim

ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

- For this result easily divide it by 256 to be in form of Q4.8 just like matlab
- Wave form loading inputs
- It took 8 cycles

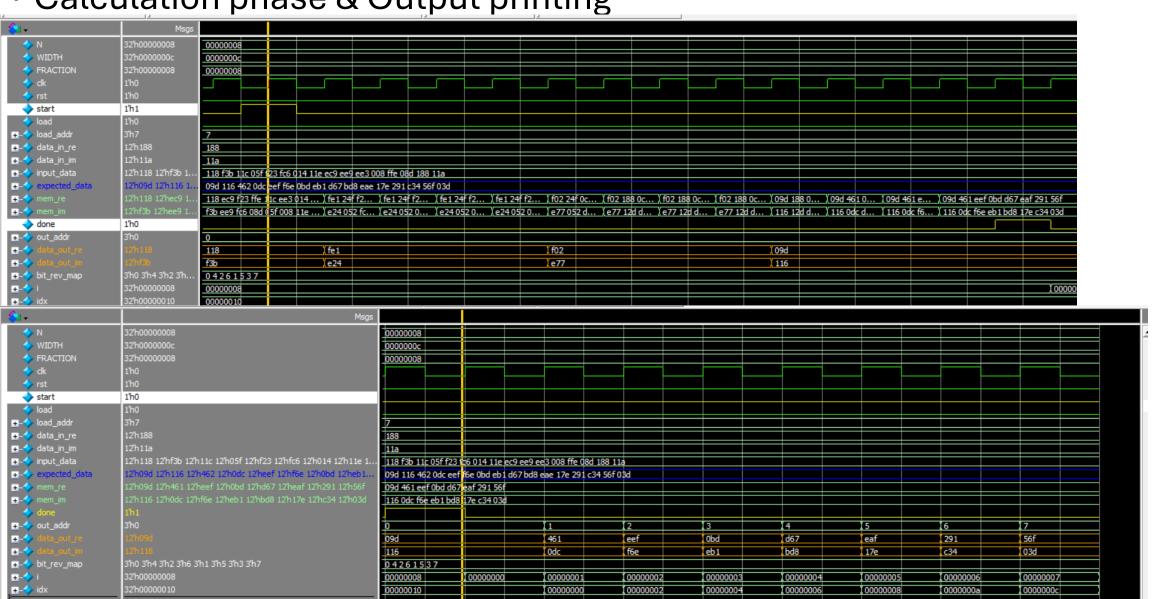
```
=== FFT Output Comparison ===
 Y[0] DUT: 157 + j278 | Expected: 157 + j278
# Y[1] DUT: 1121 + j220
                        | Expected: 1122 + j220
Y[2] DUT: -273 + j-146
                        | Expected: -273 + j-146
# Y[3] DUT: 189 + j-335 | Expected: 189 + j-335
   -> MATCH
 Y[4] DUT: -665 + j-1064
                          | Expected: -665 + i-1064
   -> MATCH
Y[5] DUT: -337 + j382
                        | Expected: -338 + j382
 Y[6] DUT: 657 + j-972 | Expected: 657 + j-972
 Y[7] DUT: 1391 + j61 | Expected: 1391 + j61
** Note: $stop
                 : fft_testbench.v(222)
    Time: 335 ns Iteration: 0 Instance: /fft8 tb
 Break in Module fft8 tb at fft testbench.v line 222
```



Questasim



Calculation phase & Output printing



Latency from the previous slide



- Latency = 9 cycles from all inputs loaded to the first output sample.
- And = 12 cycles from all inputs loaded "start=1" to "done=1" all outputs calculated.
- If we need it from the first input sample before start=1 the we will add 8 cycles since the inputs is loaded in 8-cycles.

Notes on SQNR

- For higher sqnr it is more better
- For my model in matlab the avg sqnr approx. =70dB for single run
- But when I tried 10 or 50 or 100 it drop down to 38,40dB and 70 is perfect and between 30...60dB is accepted in most DSP blocks, but below 30dB is recognized easily.

For N output samples:

$$ext{SQNR} = 10 \log_{10} \left(rac{\sum_{n=0}^{N-1} |y_{ ext{float}}(n)|^2}{\sum_{n=0}^{N-1} |y_{ ext{float}}(n) - y_{ ext{fixed}}(n)|^2}
ight) \, ext{dB}$$

- Numerator → total signal power of the ideal output.
- **Denominator** → total error power caused by fixed-point quantization.

Coverage Report

=== Instance: /fft8 tb/dut/ctrl === Design Unit: work.fft8_ctrl ______ Branch Coverage: Enabled Coverage Misses Coverage Bins Hits Branches 92.85% 14 13 -----CASE Branch--Count coming in to CASE 47 1 56 12 1 1 69 ***0*** All False Count Branch totals: 3 hits of 4 branches = 75.00% Condition Coverage: Enabled Coverage Bins Covered Misses Coverage Conditions 0 100.00% Statement Coverage: Enabled Coverage Bins Hits Misses Coverage Statements 32 32 0 100.00% Toggle Coverage: Enabled Coverage Bins Hits Misses Coverage -----Toggles 182 124 31.86%



| _ | | | | | o i dodibee |
|---|---------------------------------|----------------|--------------|------------------------|-------------|
| === Design Unit: work.twiddl | <u>e_rom</u> | | | | |
| Branch Coverage: Enabled Coverage | Bins | Hits | Misses | Coverage | |
| Branches File <u>twiddle rom.v</u> | 5 -CASE Branch | | | 80.00% | |
| 22 23 1 27 1 31 1 35 1 39 1 Branch totals: 4 hits of 5 branches | 9 4 1 3 1 ****** | | ing in to CA | | |
| Statement Coverage: Enabled CoverageStatements | Bins 11 | Hits 9 | Misses 2 | Coverage 81.81% | |
| | | | | | |
| Toggle Coverage: Enabled Coverage Toggles | Bins 52 | Hits 44 | Misses | | |

=== Design Unit: work.regfile fft

Branch Coverage: Enabled Coverage

Bins Hits Misses Coverage ---- 8 8 0 100.00%



| Branches | | 8 | 8 | 0 | 100.00% |
|---------------------|------|------|--------|----------|---------|
| Statement Coverage: | | | | _ | |
| Enabled Coverage | Bins | Hits | Misses | Coverage | |
| | | | | | |
| Statements | 18 | 18 | 0 | 100.00% | |
| Toggle Coverage: | | | | | |
| Enabled Coverage | Bins | Hits | Misses | Coverage | |
| | | | | | |
| Toggles | 398 | 330 | 68 | 82.91% | |

```
=== Design Unit: work.butterfly
 ______
 Statement Coverage:
    Enabled Coverage
                          Bins
                                       Misses Coverage
                            8
    Statements
                                          0 100.00%
Toggle Coverage:
   Enabled Coverage
                        Bins
                                      Misses Coverage
  Toggles
                                            94.79%
                         384
                                 364
```

Total Coverage By Instance (filtered view): 91.75%