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Mohamed adel abdelrahem ahmed

Analog Devices Eng. Omar fahmy

FFT

project

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AI-generated content may be incorrect.Name : Mohamed Adel Abdelrahem Ahmed   
mail : mhmdadel344@gmail.com**

**FFT**

**Introduction**

This is the final project of the internship @ Analog Devices.

We are going to implement the FFT with radix-2 and N=8 with MATLAB and then follow the hardware steps (digital flow)

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We will not cover the Verification and Backend steps till now.

**FFT**

It’s “fast fourier transform” an algorithm that computes the discrete fourier transform “DFT” of a sequence , or its inverse.

A fourier transform converts a signal from its original domain to a representation in the frequency domain and vice versa.

FFT manages to reduce the complexity of computing the DFT from O(n^2) to O(nxlog n ) where n is the data size.

The difference in speed can be enormous , especially for long data sets where n may be in the thousands or millions.

For Radix-2:

* The input size N must be a power of 2 (here, 8).
* **A blue sign with white text

  AI-generated content may be incorrect.**The algorithm recursively splits the signal into even and odd-indexed parts, computes FFT of both, and combines using twiddle factors.

**MATLAB Part**

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1st step I isolated the function file from the test files

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2nd step check for codegen

We wrote the fft in a loop based and bit-reversed iterative style

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3rd step A screenshot of a computer code

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4th , 5th ,6th step

Making type table

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Since the WL=12 and FL=8 then its 4-bit for integer and 8-bit for fraction

Then maximum +ve is 0111.11111111 = +7.996

And maximum -ve is 1000.00000000 = -8 A screenshot of a math test

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I changed my code part that randomize the input to be more general using randn

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the full codes will be in separate files .m

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**Arch design**

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We will choose iterative in place architecture

RTL blocks:

A diagram of a butterfly

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**Flow of the design :** first we inputs the 8 samples x(0) x(1) … x(7) real and img with size 12-bit to the regfile and then passed it to the butterfly inputs (U,V) and then the butterfly make the calculations to multiply the V with the W “twiddle factor” and the U multiplied by 1 and after that butterfly outputs (out1 ,out2) out1=U+V.W and out2=U-V.W , and after calculation we then rewrite the regfile with the result.

The FSM control the flow and provide the W values for the butterfly and provide the address to the regfile and tell what stage are we in now and the butterfly index.

Twiddle factor & radix-2 algorithm

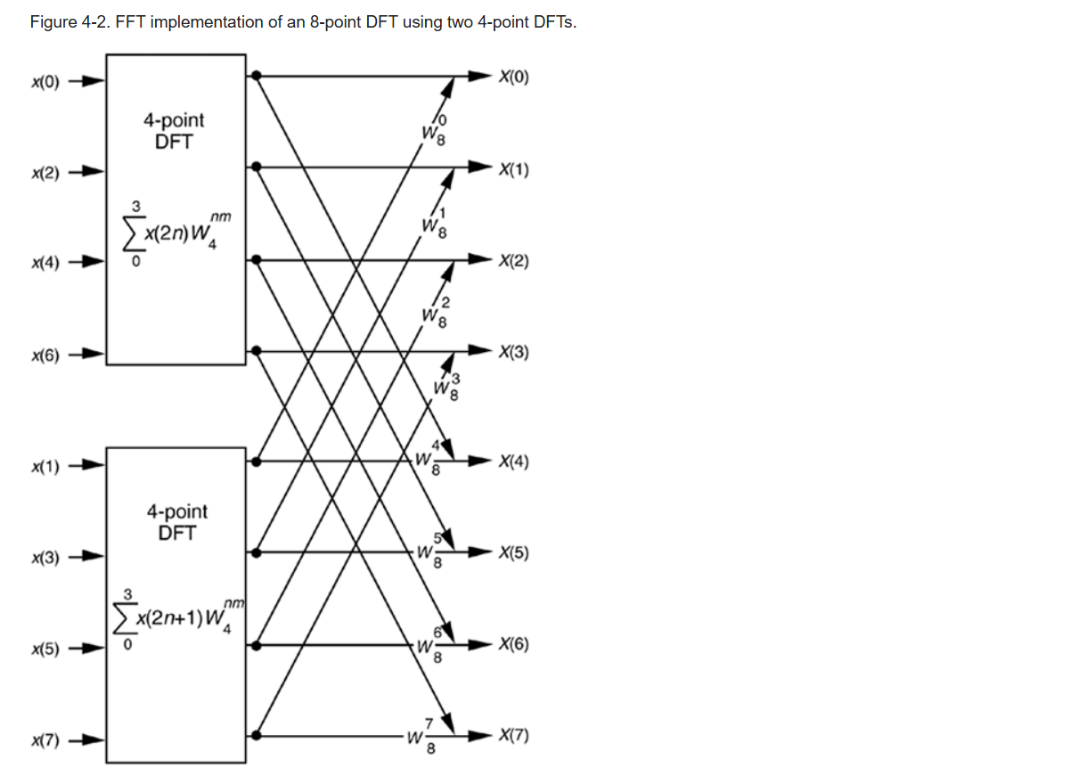
After assuming WNm=e-j2pi(m/N)

A math equations and formulas

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We can make it 4 2-points DFT

A diagram of a diagram

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Replacing the 2-point DFT by butterfly

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RTL files will be in separate folder.

**Results**

First the **MATLAB** randomize 8-sample input and then do the FFT and generate the output and compute the **AVG. SQNR** and also the error between my FFT model and internal MATLAB FFT and make 2 files one for the inputs and other for the outputs to pass them to the testbench done to test also the RTL design.

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**A computer screen shot of a computer code

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The 2 generated files input , output

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A screenshot of a computer program

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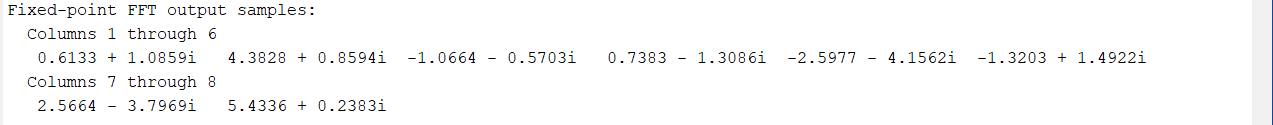
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**Questa result**

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It’s written in decimal but easily divided by 256 to see it in format Q4.8

Just like matlab 

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The full wave form

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A screen shot of a computer

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As we see here the **blue** signals is the input/output file from matlab so after the **load signal** is high we begin to take the inputs in 8 cycles so after **8 cycles** from load the **orange** signal is the internal memory in the design that hold the inputs data.

After that we have start signal it goes 1 when loading all input and then the calculation starts and after all calculations end then done signal go high.

We need to calculate the latency “number of cycles from start of the calculations to the first output”. If we need execution time it will be “number of cycles from start of the calculations to the done=1”.

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As we see from the **start** to the first **data\_out\_re , data\_out\_im** is 9 cycles and from the **start** to the **done** is 13 cycles but from the **start** to the all calculations end **mem\_re** and **mem\_im** being filled with the output is 12 cycles that because the done state take one cycle from the end of calculation to go to 1 since it’s sequential.

We can conclude that the values saved in **mem\_re , mem\_im** are the same as stored in the **expected\_data.**

**Latency=9 clock cycles.**

**Execution=12 clock cycles.**

**Reading output after done**

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**A math equations and numbers

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 Higher SQNR → less quantization noise → fixed-point result is closer to floating-point.

 Typical scale:

* **> 60 dB** → excellent (error barely noticeable)
* **40–60 dB** → acceptable for most DSP
* **< 30 dB** → large visible distortion

**Coverage Report**

Code coverage (bcst) branch , conditional , statement , toggle

**fft\_ctrl module**

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Why it’s not 100% because of the case default we can remove it since we covered all 4 cases

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Why toggle don’t reach high coverage % ,because we used only one test case. For more we can run it 100 times for example.

**twiddle\_rom module**

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Also because of the case

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**butterfly module**

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**fft8\_top module**

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**ASIC phase**

For the physical flow design we will use OpenLane opensource tool with technology and std cell used skywater 130nm , sky130\_fd\_sc\_hd.

We will run flow.tcl and then the reports will created if the flow run successfully for all steps including synthesis and routing and power and pnr and cts …..

**But we will do it later.**

**Thank**

**You**