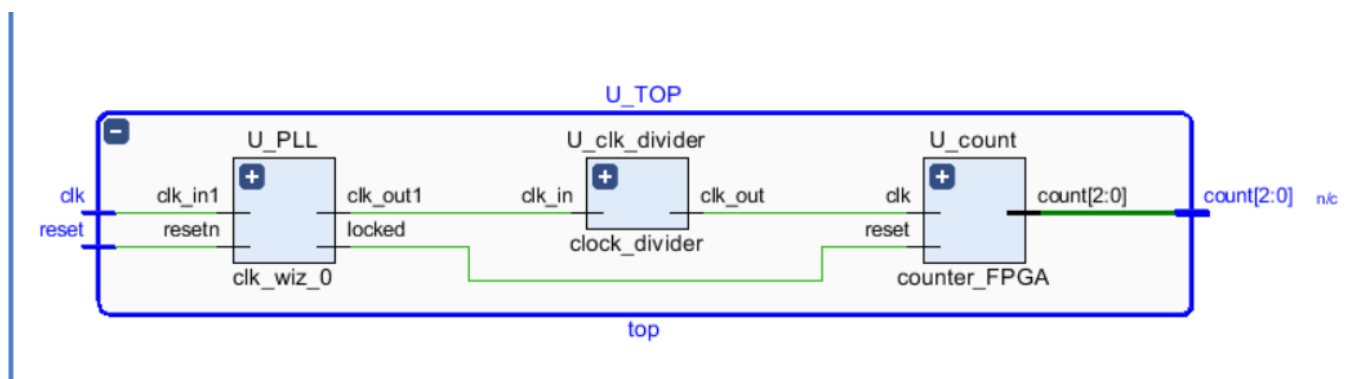


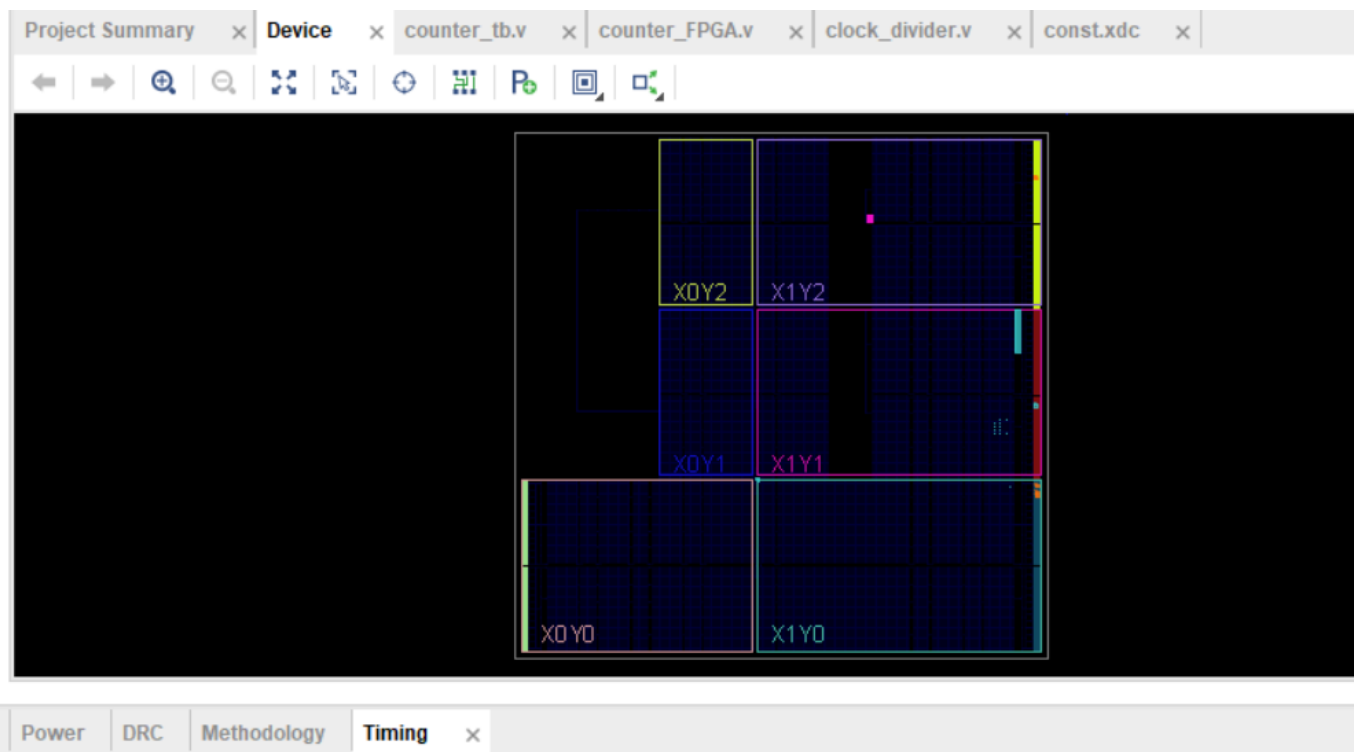
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3-bit Counter FPGA

The elaborated design after following the steps in the lab and inserting the PLL to lower the clock from 100MHZ to 8MHZ and then designed a clock divider to lower more from 8MHZ to 1HZ to be able to see the counting process in real life time



The implemented design



Summary

| Hold | | Pulse Width | |
|-------------------------|------------|--|----------|
| Worst Slack (WNS): | 121.621 ns | Worst Hold Slack (WHS): | 0.263 ns |
| Worst Slack (TNS): | 0.000 ns | Worst Pulse Width Slack (WPWS): | 2.633 ns |
| Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |

Behavioral simulation example

I divided the 8MHZ by only 800 so it will count every 100usec because the simulation take long time to count but for real 1 second we will divide by 8000000

