Team Members:

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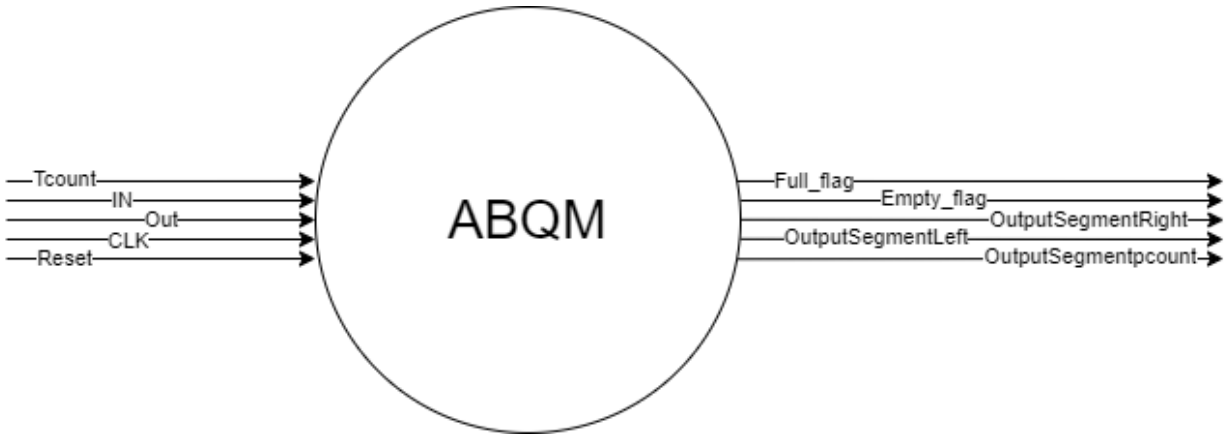
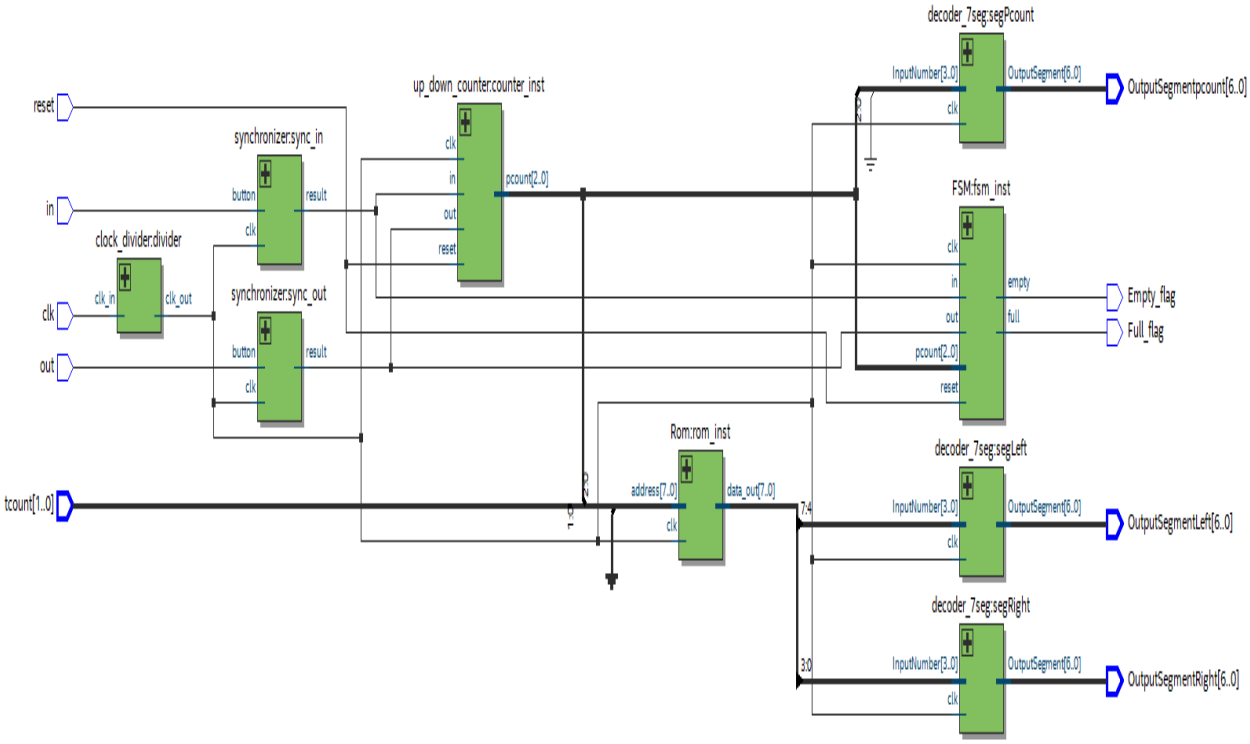
Input	Description
clk	ClK is used to synchronize all the components
reset	Is used to reset all modules to their default values
in	Represents the button at the start of the queue
out	Represents the button at the end of the queue
tcount	Represents the number of tellers

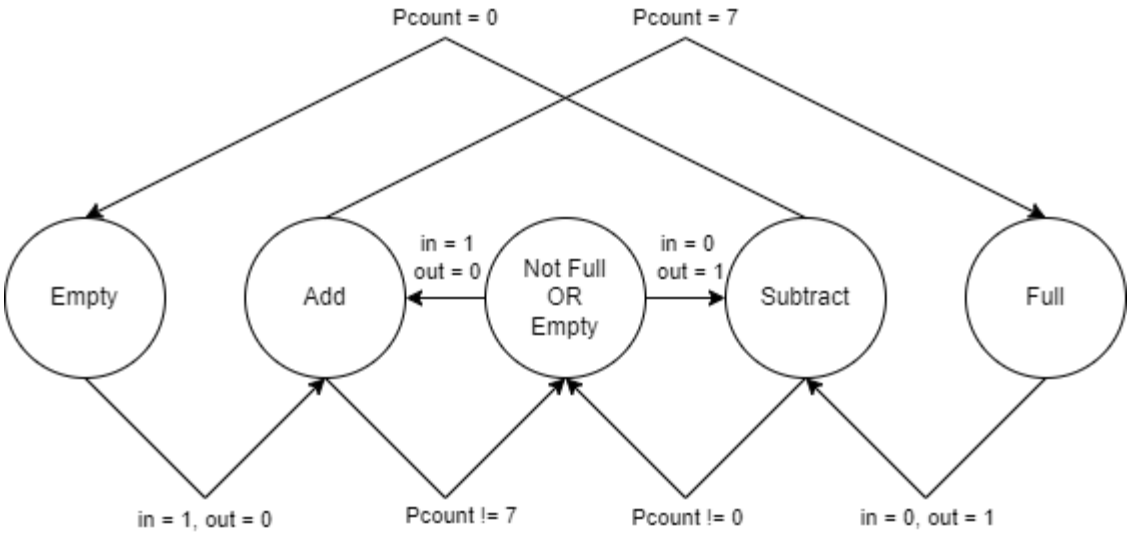
Output	Description
Full_flag	A led that lights up when the queue is full (pcount = 7)
Empty_flag	A led that lights up when the queue is empty (pcount = 0)
OutputSegmentRight	The wait time could be 2 digits so they would need to be split into two seven segments after (Wait time is outputted in BCD) OutputSegmentRight is the Seven segment display on the right (Representing the units)
OutputSegmentLeft	The wait time could be 2 digits so they would need to be split into two seven segments after (Wait time is outputted in BCD) OutputSegmentLeft is the Seven segment display on the left (Representing the tenth)
OutputSegmentpcount	Displayes the pcount (0 - 7) on a 7 segment display

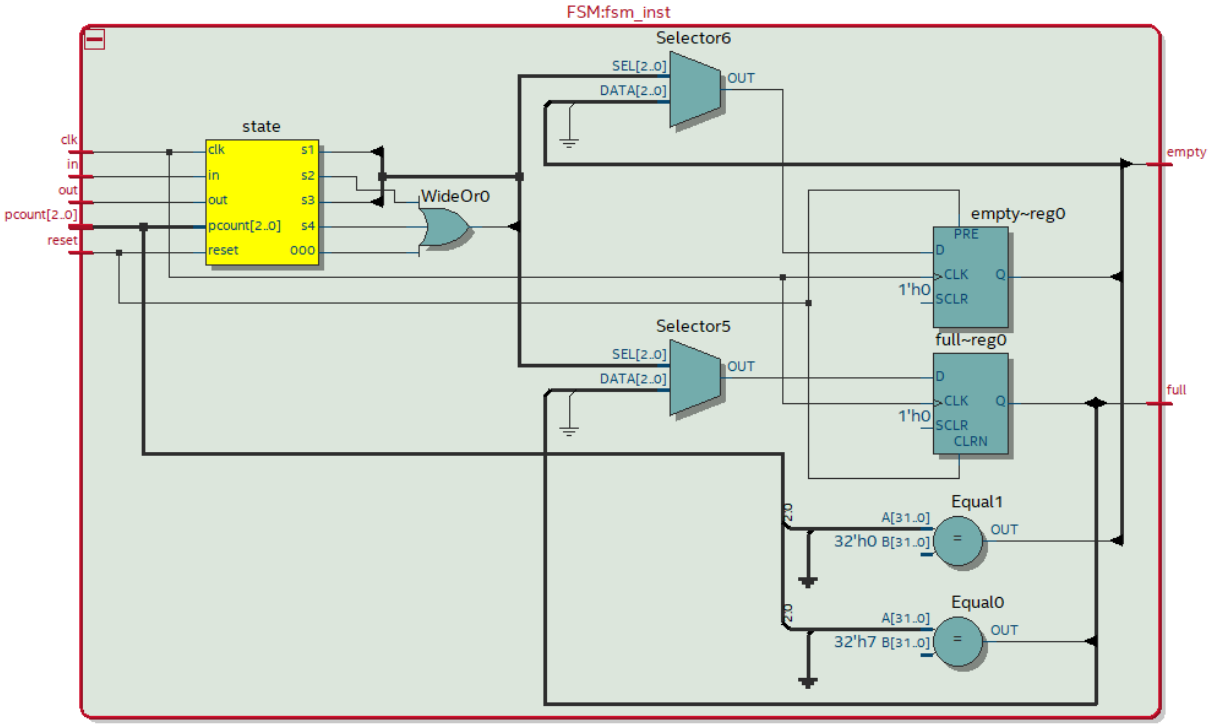
Tcount	Pcount	Wtime	index	BCD
1	0	0	00010000	00000000
1	1	3	00010001	00000011
1	2	6	00010010	00000110
1	3	9	00010011	00001001
1	4	12	00010100	00010010
1	5	15	00010101	00010101
1	6	18	00010110	00011000
1	7	21	00010111	00100001
2	0	0	00100000	00000000
2	1	3	00100001	00000011
2	2	4	00100010	00000100
2	3	6	00100011	00000110
2	4	7	00100100	00000111
2	5	9	00100101	00001001
2	6	10	00100110	00010000
2	7	12	00100111	00010010
3	0	0	00110000	00000000
3	1	3	00110001	00000011
3	2	4	00110010	00000100
3	3	5	00110011	00000101
3	4	6	00110100	00000110
3	5	7	00110101	00000111
3	6	8	00110110	00001000
3	7	9	00110111	00001001

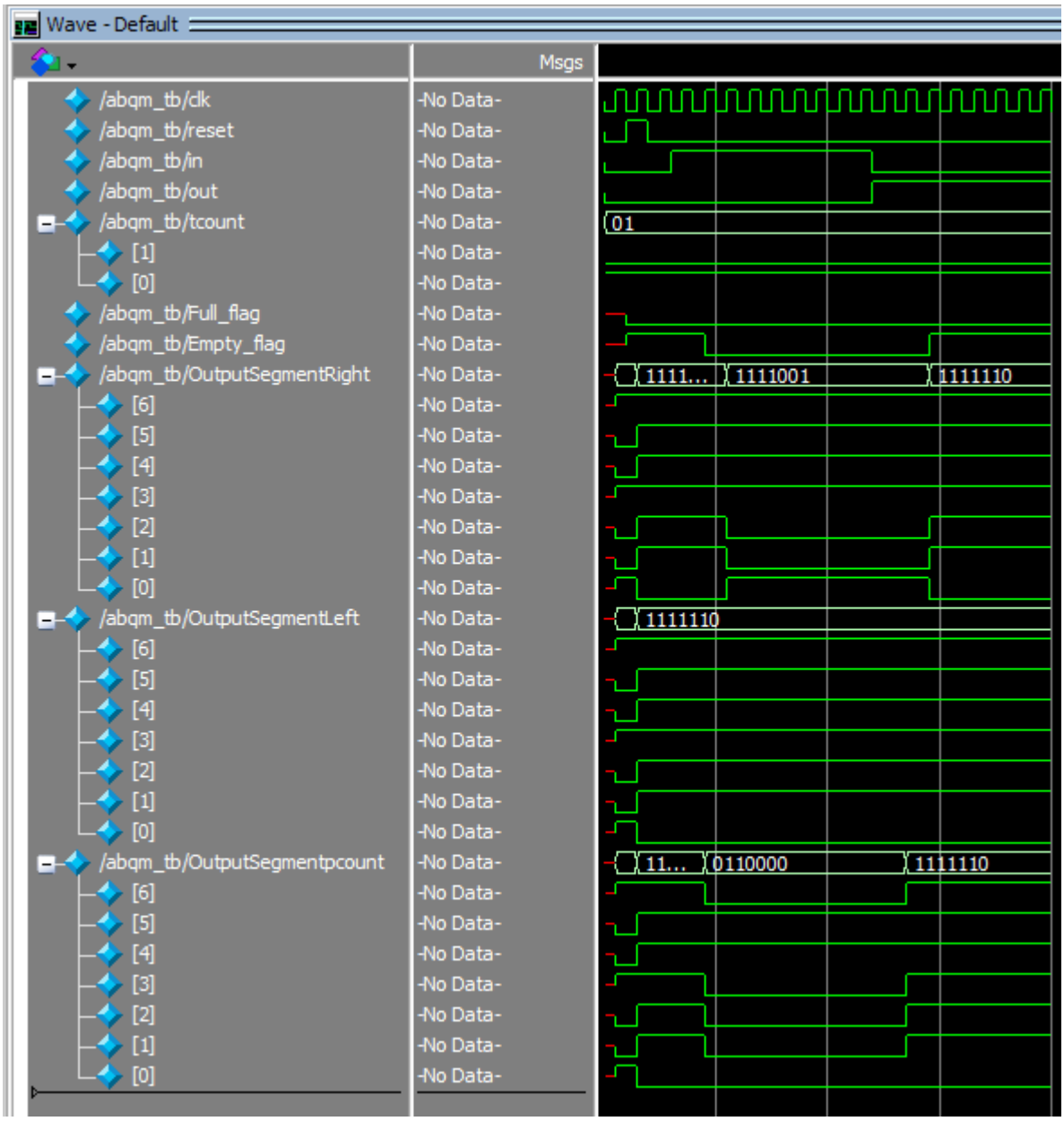
This is a Table representing all the possible Pcount – Tcount Combinations and the outputted Wait Time in both Decimal and BCD


Tcount
IN
Out
CLK
Reset
ABQM
Full_flag
Empty_flag
OutputSegmentRight
OutputSegmentLeft
OutputSegmentpcount


reset
in
clk
out
tcount[1..0]
synchronizer:sync_in
synchronizer:sync_out
clock_divider:divider
up_down_counter:counter_inst
Rom:rom_inst
decoder_7seg:segPcount
FSM:fsm_inst
decoder_7seg:segLeft
decoder_7seg:segRight
OutputSegmentpcount[6..0]
Empty_flag
Full_flag
OutputSegmentLeft[6..0]
OutputSegmentRight[6..0]


Pcount = 0
Pcount = 7
Empty
Add
in = 1
out = 0
Not Full
OR
Empty
in = 0
out = 1
Subtract
Full
in = 1, out = 0
Pcount != 7
Pcount != 0
in = 0, out = 1


FSM:fsm_inst
Selector6
SEL[2..0]
DATA[2..0]
OUT
state
clk
in
out
pcount[2..0]
reset
s1
s2
s3
s4
000
WideOr0
empty
empty~reg0
PRE
D
CLK
Q
SCLR
1'h0
Selector5
full~reg0
full
CLRN
Equal1
A[31..0]
32'h0 B[31..0]
=
Equal0
32'h7 B[31..0]



0 : outputreg = 7'b1111110; 1 : outputreg <= 7'b0110000;

2 : outputreg <= 7'b1101101; 3 : outputreg <= 7'b1111001;

4 : outputreg <= 7'b0110011; 5 : outputreg <= 7'b1011011;

6 : outputreg <= 7'b1011111; 7 : outputreg <= 7'b1110000;

8 : outputreg <= 7'b1111111; 9 : outputreg <= 7'b1111011;