Lab 9-10 – Nanoprocessor Design Competition

CS1050 Computer Organization and Digital Design

Group 14:

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Lab Task:

• Design a simple nano processor capable of executing the following assembly instructions.

1. ADD (Addition)

2. MOV (Move)

3. NEG (Negation) 2's complement

4. JZR (Jump) Jump to an instruction if condition is met.

• Build the nano processor using the following components.

1. 4-bit Add/Subtract unit

2. 3-bit adder

3. 3-bit Program Counter (PC)

4. k-way b-bit multiplexers

5. Register Bank

6. Program ROM

7. Buses

8. Instruction Decoder

- Write an assembly program to calculate the total between 1 to 3.
- Simulate addition of 1,2 and 3 and load it to R7(8th register).
- Test on BASYS 3 and verify the functionality of the nano processor.
- Demonstrate the circuit to the instructor

Assembly Program and Machine code representation:

ASSEMBLY CODE	MACHINE CODE REPRESENTATION
MOV 0,R7	101110000000
MOV 1,R1	100010000001
MOV 2,R2	100100000010
MOV 3,R3	100110000011
ADD R7,R1	001110010000
ADD R7,R2	001110100000
ADD R7,R3	001110110000
JZR R0,7	110000000111

ALL VHDL FILES AND TIMING DIAGRMS:

❖ Slow Clock

1. Design Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
   Port ( Clk_in : in STD_LOGIC;
          Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is
signal count: integer := 1;
signal clk_status:  STD_LOGIC := '1';

begin
   process(Clk_in) begin
```

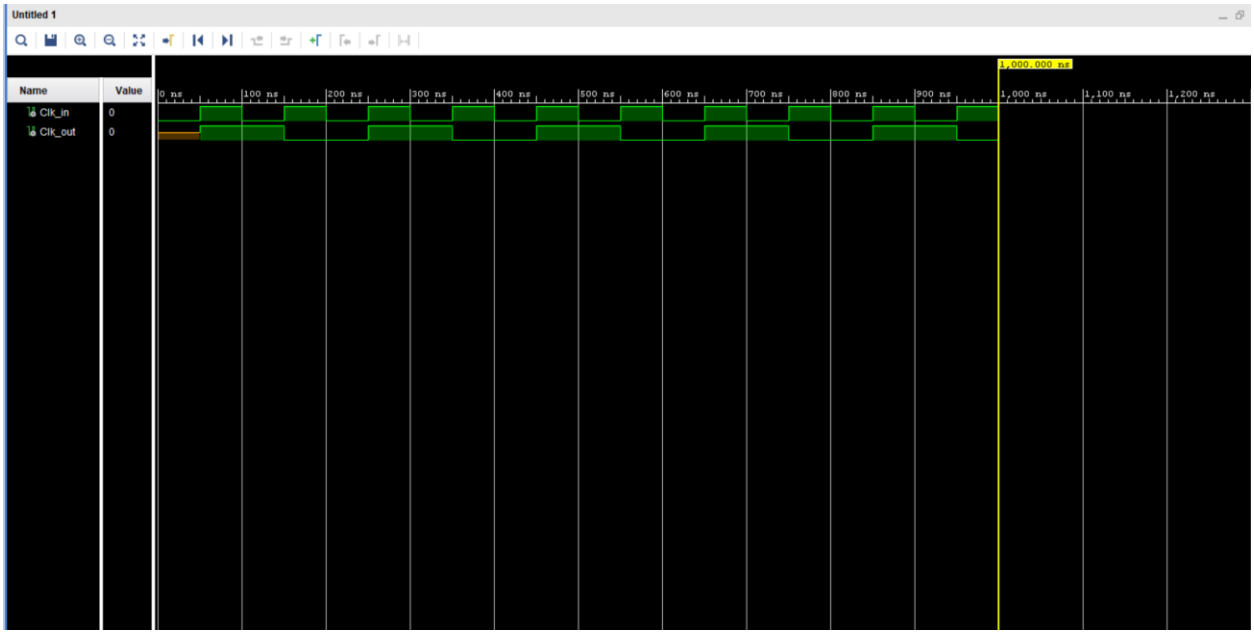
```
    if (rising_edge(Clk_in)) then
      count <= count +1;
      --if (count = 50000000) then -- for practical purposes
      if (count = 1) then --only for the simulation purposes
        clk_status <= NOT(clk_status);
        Clk_out <= clk_status;
        count <= 1;
      end if;
    end if;

  end process;

end Behavioral;
```

2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
```

```
-- Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is
 -- Component Declaration for DUT
   component Slow_Clk is
       Port (
          Clk_in : in STD_LOGIC;
          Clk_out : out STD_LOGIC
           );
 end component;

 signal Clk_in : STD_LOGIC := '0';
 signal Clk_out : STD_LOGIC;

begin

 uut: Slow_Clk port map (
   Clk_in => Clk_in,
   Clk_out => Clk_out
   );
process begin

 wait for 50ns;

 Clk_in <= NOT(Clk_in);

end process;

end Behavioral;
```

3. Timing Diagram



❖ 3-bit adder

1. Souce code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
```

```
--use UNISIM.VComponents.all;

entity Adder_3 is
    Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
       B : in STD_LOGIC_VECTOR (2 downto 0);
       S : out STD_LOGIC_VECTOR (2 downto 0);
       Carry_in : in STD_LOGIC;
       Carry_out : out STD_LOGIC);
end Adder_3;

architecture Behavioral of Adder_3 is
    component FA
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
end component;
signal FA0_C,FA1_C: STD_LOGIC;
begin
FA_0:FA
    port map(
        A => A(0),
        B => B(0),
        C_in => Carry_in,
        S => S(0),
        C_out => FA0_C
    );
FA_1:FA
    port map(
        A => A(1),
```

```
        B => B(1),
        C_in => FA0_C,
        S => S(1),
        C_out => FA1_C
    );
FA_2:FA
    port map(
        A => A(2),
        B => B(2),
        C_in => FA1_C,
        S => S(2),
        C_out => Carry_out
    );
end Behavioral;
```

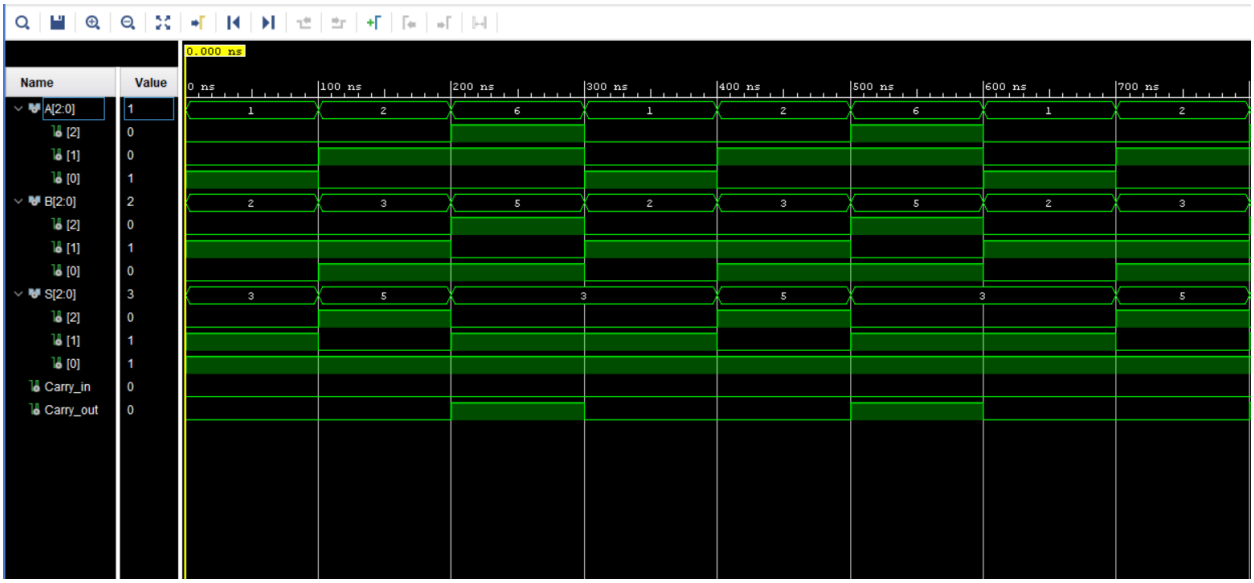
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Adder_3_sim is
```

```
--  Port ( );
end Adder_3_sim;

architecture Behavioral of Adder_3_sim is

component Adder_3

    Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
           B : in STD_LOGIC_VECTOR (2 downto 0);
           S : out STD_LOGIC_VECTOR (2 downto 0);
           Carry_in : in STD_LOGIC;
           Carry_out : out STD_LOGIC);

end component;

signal A : STD_LOGIC_VECTOR(2 downto 0);
signal B : STD_LOGIC_VECTOR (2 downto 0);
signal S : STD_LOGIC_VECTOR (2 downto 0);
signal Carry_in : STD_LOGIC;
signal Carry_out : STD_LOGIC;

begin

UUT: Adder_3
    port map(
        A => A,
        B =>B,
        S => S,
        Carry_in => Carry_in,
        Carry_out => Carry_out
        );
```

```
process
begin

        --110 011 010 001 010 001 ; 210001R
        --110 011 010 101 110 010 ; 210290A

   Carry_in <= '0';
   A <= "001"; --1
   B <= "010"; --2

wait for 100ns;

   A <= "010"; --2
   B <= "011"; --3

wait for 100ns;

   A <= "110"; --6
   B <= "101"; --5

wait for 100ns;

end process;

end Behavioral;
```

3. Timing Diagram



❖ 4-bit Adder Subtractor unit

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity ASUnit_4 is

    Port ( A : in STD_LOGIC_VECTOR(3 downto 0);
           B : in STD_LOGIC_VECTOR(3 downto 0);
           C  : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR(3 downto 0);
           Overflow,Zero : out STD_LOGIC);
           --C_out : out STD_LOGIC);

end ASUnit_4;

architecture Behavioral of ASUnit_4 is

    component FA

        port (
         A: in std_logic;
         B: in std_logic;
         C_in: in std_logic;
         S: out std_logic;
         C_out: out std_logic);
     end component;

     SIGNAL FA0_S, FA0_C, FA1_S, FA1_C, FA2_S, FA2_C, FA3_S, FA3_C ,X0,X1,X2,X3 : std_logic;

begin

     X0 <= B(0) XOR C;
     X1 <= B(1) XOR C;
     X2 <= B(2) XOR C;
```

```
X3 <= B(3) XOR C;

FA_0 : FA
  port map (
   A => A(0),
   B => X0,
   C_in => C,
   S => FA0_S,
   C_Out => FA0_C);

FA_1 : FA
   port map (
   A => A(1),
   B => X1,
   C_in => FA0_C,
   S => FA1_S,
   C_Out => FA1_C);

FA_2 : FA
    port map (
    A => A(2),
    B => X2,
    C_in => FA1_C,
    S => FA2_S,
    C_Out => FA2_C);

 FA_3 : FA
    port map (
    A => A(3),
    B => X3,
    C_in => FA2_C,
```

```
        S => FA3_S,
        C_out => FA3_C);

    S(0) <= FA0_S;
    S(1) <= FA1_S;
    S(2) <= FA2_S;
    S(3) <= FA3_S;

    --C_out <= FA3_C;
    Overflow <= FA3_C XOR FA2_C;
    Zero <= NOT(FA0_S OR FA1_S OR FA2_S OR FA3_S);

end Behavioral;
```

2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ASUnit_4_sim is
--  Port ( );
```

```
end ASUnit_4_sim;

architecture Behavioral of ASUnit_4_sim is

component ASUnit_4 is

    Port ( A : in STD_LOGIC_VECTOR(3 downto 0);
           B : in STD_LOGIC_VECTOR(3 downto 0);
           C  : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR(3 downto 0);
           Overflow,Zero : out STD_LOGIC);

end component;

signal A : STD_LOGIC_VECTOR (3 downto 0);
signal B : STD_LOGIC_VECTOR (3 downto 0);
signal C : STD_LOGIC;
signal Overflow,Zero : STD_LOGIC;
signal S : STD_LOGIC_VECTOR (3 downto 0);

begin

UUT: ASUnit_4

port map(
    A => A,
    B => B,
    C => C,
    --C_out => C_out,
    Overflow => Overflow,
    Zero => Zero,
```

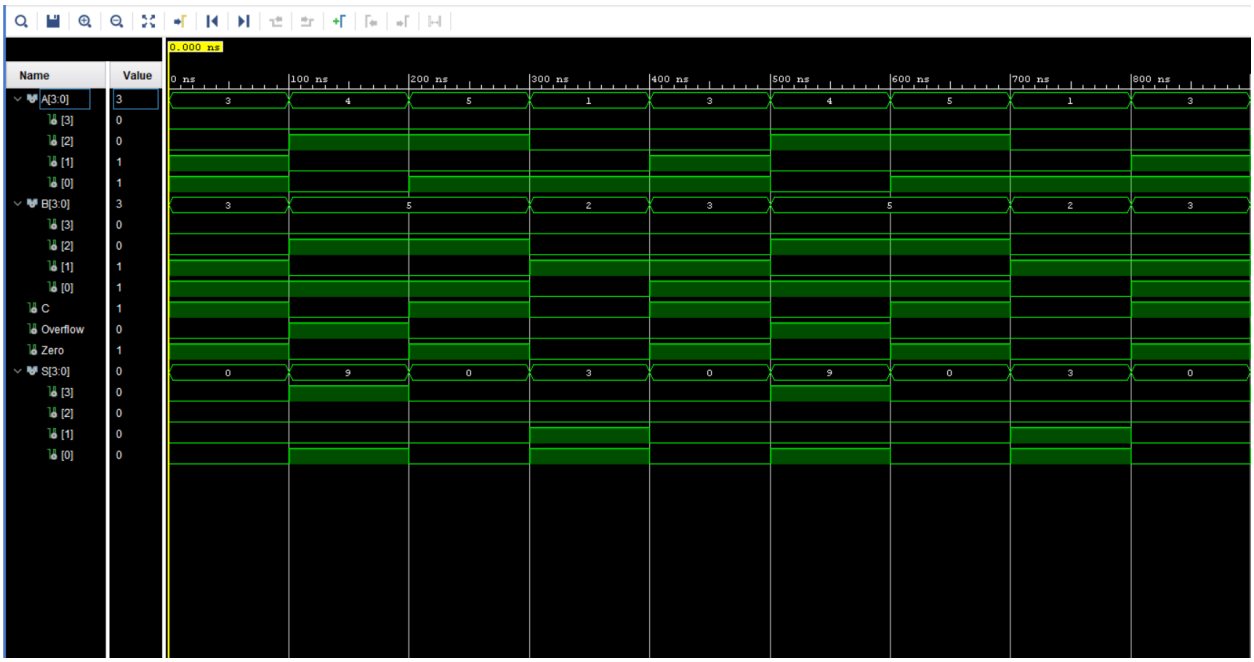
```
   S => S
);

process

begin
        --11 0011 0100 0101 0001 ; 210001R
        --11 0011 0101 0111 0010 ; 210290A

A <= "0011"; -- 3 - 3
B <= "0011";
C <= '1';

wait for 100ns;

A <= "0100"; -- 4 + 5
B <= "0101";
C <= '0';

wait for 100ns;

A <= "0101"; -- 5 - 7
B <= "0101";
C <= '1';

wait for 100ns;

A <= "0001"; -- 1 + 2
B <= "0010";
C <= '0';
```

wait for 100ns;

end process;

end Behavioral;

3. Timing Diagram



❖ 3-bit Program Counter

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity PC_3bit is

 Port ( D : in STD_LOGIC_VECTOR (2 downto 0);
       Clk : in STD_LOGIC;
       Clr : in STD_LOGIC;
       Q : out STD_LOGIC_VECTOR (2 downto 0));

end PC_3bit;

architecture Behavioral of PC_3bit is
   component D_FF
       Port (  D : in STD_LOGIC;
             Res : in STD_LOGIC;
             Clk : in STD_LOGIC;
```

```
            Q : out STD_LOGIC;
            Qbar : out STD_LOGIC
            );
end component;

begin
D_FF_0:D_FF
   port map(
      D=>D(0),
      Q=>Q(0),
      Res=>clr,
      Clk=>Clk
   );
D_FF_1:D_FF
   port map(
      D=>D(1),
      Q=>Q(1),
      Res=>clr,
      Clk=>Clk
   );
D_FF_2:D_FF
   port map(
      D=>D(2),
      Q=>Q(2),
      Res=>clr,
      Clk=>Clk
   );


end Behavioral;
```

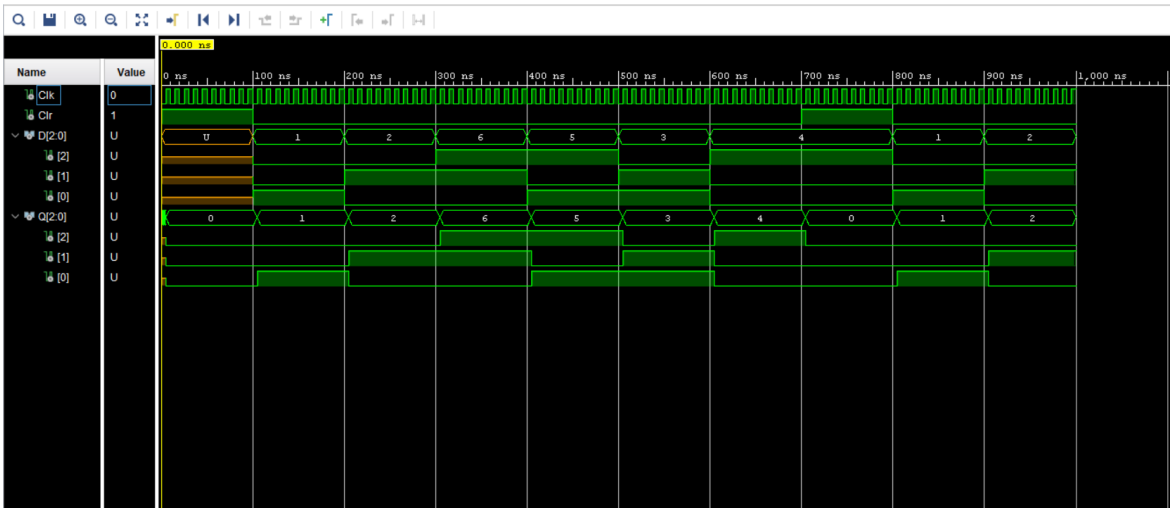
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity PC_3bit_sim is
-- Port ( );
end PC_3bit_sim;

architecture Behavioral of PC_3bit_sim is

component PC_3bit

 Port ( D : in STD_LOGIC_VECTOR (2 downto 0);
 Clk : in STD_LOGIC;
 Clr : in STD_LOGIC;
 Q : out STD_LOGIC_VECTOR (2 downto 0));
end component;

signal Clk : STD_LOGIC :='0';
signal Clr : STD_LOGIC;
```

```
signal D,Q : STD_LOGIC_VECTOR(2 downto 0);

begin

UUT : PC_3bit
 PORT MAP(
   D => D,
   Clk => Clk,
   Clr => Clr,
   Q => Q
   );

 process
 begin

 wait for 5ns;

 Clk <= not (Clk);
 end process;

 process
 begin
            --110 011 010 001 010 001 ; 210001R
            --110 011 010 101 110 010 ; 210290A

 Clr <= '1';
 wait for 100ns;

 D <= "001";
 Clr <= '0';
```

```
wait for 100ns;

D <= "010";
wait for 100ns;

D <= "110";
wait for 100ns;

D <= "101";
wait for 100ns;

D <= "011";
wait for 100ns;

D <= "100";
wait for 100ns;

end process;
```

3. Timing Diagram



❖ 2-way 3-bit multiplexer

1. Source Code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_2_to_1_3bit is
   Port (
      R0 : in STD_LOGIC_VECTOR(2 downto 0);
      R1 : in STD_LOGIC_VECTOR(2 downto 0);
      Sel : in STD_LOGIC;
      Y : out STD_LOGIC_VECTOR (2 downto 0));

   end Mux_2_to_1_3bit;

architecture Behavioral of Mux_2_to_1_3bit is

   begin

   Y <= R0 when Sel = '0' else R1;
```

```
    end Behavioral;
```

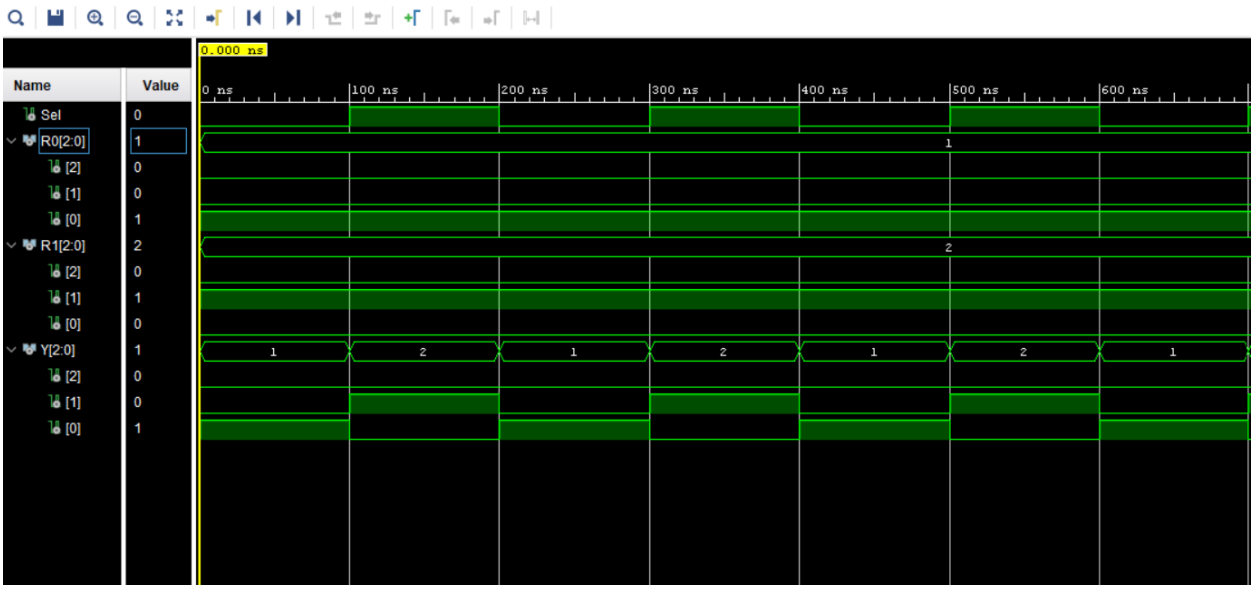
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_2_to_1_3bit_sim is
--  Port ( );
end Mux_2_to_1_3bit_sim;

architecture Behavioral of Mux_2_to_1_3bit_sim is

component Mux_2_to_1_3bit is
    Port (
        R0 : in STD_LOGIC_VECTOR(2 downto 0);
        R1 : in STD_LOGIC_VECTOR(2 downto 0);
        Sel : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR (2 downto 0));
```

```
    end component;

        --110 011 010 001 010 001 ; 210001R
        --110 011 010 101 110 010 ; 210290A

signal Sel: STD_LOGIC;
signal R0 : STD_LOGIC_VECTOR(2 downto 0):= "001";
signal R1 : STD_LOGIC_VECTOR(2 downto 0):= "010";
signal Y : STD_LOGIC_VECTOR(2 downto 0);

begin

UUT:Mux_2_to_1_3bit
port map(
    Sel => Sel,
    R0 => R0,
    R1 => R1,
    Y => Y
    );

process begin

Sel <= '0';

wait for 100ns;

Sel <= '1';

wait for 100ns;

end process;
```

end Behavioral;

3. Timing Diagram



❖ 2-way 4-bit multiplexer

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
```

```
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_2_to_1_4bit is
    Port ( Sel : in STD_LOGIC;
           R0 : in STD_LOGIC_VECTOR (3 downto 0);
           R1 : in STD_LOGIC_VECTOR (3 downto 0);
           Y : out STD_LOGIC_VECTOR (3 downto 0));

    end Mux_2_to_1_4bit;

architecture Behavioral of Mux_2_to_1_4bit is

begin

    Y <= R0 when Sel ='0' else R1;

end Behavioral;
```

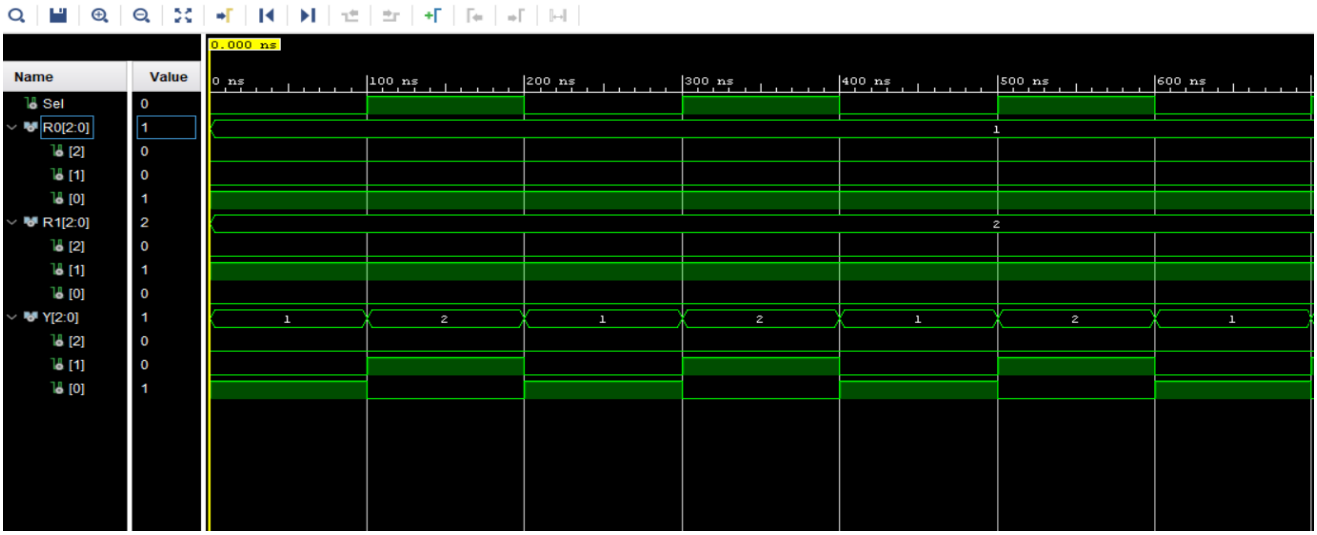
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
```

```
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_2_to_1_4bit_sim is
--  Port ( );
end Mux_2_to_1_4bit_sim;

architecture Behavioral of Mux_2_to_1_4bit_sim is

component Mux_2_to_1_4bit is
   Port (
      R0 : in STD_LOGIC_VECTOR(3 downto 0);
      R1 : in STD_LOGIC_VECTOR(3 downto 0);
      Sel : in STD_LOGIC;
      Y : out STD_LOGIC_VECTOR (3 downto 0));

   end component;

            --11 0011 0100 0101 0001 ; 210001R
            --11 0011 0101 0111 0010 ; 210290A

signal Sel: STD_LOGIC;
signal R0 : STD_LOGIC_VECTOR(3 downto 0):= "0001";
signal R1 : STD_LOGIC_VECTOR(3 downto 0):= "0010";
signal Y : STD_LOGIC_VECTOR(3 downto 0);

begin

UUT:Mux_2_to_1_4bit
port map(
   Sel => Sel,
```

```
R0 => R0,
R1 => R1,
Y => Y
);

process begin

Sel <= '0';

wait for 100ns;

Sel <= '1';

wait for 100ns;

end process;

end Behavioral;
```

3. Timing Diagram



❖ 8-way 4-bit multiplexer

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_8_to_1_4bit is
 Port (
      R0 : in STD_LOGIC_VECTOR(3 downto 0);
      R1 : in STD_LOGIC_VECTOR(3 downto 0);
      R2 : in STD_LOGIC_VECTOR(3 downto 0);
      R3 : in STD_LOGIC_VECTOR(3 downto 0);
      R4 : in STD_LOGIC_VECTOR(3 downto 0);
      R5 : in STD_LOGIC_VECTOR(3 downto 0);
      R6 : in STD_LOGIC_VECTOR(3 downto 0);
      R7 : in STD_LOGIC_VECTOR(3 downto 0);
      Sel : in STD_LOGIC_VECTOR (2 downto 0);
      Y : out STD_LOGIC_VECTOR (3 downto 0));

end Mux_8_to_1_4bit;
```

```
architecture Behavioral of Mux_8_to_1_4bit is

SIGNAL DY: STD_LOGIC_VECTOR(7 downto 0);

begin
   Y <= R0 when Sel="000" else
   R1 when Sel="001" else
   R2 when Sel="010" else
   R3 when Sel="011" else
   R4 when Sel="100" else
   R5 when Sel="101" else
   R6 when Sel="110" else
   R7 when Sel="111" ;

end Behavioral;
```

2. Simulation code

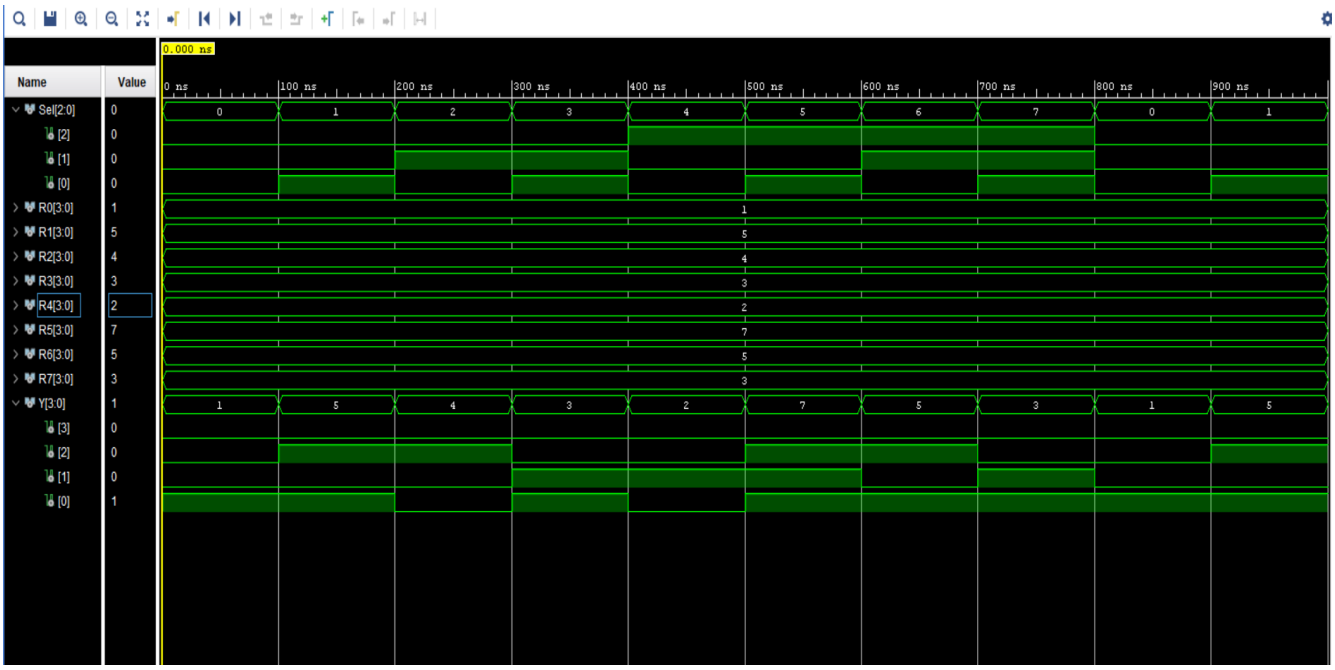
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
```

```
--use UNISIM.VComponents.all;

entity Mux_8_to_1_4bit_sim is
--  Port ( );
end Mux_8_to_1_4bit_sim;

architecture Behavioral of Mux_8_to_1_4bit_sim is

component Mux_8_to_1_4bit is
 Port (
      R0 : in STD_LOGIC_VECTOR(3 downto 0);
      R1 : in STD_LOGIC_VECTOR(3 downto 0);
      R2 : in STD_LOGIC_VECTOR(3 downto 0);
      R3 : in STD_LOGIC_VECTOR(3 downto 0);
      R4 : in STD_LOGIC_VECTOR(3 downto 0);
      R5 : in STD_LOGIC_VECTOR(3 downto 0);
      R6 : in STD_LOGIC_VECTOR(3 downto 0);
      R7 : in STD_LOGIC_VECTOR(3 downto 0);
      Sel : in STD_LOGIC_VECTOR (2 downto 0);
      Y : out STD_LOGIC_VECTOR (3 downto 0));

end component;

            --11 0011 0100 0101 0001 ; 210001R
            --11 0011 0101 0111 0010 ; 210290A

signal Sel: STD_LOGIC_VECTOR(2 downto 0);
signal R0 : STD_LOGIC_VECTOR(3 downto 0):= "0001";
signal R1 : STD_LOGIC_VECTOR(3 downto 0):= "0101";
signal R2 : STD_LOGIC_VECTOR(3 downto 0):= "0100";
signal R3 : STD_LOGIC_VECTOR(3 downto 0):= "0011";
```

```
signal R4 : STD_LOGIC_VECTOR(3 downto 0):= "0010";
signal R5 : STD_LOGIC_VECTOR(3 downto 0):= "0111";
signal R6 : STD_LOGIC_VECTOR(3 downto 0):= "0101";
signal R7 : STD_LOGIC_VECTOR(3 downto 0):= "0011";
signal Y : STD_LOGIC_VECTOR(3 downto 0);

begin

UUT: Mux_8_to_1_4bit
port map(
   Sel => Sel,
   R0 => R0,
   R1 => R1,
   R2 => R2,
   R3 => R3,
   R4 => R4,
   R5 => R5,
   R6 => R6,
   R7 => R7,
   Y => Y
   );

process begin

Sel <= "000";
wait for 100ns;

Sel <= "001";
wait for 100ns;

Sel <= "010";
```

```
wait for 100ns;

Sel <= "011";
wait for 100ns;

Sel <= "100";
wait for 100ns;

Sel <= "101";
wait for 100ns;

Sel <= "110";
wait for 100ns;

Sel <= "111";
wait for 100ns;

end process;
end Behavioral;
```

3. Timing Diagram



❖ 4-bit Register

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
```

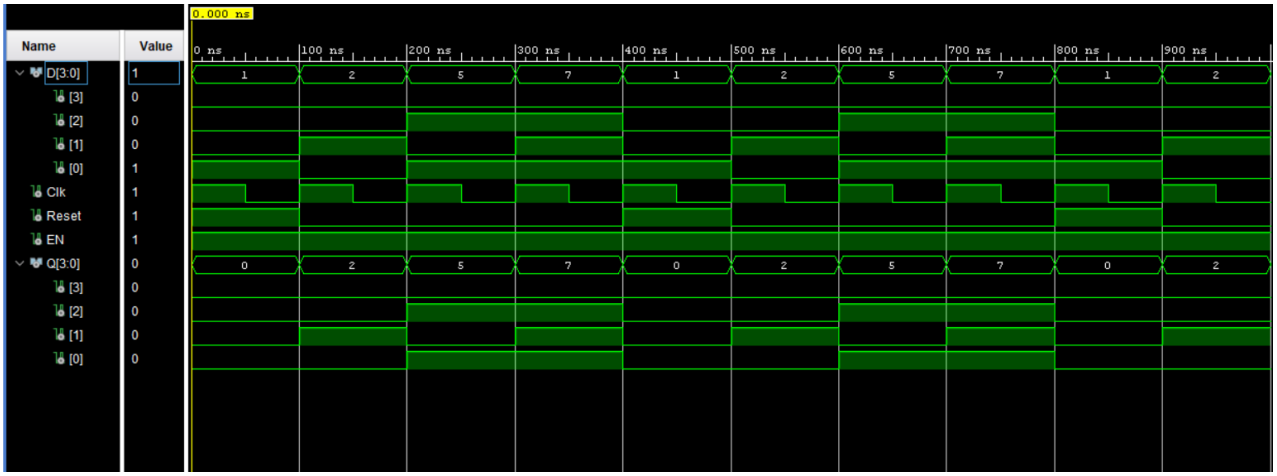
```
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg_4bit is
 Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
        Clk : in STD_LOGIC;
        Reset : in STD_LOGIC;
        EN : in STD_LOGIC;
        Q : out STD_LOGIC_VECTOR (3 downto 0));

    end Reg_4bit;

architecture Behavioral of Reg_4bit is
begin

    process(Clk)
    begin
        if (rising_edge(Clk)) then
            if( Reset = '1') then
                Q <= "0000";
            elsif (EN = '1') then
                Q <= D;
            end if;
        end if;
end process;

end Behavioral;
```

2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg_4bit is
 Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
        Clk : in STD_LOGIC;
        Reset : in STD_LOGIC;
        EN : in STD_LOGIC;
        Q : out STD_LOGIC_VECTOR (3 downto 0));

    end Reg_4bit;

architecture Behavioral of Reg_4bit is
begin

    process(Clk)
    begin
        if (rising_edge(Clk)) then
            if( Reset = '1') then
```

```
            Q <= "0000";
        elsif (EN = '1') then
            Q <= D;
        end if;
    end if;
end process;

end Behavioral;
```

3. Timing Diagram



❖ Register Bank

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg_Bank is
   Port ( EN : in STD_LOGIC;
          D : in STD_LOGIC_VECTOR (3 downto 0);
          Clk : in STD_LOGIC;
          Reset : in STD_LOGIC;
          Reg_En : in STD_LOGIC_VECTOR (2 downto 0);
          R0 : out STD_LOGIC_VECTOR (3 downto 0);
          R1 : out STD_LOGIC_VECTOR (3 downto 0);
          R2 : out STD_LOGIC_VECTOR (3 downto 0);
          R3 : out STD_LOGIC_VECTOR (3 downto 0);
          R4 : out STD_LOGIC_VECTOR (3 downto 0);
          R5 : out STD_LOGIC_VECTOR (3 downto 0);
          R6 : out STD_LOGIC_VECTOR (3 downto 0);
          R7 : out STD_LOGIC_VECTOR (3 downto 0));
```

```
end Reg_Bank;

architecture Behavioral of Reg_Bank is

component Reg_4bit
   Port (  D : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           Reset : in STD_LOGIC;
           EN : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (3 downto 0));

   end component;

component Decoder_3_to_8
   Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
          EN : in STD_LOGIC;
          Y : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal RS : STD_LOGIC_VECTOR(7 downto 0);

begin

Decoder_3_to_8_0 : Decoder_3_to_8
   PORT MAP(
      I => Reg_En,
      EN => EN,
      Y => RS
      );

Reg_4bit_0 : Reg_4bit
```

```
    PORT MAP(
        D => "0000",
        Clk => Clk,
        Reset => Reset,
        EN => RS(0),
        Q => R0
        );

Reg_4bit_1 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
        EN => RS(1),
        Q => R1
        );

Reg_4bit_2 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
        EN => RS(2),
        Q => R2
        );

Reg_4bit_3 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
```

```
        EN => RS(3),
        Q => R3
        );

Reg_4bit_4 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
        EN => RS(4),
        Q => R4
        );

Reg_4bit_5 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
        EN => RS(5),
        Q => R5
        );

Reg_4bit_6 : Reg_4bit
    PORT MAP(
        D => D,
        Clk => Clk,
        Reset => Reset,
        EN => RS(6),
        Q => R6
        );
```

```
Reg_4bit_7 : Reg_4bit
   PORT MAP(
      D => D,
      Clk => Clk,
      Reset => Reset,
      EN => RS(7),
      Q => R7
      );

end Behavioral;
```

2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Reg_Bank_sim is
--  Port ( );
end Reg_Bank_sim;

architecture Behavioral of Reg_Bank_sim is
```

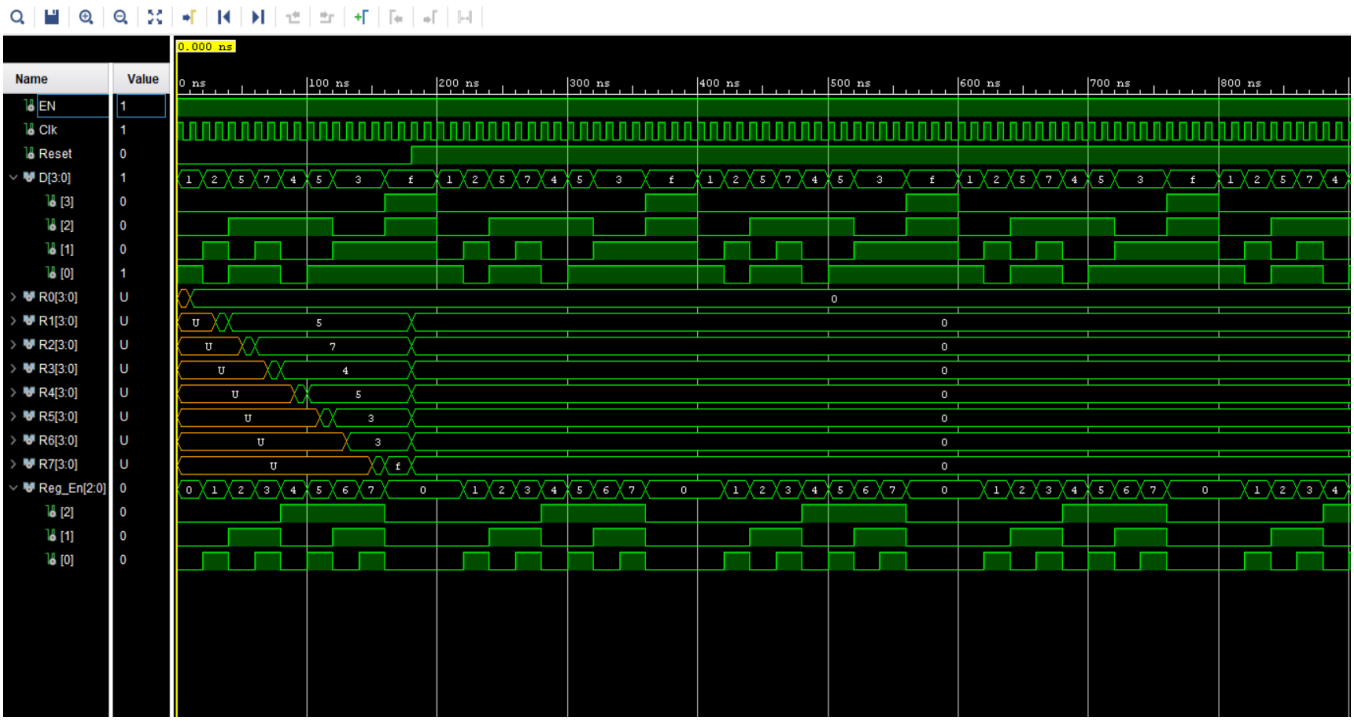
```
component Reg_Bank is
    Port ( EN : in STD_LOGIC;
           D : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           Reset : in STD_LOGIC;
           Reg_En : in STD_LOGIC_VECTOR (2 downto 0);
           R0 : out STD_LOGIC_VECTOR (3 downto 0);
           R1 : out STD_LOGIC_VECTOR (3 downto 0);
           R2 : out STD_LOGIC_VECTOR (3 downto 0);
           R3 : out STD_LOGIC_VECTOR (3 downto 0);
           R4 : out STD_LOGIC_VECTOR (3 downto 0);
           R5 : out STD_LOGIC_VECTOR (3 downto 0);
           R6 : out STD_LOGIC_VECTOR (3 downto 0);
           R7 : out STD_LOGIC_VECTOR (3 downto 0));
end component;

signal EN: STD_LOGIC:='1';
signal Clk: STD_LOGIC:='0';
signal Reset: STD_LOGIC:='0';
signal D,R0,R1,R2,R3,R4,R5,R6,R7:STD_LOGIC_VECTOR (3 downto 0):="0000"; --setting all to 0000
signal Reg_En : STD_LOGIC_VECTOR (2 downto 0);

begin

UUT:Reg_Bank port map(
    Clk => Clk,
    D => D,
    R0 => R0,
    R1 => R1,
    R2 => R2,
```

```
   R3 => R3,
   R4 => R4,
   R5 => R5,
   R6 => R6,
   R7 => R7,
   Reg_EN => Reg_EN,
   Reset => Reset,
   EN => EN
   );

process
begin

Clk <= NOT(Clk);
wait for 5ns;

end process;

process begin

            --11 0011 0100 0101 0001 ; 210001R
            --11 0011 0101 0111 0010 ; 210290A

   D <= "0001"; -- 1
   Reg_EN <= "000"; -- reg0

   wait for 20ns;

   D <= "0010"; -- 2
   Reg_EN <= "001";  -- reg1
```

```
wait for 20ns;

D <= "0101";     --5
Reg_EN <= "010"; -- reg2

wait for 20ns;

D <= "0111"; -- 7
Reg_EN <= "011"; --reg3

wait for 20ns;

D <= "0100"; -- 4
Reg_EN <= "100"; --reg4

wait for 20ns;

D <= "0101"; -- 5
Reg_EN <= "101"; --reg5

wait for 20ns;

D <= "0011"; -- 3
Reg_EN <= "110"; --reg6

wait for 20ns;

D <= "0011"; -- 3
Reg_EN <= "111"; --reg7

wait for 20ns;
```

```
    D <= "1111"; -- 15
    Reg_EN <= "000"; -- reg0

    wait for 20ns;

    Reset <= '1';

    wait for 20ns;

end process;

end Behavioral;
```

3. Timing Diagram



❖ Program Rom

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Prog_Rom is
   Port ( Address : in STD_LOGIC_VECTOR (2 downto 0);
          Ins_Bus : out STD_LOGIC_VECTOR (11 downto 0));
end Prog_Rom;

architecture Behavioral of Prog_Rom is

type rom_type is array(0 to 7) of STD_LOGIC_VECTOR(11 downto 0);
signal Rom_Instruction: rom_type := (

       --instruction set 1

--    "100010000011",-- mov 3 to reg1
--    "100100000001",-- mov 1 to reg2
```

```
--    "010100000000",-- negative of reg2
--    "001110010000",-- adding reg1 to reg7 , store in 1
--    "000010100000",--adding reg2 to reg1 and store in 1
--    "110010000111",--if value in reg1 is 0 pc=7 , else increment pc
--    "110000000011",--
--    "110000000111" --if value in reg0 is 0(always) pc=7 => stay in


        --instruction set2


    "101110000000", -- mov 0 to reg7
    "100010000001", -- mov 1 to reg1
    "100100000010", -- mov 2 to reg2
    "100110000011", -- mov 3 to reg3
    "001110010000", -- add reg 1 and 7 and store in 7 ==> reg7=1
    "001110100000", -- add reg 2 and 7 and store in 7 ==> reg7=3
    "001110110000", -- add reg 3 and 7 and store in 7 ==> reg7=6
    "110000000111" -- if reg 0 is 0 pc=7



    );

begin

    Ins_Bus <= Rom_Instruction(to_integer(unsigned(Address)));



end Behavioral;
```

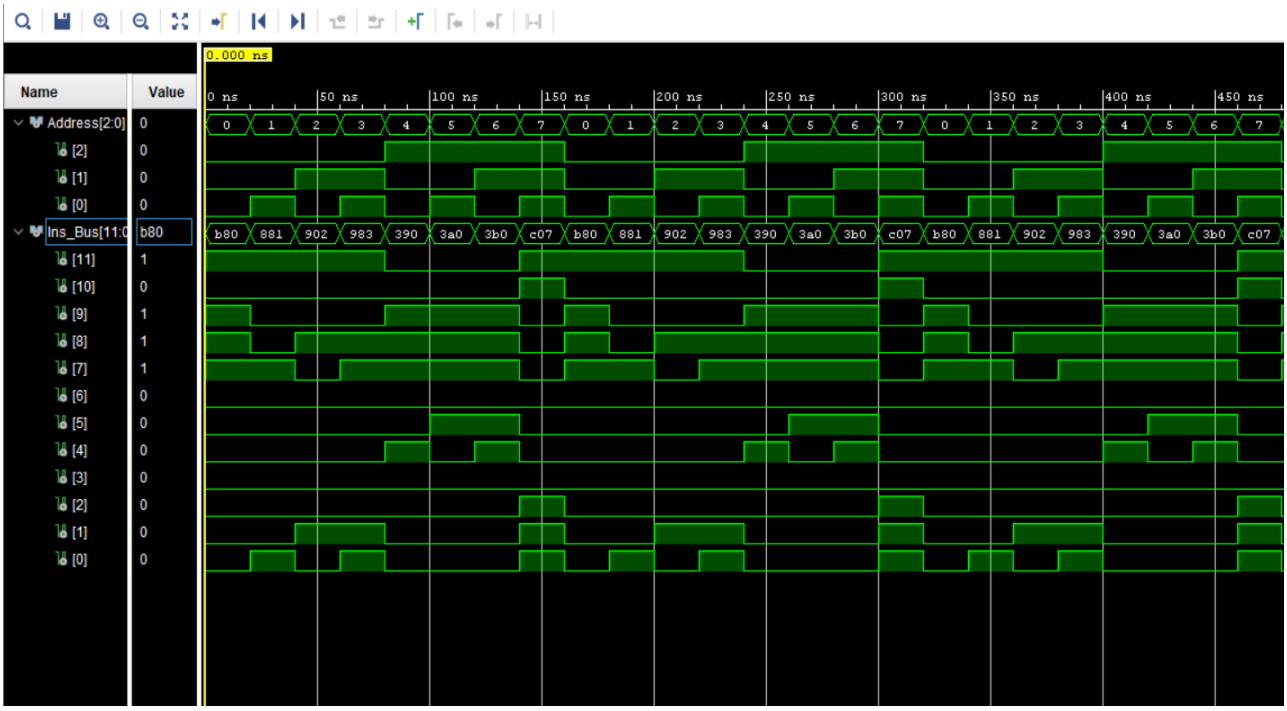
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Prog_Rom_sim is
--  Port ( );
end Prog_Rom_sim;

architecture Behavioral of Prog_Rom_sim is

component Prog_Rom is
   Port ( Address : in STD_LOGIC_VECTOR (2 downto 0);
          Ins_Bus : out STD_LOGIC_VECTOR (11 downto 0));
end component;

signal Address :STD_LOGIC_VECTOR (2 downto 0);
signal Ins_Bus : STD_LOGIC_VECTOR (11 downto 0);

begin
```

```
UUT: Prog_Rom
port map(
   Address => Address,
   Ins_Bus => Ins_Bus
   );

process
begin

Address <= "000";
wait for 20ns;

Address <= "001";
wait for 20ns;

Address <= "010";
wait for 20ns;

Address <= "011";
wait for 20ns;

Address <= "100";
wait for 20ns;

Address <= "101";
wait for 20ns;

Address <= "110";
wait for 20ns;

Address <= "111";
```

wait for 20ns;

3. Timing Diagram



❖ Instruction Decoder

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Ins_Decoder is
   Port ( Ins_Bus : in STD_LOGIC_VECTOR (11 downto 0);
          Reg_Jump_Check : in STD_LOGIC_VECTOR (3 downto 0);
          Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
          AS_Sel : out STD_LOGIC;
          RegS_Mux_A : out STD_LOGIC_VECTOR (2 downto 0);
          RegS_Mux_B : out STD_LOGIC_VECTOR (2 downto 0);
          Immediate_Value :out STD_LOGIC_Vector(3 downto 0);
          Load_Sel : out STD_LOGIC;
          Jump_Flag : out STD_LOGIC;
          Jump_Address : out STD_LOGIC_VECTOR (2 downto 0));
end Ins_Decoder;

architecture Behavioral of Ins_Decoder is
```

```
signal Instruction : STD_LOGIC_VECTOR(1 downto 0);
signal Reg_1,Reg_2 : STD_LOGIC_VECTOR(2 downto 0);
signal Data : STD_LOGIC_VECTOR(3 downto 0);

begin

process(Instruction,Reg_1,Reg_2, Reg_Jump_Check,Data,Data(2 downto 0))

begin

 --initialize jump to 0
       Jump_Flag <='0';
       Reg_EN <= "000";
       if (Instruction = "00") then --ADDITION
          AS_Sel <= '0';
          RegS_Mux_A <= Reg_1;
          RegS_Mux_B <= Reg_2;
           --TIME FOR ATITHMETIC OPERATION

          Reg_En <= Reg_1;



          Load_Sel<= '0';  --MUX SELECTOR



       elsif (Instruction = "10") then --MOVE
          Immediate_Value <=Data;
          Reg_En <= Reg_1;
          Load_Sel<= '1';  --MUX SELECTOR
```

```
    elsif (Instruction = "01") then --NEGATION
       RegS_Mux_A <= "000";
       RegS_Mux_B <= Reg_1;
        --TIME FOR ATITHMETIC OPERATION
       Reg_En <= Reg_1;
       AS_Sel <= '1';
       Load_Sel<= '0';  --MUX SELECTOR



    elsif (Instruction = "11") then --JUMPZ
       RegS_Mux_A <= Reg_1;
       if (Reg_Jump_Check="0000") then
          Jump_Flag <='1';
          Jump_Address <=Data(2 downto 0);
          Load_Sel<= '0';  --MUX SELECTOR

       end if;
    end if;



end process;

Instruction <= Ins_Bus(11 downto 10);
Reg_1 <= Ins_Bus(9 downto 7);
Reg_2 <= Ins_Bus(6 downto 4);
Data<= Ins_Bus(3 downto 0);

end Behavioral;
```

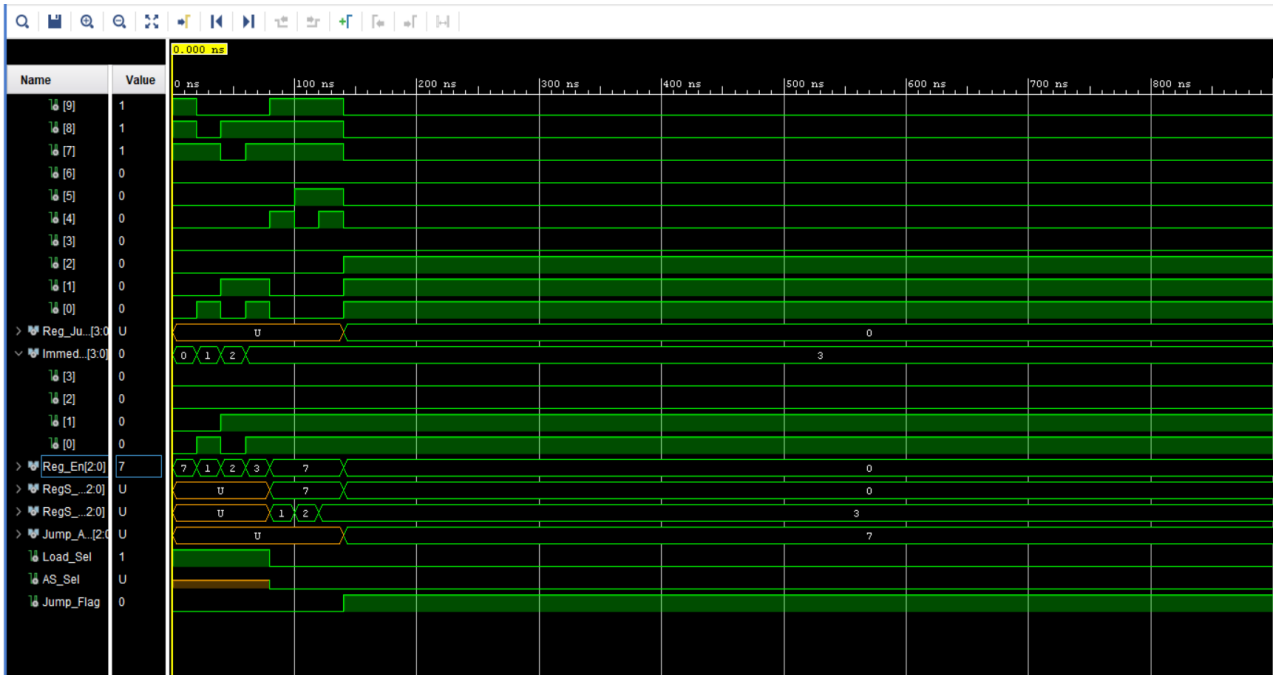
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Ins_decoder_sim is
--  Port ( );
end Ins_decoder_sim;

architecture Behavioral of Ins_decoder_sim is

component Ins_Decoder is
    Port ( Ins_Bus : in STD_LOGIC_VECTOR (11 downto 0);
           Reg_Jump_Check : in STD_LOGIC_VECTOR (3 downto 0);
           Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
           AS_Sel : out STD_LOGIC;
           RegS_Mux_A : out STD_LOGIC_VECTOR (2 downto 0);
           RegS_Mux_B : out STD_LOGIC_VECTOR (2 downto 0);
           Immediate_Value :out STD_LOGIC_Vector(3 downto 0);
           Load_Sel : out STD_LOGIC;
           Jump_Flag : out STD_LOGIC;
```

```
        Jump_Address : out STD_LOGIC_VECTOR (2 downto 0));
end component;

signal Ins_Bus : STD_LOGIC_VECTOR(11 downto 0);
signal Reg_Jump_Check,Immediate_Value : STD_LOGIC_VECTOR(3 downto 0);
signal Reg_En, RegS_Mux_A,RegS_Mux_B, Jump_Address : STD_LOGIC_VECTOR(2 downto 0);
signal Load_Sel, AS_Sel, Jump_Flag : STD_LOGIC;

begin

uut:Ins_Decoder
   port map(
        Ins_Bus => Ins_Bus,
        Reg_Jump_Check => Reg_Jump_Check,
        Reg_En => Reg_En,
        Load_Sel => Load_Sel,
        Immediate_Value => Immediate_Value,
        RegS_Mux_A  => RegS_Mux_A,
        RegS_Mux_B => RegS_Mux_B,
        AS_Sel => AS_Sel,
        Jump_Flag => Jump_Flag,
        Jump_Address => Jump_Address
   );

   process
   begin
      Ins_Bus <= "101110000000";
      wait for 20 ns;

      Ins_Bus <= "100010000001";
       wait for 20 ns;
```

```
Ins_Bus <= "100100000010";
   wait for 20 ns;

Ins_Bus <= "100110000011";
wait for 20 ns;

Ins_Bus <= "001110010000";
wait for 20 ns;

Ins_Bus <=  "001110100000";
wait for 20 ns;


Ins_Bus <=  "001110110000";
wait for 20 ns;

Ins_Bus <= "110000000111";
Reg_Jump_Check <= "0000";
wait for 20 ns;
```

3. Timing Diagram



❖ Nanoprocessor

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Nanoprocessor_4bit is
    Port ( Clk_in : in STD_LOGIC;
           Reset : in STD_LOGIC;
           Overflow : out STD_LOGIC;
           Zero : out STD_LOGIC;
           R7_out : out STD_LOGIC_VECTOR (3 downto 0));
end Nanoprocessor_4bit;

architecture Behavioral of Nanoprocessor_4bit is

component Reg_Bank is
    Port ( EN : in STD_LOGIC;
           D : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
```

```
        Reset : in STD_LOGIC;
        Reg_En : in STD_LOGIC_VECTOR (2 downto 0);
        R0 : out STD_LOGIC_VECTOR (3 downto 0);
        R1 : out STD_LOGIC_VECTOR (3 downto 0);
        R2 : out STD_LOGIC_VECTOR (3 downto 0);
        R3 : out STD_LOGIC_VECTOR (3 downto 0);
        R4 : out STD_LOGIC_VECTOR (3 downto 0);
        R5 : out STD_LOGIC_VECTOR (3 downto 0);
        R6 : out STD_LOGIC_VECTOR (3 downto 0);
        R7 : out STD_LOGIC_VECTOR (3 downto 0));
end component;

component Mux_8_to_1_4bit
    Port (
        R0 : in STD_LOGIC_VECTOR(3 downto 0);
        R1 : in STD_LOGIC_VECTOR(3 downto 0);
        R2 : in STD_LOGIC_VECTOR(3 downto 0);
        R3 : in STD_LOGIC_VECTOR(3 downto 0);
        R4 : in STD_LOGIC_VECTOR(3 downto 0);
        R5 : in STD_LOGIC_VECTOR(3 downto 0);
        R6 : in STD_LOGIC_VECTOR(3 downto 0);
        R7 : in STD_LOGIC_VECTOR(3 downto 0);
        Sel : in STD_LOGIC_VECTOR (2 downto 0);
        Y : out STD_LOGIC_VECTOR (3 downto 0));
end component;

component ASUnit_4 is

    Port ( A : in STD_LOGIC_VECTOR(3 downto 0);
        B : in STD_LOGIC_VECTOR(3 downto 0);
        C  : in STD_LOGIC;
```

```
        S : out STD_LOGIC_VECTOR(3 downto 0);
        Overflow,Zero : out STD_LOGIC);
end component;

component Mux_2_to_1_4bit is
    Port ( Sel : in STD_LOGIC;
           R0 : in STD_LOGIC_VECTOR (3 downto 0);
           R1 : in STD_LOGIC_VECTOR (3 downto 0);
           Y : out STD_LOGIC_VECTOR (3 downto 0));
end component;

component Ins_Decoder is
    Port ( Ins_Bus : in STD_LOGIC_VECTOR (11 downto 0);
           Reg_Jump_Check : in STD_LOGIC_VECTOR (3 downto 0);
           Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
           AS_Sel : out STD_LOGIC;
           RegS_Mux_A : out STD_LOGIC_VECTOR (2 downto 0);
           RegS_Mux_B : out STD_LOGIC_VECTOR (2 downto 0);
           Immediate_Value :out STD_LOGIC_Vector(3 downto 0);
           Load_Sel : out STD_LOGIC;
           Jump_Flag : out STD_LOGIC;
           Jump_Address : out STD_LOGIC_VECTOR (2 downto 0));
end component;

component Adder_3 is

  Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
       B : in STD_LOGIC_VECTOR (2 downto 0);
       S : out STD_LOGIC_VECTOR (2 downto 0);
       Carry_in : in STD_LOGIC;
       Carry_out : out STD_LOGIC);
```

```
end component;

component Mux_2_to_1_3bit is
    Port (
        R0 : in STD_LOGIC_VECTOR(2 downto 0);
        R1 : in STD_LOGIC_VECTOR(2 downto 0);
        Sel : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR (2 downto 0));
end component;

component PC_3bit is

 Port ( D : in STD_LOGIC_VECTOR (2 downto 0);
        Clk : in STD_LOGIC;
        Clr : in STD_LOGIC;
        Q : out STD_LOGIC_VECTOR (2 downto 0));
end component;

component Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end component;

component Prog_Rom is
    Port ( Address : in STD_LOGIC_VECTOR (2 downto 0);
           Ins_Bus : out STD_LOGIC_VECTOR (11 downto 0));
end component;
 -- For the Register Bank
signal Mux_Reg_Bank: STD_LOGIC_VECTOR (3 downto 0);
signal Decoder_Reg_Bank: STD_LOGIC_VECTOR (2 downto 0);
```

```
signal Reg_0_out, Reg_1_out, Reg_2_out, Reg_3_out, Reg_4_out, Reg_5_out, Reg_6_out, Reg_7_out:
STD_LOGIC_VECTOR (3 downto 0);

--  For the Mux_8_way_4_Bit

signal Reg_Sel_0,Reg_Sel_1: STD_LOGIC_VECTOR (2 downto 0);

signal Reg_Sel_0_out,Reg_Sel_1_out: STD_LOGIC_VECTOR (3 downto 0);

 -- For the AddSubUnit_4

signal AddSubSel: STD_LOGIC;

signal AddSubOut: STD_LOGIC_VECTOR (3 downto 0);

 -- For the Mux_2_way_4_Bit

signal Immediate_Value: STD_LOGIC_VECTOR (3 downto 0);

signal Mux_Decoder_Sel: STD_LOGIC;

 -- For the Instruction Decoder

signal Rom_out: STD_LOGIC_VECTOR (11 downto 0);

signal JumpAddress: STD_LOGIC_VECTOR (2 downto 0);

signal JumpFlag: STD_LOGIC;

 -- For the Bit_3_adder

signal Bit_3_adder_out: STD_LOGIC_VECTOR (2 downto 0);

-- For the Program Counter

signal PC_in,PC_out: STD_LOGIC_VECTOR (2 downto 0);


signal Clk: STD_LOGIC;




begin

Slow_Clk_0: Slow_Clk

Port Map(

      Clk_in => Clk_in,

      Clk_out => Clk

);
```

```
Reg_Bank_0: Reg_Bank
Port Map(
    Clk => Clk,
    D => Mux_Reg_Bank,
    Reg_EN => Decoder_Reg_Bank,
    R0 => Reg_0_out,
    R1 => Reg_1_out,
    R2 => Reg_2_out,
    R3 => Reg_3_out,
    R4 => Reg_4_out,
    R5 => Reg_5_out,
    R6 => Reg_6_out,
    R7 => Reg_7_out,
    Reset => Reset,
    EN => '1'
);

Mux_8_to_1_4bit_0: Mux_8_to_1_4bit
Port Map(
      R0 => Reg_0_out,
      R1 => Reg_1_out,
      R2 => Reg_2_out,
      R3 => Reg_3_out,
      R4 => Reg_4_out,
      R5 => Reg_5_out,
      R6 => Reg_6_out,
      R7 => Reg_7_out,
      Sel  => Reg_Sel_0,
      Y => Reg_Sel_0_out
      --EN => '1'
);
```

```
Mux_8_to_1_4bit_1: Mux_8_to_1_4bit
Port Map(
        R0 => Reg_0_out,
        R1 => Reg_1_out,
        R2 => Reg_2_out,
        R3 => Reg_3_out,
        R4 => Reg_4_out,
        R5 => Reg_5_out,
        R6 => Reg_6_out,
        R7 => Reg_7_out,
        Sel  => Reg_Sel_1,
        Y => Reg_Sel_1_out
        --EN => '1'
);

ASunit_4_0:ASUnit_4
Port Map(
        A => Reg_Sel_0_out,
        B => Reg_Sel_1_out,
        C => AddSubSel,
        S => AddSubOut,
        Overflow => Overflow,
        Zero => Zero
        --C_out => C_out
);

Mux_2_to_1_4bit_0 : Mux_2_to_1_4bit
Port Map(
        R0 => AddSubOut,
        R1 => Immediate_Value,
```

```
        Y => Mux_Reg_Bank,
        Sel => Mux_Decoder_Sel
        --EN => '1'
    );

Ins_Decoder_0 : Ins_Decoder
Port Map (
        Ins_Bus => Rom_out,
        Reg_Jump_Check =>Reg_Sel_0_out,
        Reg_En => Decoder_Reg_Bank,
        Load_Sel => Mux_Decoder_Sel,
        Immediate_Value => Immediate_Value,
        RegS_Mux_A => Reg_Sel_0,
        RegS_Mux_B => Reg_Sel_1,
        AS_Sel => AddSubSel,
        Jump_Flag => JumpFlag,
        Jump_Address =>JumpAddress
);

Adder_3_0: Adder_3
Port Map (
      A => PC_out,
      B => "001",
      S => Bit_3_adder_out,
      Carry_in => '0'
--      Carry_out =>  -- Not mapped
);

Mux_2_to_1_3bit_0:Mux_2_to_1_3bit
Port Map(
        R0 => Bit_3_adder_out,
```

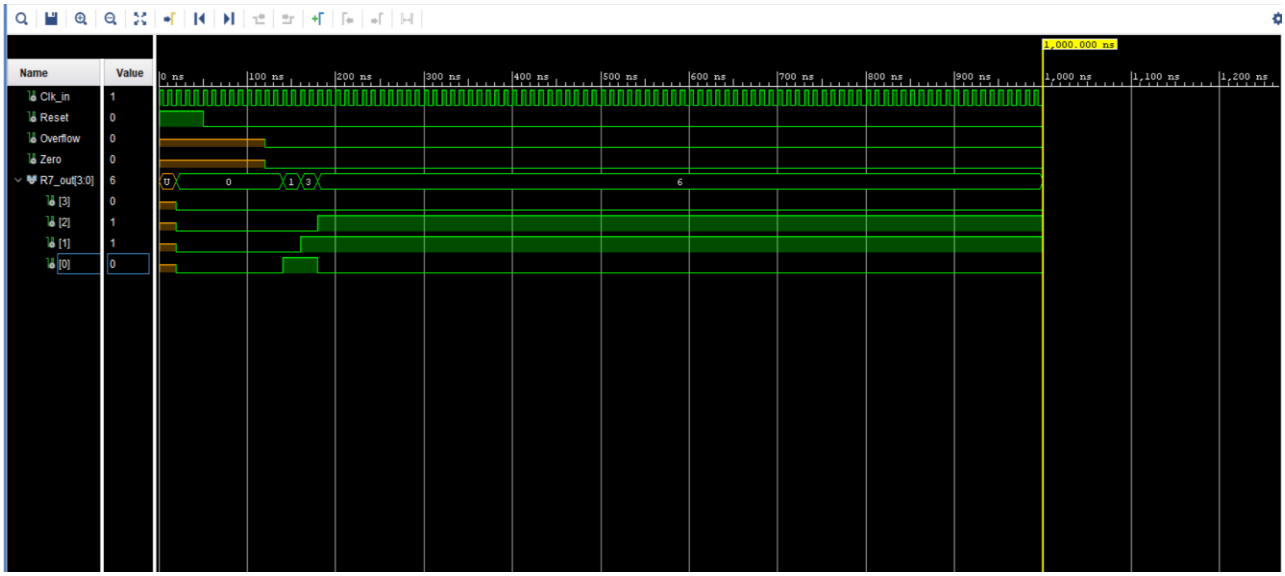
```
        R1 => JumpAddress,
        Y => PC_in,
        Sel => JumpFlag
        --EN => '1'
);

PC_3bit_0: PC_3bit
Port Map(
        D => PC_in,
        Q => PC_out,
        clr => Reset,
        Clk => Clk
);

Prog_ROM_0:Prog_ROM
Port Map(
        Address => PC_out,
        Ins_Bus => Rom_out
);

R7_out <= Reg_7_out;

end Behavioral;
```

2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Nanoprocessor_4bit_sim is
--  Port ( );
end Nanoprocessor_4bit_sim;

architecture Behavioral of Nanoprocessor_4bit_sim is

component Nanoprocessor_4bit is
    Port ( Clk_in : in STD_LOGIC;
           Reset : in STD_LOGIC;
           Overflow : out STD_LOGIC;
           Zero : out STD_LOGIC;
           R7_out : out STD_LOGIC_VECTOR (3 downto 0));
end component;

signal Clk_in,Reset,Overflow,Zero : STD_LOGIC:='0';
signal R7_out :STD_LOGIC_VECTOR (3 downto 0);
```

```
begin

UUT:Nanoprocessor_4bit
port map(
        R7_out=>R7_out,
        Clk_in => Clk_in,
        Overflow => Overflow,
        Zero => Zero,
        Reset => Reset
        );

process
begin
        Clk_in <= not Clk_in;
        wait for 5ns;
        end process;

process
begin
        Reset <= '1';
        wait for 50ns;

        Reset <= '0';
        wait for 3000ns;
```

3. Timing Diagram



❖ Lookup table

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity LUT_16_7 is
   Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
          data : out STD_LOGIC_VECTOR (6 downto 0));
end LUT_16_7;

architecture Behavioral of LUT_16_7 is

type rom_type is array (0 to 15) of std_logic_vector (6 downto 0);

   signal sevenSegment_ROM: rom_type := (

              "1000000", --0
              "1111001", --1
```

```
        "0100100", --2
        "0110000", --3
        "0011001", --4
        "0010010", --5
        "0000010", --6
        "1111000", --7
        "0000000", --8
        "0010000", --9
        "0001000", --a
        "0000011", --b
        "1000110", --c
        "0100001", --d
        "0000110", --e
        "0001110" --f
    );

begin

data <= sevenSegment_ROM(to_integer(unsigned(address)));

end Behavioral;
```

❖ Final Project

1. Source code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Final_Project is
   Port ( Clk_in : in STD_LOGIC;
      Reset : in STD_LOGIC;
      Overflow : out STD_LOGIC;
      Zero : out STD_LOGIC;
      R7_out : out STD_LOGIC_VECTOR (3 downto 0);
      Sev_Seg_Out:out STD_LOGIC_VECTOR (6 downto 0);
      an : out STD_LOGIC_VECTOR (3 downto 0)
      );

end Final_Project;

architecture Behavioral of Final_Project is
```

```
component LUT_16_7
   Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
      data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

component Nanoprocessor_4bit
   Port ( Clk_in : in STD_LOGIC;
      Reset : in STD_LOGIC;
      Overflow : out STD_LOGIC;
      Zero : out STD_LOGIC;
      R7_out : out STD_LOGIC_VECTOR (3 downto 0));
end component;


signal Reg_7_Out: STD_LOGIC_VECTOR (3 downto 0);


begin
LUT_16_7_0:LUT_16_7
   Port Map(
       address => Reg_7_Out,
       data => Sev_Seg_Out
   );

Nanoprocessor_4bit_0:Nanoprocessor_4bit
   Port Map(
      Clk_in =>Clk_in,
      Reset  =>Reset,
      Overflow =>Overflow,
      Zero =>Zero,
      R7_out  => Reg_7_Out
```

```
  );
an<="1110";
R7_out<=Reg_7_Out;
end Behavioral;
```

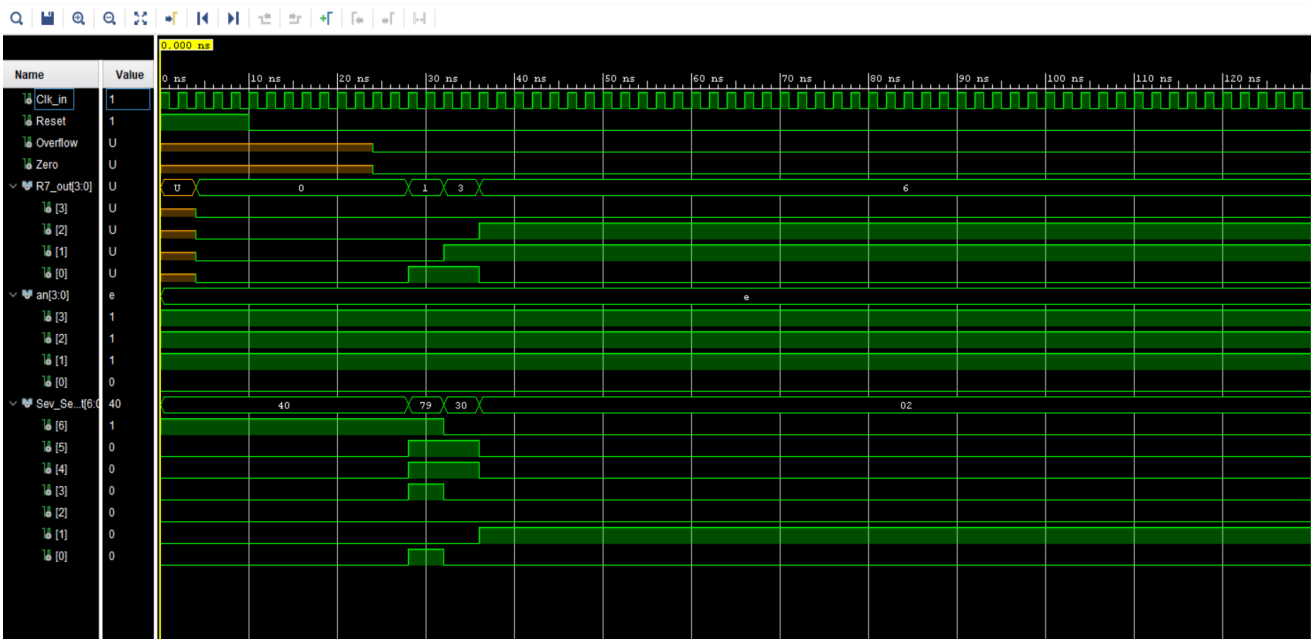
2. Simulation code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Final_Project_sim is
--  Port ( );
end Final_Project_sim;

architecture Behavioral of Final_Project_sim is
   component Final_Project
      Port ( Clk_in : in STD_LOGIC;
           Reset : in STD_LOGIC;
           Overflow : out STD_LOGIC;
           Zero : out STD_LOGIC;
           R7_out : out STD_LOGIC_VECTOR (3 downto 0);
```

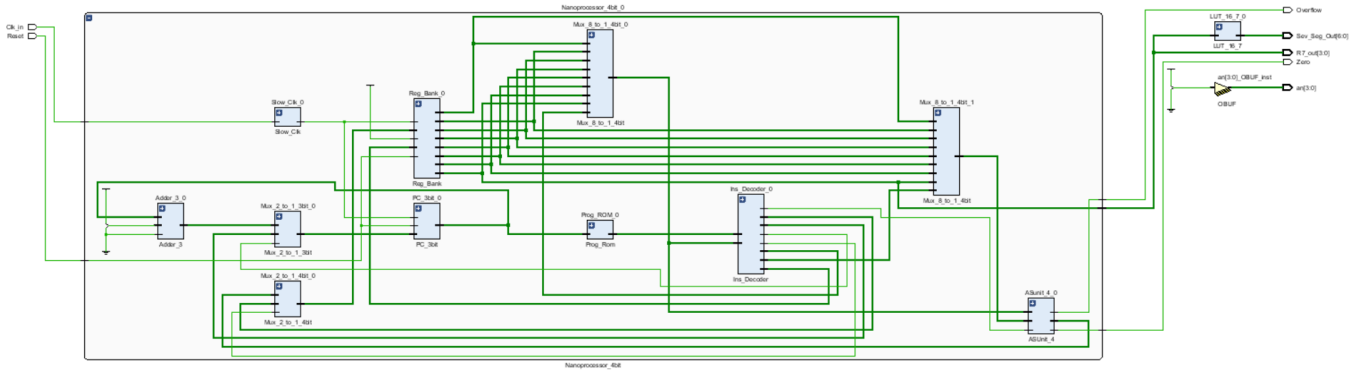
```
            Sev_Seg_Out:out STD_LOGIC_VECTOR (6 downto 0);
            an : out STD_LOGIC_VECTOR (3 downto 0)
            );
    end component;

    signal Clk_in: STD_LOGIC:='0';
    signal Reset,Overflow,Zero:  STD_LOGIC;
    signal R7_out,an :  STD_LOGIC_VECTOR (3 downto 0);
    signal Sev_Seg_Out: STD_LOGIC_VECTOR (6 downto 0);


begin
    uut:Final_Project
     port map(
            Clk_in =>Clk_in,
            Reset => Reset,
            Overflow => Overflow,
            Zero => Zero,
            R7_out => R7_out,
            Sev_Seg_Out => Sev_Seg_Out,
            an => an
    );

    process
    begin
        Clk_in <= not(Clk_in);
        wait for 1ns;
    end process;

    process
    begin
```

```
        Reset<='1';
        wait for 10ns;
        Reset<='0';
        wait;
    end process;



end Behavioral;
```

3. Timing Diagram



Elaborated Design:



Synthesis Report:

#---

Vivado v2018.1 (64-bit)

SW Build 2188600 on Wed Apr 4 18:40:38 MDT 2018

IP Build 2185939 on Wed Apr 4 20:55:05 MDT 2018

Start of session at: Sun Jun 11 16:51:37 2023

Process ID: 17664

Current directory: C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.runs/synth_1

Command line: vivado.exe -log Final_Project.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source Final_Project.tcl

Log file: C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.runs/synth_1/Final_Project.vds

Journal file: C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.runs/synth_1\vivado.jou

#---

source Final_Project.tcl -notrace

Command: synth_design -top Final_Project -part xc7a35tcpg236-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 8804

Starting RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:07 . Memory (MB): peak = 384.012 ; gain = 97.230

INFO: [Synth 8-638] synthesizing module 'Final_Project' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Final_Project.vhd:46]

INFO: [Synth 8-3491] module 'LUT_16_7' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/LUT_16_7.vhd:34' bound to instance 'LUT_16_7_0' of component 'LUT_16_7' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Final_Project.vhd:66]

INFO: [Synth 8-638] synthesizing module 'LUT_16_7' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/LUT_16_7.vhd:39]

INFO: [Synth 8-256] done synthesizing module 'LUT_16_7' (1#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/LUT_16_7.vhd:39]

INFO: [Synth 8-3491] module 'Nanoprocessor_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:34' bound to instance 'Nanoprocessor_4bit_0' of component 'Nanoprocessor_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Final_Project.vhd:72]

INFO: [Synth 8-638] synthesizing module 'Nanoprocessor_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:42]

INFO: [Synth 8-3491] module 'Slow_Clk' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Slow_Clk.vhd:34' bound to instance 'Slow_Clk_0' of component 'Slow_Clk' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:165]

INFO: [Synth 8-638] synthesizing module 'Slow_Clk' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Slow_Clk.vhd:39]

INFO: [Synth 8-256] done synthesizing module 'Slow_Clk' (2#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Slow_Clk.vhd:39]

INFO: [Synth 8-3491] module 'Reg_Bank' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:34' bound to instance 'Reg_Bank_0' of component 'Reg_Bank' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:171]

INFO: [Synth 8-638] synthesizing module 'Reg_Bank' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:50]

INFO: [Synth 8-3491] module 'Decoder_3_to_8' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:34' bound to instance 'Decoder_3_to_8_0' of component 'Decoder_3_to_8' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:71]

INFO: [Synth 8-638] synthesizing module 'Decoder_3_to_8' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:40]

INFO: [Synth 8-3491] module 'Decoder_2_to_4' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:34' bound to instance 'Decoder_2_to_4_0' of component 'Decoder_2_to_4' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:56]

INFO: [Synth 8-638] synthesizing module 'Decoder_2_to_4' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:40]

INFO: [Synth 8-256] done synthesizing module 'Decoder_2_to_4' (3#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:40]

INFO: [Synth 8-3491] module 'Decoder_2_to_4' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:34' bound to instance 'Decoder_2_to_4_1' of component 'Decoder_2_to_4' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:63]

INFO: [Synth 8-256] done synthesizing module 'Decoder_3_to_8' (4#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:40]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_0' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:78]

INFO: [Synth 8-638] synthesizing module 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:43]

INFO: [Synth 8-256] done synthesizing module 'Reg_4bit' (5#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:43]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_1' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:87]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_2' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:96]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_3' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:105]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_4' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:114]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_5' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:123]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_6' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:132]

INFO: [Synth 8-3491] module 'Reg_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_4bit.vhd:34' bound to instance 'Reg_4bit_7' of component 'Reg_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:141]

INFO: [Synth 8-256] done synthesizing module 'Reg_Bank' (6#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Reg_Bank.vhd:50]

INFO: [Synth 8-3491] module 'Mux_8_to_1_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_8_to_1_4bit.vhd:34' bound to instance 'Mux_8_to_1_4bit_0' of component 'Mux_8_to_1_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:188]

INFO: [Synth 8-638] synthesizing module 'Mux_8_to_1_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_8_to_1_4bit.vhd:50]

INFO: [Synth 8-256] done synthesizing module 'Mux_8_to_1_4bit' (7#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_8_to_1_4bit.vhd:50]

INFO: [Synth 8-3491] module 'Mux_8_to_1_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_8_to_1_4bit.vhd:34' bound to instance 'Mux_8_to_1_4bit_1' of component 'Mux_8_to_1_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:203]

INFO: [Synth 8-3491] module 'ASUnit_4' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:34' bound to instance 'ASunit_4_0' of component 'ASUnit_4' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:218]

INFO: [Synth 8-638] synthesizing module 'ASUnit_4' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:45]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_0' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:66]

INFO: [Synth 8-638] synthesizing module 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:42]

INFO: [Synth 8-3491] module 'HA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/HA.vhd:34' bound to instance 'HA_0' of component 'HA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:59]

INFO: [Synth 8-638] synthesizing module 'HA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/HA.vhd:41]

INFO: [Synth 8-256] done synthesizing module 'HA' (8#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/HA.vhd:41]

INFO: [Synth 8-3491] module 'HA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/HA.vhd:34' bound to instance 'HA_1' of component 'HA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:66]

INFO: [Synth 8-256] done synthesizing module 'FA' (9#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:42]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_1' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:74]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_2' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:82]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_3' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:90]

INFO: [Synth 8-256] done synthesizing module 'ASUnit_4' (10#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/ASUnit_4.vhd:45]

INFO: [Synth 8-3491] module 'Mux_2_to_1_4bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_4bit.vhd:34' bound to instance 'Mux_2_to_1_4bit_0' of component 'Mux_2_to_1_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:229]

INFO: [Synth 8-638] synthesizing module 'Mux_2_to_1_4bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_4bit.vhd:42]

INFO: [Synth 8-256] done synthesizing module 'Mux_2_to_1_4bit' (11#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_4bit.vhd:42]

INFO: [Synth 8-3491] module 'Ins_Decoder' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:34' bound to instance 'Ins_Decoder_0' of component 'Ins_Decoder' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:238]

INFO: [Synth 8-638] synthesizing module 'Ins_Decoder' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:47]

INFO: [Synth 8-256] done synthesizing module 'Ins_Decoder' (12#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:47]

INFO: [Synth 8-3491] module 'Adder_3' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:34' bound to instance 'Adder_3_0' of component 'Adder_3' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:252]

INFO: [Synth 8-638] synthesizing module 'Adder_3' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:42]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_0' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:52]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_1' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:60]

INFO: [Synth 8-3491] module 'FA' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA_2' of component 'FA' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:68]

INFO: [Synth 8-256] done synthesizing module 'Adder_3' (13#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Adder_3.vhd:42]

INFO: [Synth 8-3491] module 'Mux_2_to_1_3bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_3bit.vhd:34' bound to instance 'Mux_2_to_1_3bit_0' of component 'Mux_2_to_1_3bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:261]

INFO: [Synth 8-638] synthesizing module 'Mux_2_to_1_3bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_3bit.vhd:43]

INFO: [Synth 8-256] done synthesizing module 'Mux_2_to_1_3bit' (14#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_2_to_1_3bit.vhd:43]

INFO: [Synth 8-3491] module 'PC_3bit' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:34' bound to instance 'PC_3bit_0' of component 'PC_3bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:270]

INFO: [Synth 8-638] synthesizing module 'PC_3bit' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:43]

INFO: [Synth 8-3491] module 'D_FF' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:34' bound to instance 'D_FF_0' of component 'D_FF' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:54]

INFO: [Synth 8-638] synthesizing module 'D_FF' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:42]

INFO: [Synth 8-256] done synthesizing module 'D_FF' (15#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:42]

INFO: [Synth 8-3491] module 'D_FF' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:34' bound to instance 'D_FF_1' of component 'D_FF' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:61]

INFO: [Synth 8-3491] module 'D_FF' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:34' bound to instance 'D_FF_2' of component 'D_FF' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:68]

INFO: [Synth 8-256] done synthesizing module 'PC_3bit' (16#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/PC_3bit.vhd:43]

INFO: [Synth 8-3491] module 'Prog_Rom' declared at 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Prog_Rom.vhd:34' bound to instance 'Prog_ROM_0' of component 'Prog_Rom' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:278]

INFO: [Synth 8-638] synthesizing module 'Prog_Rom' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Prog_Rom.vhd:39]

INFO: [Synth 8-256] done synthesizing module 'Prog_Rom' (17#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Prog_Rom.vhd:39]

INFO: [Synth 8-256] done synthesizing module 'Nanoprocessor_4bit' (18#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Nanoprocessor_4bit.vhd:42]

INFO: [Synth 8-256] done synthesizing module 'Final_Project' (19#1) [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Final_Project.vhd:46]

WARNING: [Synth 8-3917] design Final_Project has port an[3] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[2] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[1] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[0] driven by constant 0

Finished RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory (MB): peak = 439.750 ; gain = 152.969

Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 439.750 ; gain = 152.969

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 439.750 ; gain = 152.969

INFO: [Device 21-403] Loading part xc7a35tcpg236-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/constrs_1/new/Basys3.xdc]

Finished Parsing XDC File [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/constrs_1/new/Basys3.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/constrs_1/new/Basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Final_Project_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/Final_Project_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.005 . Memory (MB): peak = 771.184 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:26 ; elapsed = 00:00:34 . Memory (MB): peak = 771.184 ; gain = 484.402

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:26 ; elapsed = 00:00:34 . Memory (MB): peak = 771.184 ; gain = 484.402

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:26 ; elapsed = 00:00:34 . Memory (MB): peak = 771.184 ; gain = 484.402

INFO: [Synth 8-5544] ROM "sevenSegment_ROM" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5545] ROM "count" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "clk_status" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5544] ROM "Jump_Flag" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "AS_Sel" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "AS_Sel" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "Load_Sel" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "Rom_Instruction" won't be mapped to Block RAM because address size (3) smaller than threshold (5)

WARNING: [Synth 8-327] inferring latch for variable 'Y_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Mux_8_to_1_4bit.vhd:55]

WARNING: [Synth 8-327] inferring latch for variable 'AS_Sel_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:63]

WARNING: [Synth 8-327] inferring latch for variable 'RegS_Mux_A_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:64]

WARNING: [Synth 8-327] inferring latch for variable 'RegS_Mux_B_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:65]

WARNING: [Synth 8-327] inferring latch for variable 'Immediate_Value_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:75]

WARNING: [Synth 8-327] inferring latch for variable 'Load_Sel_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:71]

WARNING: [Synth 8-327] inferring latch for variable 'Jump_Address_reg' [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/new/Ins_Decoder.vhd:95]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:27 ; elapsed = 00:00:35 . Memory (MB): peak = 771.184 ; gain = 484.402

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 1

+---XORs :

2 Input 1 Bit XORs := 19

+---Registers :

32 Bit Registers := 1

4 Bit Registers := 8

1 Bit Registers := 8

+---Muxes :

2 Input 32 Bit Muxes := 1

9 Input 12 Bit Muxes := 1

17 Input 7 Bit Muxes := 1

2 Input 4 Bit Muxes := 1

4 Input 3 Bit Muxes := 1

2 Input 3 Bit Muxes := 4

2 Input 1 Bit Muxes := 11

4 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 2

3 Input 1 Bit Muxes := 2

Finished RTL Component Statistics

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module LUT_16_7

Detailed RTL Component Info :

+---Muxes :

17 Input 7 Bit Muxes := 1

Module Slow_Clk

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 1

+---Registers :

32 Bit Registers := 1

1 Bit Registers := 2

+---Muxes :

2 Input 32 Bit Muxes := 1

2 Input 1 Bit Muxes := 1

Module Reg_4bit

Detailed RTL Component Info :

+---Registers :

4 Bit Registers := 1

Module HA

Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 1

Module ASUnit_4

Detailed RTL Component Info :

+---XORs :

2 Input 1 Bit XORs := 5

Module Mux_2_to_1_4bit

Detailed RTL Component Info :

+---Muxes :

2 Input 4 Bit Muxes := 1

Module Ins_Decoder

Detailed RTL Component Info :

+---Muxes :

4 Input 3 Bit Muxes := 1

2 Input 3 Bit Muxes := 3

2 Input 1 Bit Muxes := 10

4 Input 1 Bit Muxes := 1

5 Input 1 Bit Muxes := 2

3 Input 1 Bit Muxes := 2

Module Mux_2_to_1_3bit

Detailed RTL Component Info :

+---Muxes :

2 Input 3 Bit Muxes := 1

Module D_FF

Detailed RTL Component Info :

+---Registers :

1 Bit Registers := 2

Module Prog_Rom

Detailed RTL Component Info :

+---Muxes :

9 Input 12 Bit Muxes := 1

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 90 (col length:60)

BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

Warning: Parallel synthesis criteria is not met

WARNING: [Synth 8-6014] Unused sequential element Nanoprocessor_4bit_0/PC_3bit_0/D_FF_0/Qbar_reg was removed. [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:50]

WARNING: [Synth 8-6014] Unused sequential element Nanoprocessor_4bit_0/PC_3bit_0/D_FF_1/Qbar_reg was removed. [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:50]

WARNING: [Synth 8-6014] Unused sequential element Nanoprocessor_4bit_0/PC_3bit_0/D_FF_2/Qbar_reg was removed. [C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.srcs/sources_1/imports/new/D_FF.vhd:50]

INFO: [Synth 8-5545] ROM "Nanoprocessor_4bit_0/Slow_Clk_0/count" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5545] ROM "Nanoprocessor_4bit_0/Slow_Clk_0/clk_status" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

WARNING: [Synth 8-3917] design Final_Project has port an[3] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[2] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[1] driven by constant 1

WARNING: [Synth 8-3917] design Final_Project has port an[0] driven by constant 0

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Ins_Decoder_0/Immediate_Value_reg[3])

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[0]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[1]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[1]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[2]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[2]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[3]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[3])

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_0/Y_reg[3]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_0/Y_reg[2]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_0/Y_reg[1]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_0/Y_reg[0]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_1/Y_reg[3]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_1/Y_reg[2]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_1/Y_reg[1]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Mux_8_to_1_4bit_1/Y_reg[0]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Ins_Decoder_0/Immediate_Value_reg[3]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_0/Q_reg[3]) is unused and will be removed from module Final_Project.

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:28 ; elapsed = 00:00:37 . Memory (MB): peak = 771.184 ; gain = 484.402

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:37 ; elapsed = 00:00:47 . Memory (MB): peak = 771.184 ; gain = 484.402

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:37 ; elapsed = 00:00:47 . Memory (MB): peak = 786.246 ; gain = 499.465

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

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Start Technology Mapping

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_4/Q_reg[1]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[1]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_5/Q_reg[1]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[1])

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_4/Q_reg[0]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[0]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_5/Q_reg[0]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[0]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[0])

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_4/Q_reg[2]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[2]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_5/Q_reg[2]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[2]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[2])

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_4/Q_reg[3]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[3]'

INFO: [Synth 8-3886] merging instance 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_5/Q_reg[3]' (FDRE) to 'Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[3]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[3])

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[1]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[0]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[2]) is unused and will be removed from module Final_Project.

WARNING: [Synth 8-3332] Sequential element (Nanoprocessor_4bit_0/Reg_Bank_0/Reg_4bit_6/Q_reg[3]) is unused and will be removed from module Final_Project.

Finished Technology Mapping : Time (s): cpu = 00:00:37 ; elapsed = 00:00:47 . Memory (MB): peak = 786.246 ; gain = 499.465

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+----------+----------+---------+

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Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Report Check Netlist:

+------+-----------------+-------+---------+-------+-----------------+

| |Item |Errors |Warnings |Status |Description |

+------+-----------------+-------+---------+-------+-----------------+

|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |

+------+-----------------+-------+---------+-------+-----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Start Writing Synthesis Report

Report BlackBoxes:

+-+--------------+----------+

| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 8|

|3 |LUT1 | 1|

|4 |LUT2 | 1|

|5 |LUT3 | 23|

|6 |LUT4 | 18|

|7 |LUT5 | 15|

|8 |LUT6 | 10|

|9 |MUXF7 | 6|

|10 |FDRE | 53|

|11 |LD | 12|

|12 |LDC | 1|

|13 |IBUF | 2|

|14 |OBUF | 17|

+------+-------+------+

Report Instance Areas:

+------+----------------------+-------------------+------+

| |Instance |Module |Cells |

+------+----------------------+-------------------+------+

|1 |top | | 168|

|2 | Nanoprocessor_4bit_0 |Nanoprocessor_4bit | 148|

|3 | Ins_Decoder_0 |Ins_Decoder | 39|

|4 | PC_3bit_0 |PC_3bit | 24|

|5 | D_FF_0 |D_FF | 13|

|6 | D_FF_1 |D_FF_3 | 3|

|7 | D_FF_2 |D_FF_4 | 8|

|8 | Reg_Bank_0 |Reg_Bank | 31|

|9 | Reg_4bit_1 |Reg_4bit | 4|

|10 | Reg_4bit_2 |Reg_4bit_0 | 4|

|11 | Reg_4bit_3 |Reg_4bit_1 | 12|

|12 | Reg_4bit_7 |Reg_4bit_2 | 11|

|13 | Slow_Clk_0 |Slow_Clk | 54|

+------+----------------------+-------------------+------+

Finished Writing Synthesis Report : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

Synthesis finished with 0 errors, 0 critical warnings and 28 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:24 ; elapsed = 00:00:38 . Memory (MB): peak = 786.246 ; gain = 168.031

Synthesis Optimization Complete : Time (s): cpu = 00:00:38 ; elapsed = 00:00:48 . Memory (MB): peak = 786.246 ; gain = 499.465

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 29 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

A total of 13 instances were transformed.

LD => LDCE: 12 instances

LDC => LDCE: 1 instances

INFO: [Common 17-83] Releasing license: Synthesis

113 Infos, 32 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:40 ; elapsed = 00:00:52 . Memory (MB): peak = 786.305 ; gain = 511.516

INFO: [Common 17-1381] The checkpoint 'C:/Users/Uzma/Desktop/Final/New folder/Lab 9 final/Lab 9 final.runs/synth_1/Final_Project.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file Final_Project_utilization_synth.rpt -pb Final_Project_utilization_synth.pb

report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.031 . Memory (MB): peak = 786.305 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Sun Jun 11 16:52:34 2023...

Conclusions:

- In this lab designed and developed a functional nano-processor that could execute simple assembly instructions like ADD, MOV, NEG and JNZ and display the output value on a seven segment display and a set of LEDs too.
- In attempt to reduce the LUT and Flip Flop count we tried our best to minimize the number of if-else statements and we were able to optimize it as desired.

- In addition we were able to further optimize the design by using a behavioral approach to design the MUXs instead of decoders.
- Initially we faced an issue where our nano-processor was apparently perfectly functioning when simulated, but it failed to display the result on the seven-segment display when tested on Basys3. Later after careful debugging we were able to pinpoint the reason. And it was as we had not assigned a value for load select after a jump instruction. Even though logically it was unnecessary for such an assignment we concluded that in practice it was necessary.

Contribution:

MEMBER	TOTAL HOURS SPENT
AATHIF M.N.M	27
KHAN M.I	25

NAME	DESIGN	HOURS
AATHIF	• 4 bit AddSub unit • Multiplexers • Register bank • Program ROM	1 hour 1 hours 1 hour ½ hour
IYADH	• 3 bit Adder • Program counter • Instruction decoder	1 hour 1 hour 2 hours

Nano processor and Final project:

We worked together to build them and implement taking turns. Totally spending around 4 hours each.

Testing, Debugging and Optimization:

We worked together trying to optimize the design and debug along the way. Total time spent on optimizing and debugging amounted to around 15 hours each.