Assignment 6

Digital Design Verification

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1 Q1: ALSU

1.1 1. Drive Link for Complete Environment

Here is a link to Complete UVM Environment For ALSU Design.

1.2 2. Verification Plan

| Label | Description | Stimulus Generation | Functional Coverage | Functionality Check |
|--------|--|---|---|--|
| ALSU_1 | When the reset is asserted, the outputs should be low. | Directed reset is applied at simulation start via the do_reset() task. Afterwards, the reset signal is randomized with the constraint c_reset_low_prob (5% chance of rst=1). | A covergroup in alsu_rand_class monitors transitions on rst. Coverage bins ensure that enough reset assertions are observed during randomization. | The golden model is invoked during reset to verify that both out and leds are 0. Any deviation (non-zero outputs when rst is high) flags an error. |
| ALSU_2 | In the absence of invalid conditions, when the opcode is ADD, the output should perform addition on ports A and B, incorporating cin if FULL_ADDER is enabled. | The random stimulus is generated with the weighted constraint c_opcode_distribution to ensure frequent selection of ADD (3'h2). Inputs A and B are randomized using c_adder_mult_corner to emphasize corner cases (values MAXNEG, ZERO, MAXPOS). Reduction control signals (red_op_A and red_op_B) are mostly deasserted to avoid invalid conditions. | The covergroup within alsu_rand_class collects data on opcode, A, B, and cin along with other control signals. Specific bins track the occurrence of corner-case operand values and the frequency of the ADD opcode. | After each randomized transaction, the golden_model() task computes the expected output (i.e. A+B plus cin when relevant). The testbench compares the DUT output against the golden model; any mismatch in the computed sum flags an error. |

Table 1: Verification Plan

1.3 3. Do File

vlib work

```
vlog -f src_files.list +cover -covercells
vsim -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover
do wave.do
coverage save ALSU.ucdb -onexit
run -all
do coverage.do

# to run do file
#— do run.do
#to execute coverage report
#— vcover report ALSU.ucdb -details -annotate -all -output code_coverage_rpt.txt -du=ALSU
#— vcover report -details -cvg -output functional_coverage_report.txt ALSU.ucdb
```

1.4 4. functional Coverage Report

Coverage Report by instance with details

=== Instance: /alsu_coverage_pkg == Design Unit: work.alsu_coverage_pkg Covergroup Coverage: 98.38%Covergroups nanaCoverpoints/Crosses 22nananaCovergroup Bins 989192.85%7

| overgroup | ${ m Metric}$ | Goal | $_{ m Bins}$ | Status |
|------------------------|---------------|-----------------------|--------------|--------------------------|
| | 98.38% | 100 | | Uncovered |
| covered/total bins: | 91 | 98 | _ | |
| missing/total bins: | 7 | 98 | _ | |
| % Hit: | 92.85% | 100 | _ | |
| Coverpoint rst_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint cin_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint red_op_A_cp | 100.00% | 100 | _ | $\operatorname{Covered}$ |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint red_op_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |

| | 10000 | 4.0.0 | | |
|--|---|--|---|---|
| Coverpoint bypass_A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint bypass_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint direction_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | Covered |
| missing/total bins: | 0 | $\frac{2}{2}$ | | |
| % Hit: | 100.00% | | _ | |
| | | 100 | _ | |
| Coverpoint serial_in_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| $\operatorname{Coverpoint} A_{\operatorname{-cp}}$ | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | _ | |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | _ | Covered |
| | | | _ | |
| missing/total bins: | 100.0007 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| $\operatorname{Coverpoint} A_\operatorname{cp_mod}$ | 100.00% | 100 | _ | Covered |
| covered/total bins: | 3 | 3 | _ | |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint B_cp_mod | 100.00% | 100 | _ | Covered |
| covered/total bins: | 3 | 3 | _ | |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint ALU_cp | 87.50% | 100 | _ | Uncovered |
| covered/total bins: | | | | Oncovered |
| , | 7 | 8 | _ | |
| missing/total bins: | 1 | 8 | _ | |
| % Hit: | 87.50% | 100 | _ | |
| $Cross \#cross_{-}0\#$ | 100.00% | 100 | _ | Covered |
| covered/total bins: | 8 | 8 | _ | |
| missing/total bins: | 0 | 8 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Cross #cross1# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 18 | 18 | _ | |
| missing/total bins: | 0 | 18 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| $Cross \#cross_{-2}\#$ | 100.00% | 100 | | Covered |
| | | | _ | Covered |
| covered/total bins: | 1 | 1 | _ | |
| missing/total bins: | 0 | 1 | _ | |
| | 100 000 | 100 | | |
| % Hit: | 100.00% | | _ | |
| % Hit: Cross #cross3# | 100.00% | 100 | _ | $\operatorname{Covered}$ |
| | | | _ | Covered |
| Cross #cross3# covered/total bins: | 100.00% | 100 | _ _ _ _ | Covered |
| Cross #cross3# covered/total bins: missing/total bins: | $100.00\% \ 1 \ 0$ | $100\\1\\1$ | _ _ _ _ | Covered |
| Cross #cross3# covered/total bins: missing/total bins: % Hit: | $100.00\% \ 1 \ 0 \ 100.00\%$ | $100 \\ 1 \\ 1 \\ 100$ | _ _ _ _ _ | |
| Cross #cross3# covered/total bins: missing/total bins: % Hit: Cross #cross4# | 100.00% 1 0 $100.00%$ $100.00%$ | 100 1 1 100 100 | | Covered |
| Cross #cross3# covered/total bins: missing/total bins: % Hit: Cross #cross4# covered/total bins: | 100.00% 1 0 $100.00%$ $100.00%$ 1 | 100 1 1 100 100 1 | - - - - - | |
| Cross #cross3# covered/total bins: missing/total bins: % Hit: Cross #cross4# covered/total bins: missing/total bins: | 100.00% 1 0 $100.00%$ $100.00%$ 1 | 100 1 1 100 100 1 1 | - - - - - - | |
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| Cross #cross3# | 100.00% 1 0 100.00% 100.00% 1 0 100.00% 100.00% 1 0 100.00% 1 0 100.00% 1 0 100.00% 1 0 100.00% 20 6 76.92% verage::cg 98.38% 91 7 | 100 1 1 1 100 100 100 1 1 1 100 100 1 1 1 100 100 1 1 1 100 100 26 26 100 100 98 98 | | Covered Covered Covered Uncovered |
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| Cross #cross3# | 100.00% | 100 1 1 1 100 100 100 1 1 1 100 100 100 | | Covered Covered Uncovered Uncovered Covered Covered Covered Covered Covered Covered |
| Cross #cross3# | 100.00% | 100 1 1 1 100 100 100 1 1 1 100 100 1 1 1 100 100 1 1 1 100 100 26 26 26 100 100 26 26 100 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1 | | Covered Covered Uncovered Uncovered Covered Covered Covered Covered Covered Covered Covered |
| Cross #cross3# | 100.00% | 100 1 1 1 100 100 100 1 1 1 100 100 100 | | Covered Covered Uncovered Uncovered Covered Covered Covered Covered Covered Covered Covered |

| Of TIPE | | | | |
|--|---|---|----------------------------|---|
| % Hit: | 100.00% | 100 | _ | |
| $\operatorname{bin} \operatorname{red}_{-}\operatorname{op}_{-}A_{-}0$ | 185 | 1 | _ | Covered |
| bin red_op_A_1 | 815 | 1 | _ | Covered |
| default bin red_op_A_default | 0 | | _ | ZERO |
| Coverpoint red_op_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | $\frac{2}{2}$ | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | Corrored |
| bin red_op_B_0 bin red_op_B_1 | $155 \\ 845$ | 1 1 | _ | Covered Covered |
| default bin red_op_B_default | 0 | 1 | _ | ZERO |
| Coverpoint bypass_A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | Covered |
| missing/total bins: | 0 | $\frac{2}{2}$ | _ | |
| % Hit: | 100.00% | 100 | _ | |
| bin auto [0] | 733 | 1 | _ | Covered |
| bin auto [1] | 267 | 1 | _ | Covered |
| Coverpoint bypass_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| bin auto [0] | 753 | 1 | _ | Covered |
| bin auto[1] | 247 | 1 | _ | Covered |
| Coverpoint direction_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | $\frac{2}{2}$ | $\frac{2}{2}$ | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | $100.00\% \ 534$ | 100 | _ | Covered |
| bin auto[0] | 466 | 1 1 | _ | Covered |
| bin auto[1] Coverpoint serial_in_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | $\frac{100.00\%}{2}$ | $\frac{100}{2}$ | _ | Covered |
| missing/total bins: | 0 | $\frac{2}{2}$ | _ | |
| % Hit: | 100.00% | 100 | | |
| bin auto [0] | 521 | 1 | | Covered |
| bin auto[0] | $\frac{321}{479}$ | 1 | | Covered |
| Coverpoint A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | | Covered |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| bin A_{data_0} | $\frac{263}{263}$ | 1 | _ | Covered |
| bin A_data_max | 150 | 1 | _ | Covered |
| $\operatorname{bin} A_{\operatorname{data}_{-}\operatorname{min}}$ | 130 | 1 | _ | Covered |
| bin A_data_walkingones[1] | 108 | 1 | _ | Covered |
| bin A_data_walkingones[2] | 92 | 1 | _ | Covered |
| default bin A_data_default | 257 | | _ | Occurred |
| $\operatorname{Coverpoint}\ \operatorname{B_cp}$ | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | _ | |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| $\operatorname{bin}\ \mathrm{B_data_0}$ | 257 | 1 | _ | Covered |
| $\operatorname{bin}\ \operatorname{B_data_max}$ | 143 | 1 | _ | $\operatorname{Covered}$ |
| bin B_data_min | 162 | 1 | _ | Covered |
| bin B_data_walkingones[1] | 91 | 1 | _ | Covered |
| bin B_data_walkingones[2] | 97 | 1 | _ | Covered |
| default bin B_data_default | 250 | 100 | _ | Occurred |
| Coverpoint A_cp_mod | 100.00% | 100 | _ | Covered |
| <pre>covered/total bins: missing/total bins:</pre> | 3 0 | 3 | _ | |
| % Hit: | | 3 | | |
| | | 3 | _ | |
| bin A data O | 100.00% | 100 | | Covered |
| bin A_data_0 bin A_data_max | $100.00\% \\ 263$ | $100\\1$ | _ _ _ | Covered Covered |
| $\operatorname{bin} A_{\operatorname{data_max}}$ | $100.00\% \ 263 \ 150$ | $100\\1\\1$ | _ | Covered |
| $egin{array}{ll} egin{array}{ll} egin{array}{ll} A_{ m data_min} \end{array} \end{array}$ | $100.00\% \ 263 \ 150 \ 130$ | $100 \\ 1 \\ 1 \\ 1$ | | Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod | 100.00% 263 150 130 $100.00%$ | $100 \\ 1 \\ 1 \\ 1 \\ 100$ | _ _ | Covered |
| $egin{array}{ll} egin{array}{ll} egin{array}{ll} A_{ m data_min} \end{array} \end{array}$ | $100.00\% \ 263 \ 150 \ 130$ | $100 \\ 1 \\ 1 \\ 1$ | _ _ | Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: | 100.00% 263 150 130 $100.00%$ 3 | 100 1 1 1 1 100 3 | _ _ | Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: | 100.00% 263 150 130 $100.00%$ 3 0 | 100 1 1 1 1 100 3 3 | _ _ | Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ | $ \begin{array}{c} 100 \\ 1 \\ 1 \\ 1 \\ 100 \\ 3 \\ 3 \\ 100 \\ \end{array} $ | - - - - - | Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 | 100 1 1 1 100 3 3 100 1 1 | - - - - - | Covered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 | 100 1 1 1 100 3 3 100 1 1 | - - - - - - | Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 | 100 1 1 1 100 3 3 100 1 1 1 100 8 | - - - - - - | Covered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 | 100 1 1 1 100 3 3 100 1 1 1 100 8 | - - - - - - | Covered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ | 100 1 1 1 100 3 3 100 1 1 1 100 8 8 100 | - - - - - - | Covered Covered Covered Covered Covered Uncovered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 | 100 1 1 1 100 3 3 100 1 1 1 100 8 8 100 1 | - - - - - - | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 | - - - - - - | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 | 100 1 1 1 100 3 3 100 1 1 1 100 8 8 100 1 1 1 | - - - - - - | Covered Covered Covered Covered Uncovered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 | 100 1 1 1 100 3 3 100 1 1 1 100 8 8 100 1 1 1 1 1 | - - - - - - | Covered Covered Covered Covered Uncovered Covered Covered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered Covered Covered Covered Covered Covered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 1 | - - - - - - | Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_invalid | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_invalid bin Bins_trans | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_invalid bin Bins_trans Cross #cross_0# | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_invalid bin Bins_trans | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_trans Cross #cross0# covered/total bins: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_trans Cross #cross0# covered/total bins: missing/total bins: missing/total bins: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_trans Cross #cross0# covered/total bins: missing/total bins: missing/total bins: % Hit: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered Covered Covered Covered Uncovered Covered |
| bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_trans Cross #cross_0# covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 $100.00%$ | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 100 1 1 1 1 1 1 1 1 | | Covered |
| bin A_data_max bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_shift [5] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_trans Cross #cross_0# covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <a_data_walkingones [2],="" red_op_a_0=""> bin <a_data_walkingones [1],="" red_op_a_0=""> bin <a_data_min, red_op_a_1=""></a_data_min,></a_data_walkingones></a_data_walkingones> | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 $100.00%$ | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered |
| bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_irans Cross #cross0# covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <a_data_walkingones [2],="" red_op_a_0=""> bin <a_data_min, red_op_a_1=""> bin <a_data_min, red_op_a_0=""></a_data_min,></a_data_min,></a_data_walkingones> | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 $100.00%$ | 100 1 1 1 100 3 3 100 1 1 100 8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 | | Covered |
| bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift[4] bin Bins_shift[5] bin Bins_arith[2] bin Bins_arith[3] bin Bins_bitwise[0] bin Bins_bitwise[1] bin Bins_invalid bin Bins_trans Cross #cross_0# covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <a_data_walkingones[2], red_op_a_0=""> bin <a_data_min, red_op_a_1=""> bin <a_data_min, red_op_a_1=""> bin <a_data_min, red_op_a_1=""> bin <a_data_max, red_op_a_1=""> bin <a_data_max, red_op_a_1=""> bin <a_data_max, red_op_a_1=""></a_data_max,></a_data_max,></a_data_max,></a_data_min,></a_data_min,></a_data_min,></a_data_walkingones[2],> | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 $100.00%$ 12 12 12 121 9 133 | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered |
| bin A_data_min Coverpoint B_cp_mod covered/total bins: missing/total bins: % Hit: bin B_data_0 bin B_data_max bin B_data_min Coverpoint ALU_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin Bins_shift [4] bin Bins_arith [2] bin Bins_arith [3] bin Bins_bitwise [0] bin Bins_bitwise [1] bin Bins_irans Cross #cross0# covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <a_data_walkingones [2],="" red_op_a_0=""> bin <a_data_min, red_op_a_1=""> bin <a_data_min, red_op_a_0=""></a_data_min,></a_data_min,></a_data_walkingones> | 100.00% 263 150 130 $100.00%$ 3 0 $100.00%$ 257 143 162 $87.50%$ 7 1 $87.50%$ 166 173 188 175 110 116 72 0 $100.00%$ 8 0 $100.00%$ | 100 1 1 1 1 100 3 3 3 100 1 1 1 1 100 8 8 8 100 1 1 1 1 1 1 1 | | Covered |

| <pre>bin <a_data_max,red_op_a_0> bin <a_data_0,red_op_a_0> Illegal and Ignore Bins:</a_data_0,red_op_a_0></a_data_max,red_op_a_0></pre> | 17 95 | 1 1 | _ _ | Covered Covered |
|--|---|--|--------|---|
| ignore_bin assert_red_op_A Cross #cross1# | $176 \\ 100.00\%$ | 100 | _ | Occurred Covered |
| covered/total bins: | 18 | 18 | _ | Covered |
| missing/total bins: % Hit: | $0\\100.00\%$ | $18 \\ 100$ | _ | |
| Auto, Default and User Defined Bins: bin <b_data_walkingones[2], red_op_a_1<="" td=""><td></td><td></td><td></td><td></td></b_data_walkingones[2],> | | | | |
| | 58 | 1 | _ | Covered |
| $bin < B_data_walkingones [2], red_op_A_1$ | 4 | 1 | _ | Covered |
| $bin < B_{-}data_{-}walking ones [1], red_{-}op_{-}A_{-}1$ | 62 | 1 | _ | Covered |
| $bin < B_data_walkingones[1], red_op_A_1$ | $, red_op_B_0> 7$ | 1 | _ | Covered |
| bin <b_data_min, red_op_a_1,="" red_op_b_1<="" td=""><td>> 122</td><td>1</td><td>_</td><td>Covered</td></b_data_min,> | > 122 | 1 | _ | Covered |
| $\begin{array}{ll} bin < & B_{-}data_{-}min , red_{-}op_{-}A_{-}1 , red_{-}op_{-}B_{-}0 \\ bin < & B_{-}data_{-}max , red_{-}op_{-}A_{-}1 , red_{-}op_{-}B_{-}1 \end{array}$ | | 1 1 | _ | $\begin{array}{c} { m Covered} \\ { m Covered} \end{array}$ |
| $\begin{array}{ll} bin < & B_{-}data_{-}0 \;, red_op_A_1 \;, red_op_B_1 > \\ bin < & B_{-}data_max \;, red_op_A_1 \;, red_op_B_0 \end{array}$ | 170 | 1 1 | _ | Covered Covered |
| bin $\langle B_{\text{data}} = \max_{\text{red}}, \text{red} = \text{op}_{\text{A}} = 1, \text{red} = \text{op}_{\text{B}} = 0 \rangle$ | > 5 71 | 1 | _ | Covered |
| $bin < B_data_walkingones [2], red_op_A_0$ | $,\operatorname{red}_{-}\operatorname{op}_{-}B_{-}0>\\ 8$ | 1 | _ | Covered |
| bin $<$ B_data_walkingones[1], red_op_A_0 | $,\mathrm{red}_{-}\mathrm{op}_{-}\mathrm{B}_{-}\mathrm{0}\!>$ | | | |
| bin <b_data_min, red_op_a_0,="" red_op_b_1<="" td=""><td>> 26</td><td>1 1</td><td>_</td><td>Covered Covered</td></b_data_min,> | > 26 | 1 1 | _ | Covered Covered |
| $bin < Bdata_min, red_op_A_0, red_op_B_0$ | > 7 | 1 | _ | Covered |
| bin <b_data_max, red_op_a_0,="" red_op_b_1<br="">bin <b_data_0, red_op_a_0,="" red_op_b_1=""></b_data_0,></b_data_max,> | > 15 12 | 1 1 | _ | Covered Covered |
| $\label{eq:bin_scale} bin_{} < B_{-} data_{-} max_{}, red_{-} op_{-} A_{-} 0_{}, red_{-} op_{-} B_{-} 0_{}$ | > 9 | 1 | _ | Covered |
| bin <b_data_0, red_op_a_0,="" red_op_b_0=""> Illegal and Ignore Bins:</b_data_0,> | 4 | 1 | _ | Covered |
| ignore_bin assert_red_op_B | 47 | | _ | Occurred |
| $\frac{\text{Cross } \#\text{cross}_{-2}\#}{\text{covered/total bins:}}$ | 100.00% | $100\\1$ | _ | Covered |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: Auto, Default and User Defined Bins: | 100.00% | 100 | _ | |
| bin arith_permutations | 155 | 1 | _ | Covered |
| Cross $\#cross_{-2}3\#$ covered/total bins: | 100.00% | $100\\1$ | _ | Covered |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: Auto, Default and User Defined Bins: | 100.00% | 100 | _ | |
| bin addition_cin | 188 | 1 | _ | Covered |
| $\frac{\text{Cross } \#\text{cross}_{-4}\#}{\text{covered/total bins:}}$ | 100.00% | $100\\1$ | _ | Covered |
| missing/total bins: % Hit: | $0\\100.00\%$ | 1 | _ | |
| Auto, Default and User Defined Bins: | 100.00% | 100 | _ | |
| bin shift_rotate_direction | $339 \\ 100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | Covered Covered |
| Cross $\#cross_{-2}5\#$ covered/total bins: | 100.00% | 100 | _ | Covered |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\begin{matrix}1\\100\end{matrix}$ | _ | |
| Auto, Default and User Defined Bins: | 100.00% | 100 | _ | |
| bin shift_serial_in Cross #cross6# | $166 \\ 100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | Covered Covered |
| covered/total bins: | 1 | 1 | _ | Covered |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | |
| Auto, Default and User Defined Bins: | | 100 | | |
| bin or_xor_red_op_A Cross #cross7# | $\frac{22}{100.00\%}$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | Covered Covered |
| covered/total bins: | 1 | 1 | _ | 00,0104 |
| missing/total bins: % Hit: | $0 \\ 100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | |
| Auto, Default and User Defined Bins: | | | | 0 1 |
| bin or_xor_red_op_B Cross #cross8# | $\frac{33}{76.92\%}$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | Covered Uncovered |
| covered/total bins: | 20 | 26 | _ | |
| missing/total bins: % Hit: | $6\atop76.92\%$ | $\begin{array}{c} 26 \\ 100 \end{array}$ | _ | |
| Auto, Default and User Defined Bins: bin <bins_invalid, red_op_a_1,="" red_op_b<="" td=""><td>1 \</td><td></td><td></td><td></td></bins_invalid,> | 1 \ | | | |
| | 14 | 1 | _ | Covered |
| bin <bins_invalid ,red_op_a_1="" ,red_op_b<="" td=""><td>_0></td><td>1</td><td>_</td><td>Covered</td></bins_invalid> | _0> | 1 | _ | Covered |
| $bin < Bins_invalid , red_op_A_0 , red_op_B$ | | | | Covered |
| $bin < Bins_invalid , red_op_A_0 , red_op_B$ | _0> | 1 | _ | |
| bin <bins_bitwise[1], red_op<="" red_op_a_0,="" td=""><td>21 p_B_0></td><td>1</td><td>_</td><td>Covered</td></bins_bitwise[1],> | 21 p_B_0> | 1 | _ | Covered |
| bin <bins_bitwise[0], red_op<="" red_op_a_0,="" td=""><td>12 p_B_0></td><td>1</td><td>_</td><td>Covered</td></bins_bitwise[0],> | 12 p_B_0> | 1 | _ | Covered |
| | 14 | 1 | _ | Covered |
| ${ m bin} < { m Bins_arith} [3], { m red_op_A_1}, { m red_op_B}$ | B ₋ 1> | 1 | _ | Covered |
| $bin < Bins_shift [5], red_op_A_1, red_op_1$ | | | | Covered |
| | 102 | 1 | _ | Coverea |

| bin <bins_arith[3], red_op_a_1,="" red_op_b_0=""></bins_arith[3],> | | | | |
|--|-----|---|---|----------|
| | 4 | 1 | _ | Covered |
| bin <bins_shift[5], red_op_a_1,="" red_op_b_0=""></bins_shift[5],> | 5 | 1 | _ | Covered |
| bin <bins_arith[2], red_op_a_1,="" red_op_b_1=""></bins_arith[2],> | 9 | 1 | | Covered |
| | 172 | 1 | _ | Covered |
| bin <bins_shift[4], red_op_a_1,="" red_op_b_1=""></bins_shift[4],> | 145 | 1 | | Covered |
| bin <bins_arith[2], red_op_a_1,="" red_op_b_0=""></bins_arith[2],> | 140 | 1 | _ | Covered |
| [-],,, | 9 | 1 | _ | Covered |
| bin <bins_shift[4], red_op_a_1,="" red_op_b_0=""></bins_shift[4],> | 0 | 4 | | G 1 |
| bin <bins_arith[3], red_op_a_0,="" red_op_b_1=""></bins_arith[3],> | 8 | 1 | _ | Covered |
| | 10 | 1 | _ | Covered |
| $\label{eq:bins_shift} bin < Bins_shift [5] , red_op_A_0 , red_op_B_1 >$ | _ | | | - |
| bin <bins_arith[3], red_op_a_0,="" red_op_b_0=""></bins_arith[3],> | 6 | 1 | _ | Covered |
| on Sinstantin [3], red-op_A_0, red-op_b_0/ | 1 | 1 | _ | Covered |
| $\label{eq:bins_arith_2} \ \ bin \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$ | | | | |
| him (Pinn shift [4] and an A O and an P 15 | 7 | 1 | _ | Covered |
| bin $<$ Bins_shift [4], red_op_A_0, red_op_B_1> | 12 | 1 | _ | Covered |
| bin <bins_shift [4],="" red_op_a_0,="" red_op_b_0=""></bins_shift> | | _ | | |
| | 1 | 1 | _ | Covered |
| <pre>bin <bins_trans ,*,*=""> bin <bins_shift ,="" [5]="" red_op_a_0="" red_op_b_0=""></bins_shift></bins_trans></pre> | 0 | 1 | 4 | ZERO |
| om \Dins_smir([o], red_op_n_o, red_op_b_o> | 0 | 1 | 1 | ZERO |
| $\label{eq:bins_arith_2} \ \ bin \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$ | | | | |
| Illagal and Ignara Ping. | 0 | 1 | 1 | ZERO |
| Illegal and Ignore Bins: ignore_bin invalid_reduction | 200 | | _ | Occurred |
| -0 | -00 | | | |

COVERGROUP COVERAGE:

| vergroup | Metric | Goal | Bins | Status |
|---|---------|------|------|-------------|
| YPE /alsu_coverage_pkg/alsu_coverage/cg | 98.38% | 100 | | Uncovered |
| covered/total bins: | 91 | 98 | _ | |
| missing/total bins: | 7 | 98 | _ | |
| % Hit: | 92.85% | 100 | _ | |
| Coverpoint rst_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint cin_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint red_op_A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint red_op_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint bypass_A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint bypass_B_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint direction_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint serial_in_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 2 | 2 | _ | |
| missing/total bins: | 0 | 2 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint A_cp | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | _ | |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint B _{cp} | 100.00% | 100 | _ | Covered |
| covered/total bins: | 5 | 5 | _ | |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint A_cp_mod | 100.00% | 100 | _ | Covered |
| covered/total bins: | 3 | 3 | _ | |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint B_cp_mod | 100.00% | 100 | _ | Covered |
| covered/total bins: | 3 | 3 | _ | |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Coverpoint ALU_cp | 87.50% | 100 | _ | Uncovered |
| covered/total bins: | 7 | 8 | _ | Jiloovorou |
| missing/total bins: | 1 | 8 | _ | |
| | 1 | 0 | | |

| % Hit: | 87.50% | 100 | _ | | |
|---|---------------------------|---|---|--------------------------|--|
| Cross #cross0# | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 8 | 8 | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\frac{8}{100}$ | _ | | |
| Cross #cross1# | 100.00% $100.00%$ | 100 | _ | Covered | |
| covered/total bins: | 18 | 18 | _ | | |
| missing/total bins: | 0 | 18 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| Cross #cross2# | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 1 | 1 | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $1\\100$ | _ | | |
| Cross #cross3# | 100.00% | 100 | _ | Covered | |
| $\frac{1}{1000000000000000000000000000000000$ | 1 | 1 | _ | Covered | |
| missing/total bins: | 0 | 1 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| Cross #cross4# | 100.00% | 100 | _ | $\operatorname{Covered}$ | |
| covered/total bins: | 1 | 1 | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $1\\100$ | _ | | |
| Cross #cross5# | 100.00% $100.00%$ | 100 | _ | Covered | |
| $\frac{1}{1000000000000000000000000000000000$ | 1 | 1 | _ | Covered | |
| missing/total bins: | 0 | 1 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| $Cross \#cross\6\#$ | 100.00% | 100 | _ | $\operatorname{Covered}$ | |
| covered/total bins: | 1 | 1 | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | 1 | _ | | |
| % Hit: Cross #cross7# | 100.00% $100.00%$ | $100 \\ 100$ | | Covered | |
| covered/total bins: | 100.00% | 1 | | Covered | |
| missing/total bins: | 0 | 1 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| Cross #cross8# | 76.92% | 100 | _ | ${ m Uncovered}$ | |
| covered/total bins: | 20 | 26 | _ | | |
| missing/total bins: | 6 | 26 | _ | | |
| % Hit: | 76.92% | 100 | _ | | |
| Covergroup instance \/alsu_coverage_pkg::alsu | _coverage :: cg 98.38% | 100 | _ | Uncovered | |
| covered/total bins: | 98.3870 | 98 | | Uncovered | |
| missing/total bins: | 7 | 98 | _ | | |
| % Hit: | 92.85% | 100 | _ | | |
| Coverpoint rst_cp | 100.00% | 100 | _ | $\operatorname{Covered}$ | |
| covered/total bins: | 2 | 2 | _ | | |
| missing/total bins: | 0 | 2 | _ | | |
| % Hit: | 100.00% | 100 | _ | G 1 | |
| $egin{array}{ll} 	ext{bin} & 	ext{auto} \left[0 ight] \ 	ext{bin} & 	ext{auto} \left[1 ight] \end{array}$ | 947 53 | 1 1 | _ | Covered Covered | |
| Coverpoint cin_cp | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 2 | $\frac{100}{2}$ | _ | Covered | |
| missing/total bins: | 0 | 2 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| $ \text{bin } \text{ auto} \left[0 \right]$ | 493 | 1 | _ | $\operatorname{Covered}$ | |
| bin auto[1] | 507 | 1 | _ | Covered | |
| Coverpoint red_op_A_cp | 100.00% | 100 | _ | Covered | |
| <pre>covered/total bins: missing/total bins:</pre> | $\frac{2}{0}$ | $rac{2}{2}$ | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| bin red_op_A_0 | 185 | 1 | _ | $\operatorname{Covered}$ | |
| $\operatorname{bin} \operatorname{red_opA1}$ | 815 | 1 | _ | Covered | |
| $\operatorname{default}$ bin $\operatorname{red_op_A_default}$ | 0 | | _ | ZERO | |
| $Coverpoint red_op_B_cp$ | 100.00% | 100 | _ | $\operatorname{Covered}$ | |
| covered/total bins: | 2 | $\frac{2}{2}$ | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\frac{2}{100}$ | _ | | |
| bin red_op_B_0 | 100.00% 155 | 100 | _ | Covered | |
| bin red_op_B_1 | 845 | 1 | _ | Covered | |
| default bin red_op_B_default | 0 | | _ | ZERO | |
| Coverpoint bypass_A_cp | 100.00% | 100 | _ | $\operatorname{Covered}$ | |
| covered/total bins: | 2 | 2 | _ | | |
| missing/total bins: | 0 | 2 | _ | | |
| % Hit: | 100.00% | 100 | _ | C 1 | |
| bin auto[0] | 733 267 | 1 | _ | Covered Covered | |
| bin auto[1] Coverpoint bypass_B_cp | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 2 | $\frac{100}{2}$ | _ | Covered | |
| missing/total bins: | 0 | 2 | _ | | |
| % Hit: | 100.00% | 100 | _ | | |
| $ \text{bin } \text{ auto} \left[0 \right]$ | 753 | 1 | _ | $\operatorname{Covered}$ | |
| bin auto[1] | 247 | 1 | _ | Covered | |
| Coverpoint direction_cp | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 2 | $\frac{2}{2}$ | _ | | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\begin{array}{c} 2 \\ 100 \end{array}$ | _ | | |
| bin auto $[0]$ | 100.00% 534 | 1 | _ | Covered | |
| bin auto[1] | 466 | 1 | _ | Covered | |
| Coverpoint serial_in_cp | 100.00% | 100 | _ | Covered | |
| covered/total bins: | 2 | 2 | _ | | |
| missing/total bins: | 0 | 2 | _ | | |
| % Hit: | 100.00% | 100 | _ | C1 | |
| $egin{array}{ll} 	ext{bin auto} \left[0 ight] \ 	ext{bin auto} \left[1 ight] \end{array}$ | 521 479 | 1 1 | _ | Covered Covered | |
| om auto[1] | 4 (9 | 1 | _ | Covered | |
| | | | | | |

| Coverpoint A_cp | 100.00% | 100 | _ | Covered |
|---|---|--|---|--------------------------|
| covered/total bins: | 5 | 5 | _ | |
| missing/total bins: | 0 | 5 | _ | |
| $\%$ Hit: bin A_data_0 | $100.00\% \ 263$ | $100 \\ 1$ | _ | Covered |
| bin A_data_max | $\frac{263}{150}$ | 1 | _ | Covered |
| bin A_data_min | 130 | 1 | _ | Covered |
| bin A_data_walkingones[1] | 108 | 1 | _ | Covered |
| bin A_data_walkingones[2] default bin A_data_default | 92 | 1 | _ | Covered |
| Coverpoint B _c cp | $257 \\ 100.00\%$ | 100 | _ | Occurred Covered |
| covered/total bins: | 5 | 5 | _ | Covered |
| missing/total bins: | 0 | 5 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| bin B_data_0 bin B_data_max | $\begin{array}{c} 257 \\ 143 \end{array}$ | 1 | _ | Covered Covered |
| bin B ₋ data ₋ max bin B ₋ data ₋ min | 143 162 | 1 1 | _ | Covered |
| bin B_data_walkingones[1] | 91 | 1 | _ | Covered |
| bin B_data_walkingones [2] | 97 | 1 | _ | Covered |
| default bin B_data_default | 250 | 100 | _ | Occurred |
| Coverpoint A_cp_mod covered/total bins: | 100.00% 3 | $\frac{100}{3}$ | _ | Covered |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| $bin A_data_0$ | 263 | 1 | _ | Covered |
| bin A_data_max | 150 | 1 | _ | Covered |
| bin A_data_min Coverpoint B_cp_mod | $130 \\ 100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | Covered Covered |
| covered/total bins: | $\frac{100.0076}{3}$ | 3 | _ | Covered |
| missing/total bins: | 0 | 3 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| bin B_data_0 | 257 | 1 | _ | Covered |
| bin B ₋ data ₋ max bin B ₋ data ₋ min | $\begin{array}{c} 143 \\ 162 \end{array}$ | 1 1 | _ | Covered Covered |
| Coverpoint ALU_cp | 87.50% | 100 | | Uncovered |
| covered/total bins: | 7 | 8 | _ | |
| missing/total bins: | 1 | 8 | _ | |
| % Hit: | 87.50% | 100 | _ | |
| bin Bins_shift [4] bin Bins_shift [5] | $\frac{166}{173}$ | 1 1 | | Covered Covered |
| bin Bins_arith[2] | 188 | 1 | | Covered |
| bin Bins_arith[3] | 175 | 1 | _ | Covered |
| bin Bins_bitwise[0] | 110 | 1 | _ | Covered |
| bin Bins_bitwise[1] | 116 | 1 | _ | Covered |
| bin Bins_invalid bin Bins_trans | 72 | 1 1 | _ | Covered ZERO |
| Cross #cross0# | 100.00% | 100 | | Covered |
| covered/total bins: | 8 | 8 | _ | 00.0100 |
| missing/total bins: | 0 | 8 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: bin <a_data_walkingones[2], red_op_a_0=""></a_data_walkingones[2],> | 12 | 1 | | Covered |
| bin $\langle A_1 data_2 walkingones[2], red_op_A_0 \rangle$ bin $\langle A_1 data_2 walkingones[1], red_op_A_0 \rangle$ | $\frac{12}{12}$ | 1 | | Covered |
| bin $<$ A_data_min, red_op_A_1 $>$ | 121 | 1 | _ | Covered |
| $\mathrm{bin} \ <\! \mathrm{A_data_min} \ , \mathrm{red_op_A_0} \! > \\$ | 9 | 1 | _ | Covered |
| bin <a_data_max, red_op_a_1=""></a_data_max,> | 133 | 1 | _ | Covered |
| $egin{aligned} & 	ext{bin} & <& 	ext{A_data_0} \ , & 	ext{red_op_A_1} > \ & 	ext{bin} & <& 	ext{A_data_max} \ , & 	ext{red_op_A_0} > \end{aligned}$ | $\frac{168}{17}$ | 1 1 | _ | Covered Covered |
| bin $<$ A_data_0, red_op_A_0 $>$ | 95 | 1 | _ | Covered |
| Illegal and Ignore Bins: | | | | |
| ignore_bin assert_red_op_A | 176 | | _ | Occurred |
| Cross #cross1# | 100.00% | 100 | _ | $\operatorname{Covered}$ |
| covered/total bins: missing/total bins: | $\frac{18}{0}$ | 18 18 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| $bin < B_{data_walkingones}[2], red_{op_A_1}, red_{op_A_1}$ | - | | | |
| $bin < B_{data_walkingones}[2], red_op_A_1, red_op_A_1$ | 58 ed on B 0> | 1 | _ | Covered |
| bin \b_data_warkingones[2], red_op_A_1, red_op_A_1 | 4 | 1 | _ | Covered |
| $bin < B_{data_walkingones}[1], red_op_A_1, red_op_A_1$ | ed_op_B_1> | _ | | |
| | 62 | 1 | _ | Covered |
| bin $<$ B_data_walkingones[1], red_op_A_1, red_ | ed_op_B_0> | 1 | | Covered |
| bin <b_data_min, red_op_a_1,="" red_op_b_1=""></b_data_min,> | $7\\122$ | 1 1 | _ | Covered Covered |
| bin <b_data_min, red_op_a_1,="" red_op_b_0=""></b_data_min,> | 7 | 1 | _ | Covered |
| bin <b_data_max, red_op_a_1,="" red_op_b_1=""></b_data_max,> | 114 | 1 | _ | Covered |
| bin <b_data_0, red_op_a_1,="" red_op_b_1=""></b_data_0,> | 170 | 1 | _ | Covered |
| bin <b_data_max, red_op_a_1,="" red_op_b_0=""> bin <b_data_0, red_op_a_1,="" red_op_b_0=""></b_data_0,></b_data_max,> | $5\\71$ | 1 1 | _ | Covered Covered |
| bin $\langle B_{data} = 0, red_{p-A-1}, red_{p-B-0} \rangle$ bin $\langle B_{data} = valkingones [2], red_{p-A-0}, red_{p-A-0}$ | | 1 | _ | Oreled |
| | 8 | 1 | _ | Covered |
| bin $<$ B_data_walkingones[1], red_op_A_0, red_op_A | - | | | |
| Lim and Later 1 1 1 1 1 2 2 2 2 2 2 | $\frac{2}{2}$ | 1 | _ | Covered |
| <pre>bin <b_data_min, red_op_a_0,="" red_op_b_1=""> bin <b_data_min, red_op_a_0,="" red_op_b_0=""></b_data_min,></b_data_min,></pre> | $\frac{26}{7}$ | 1 1 | _ | Covered Covered |
| bin <b_data_max, red_op_a_0,="" red_op_b_1=""></b_data_max,> | 15 | 1 | _ | Covered |
| bin <b_data_0, red_op_a_0,="" red_op_b_1=""></b_data_0,> | 12 | 1 | _ | Covered |
| $\label{eq:bin} $$ \ \ $ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$ | 9 | 1 | _ | Covered |
| $\label{eq:bin_scale} \begin{array}{ll} \text{bin} & <\!\! \text{B_data_0} \;, \text{red_op_A_0} \;, \text{red_op_B_0} \!\!> \\ \end{array}$ | | | | |
| III | 4 | 1 | _ | Covered |
| Illegal and Ignore Bins: | | 1 | _ | |
| Illegal and Ignore Bins: ignore_bin assert_red_op_B | 4 47 | 1 | _ | Covered Occurred |

| Cross #cross2# | 100.00% | 100 | _ | Covered |
|--|---------------|--|---|--------------------------|
| $\frac{1}{1000000000000000000000000000000000$ | 100.0070 | 1 | _ | Covered |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| bin arith_permutations | 155 | 1 | _ | Covered |
| Cross #cross3# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 1 | 1 | _ | |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| bin addition_cin | 188 | 1 | _ | Covered |
| Cross #cross4# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 1 | 1 | _ | |
| missing/total bins: | $0\\100.00\%$ | 1 | _ | |
| % Hit: Auto, Default and User Defined Bins: | 100.0070 | 100 | _ | |
| bin shift_rotate_direction | 339 | 1 | _ | Covered |
| Cross #cross_5# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 1 | 1 | _ | Covered |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| bin shift_serial_in | 166 | 1 | _ | Covered |
| Cross #cross6# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 1 | 1 | _ | |
| missing/total bins: | 0 | 1 | _ | |
| % Hit: | 100.00% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| bin or_xor_red_op_A | 22 | 1 | _ | Covered |
| Cross #cross7# | 100.00% | 100 | _ | Covered |
| covered/total bins: | 1 | 1 | _ | |
| missing/total bins: % Hit: | $0\\100.00\%$ | $\begin{matrix} 1 \\ 100 \end{matrix}$ | _ | |
| Auto, Default and User Defined Bins: | 100.00% | 100 | _ | |
| bin or_xor_red_op_B | 33 | 1 | _ | Covered |
| Cross #cross_8# | 76.92% | 100 | | Uncovered |
| covered/total bins: | 20 | $\frac{100}{26}$ | _ | Oncovered |
| missing/total bins: | 6 | $\frac{26}{26}$ | _ | |
| % Hit: | 76.92% | 100 | _ | |
| Auto, Default and User Defined Bins: | | | | |
| bin <bins_invalid ,="" red_op_a_1="" red_op_b_1<="" td=""><td>></td><td></td><td></td><td></td></bins_invalid> | > | | | |
| | 14 | 1 | _ | Covered |
| bin <bins_invalid ,="" red_op_a_1="" red_op_b_0=""></bins_invalid> | | | | |
| | 16 | 1 | _ | Covered |
| bin <bins_invalid ,="" red_op_a_0="" red_op_b_1=""></bins_invalid> | | | | ~ . |
| | 21 | 1 | _ | Covered |
| bin <bins_invalid ,="" red_op_a_0="" red_op_b_0<="" td=""><td></td><td>1</td><td></td><td>C1</td></bins_invalid> | | 1 | | C1 |
| bin <bins_bitwise[1], red_op_a_0,="" red_op_e<="" td=""><td>21</td><td>1</td><td>_</td><td>Covered</td></bins_bitwise[1],> | 21 | 1 | _ | Covered |
| bin bins_bitwise[i],red_op_A_0,red_op_E | 12 | 1 | _ | Covered |
| bin <bins_bitwise[0], red_op_a_0,="" red_op_e<="" td=""><td></td><td>1</td><td>_</td><td>Covered</td></bins_bitwise[0],> | | 1 | _ | Covered |
| bin \Bins_bit wise [0], red_op_m_o, red_op_n | 14 | 1 | _ | Covered |
| bin <bins_arith[3], red_op_a_1,="" red_op_b_1<="" td=""><td></td><td>1</td><td></td><td>Covered</td></bins_arith[3],> | | 1 | | Covered |
| [0],100104-11-1,1001-04-04-04-04-04-04-04-04-04-04-04-04-04- | 160 | 1 | _ | Covered |
| bin <bins_shift[5], red_op_a_1,="" red_op_b_1<="" td=""><td></td><td>-</td><td></td><td>00,0104</td></bins_shift[5],> | | - | | 00,0104 |
| 1 | 162 | 1 | _ | Covered |
| bin <bins_arith[3], red_op_a_1,="" red_op_b_0<="" td=""><td></td><td></td><td></td><td></td></bins_arith[3],> | | | | |
| • | 4 | 1 | _ | Covered |
| bin <bins_shift[5], red_op_a_1,="" red_op_b_0<="" td=""><td>)></td><td></td><td></td><td></td></bins_shift[5],> |)> | | | |
| | 5 | 1 | _ | $\operatorname{Covered}$ |
| $bin < Bins_arith[2], red_op_A_1, red_op_B_1$ | | | | |
| | 172 | 1 | _ | Covered |
| $bin < Bins_shift [4], red_op_A_1, red_op_B_1$ | | | | |
| 1: 4D: :41 [0] 1 A 1 1 D 0 | 145 | 1 | _ | $\operatorname{Covered}$ |
| $bin < Bins_arith[2], red_op_A_1, red_op_B_0$ | | 1 | | Command |
| bin <bins_shift [4],="" red_op_a_1,="" red_op_b_0<="" td=""><td>9</td><td>1</td><td>_</td><td>Covered</td></bins_shift> | 9 | 1 | _ | Covered |
| om oms_smitt[4],fed_op_A_i,fed_op_b_c | 8 | 1 | _ | Covered |
| bin <bins_arith[3], red_op_a_0,="" red_op_b_1<="" td=""><td></td><td>1</td><td>_</td><td>Covered</td></bins_arith[3],> | | 1 | _ | Covered |
| bin \Dins_aritin[b], red_op_n_o, red_op_b_r | 10 | 1 | _ | Covered |
| bin <bins_shift[5], red_op_a_0,="" red_op_b_1<="" td=""><td></td><td>1</td><td></td><td>Covered</td></bins_shift[5],> | | 1 | | Covered |
| (Dinoconiio [o], rodiopilio, rodiopilio | 6 | 1 | _ | Covered |
| bin <bins_arith[3], red_op_a_0,="" red_op_b_0<="" td=""><td></td><td></td><td></td><td></td></bins_arith[3],> | | | | |
| | 1 | 1 | _ | Covered |
| bin <bins_arith[2], red_op_a_0,="" red_op_b_1<="" td=""><td>.></td><td></td><td></td><td></td></bins_arith[2],> | .> | | | |
| | 7 | 1 | _ | Covered |
| $bin < Bins_shift [4], red_op_A_0, red_op_B_1$ | | | | |
| | 12 | 1 | _ | $\operatorname{Covered}$ |
| bin <bins_shift [4],="" red_op_a_0,="" red_op_b_0<="" td=""><td>)></td><td></td><td></td><td></td></bins_shift> |)> | | | |
| | 1 | 1 | _ | Covered |
| bin <bins_trans,*,*></bins_trans,*,*> | 0 | 1 | 4 | ZERO |
| $bin < Bins_shift[5], red_op_A_0, red_op_B_0$ | | 4 | 4 | ZEDO |
| him >Din= | 0 | 1 | 1 | ZERO |
| $bin < Bins_arith[2], red_op_A_0, red_op_B_0$ | | 1 | 1 | 7EDO |
| Illegal and Ignore Bins: | 0 | 1 | 1 | ZERO |
| ignore_bin invalid_reduction | 200 | | _ | Occurred |
| 101101011 1111011011011011 | 200 | | | Journa |
| | | | | |

TOTAL COVERGROUP COVERAGE: 98.38% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 98.38%

1.5 5. code Coverage Report

Coverage Report by DU with details

| — Design Unit: work | .ALSU | | | | |
|---|--------------------|--|--------|---|------------|
| Branch Coverage: Enabled Coverage | Bins | $_{ m Hits}$ | Misses | Coverage | |
| Branches | 32 | 32 | 0 | 100.00% | |
| | Branch | Details=== | | | |
| Branch Coverage for D | Design Unit work.A | LSU | | | |
| Line Item | | Count | Source | | |
| File ALSU.sv | IF | Branch | | | |
| $ \begin{array}{ccc} 24 \\ 24 & 1 \end{array} $ | | $1048 \\ 101$ | | coming in to IF st) begin | |
| 35 1 Branch totals: 2 hits | | $947\\100.00\%$ | end | else begin | |
| F1 | IF | Branch— | | | |
| 51 51 1 53 1 | | $1048 \\ 101 \\ 947$ | if(r | coming in to IF st) begin else begin | |
| Branch totals: 2 hits | | | | | |
| 54 | | Branch———————————————————————————————————— | | coming in to IF | |
| 54 1 56 1 Branch totals: 2 hits | | $\frac{690}{257}$ 100.00% | | if (invalid) else | |
| | | Branch | | | |
| 63 63 1 | | $1048 \\ 101$ | if(r | coming in to IF st) begin | |
| 66 1 Branch totals: 2 hits | | $947\\100.00\%$ | else | begin | |
| 67 | IF | Branch———————————————————————————————————— | Count | coming in to IF | |
| $ \begin{array}{ccc} 67 & & 1 \\ 69 & & 1 \end{array} $ | | $\begin{array}{c} 59 \\ 176 \end{array}$ | i f | (bypass_A_reg && bypa se if (bypass_A_reg) | ss_B_reg |
| 71 1 73 1 | | $\frac{164}{387}$ | el | se if (bypass_B_reg) se if (invalid) | |
| 75 1 Branch totals: 5 hits | | $100.00\%^{161}$ | el | se begin | |
| 76 | CA | SE Branch— 161 | Count | coming in to CASE | |
| 77 1 87 1 | | $\begin{array}{c} 101 \\ 24 \\ 19 \end{array}$ | Count | 3'h0: begin 3'h1: begin | |
| 97 1 98 1 | | $\begin{array}{c} 29 \\ 24 \end{array}$ | | 3'h2: out <= A_reg 3'h3: out <= A_reg | |
| 99 1 105 1 | | $\begin{array}{c} 31 \\ 27 \end{array}$ | | 3'h4: begin 3'h5: begin | 0 1 |
| Branch totals: 7 hits | of 7 branches = | $\begin{array}{c} 7 \\ 100.00\% \end{array}$ | All Fa | alse Count | |
| | IF | Branch | | | |
| 78 78 1 | | $\begin{array}{c} 24 \\ 5 \end{array}$ | Count | coming in to IF if (red_op_A_reg | |
| 80 1 82 1 | | 5 4 | | else if (red_op_A else if (red_op_B | |
| 84 1 Branch totals: 4 hits | | 100.00% | | else | |
| 88 | IF | Branch——— | Count | coming in to IF | |
| 88 1 90 1 | | 2 5 | Count | if (red_op_A_reg else if (red_op_A | |
| $ \begin{array}{ccccccccccccccccccccccccccccccccccc$ | | 5 7 | | else if (red_op_H | |
| Branch totals: 4 hits | of 4 branches = | • | | | |
| 100 | | Branch———31 | Count | coming in to IF | |
| $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | | 11 20 | | if (direction_reg else | ;) |
| Branch totals: 2 hits | | | | | |
| 106 106 1 | | Branch———————————————————————————————————— | Count | coming in to IF if (direction_reg | .) |
| $ \begin{array}{ccc} 106 & 1 \\ 108 & 1 \end{array} $ | | 8 19 | | else | .) |

```
Condition Coverage:
    Enabled Coverage
                                    Bins
                                            Covered
                                                        Misses
                                                                Coverage
                                       6
    Conditions
                                                  6
                                                             0
                                                                 100.00\%
                                  =Condition Details:
Condition Coverage for Design Unit work.ALSU —
  File ALSU.sv
                 -Focused Condition View-
Line
           67 Item
                      1 (bypass_A_reg && bypass_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00\%
                  Covered Reason for no coverage
    Input Term
                                                      Hint
  bypass_A_reg
                        Υ
                        Y
  bypass_B_reg
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
                        bypass_A_reg_0
  Row
        1:
                        bypass_A_reg_1
  Row
        2:
                                                bypass_B_reg
                     1
  Row
        3:
                        bypass_B_reg_0
                                                bypass_A_reg
                     1
                        bypass_B_reg_1
  Row
        4:
                                                bypass_A_reg
                     1
                 -Focused Condition View-
Line
           78 Item
                     1 (red_op_A_reg && red_op_B_reg)
Condition totals: 2 of 2 input terms covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                      _{
m Hint}
                        Υ
  red_op_A_reg
                        Y
  red_op_B_reg
     Rows:
                  Hits
                       FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        red_op_A_reg_0
                     1
  Row
        2:
                        red_op_A_reg_1
                                                red_op_B_reg
  Row
        3:
                        red_op_B_reg_0
                                                red_op_A_reg
                        red_op_B_reg_1
                                                red_op_A_reg
  Row
        4:
                     1
                 -Focused Condition View-
           88 Item
                      1 (red_op_A_reg && red_op_B_reg)
Line
Condition totals: 2 of 2 input terms covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                      _{
m Hint}
  red_op_A_reg
                        Υ
  red_op_B_reg
                        Y
     Rows:
                  Hits
                       FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        red_op_A_reg_0
  Row
        2:
                        red_op_A_reg_1
                                                red_op_B_reg
  Row
        3:
                        red_op_B_reg_0
                                                red_op_A_reg
  Row
        4:
                        red_op_B_reg_1
                                                red_op_A_reg
Expression Coverage:
    Enabled Coverage
                                    Bins
                                            Covered
                                                                Coverage
                                                        Misses
    Expressions
                                       8
                                                             0
                                                                 100.00\%
                                 =Expression Details=
Expression Coverage for Design Unit work.ALSU —
  File ALSU.sv
                 -Focused Expression View-
           18 Item 1 ((red_op_A_reg | red_op_B_reg) & (opcode_reg[1] | opcode_reg[2]))
Expression totals: 4 of 4 input terms covered = 100.00\%
     Input Term
                   \operatorname{Covered}
                            Reason for no coverage
                                                        \operatorname{Hint}
   red_op_A_reg
                         Y
   red_op_B_reg
                         Υ
                         Y
  opcode_reg[1]
                         Y
  opcode_reg[2]
     Rows:
                  Hits
                        FEC Target
                                                Non-masking condition(s)
                                                                    opcode_reg[2]) && ~red_op_B_reg)
  Row
        1:
                     1
                        red_op_A_reg_0
                                                ((\text{opcode}_{\text{reg}}[1]
        2:
                                                                    opcode_reg[2]) && ~red_op_B_reg)
  Row
                        red_op_A_reg_1
                                                ((\text{opcode}_{\text{reg}}[1]
                     1
        3:
                        red_op_B_reg_0
                                                                    opcode_reg[2]) && ~red_op_A_reg)
  Row
                     1
                                                ((opcode_reg[1]
                                                                    opcode_reg[2]) && ~red_op_A_reg)
                        red_op_B_reg_1
  Row
        4:
                     1
                                                ((opcode_reg[1]
  Row
        5:
                        opcode_reg[1]_0
                                                ((red_op_A_reg)
                                                                   red_op_B_reg) && ~opcode_reg[2])
                     1
                        opcode_reg[1]_1
        6:
                                                                  red_op_B_reg) && ~opcode_reg[2])
  Row
                                                ((red_op_A_reg)
                     1
        7:
                        opcode_reg[2]_0
                                                                  red_op_B_reg) && ~opcode_reg[1])
  Row
                                                ((red_op_A_reg)
```

1

Row

8:

 $opcode_reg[2]_1$

red_op_B_reg) && ~opcode_reg[1])

((red_op_A_reg

```
-Focused Expression View-
            19 Item
                      1 (\operatorname{opcode\_reg}[1] \& \operatorname{opcode\_reg}[2])
Line
Expression totals: 2 of 2 input terms covered = 100.00%
     Input Term
                    Covered Reason for no coverage
  \operatorname{opcode\_reg}[1]
                          Y
  opcode_reg[2]
                          Y
                                                   Non-masking condition(s)
                   _{
m Hits}
                         FEC Target
     Rows:
                          opcode_reg[1]_0
                                                   opcode_reg[2]
  Row
         1:
                      1
                          opcode_reg[1]_1
                                                   opcode_reg[2]
  Row
         2:
                          opcode_reg[2]_0
                                                   opcode_reg[1]
  Row
         3:
                          opcode_reg[2]_1
                                                   opcode_reg[1]
                      1
  Row
         4:
                  -Focused Expression View-
            20 Item
                      1 (invalid_red_op | invalid_opcode)
Line
Expression totals: 2 of 2 input terms covered = 100.00\%
      Input Term
                     Covered Reason for no coverage
                                                            _{
m Hint}
                            Y
  invalid\_red\_op
  invalid_opcode
                            \mathbf{Y}
     Rows:
                   _{
m Hits}
                        FEC Target
                                                   Non-masking condition(s)
         1:
                          invalid_red_op_0
                                                   ~invalid_opcode
  Row
                      1
                          invalid\_red\_op\_1
                                                   ~invalid_opcode
  Row
         2:
                          invalid_opcode_0
                                                   ~invalid_red_op
  Row
         3:
                      1
  Row
         4:
                          invalid_opcode_1
                                                   \tilde{invalid}_{red_op}
Statement Coverage:
                                      _{\rm Bins}
    Enabled Coverage
                                                  _{
m Hits}
                                                           Misses
                                                                   Coverage
    Statements
                                        48
                                                    48
                                                                0
                                                                     100.00\%
                                   Statement Details
Statement Coverage for Design Unit work.ALSU —
    Line
                                                 Count
                   Item
                                                            Source
```

| Line | ${\rm Item}$ | Count | Source |
|-----------------|--------------|------------------------|--|
| File ALSU. | SV | | |
| 1 | | | module ALSU(A, B, cin, serial_in, red_op_A, red_op_B, opcode, bypass_A, bypass_B, c |
| 2 | | | parameter INPUT_PRIORITY = "A"; |
| 3 | | | parameter FULL_ADDER = "ON"; |
| 4 | | | input clk, cin, rst, red_op_A, red_op_B, bypass_A, bypass_B, direction, serial_in; |
| 5 | | | input [2:0] opcode; |
| 6 | | | input signed [2:0] A, B; |
| 7 | | | output reg [15:0] leds; |
| 8 9 | | | output reg signed [5:0] out; |
| 10 | | | reg_red_op_A_reg, red_op_B_reg, bypass_A_reg, bypass_B_reg, direction_reg, serial_in |
| 11 | | | reg signed cin_reg; |
| $\frac{11}{12}$ | | | reg [2:0] opcode_reg; |
| 13 | | | $reg \ signed \ [2:0] \ A_{reg}$, B_{reg} ; |
| 14 | | | |
| 15 | | | wire invalid_red_op, invalid_opcode, invalid; |
| 16 | | | ,, |
| 17 | | | //Invalid handling |
| 18 | 1 | 889 | assign invalid_red_op = (red_op_A_reg red_op_B_reg) & (opcode_reg[1] opcode_reg |
| 19 | 1 | 848 | assign invalid_opcode = opcode_reg[1] & opcode_reg[2]; |
| 20 | 1 | 505 | assign invalid = invalid_red_op invalid_opcode; |
| 21 | | | |
| 22 | | | //Registering input signals |
| 23 | 1 | 1048 | always @(posedge clk or posedge rst) begin |
| 24 | | | if(rst) begin |
| 25 | 1 | 101 | $\operatorname{cin}_{\operatorname{reg}} = 0;$ |
| 26 | 1 | 101 | $red_op_B_reg <= 0;$ |
| 27 | 1 | 101 | $red_{op}A_{reg} \le 0;$ |
| 28 | 1 | 101 | $bypass_B reg <= 0;$ |
| 29 | 1 | 101 | $bypass_A_reg <= 0;$ |
| $\frac{30}{31}$ | 1 | 101 101 | <pre>direction_reg <= 0; serial_in_reg <= 0;</pre> |
| $\frac{31}{32}$ | 1 | 101 | $opcode_reg \le 0;$ |
| 33 | 1 | 101 | $A_{reg} \leq 0;$ |
| 34 | 1 | 101 | $B_{reg} \leq 0$; |
| 35 | 1 | 101 | end else begin |
| 36 | 1 | 947 | cin_reg <= cin; |
| 37 | 1 | 947 | red_op_B_reg <= red_op_B; |
| 38 | 1 | 947 | $red_op_A_reg \ll red_op_A;$ |
| 39 | 1 | 947 | bypass_B_reg <= bypass_B; |
| 40 | 1 | 947 | bypass_A_reg <= bypass_A; |
| 41 | 1 | 947 | direction_reg <= direction; |
| 42 | 1 | 947 | serial_in_reg <= serial_in; |
| 43 | 1 | 947 | opcode_reg <= opcode; |
| 44 | 1 | 947 | $A_{reg} \le A;$ |
| 45 | 1 | 947 | $B_{reg} \le B;$ |
| 46 | | | end |
| 47 | | | end |

```
48
                                                              //leds output blinking
    49
    50
                       1
                                                    1048
                                                              always @(posedge clk or posedge rst) begin
                                                                 if (rst) begin
    51
                       1
                                                     101
                                                                    leds \ll 0;
    52
                                                                 end else begin
    53
                                                                      if (invalid)
    54
                                                                        leds \le ~leds;
                       1
                                                     690
    55
    56
                                                                      else
                       1
                                                     257
                                                                        leds \ll 0;
    57
    58
                                                                _{\mathrm{end}}
    59
                                                              _{\mathrm{end}}
    60
                                                              //ALSU output processing
    61
                       1
                                                    1048
                                                              always @(posedge clk or posedge rst) begin
    62
                                                                 if (rst) begin
    63
                       1
                                                     101
                                                                   out \leq 0;
    64
    65
                                                                 \operatorname{end}
    66
                                                                 else begin
                                                                   if (bypass_A_reg && bypass_B_reg)
    67
                                                                     out <= (INPUT_PRIORITY == "A")? A_reg: B_reg;
                       1
                                                      59
    68
                                                                   else if (bypass_A_reg)
    69
                                                                     out \leq A_reg;
    70
                       1
                                                     176
                                                                   else if (bypass_B_reg)
    71
    72
                       1
                                                     164
                                                                     out \leq B_reg;
                                                                   else if (invalid)
    73
                                                                        out \leq 0;
                       1
                                                     387
    74
                                                                   else begin
    75
    76
                                                                        case (opcode)
    77
                                                                          3'h0: begin
                                                                             if \ (\texttt{red\_op\_A\_reg \&\& red\_op\_B\_reg})
    78
                                                                               out <= (INPUT_PRIORITY == "A")? | A_reg: | B_reg;
                       1
                                                       5
    79
                                                                             else if (red_op_A_reg)
    80
                                                                               out \leq |A_reg|;
                       1
                                                       5
    81
                                                                             else if (red_op_B_reg)
    82
                       1
                                                       4
                                                                               out \leq |B_reg|;
    83
                                                                             else
    84
                                                      10
                       1
                                                                               out \leq A_reg | B_reg;
    85
    86
                                                                          end
    87
                                                                          3'h1: begin
                                                                             if \ (red\_op\_A\_reg \ \&\& \ red\_op\_B\_reg)\\
    88
                                                                               out <= (INPUT_PRIORITY == "A")? ^A_reg: ^B_reg;
                       1
                                                       2
    89
                                                                             else if (red_op_A_reg)
    90
                       1
                                                                               out \leq ^A_reg;
    91
                                                       5
                                                                             else if (red_op_B_reg)
    92
                                                                               out \leq ^B_reg;
    93
                       1
                                                       5
                                                                             else
    94
                       1
                                                       7
                                                                               out \leq A_reg \hat{} B_reg;
    95
    96
                                                                          end
    97
                       1
                                                      ^{29}
                                                                          3'h2: out \ll A_reg + B_reg;
    98
                       1
                                                      24
                                                                          3'h3: out \ll A_reg * B_reg;
    99
                                                                          3'h4: begin
    100
                                                                             if (direction_reg)
    101
                       1
                                                      11
                                                                               out \leq \{ \text{out} [4:0], \text{ serial\_in\_reg} \};
    102
                                                                             else
    103
                       1
                                                      20
                                                                               out \leq \{ serial_in_reg, out [5:1] \};
    104
                                                                          end
    105
                                                                          3'h5: begin
    106
                                                                             if (direction_reg)
    107
                       1
                                                       8
                                                                               out \le \{out [4:0], out [5]\};
    108
    109
                       1
                                                      19
                                                                               out \leq \{ \text{out} [0], \text{ out} [5:1] \};
Toggle Coverage:
                                                                      Coverage
    Enabled Coverage
                                        Bins
                                                    Hits
                                                             Misses
    Toggles
                                                                       100.00\%
                                         118
                                                     118
                                                                   0
```

Toggle Details

Toggle Coverage for Design Unit work.ALSU

| Node | $1\mathrm{H}\!\!-\!\!>\!\!0\mathrm{L}$ | 0L->1H | "Coverage" |
|---|--|--------|------------|
| A[0-2] | 1 | 1 | 100.00 |
| $A \operatorname{reg} \left[0 - 2 \right]$ | 1 | 1 | 100.00 |
| B[0-2] | 1 | 1 | 100.00 |
| $B_{reg}[0-2]$ | 1 | 1 | 100.00 |
| $bypass_A$ | 1 | 1 | 100.00 |
| bypass_A_reg | 1 | 1 | 100.00 |
| $bypass_B$ | 1 | 1 | 100.00 |
| bypass_B_reg | 1 | 1 | 100.00 |
| cin | 1 | 1 | 100.00 |
| cin_reg | 1 | 1 | 100.00 |
| clk | 1 | 1 | 100.00 |
| direction | 1 | 1 | 100.00 |
| direction_reg | 1 | 1 | 100.00 |
| invalid | 1 | 1 | 100.00 |
| invalid_opcode | 1 | 1 | 100.00 |
| invalid_red_op | 1 | 1 | 100.00 |
| leds[0-15] | 1 | 1 | 100.00 |
| $\operatorname{opcode}\left[0-2\right]$ | 1 | 1 | 100.00 |

```
\operatorname{opcode}_{-}\operatorname{reg}[0-2]
                                                 1
                                                           100.00
        \operatorname{out}\left[0-5\right]
                                 1
                                                           100.00
                                                 1
        red_op_A
                                 1
                                                 1
                                                           100.00
   red_op_A_reg
                                 1
                                                           100.00
                                                 1
        {
m red\_op\_B}
                                 1
                                                 1
                                                           100.00
   red_op_B_reg
                                 1
                                                 1
                                                           100.00
                                                           100.00
                                 1
                                                 1
       serial_in
                                1
                                                           100.00
                                                 1
  serial_in_reg
                                1
                                                 1
                                                           100.00
```

 $\begin{array}{lll} {\rm Total~Node~Count} & = & 59 \\ {\rm Toggled~Node~Count} & = & 59 \\ {\rm Untoggled~Node~Count} & = & 0 \\ \end{array}$

Toggle Coverage = 100.00% (118 of 118 bins)

Total Coverage By Design Unit (filtered view): 100.00%

1.6 6. Waveform

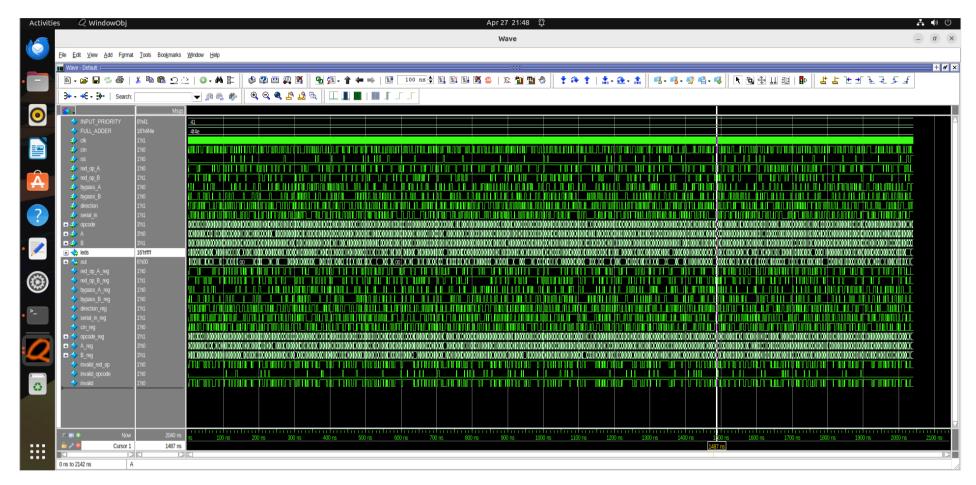


Figure 1: simulation waveform

```
(C) 2006-2013 Synopsys, Inc.
 (C) 2011-2013 Cypress Semiconductor Corp.
                    IMPORTANT RELEASE NOTES
   You are using a version of the UVM library that has been compiled
   with `UVM_NO_DEPRECATED undefined.
   See http://www.eda.org/svdb/view.php?id=3313 for more details.
   You are using a version of the UVM library that has been compiled
   with 'UVM OBJECT MUST HAVE CONSTRUCTOR undefined.
   See http://www.eda.org/svdb/view.php?id=3770 for more details.
       (Specify +UVM NO RELNOTES to turn off this notice)
 UVM INFO verilog src/questa uvm pkg-1.2/src/questa uvm pkg.sv(277) 0 0: reporter [Questa UVM] QUESTA UVM-1.2.3
 UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(278) @ 0: reporter [Questa_UVM] questa_uvm::init(all)
 UVM_INFO @ 0: reporter [RNTST] Running test alsu_test...
 ** Warning: (vsim-8474) A higher value '4' is found in bin 'A data walkingones' of Coverpoint 'A cp'. It is invalid and will be ignored.
   Time: 0 ns Iteration: 7 Process: /uvm_pkg::uvm_phase::m_run_phases/#FORK#1847_7feff0488f8 File: alsu_coverage_pkg.sv Line: 52
 ** Warning: (vsim-8474) A higher value '4' is found in bin 'B_data_walkingones' of Coverpoint 'B_cp'. It is invalid and will be ignored.
  Time: 0 ns Iteration: 7 Process: /uvm_pkg::uvm_phase::m_run_phases/#FORK#1847_7feff0488f8 File: alsu_coverage_pkg.sv Line: 59
 UVM INFO alsu test pkg.sv(35) @ 0: uvm test top [run phase] Inside the ALSU test.
 ******************
# * Questa UVM Transaction Recording Turned ON.
# * recording_detail has been set.
# * To turn off, set 'recording_detail' to off:
UVM_INFO verilog_src/uvm-1.ld/src/base/uvm_objection.svh(1267) @ 2040: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
 UVM_INFO alsu_scoreboard_pkg.sv(130) @ 2040: uvm_test_top.env.sb [REPORT] Total correct transactions: 1020
 UVM_INFO alsu_scoreboard_pkg.sv(131) @ 2040: uvm_test_top.env.sb [REPORT] Total mismatches: 0
 --- UVM Report Summary ---
 ** Report counts by severity
# UVM_INFO : 7
 UVM WARNING :
# UVM_ERROR : 0
# UVM_FATAL : 0
 ** Report counts by id
 [Questa UVM]
# [REPORT]
# [RNTST]
            1
# [TEST DONE]
# [run_phase]
# ** Note: $finish : /usr/local/questasim/linux x86 64/../verilog src/uvm-1.1d/src/base/uvm root.svh(430)
   Time: 2040 ns | Theration: 61 | Instance: /top
```

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Figure 2: Transcript : all test cases passed