SV Project

Digital Design Verification

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1 Synchronous FIFO

1.1 Shared package

```
package Shared_pkg;
              // ===== Global parameter for Signal Declaration =====
              parameter FIFO_WIDTH = 16;
              parameter FIFO_DEPTH = 8;
              // ===== Signals For Test Control ======
              // ===== #No of Randomization ======
              parameter TEST_COUNT = 1000;
              // ===== Counter For Failed and Successed Test Transactions =====
              int unsigned error_count = 0;
              int unsigned correct_count = 0;
              // ===== When eq 1 Trim Test =====
              bit test_finished = 0;
14 endpackage
      1.2 Interface
      import Shared_pkg::*;
     interface FIFO_IF (input logic clk);
              // ==== For testing synchronization ====
              event data_sampled;
                      //===== signals Declartion ======
              logic [FIFO_WIDTH-1:0] data_in;
              logic rst_n, wr_en, rd_en;
              logic [FIFO_WIDTH-1:0] data_out;
              logic wr_ack, overflow;
              logic full, empty, almostfull, almostempty, underflow;
                      //====== modpots =======
              modport DUT ( input data_in, clk, rst_n, wr_en, rd_en
18
                               , output data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow);
19
              modport TB ( input data_out, wr_ack, overflow, full, empty, almostfull, almostempty, underflow
21
                               , output data_in, clk, rst_n, wr_en, rd_en, import trigger_sample);
22
              \verb|modport MON ( input data_in, clk, rst_n, wr_en, rd_en, data_out, full, empty, almostfull, almostempty, almostempty, almostempty, almostempty, almostfull, almostempty, almoste
                                           overflow, underflow, wr_ack, import trigger_sample);
              // ==== Task to trigger sampling event ====
                      task trigger_sample();
                      -> data_sampled;
                      endtask
32 endinterface
     1.3 Top Module
 import Shared_pkg::*;
 3 module FIFO_top;
              // ===== Generate Clock =====
              bit clk;
              initial begin
                      clk = 0;
                      forever #5 clk = ~clk; // 200 MHZ
              // ===== interface instance =====
              FIFO_IF fifo_intf (clk);
              // ===== Instantiate DUT =====
              FIFO #(
                      .FIFO_WIDTH(FIFO_WIDTH),
                      .FIFO_DEPTH(FIFO_DEPTH)
             ) dut (
                      .fifo_intf(fifo_intf)
              // ===== Instantiate testbench =====
              FIFO_tb tb (
                      .fifo_intf(fifo_intf)
25
26
27
              // ===== Instantiate monitor =====
28
              FIFO_monitor mon
                       .fifo_intf(fifo_intf)
31
32
```

1.4 Transaction Package

33

34 endmodule

```
package FIFO_transaction_pkg;

import Shared_pkg::*;
```

```
5 class FIFO_transaction;
      // -----
      // Transaction Distribution "Set to Default Values"
      // Variable For parametrized Class "Class Signature"
      // -----
      int RD_EN_ON_DIST;
      int WR_EN_ON_DIST;
      // ==== input signals ====
      rand bit rst_n;
      rand bit [FIFO_WIDTH-1:0] data_in;
      rand bit wr_en;
      rand bit rd_en;
      // ==== output signals ====
      bit [FIFO_WIDTH-1:0] data_out;
      bit wr_ack, overflow;
22
      bit full, empty, almostfull, almostempty, underflow;
         // -----
      // Dassert Reset "Asyn - Active Low" most of the times
      // -----
         constraint rst_c { rst_n dist {0:/15 , 1:/85};}
      // -----
      // Only, Enable Write Enable Signal During "WR_EN_ON_DIST"
      // -----
      constraint wr_en_c { wr_en dist {1 := WR_EN_ON_DIST, 0 := 100-WR_EN_ON_DIST};}
      // -----
      // Only, Enable Read Enable Signal During "RD_EN_ON_DIST"
      // -----
      constraint rd_en_c { rd_en dist {1 := RD_EN_ON_DIST, 0 := 100-RD_EN_ON_DIST};}
      // ======
      // Class Constructor
      // =========
      function new (int rd_dist = 30 ,int wr_dist = 70);
         RD_EN_ON_DIST = rd_dist;
         WR_EN_ON_DIST = wr_dist;
      endfunction
48 endclass
49 endpackage
  1.5 Coverage Package
package FIFO_coverage_pkg;
  import FIFO_transaction_pkg::*;
  import Shared_pkg::*;
  class FIFO_coverage;
      // ===== create object ======
      FIFO_transaction F_cvg_txn;
         // ===== Cover Group =====
      covergroup fifo_cg;
12
         // ===== Cover I/O Ports =====
         rst_n_cp: coverpoint F_cvg_txn.rst_n;
         data_in_cp: coverpoint F_cvg_txn.data_in;
         r_en_cp: coverpoint F_cvg_txn.rd_en;
         w_en_cp: coverpoint F_cvg_txn.wr_en;
         data_out_cp: coverpoint F_cvg_txn.data_out;
                       coverpoint F_cvg_txn.wr_ack;
         wr_ack_cp:
         wr_ack_cp: coverpoint F_cvg_txn.wr_ack;
overflow_cp: coverpoint F_cvg_txn.overflow;
21
         full_cp: coverpoint F_cvg_txn.full;
                   coverpoint F_cvg_txn.empty;
         empty_cp:
         almostfull_cp: coverpoint F_cvg_txn.almostfull;
         almostempty_cp: coverpoint F_cvg_txn.almostempty;
         underflow_cp: coverpoint F_cvg_txn.underflow;
         // ===== "7" Cross Coverage =====
         wr_ack_cross: cross r_en_cp ,w_en_cp ,wr_ack_cp{
             ignore_bins w_en_nactv_wr_ack
                                            = binsof(w_en_cp) intersect {1'b0} && binsof(wr_ack_cp) intersect {1'b1};
32
         full_cross:
                         cross r_en_cp ,w_en_cp ,full_cp{
33
            // full not asserted when both read and write enabled
34
             ignore_bins w_en_r_en_allactv_full = binsof(w_en_cp) intersect {1'b1} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
35
                intersect {1'b1};
             // full not asserted when read enabled
36
             ignore_bins r_en_actv_wr_full
                                           = binsof(w_en_cp) intersect {1'b0} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
37
                intersect {1'b1};
         }
38
39
                          cross r_en_cp ,w_en_cp ,empty_cp{
         empty_cross:
                                            = binsof(r_en_cp) intersect {1'b0} && binsof(empty_cp) intersect {1'b1};
41
             ignore_bins read_nactv_empty
42
43
         almostfull\_cross: cross r\_en\_cp , w\_en\_cp , almostfull\_cp\{
44
                // who almostfull with read
45
                                           = binsof(r_en_cp) intersect {1'b0} && binsof(almostfull_cp) intersect {1'b1};
             ignore_bins w_en_nactv_almostfull
46
         }
47
         49
             // who almostempty with write
```

```
}
           overflow_cross:
                            cross r_en_cp ,w_en_cp ,overflow_cp{
               ignore_bins w_en_nactv_wr_ack
                                               = binsof(w_en_cp) intersect {1'b0} && binsof(overflow_cp) intersect {1'b1};
56
57
           underflow_cross: cross r_en_cp ,w_en_cp ,underflow_cp{
59
               ignore_bins r_en_nactv_wr_ack
                                                     = binsof(r_en_cp) intersect {1'b0} && binsof(underflow_cp) intersect {1'b1};
61
62
63
       endgroup
64
       // ===== Constructor =====
65
       function new();
           fifo_cg = new();
67
           F_cvg_txn = new();
68
       endfunction
       // ===== Sample Data Method =====
71
       function void sample_data(FIFO_transaction F_txn);
       F_cvg_txn = F_txn;
73
74
       // === Trigger Sampling ===
       fifo_cg.sample();
       endfunction
78 endclass
79 endpackage
        scoreboard Package
package FIFO_scoreboard_pkg;
     import FIFO_transaction_pkg::*;
     import Shared_pkg::*;
     class FIFO_scoreboard;
       // ====== Reference Model Signals =======
       bit [FIFO_WIDTH-1:0] data_out_ref;
       bit wr_ack_ref, overflow_ref;
       \verb|bit full_ref|, \verb|empty_ref|, \verb|almostfull_ref|, \verb|almostempty_ref|, \verb|underflow_ref|; \\
       // ===== #No Of Location In FIFO =====
       localparam max_fifo_addr = $clog2(FIFO_DEPTH);
13
14
       // ====== Internal FIFO model =======
       bit [FIFO_WIDTH-1:0] FIFO [$]; // FIFO == Queue "first in - first out"
       bit [max_fifo_addr-1:0] write_ptr;
       bit [max_fifo_addr-1:0] read_ptr;
       int count;
19
       bit [FIFO_WIDTH-1:0] last_data_in;
       // ====== Create object ======
22
       FIFO_transaction F_txn = new();
24
       // ====== Reference model to calculate expected outputs ======
25
       function void reference_model(FIFO_transaction F_txn);
26
           // ====== Capture input ======
27
           last_data_in = F_txn.data_in;
28
           // ======= Handle reset: clear pointers, count, memory, and outputs =======
31
           if (F_txn.rst_n == 0) begin
               write_ptr = 'b0;
                              = 'b0;
33
               read_ptr
                              = 0;
34
               data_out_ref = 'b0;
               wr_ack_ref
                              = 0;
36
               overflow_ref
                              = 0;
37
               underflow_ref = 0;
                              = 0;
               {\tt full\_ref}
                              = 1;
               empty_ref
               almostfull_ref = 0;
               almostempty_ref = 0;
42
43
               FIFO.delete();
                  end else begin
               // ===== Default outputs for non-reset =====
                //overflow_ref
                                = 0;
               //underflow_ref = 0;
48
                   // Case: Write Enable
50
                   if (F_txn.wr_en && count < FIFO_DEPTH) begin</pre>
51
                   FIFO.push_back(last_data_in);
                   write_ptr = write_ptr + 'b1;
53
                   wr_ack_ref = 1'b1;
54
55
                  end else begin
                            wr_ack_ref = 1'b0;
56
                            if (F_txn.wr_en && count == FIFO_DEPTH) begin
57
                        // overflow when full
                       overflow_ref = 1'b1;
59
                    end else begin
60
61
                       overflow_ref = 1'b0;
                    end
62
                   end
63
64
                   // Case: Read Enable
65
                   if (F_txn.rd_en && count != 0) begin
66
                     data_out_ref = FIFO.pop_front();
67
                     read_ptr = read_ptr + 'b1 ;
```

ignore_bins w_en_nactv_almostempty = binsof(w_en_cp) intersect {1'b0} && binsof(almostempty_cp) intersect {1'b1};

```
end else begin
                                      if (F_txn.rd_en && count == 0) begin
                                          // underflow when empty
                                          underflow_ref = 1'b1;
                               end else begin
                                          underflow_ref = 1'b0;
                       end
                       // Case: write Enable and not Full
                       if (!F_txn.rd_en && F_txn.wr_en && !full_ref) begin
                                             count++;
                               // Case: Read Enable and not Empty
                               end else if (F_txn.rd_en && !F_txn.wr_en && !empty_ref) begin
                                      count --;
                       // Case: simultaneous read & write
                       end else if (F_txn.wr_en && F_txn.rd_en && empty_ref) begin
                                       // empty: only write
                               count++;
                       end else if (F_txn.wr_en && F_txn.rd_en && full_ref) begin
                               // full: only read
                                count --;
                               end
               // ===== Update status flags =====
                                          = (count == 0);
               empty_ref
                                            = (count == FIFO_DEPTH);
               full_ref
               almostfull_ref = (count == FIFO_DEPTH-1);
               almostempty_ref = (count == 1);
        endfunction
        // ===== Function to check data by comparing actual outputs with reference model ======
        function void check_data(FIFO_transaction F_txn);
               // ===== Compute expected =====
               reference_model(F_txn);
               // ===== Compare =====
               // === Use Force Equality ===
               if (F_txn.data_out === data_out_ref
                                                                                            &&
                                                        === wr_ack_ref
                       F_{txn.wr_ack}
                       F_txn.overflow === overflow_ref
                                                                                           &&
                       F_txn.underflow === underflow_ref &&
                                                        === full_ref
                       F_txn.full
                               F_{txn.empty}
                                                           === empty_ref
                       F_txn.almostfull === almostfull_ref &&
                               F_txn.almostempty=== almostempty_ref) begin
                               correct_count++;
               end else begin
                               error_count++;
                               $display("ERROR_at_time_%Ot:", $time);
                                                                                                                 \texttt{$display("$_{\sqcup\sqcup}$ data$_{\out}$:$_{\sqcup}$Exp=%h,$_{\sqcup}$Got=%h", $data$_{\out}$ref, $F_{txn}.data$_{\out}$);}
                               if (F_txn.data_out !== data_out_ref)
                                                                        !== wr_ack_ref)
                                                                                                                 $display("uuwr_ackuuuuu:uExp=%b,uGot=%b", wr_ack_ref, F_txn.wr_ack);
                               if (F_txn.wr_ack
                                                                                                                 \texttt{$display("$_{\sqcup\sqcup}$ overflow$_{\sqcup\sqcup\sqcup}:$_{\sqcup}$ Exp=$_{b},$_{\sqcup}$ Got=$_{b}", overflow$_{ref}, F$_{txn.overflow});}
                               if (F_txn.overflow
                                                                      !== overflow_ref)
                               if (F_txn.underflow !== underflow_ref)
                                                                                                                 $display("uunderflowuu:uExp=%b,uGot=%b", underflow_ref, F_txn.underflow);
                                                                       !== full_ref)
                                                                                                                 $display("uufulluuuuuu:uExp=%b,uGot=%b", full_ref, F_txn.full);
                               if (F_txn.full
                                                                       !== empty_ref)
                                                                                                                 display("uuemptyuuuuuu: uExp=%b,uGot=%b", empty_ref, F_txn.empty);
                               if (F_txn.empty
                               if (F_txn.almostfull !== almostfull_ref)
                                                                                                                \texttt{$display("$\sqcup$\sqcup$almostfull$\sqcup$:$\sqcup$Exp=$b$,$\sqcup$Got=$b$", almostfull$\_ref, F$\_txn.almostfull);}
                               if (F_txn.almostempty! == almostempty_ref) $\frac{1}{3}\text{display}(\(\pi_{\pi_\pi}\almostempty:\pi\binostempty:\pi\binostempty:\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostempty.\pi\binostem
               end
        endfunction
    endclass
endpackage
         Monitor Package
import Shared_pkg::*;
```

```
module FIF0_monitor (FIF0_IF.MON fifo_intf);
     // ===== Import required packages =====
     import FIFO_transaction_pkg::*;
     import FIFO_coverage_pkg::*;
     import FIFO_scoreboard_pkg::*;
     import Shared_pkg::*;
     // ===== Create class objects =====
     FIFO_transaction fifo_txn;
12
     FIFO_scoreboard fifo_scb;
13
     FIFO_coverage fifo_cov;
14
15
     initial begin
       // ==== Create objects ====
17
       fifo_txn = new();
18
       fifo_scb = new();
19
       fifo_cov = new();
20
21
       // ==== Start monitoring ====
22
       forever begin
23
         // ==== Wait for negedge clock to sample data ====
24
         @(negedge fifo_intf.clk);
25
26
         // ==== Wait for sampling event from testbench ====
27
         fifo_intf.trigger_sample();
28
29
         // ==== Sample the interface and update transaction object ====
30
         // ==== Input =====
31
         fifo_txn.data_in = fifo_intf.data_in;
```

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129 130

131 132

```
fifo_txn.wr_en = fifo_intf.wr_en;
        fifo_txn.rd_en = fifo_intf.rd_en;
        fifo_txn.rst_n = fifo_intf.rst_n;
        // ==== Output =====
        fifo_txn.data_out = fifo_intf.data_out;
        fifo_txn.full = fifo_intf.full;
        fifo_txn.empty = fifo_intf.empty;
39
        fifo_txn.almostfull = fifo_intf.almostfull;
        fifo_txn.almostempty = fifo_intf.almostempty;
41
        fifo_txn.overflow = fifo_intf.overflow;
        fifo_txn.underflow = fifo_intf.underflow;
43
        fifo_txn.wr_ack = fifo_intf.wr_ack;
44
        // ==== Fork-join to run coverage and scoreboard in parallel ====
          // ==== Process 1: Sample coverage ====
          fifo_cov.sample_data(fifo_txn);
                  begin
50
              // ==== Process 2: Check data with scoreboard ====
              @(posedge fifo_intf.clk);
              // ====== Wait Output To Be Stable ======
              fifo_scb.check_data(fifo_txn);
         join
        // Check if test is finished
        if (test_finished) begin
          // Display test summary
61
          $display("Test_Summary:");
62
          $display("□□Total□Correct:□%0d", correct_count);
          display("uuCoverage:u%0.2f%%", fifo_cov.fifo_cg.get_coverage());
          $stop;
        end
      end
    end
70 endmodule
  1.8 Testbench
module FIFO_tb(FIFO_IF.TB fifo_intf);
    import FIFO_transaction_pkg::*;
    import Shared_pkg::*;
    // ===== Create transaction object =====
    FIFO_transaction fifo_txn;
    initial begin
      // ===== Create transaction object =====
      fifo_txn = new();
11
      // ===== Disable randomization & constrain =====
13
      fifo_txn.rand_mode(0);
      fifo_txn.constraint_mode(0);
15
16
```

```
// ===== Initialize fifo inputs =====
       fifo_intf.data_in = 0;
       fifo_intf.wr_en = 0;
19
       fifo_intf.rd_en = 0;
       fifo_intf.rst_n = 0;
21
22
       // ===== Trigger sample event for monitor =====
       fifo_intf.trigger_sample();
24
       // ===== Apply reset for a few cycles =====
       repeat(2) @(posedge fifo_intf.clk);
28
       // ===== Apply Release reset =====
       fifo_intf.rst_n = 1;
       repeat(2) @(posedge fifo_intf.clk);
34
       // ==== Enable randomization & constrain =====
       fifo_txn.rand_mode(1);
       fifo_txn.constraint_mode(1);
       // ===== Start Randomaize Test Tramsactions
       for (int i = 0; i < TEST_COUNT; i++) begin</pre>
           // ===== Randomize transaction =====
           if (!fifo_txn.randomize()) begin
41
               $error("Randomization_failed_at_iteration_%0d", i);
42
44
45
           // ===== Wait for negedge clock =====
           @(negedge fifo_intf.clk);
47
48
           // ===== Drive inputs from transaction =====
           fifo_intf.data_in = fifo_txn.data_in;
50
           fifo_intf.wr_en = fifo_txn.wr_en;
51
                            = fifo_txn.rd_en;
           fifo_intf.rd_en
52
           fifo_intf.rst_n = fifo_txn.rst_n;
53
54
           // ===== Trigger sample event for monitor =====
55
           fifo_intf.trigger_sample();
56
57
58
       end
```

```
// ===== Signal end of test =====
       repeat(5) @(posedge fifo_intf.clk);
       test_finished = 1;
       // ===== Wait a few more cycles for monitor to process results =====
       repeat(5) @(posedge fifo_intf.clk);
65
68 endmodule
        Design With Bugs + SVA
module FIFO(FIFO_IF.DUT fifo_intf);
parameter FIFO_WIDTH = 16;
  parameter FIFO_DEPTH = 8;
5 localparam max_fifo_addr = $clog2(FIFO_DEPTH);
   reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];
9 reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
       if (!fifo_intf.rst_n) begin
13
           wr_ptr <= 0;
15
       else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin</pre>
16
           mem[wr_ptr] <= fifo_intf.data_in;</pre>
           fifo_intf.wr_ack <= 1;
           wr_ptr <= wr_ptr + 1;
19
21
       else begin
           fifo_intf.wr_ack <= 0;
22
           if (fifo_intf.full & fifo_intf.wr_en)
               fifo_intf.overflow <= 1;</pre>
24
               fifo_intf.overflow <= 0;</pre>
27
       end
28 end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
       if (!fifo_intf.rst_n) begin
31
           rd_ptr <= 0;
33
       else if (fifo_intf.rd_en && count != 0) begin
34
          fifo_intf.data_out <= mem[rd_ptr];</pre>
35
           rd_ptr <= rd_ptr + 1;
38 end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
41
       if (!fifo_intf.rst_n) begin
           count <= 0;
42
       else begin
          if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
45
               count <= count + 1;</pre>
           else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
               count <= count - 1;</pre>
50 end
51
assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0)? 1 : 0;
assign fifo_intf.underflow = (fifo_intf.empty && fifo_intf.rd_en)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;
_{60} // Assertions using conditional compilation
'ifdef SIM
       // ===== Reset behavior assertion =====
64
       property reset_behavior;
           @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=> (count == 0 && rd_ptr == 0 && wr_ptr == 0
                        && !fifo_intf.wr_ack && !fifo_intf.overflow && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
       endproperty
       // ===== Write acknowledge assertion =====
69
       property write_ack_check;
70
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
71
       endproperty
72
73
       // ===== Overflow detection assertion =====
74
       property overflow_check;
75
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
76
              fifo_intf.overflow;
       endproperty
78
       // ===== Underflow detection assertion =====
79
       property underflow_check;
80
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
81
       endproperty
82
83
       // ===== Empty flag assertion =====
84
       property empty_flag_check;
85
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == 0) |-> fifo_intf.empty;
       endproperty
```

```
// ===== Full flag assertion =====
        property full_flag_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH) |-> fifo_intf.full;
        endproperty
93
        // ===== Almost full condition assertion =====
94
        property almost_full_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
        endproperty
98
        // ===== Almost empty condition assertion =====
99
100
        property almost_empty_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == 1) |-> fifo_intf.almostempty;
101
        endproperty
103
        // ===== Pointer wraparound assertion for write_ptr =====
104
        property write_ptr_wraparound;
105
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && wr_ptr == FIF0_DEPTH-1) |=>
                (wr_ptr == 0);
        endproperty
        // ===== Pointer wraparound assertion for read_ptr =====
109
        property read_ptr_wraparound;
110
            Q(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && rd_ptr == FIFO_DEPTH-1) |=>
111
               (rd_ptr == 0);
        endproperty
112
113
        // ==== Pointer threshold assertion for write_ptr =====
114
        property write_ptr_threshold;
115
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (wr_ptr < FIFO_DEPTH);</pre>
116
        endproperty
117
118
        // ===== Pointer threshold assertion for read_ptr =====
119
        property read_ptr_threshold;
120
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (rd_ptr < FIFO_DEPTH);
121
122
        endproperty
123
        // ===== Counter threshold assertion =====
124
125
        property counter_threshold;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count <= FIFO_DEPTH);</pre>
126
        endproperty
127
128
        // ===== Assert all the properties =====
129
        assert property (reset_behavior)
                                                else $error("Reset_behavior_assertion_failed!");
        assert property (write_ack_check)
                                                else $error("Write acknowledge assertion failed!");
131
        assert property (overflow_check)
                                                else $error("Overflow_detection_assertion_failed!");
132
        assert property (underflow_check)
                                                 else $error("Underflow_detection_assertion_failed!");
133
                                                else $error("Emptyuflaguassertionufailed!");
        assert property (empty_flag_check)
134
        assert property (full_flag_check)
                                                else $error("Full_flag_assertion_failed!");
135
        assert property (almost_full_check)
                                                else $error("Almost | full | condition | assertion | failed!");
136
                                                else $error("Almost⊥empty⊥condition⊥assertion⊥failed!");
137
        assert property (almost_empty_check)
        assert property (write_ptr_wraparound) else $error("Write_pointer_wraparound_assertion_failed!");
138
139
        assert property (read_ptr_wraparound)
                                                else $error("Read_pointer_wraparound_assertion_failed!");
                                                else $error("Write pointer threshold assertion failed!");
        assert property (write_ptr_threshold)
140
        assert property (read_ptr_threshold)
                                                 else $error("Read_pointer_threshold_assertion_failed!");
141
        assert property (counter_threshold)
                                                else $error("Counter threshold assertion failed!");
142
143
144
        cover property (reset_behavior);
145
        cover property (write_ack_check);
        cover property (overflow_check);
146
        cover property (underflow_check);
147
        cover property (empty_flag_check);
148
        cover property (full_flag_check);
149
150
        cover property (almost_full_check);
        cover property (almost_empty_check);
151
        cover property (write_ptr_wraparound);
152
        cover property (read_ptr_wraparound);
153
154
        cover property (write_ptr_threshold);
        cover property (read_ptr_threshold);
155
        cover property (counter_threshold);
156
157
158 'endif
160 endmodule
    1.10 Corrected Design + SVA
    module FIFO(FIFO_IF.DUT fifo_intf);
   parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 8;
 5 localparam max_fifo_addr = $clog2(FIFO_DEPTH);
 reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
    reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;
11
    always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13
        if (!fifo_intf.rst_n) begin
            wr_ptr <= 0;
14
            fifo_intf.wr_ack <= 0;
15
            fifo_intf.overflow <= 0;</pre>
16
17
        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin</pre>
18
            mem[wr_ptr] <= fifo_intf.data_in;</pre>
19
            fifo_intf.wr_ack <= 1;</pre>
20
            wr_ptr <= wr_ptr + 1;
21
        end
```

```
else begin
24
           fifo_intf.wr_ack <= 0;
            if (fifo_intf.full & fifo_intf.wr_en)
               fifo_intf.overflow <= 1;</pre>
            else
                fifo_intf.overflow <= 0;</pre>
28
29
30 end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
       if (!fifo_intf.rst_n) begin
           rd_ptr <= 0;
34
35
            fifo_intf.underflow <= 0;</pre>
           fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};</pre>
36
37
       else if (fifo_intf.rd_en && count != 0) begin
           fifo_intf.data_out <= mem[rd_ptr];</pre>
39
           rd_ptr <= rd_ptr + 1;
40
41
       else begin
42
           if (fifo_intf.empty & fifo_intf.rd_en)
43
               fifo_intf.underflow <= 1;</pre>
            else
45
               fifo_intf.underflow <= 0;</pre>
46
47
       end
48 end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
       if (!fifo_intf.rst_n) begin
51
52
            count <= 0;
53
       end
       else begin
54
           if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
                count <= count + 1;</pre>
           else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
57
               count <= count - 1;</pre>
            else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.full)
               count <= count - 1;</pre>
            else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.empty)
62
                count <= count + 1;</pre>
       end
63
64 end
assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;
73 // Assertions using conditional compilation
'ifdef SIM
75
       // ===== Reset behavior assertion =====
76
       property reset_behavior;
            @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=> (count == 0 && rd_ptr == 0 && wr_ptr == 0
78
                         && !fifo_intf.wr_ack && !fifo_intf.overflow && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
79
       endproperty
80
81
       // ===== Write acknowledge assertion =====
82
       property write_ack_check;
83
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
85
       endproperty
86
87
       // ===== Overflow detection assertion =====
       property overflow_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
               fifo_intf.overflow;
       endproperty
91
        // ===== Underflow detection assertion =====
       property underflow_check;
93
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
94
        endproperty
       // ===== Empty flag assertion =====
97
       property empty_flag_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == 0) |-> fifo_intf.empty;
        endproperty
100
       // ===== Full flag assertion =====
102
       property full_flag_check;
103
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH) |-> fifo_intf.full;
104
        endproperty
105
106
       // ===== Almost full condition assertion =====
107
       property almost_full_check;
108
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
109
110
       endproperty
112
       // ===== Almost empty condition assertion =====
113
       property almost_empty_check;
           @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count == 1) |-> fifo_intf.almostempty;
114
115
        endproperty
116
       // ===== Pointer wraparound assertion for write_ptr =====
117
       property write_ptr_wraparound;
118
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && wr_ptr == FIFO_DEPTH-1) |=>
119
               (wr_ptr == 0);
       endproperty
```

```
// ===== Pointer wraparound assertion for read_ptr =====
    property read_ptr_wraparound;
        @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && rd_ptr == FIFO_DEPTH-1) |=>
           (rd_ptr == 0);
    endproperty
    // ===== Pointer threshold assertion for write_ptr =====
    property write_ptr_threshold;
        @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (wr_ptr < FIFO_DEPTH);</pre>
    endproperty
    // ===== Pointer threshold assertion for read_ptr =====
    property read_ptr_threshold;
        @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (rd_ptr < FIFO_DEPTH);
    endproperty
    // ===== Counter threshold assertion =====
    property counter_threshold;
        @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (count <= FIFO_DEPTH);
    endproperty
    // ===== Assert all the properties =====
    assert property (reset_behavior)
                                           else $error("Reset_behavior_assertion_failed!");
    assert property (write_ack_check)
                                           else $error("Write acknowledge assertion failed!");
    assert property (overflow_check)
                                           else $error("Overflowudetectionuassertionufailed!");
    assert property (underflow_check)
                                           else $error("Underflow_detection_assertion_failed!");
    assert property (empty_flag_check)
                                           else $error("Empty_flag_assertion_failed!");
                                           else $error("Full | flag | assertion | failed!");
    assert property (full_flag_check)
    assert property (almost_full_check)
                                           else $error("Almostufulluconditionuassertionufailed!");
    assert property (almost_empty_check)
                                           else $error("Almost uempty condition assertion failed!");
    assert property (write_ptr_wraparound) else $error("Write_pointer_wraparound_assertion_failed!");
    assert property (read_ptr_wraparound)
                                           else $error("Read_pointer_wraparound_assertion_failed!");
    assert property (write_ptr_threshold)
                                           else $error("Write_pointer_threshold_assertion_failed!");
    assert property (read_ptr_threshold)
                                           else $error("Read, pointer, threshold, assertion, failed!");
    assert property (counter_threshold)
                                            else $error("Counter threshold assertion failed!");
    cover property (reset_behavior);
    cover property (write_ack_check);
    cover property (overflow_check);
    cover property (underflow_check);
    cover property (empty_flag_check);
    cover property (full_flag_check);
    cover property (almost_full_check);
    cover property (almost_empty_check);
    cover property (write_ptr_wraparound);
    cover property (read_ptr_wraparound);
    cover property (write_ptr_threshold);
    cover property (read_ptr_threshold);
    cover property (counter_threshold);
'endif
endmodule
```

2 Bugs report

123

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Here is a summary of all the bugs in the original FIFO implementation and how each was fixed in the corrected version:

Table 1: Bugs report Bug Original Behavior Fix in Corrected Code Uninitialized On reset, only wr_ptr was cleared. wr_ack and overflow Added wr_ack <= 0; and overflow <= 0; in the reset wr_ack remained unknown until the first write cycle. branch of the write block. overflow unknown data after reset. In the read block's reset clause, added data_out <= data_out never reset {FIFO_WIDTH{1'b0}};. underflow not registered Was a combinational assign (assign underflow = empty Moved underflow into the read always block with its own && rd_en), causing glitches and no clear reset. reset and clear logic "Like overflow". When both wr_en and rd_en were high, count did not Simultaneous read+write Added explicit cases for {wr_en,rd_en}==2'b11: decrement if full, increment if empty. Now cleared (overflow <= 0) whenever !(full & wr_en) Incomplete overflow clearing overflow stayed asserted if writes retried while full. in the write block. "Almost-full" threshold off by Triggered at count == FIFO_DEPTH-2 (two slots left). Changed to almostfull = (count == FIFO_DEPTH-1) (one slot left). Count logic incomplete Only handled two cases (10 and 01), missing the four-state Fully enumerated all four conditions (2'b10, 2'b01, nature of {wr_en,rd_en} 2'b11 & full, 2'b11 & empty).

3 Makefile Contain Do File

```
VSIM = vsim
RUN = run
VLOG = qverilog

# Define testbench Directory
TBDIR = ${FIFO_ROOT}/sv_verification

# Target flist
target = src_files
FLIST = ${target}.list

VPATH = $(TEST_DIR) $(TBDIR)
TBFILES = $(TBDIR)/$(FLIST)

# Define 5 seed values
```

```
SEEDS = 1111 \ 1511 \ 2515 \ 2236 \ 5215
# Targets
clean:
             rm -rf *.log *.dis *.tbl vcs* simv* *.map transcript *.ucdb *.wlf *.txt \
              work dataset.asdb library.cfg work
questa: ${TBFILES}
              $(VLOG) -1 vlog.log -sv -mfcu -f ${TBFILES} +cover -covercells -R +nowarn3829
              $(VSIM) -voptargs=+acc work.FIFO_top -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"
questa+SIM: ${TBFILES}
              VOG -1 vlog.log -sv -mfcu -f TBFILES +define+SIM +cover -covercells -R +nowarn3829
              $(VSIM) -voptargs=+acc work.FIFO-top -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"
# Run simulation with a specific seed
seed%: ${TBFILES}
              @echo "Running simulation with seed $*"
              VLOG - 1 \ vlog \cdot log - sv - mfcu - f  {TBFILES} + define+SIM + cover + cover - covercells - R + nowarn 3829
              $(VSIM) -voptargs=+acc work.FIFO_top -cover -sv_seed $* -do "do wave.do; coverage save FIFO_seed$*.ucdb -onexit; run -all"
              vcover\ report\ FIFO\_seed\$*.ucdb\ -details\ -annotate\ -all\ -output\ code\_coverage\_rpt\_seed\$*.txt\ -du=FIFO\_seed\$*.txt\ -du=FIFO\_see
              vcover\ report\ -details\ -cvg\ -output\ functional\_coverage\_report\_seed\$*.txt\ FIFO\_seed\$*.ucdb
# Run all seeds in sequence
all_seeds: ${TBFILES}
              @echo "Running simulations with all seeds"
              $(VLOG) -1 vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover +cover -covercells -R +nowarn3829
              @for seed in $(SEEDS); do \
                           echo ""; \
                           echo "Running simulation with seed $$seed"; \
                           $(VSIM) -voptargs=+acc work.FIFO_top -cover -sv_seed $$seed -do "do wave.do; coverage save FIFO_seed$$seed.ucdb -onexit;
                           vcover report FIFO_seed$$seed.ucdb -details -annotate -all -output code_coverage_rpt_seed$$seed.txt -du=FIFO; \
                           vcover report -details -cvg -output functional_coverage_report_seed$$seed.txt FIFO_seed$$seed.ucdb; \
              done
              @echo "All seed runs completed"
# Merge coverage results from all seeds
merge_coverage:
              @echo "Merging coverage from all seed runs"
              vcover merge merged.ucdb FIFO_seed*.ucdb
              $(VSIM) -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
              vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
              vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
              @echo "Coverage merged to merged.ucdb and reports saved"
# Run all seeds and merge coverage
run_seeds: all_seeds merge_coverage
              @echo "Complete seed-based simulation and coverage analysis finished"
help:
              @echo Make sure the environment variable FIFO_ROOT is set.
              @echo Possible targets:
              @echo "
                                                     - Run basic simulation"
                             questa
              @echo "
                                                    - Run simulation with +SIM defined"
                             questa+SIM
              @echo "
                             seed < number > - Run simulation with specific seed (e.g., seed1, seed2)"
              @echo "
                                                - Run simulations with all predefined seeds"
                             merge_coverage - Merge coverage data from all seed runs"
              @echo "
                                                    - Run all seeds and merge coverage"
                             {
m run\_seeds}
             @echo "
                             clean
                                                    - Clean up simulation files"
      Functional Coverage Report
        Functional Coverage "seed1" Report
```

Coverage Report by instance with details

```
= Instance: /FIFO_coverage_pkg
— Design Unit: work.FIFO_coverage_pkg
Covergroup Coverage:
    Covergroups
                                      1
                                                                 99.75\%
                                                na
                                                          na
        Coverpoints/Crosses
                                     19
                                                na
                                                          na
                                                                     na
            Covergroup Bins
                                    194
                                               191
                                                           3
                                                                 98.45\%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100		Uncovered
covered/total bins:	191	194	_	
missing/total bins:	3	194	_	
% Hit:	98.45%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	161	1	_	Covered
bin auto [1]	847	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered

covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	18	1	_	Covered
bin auto [1024:2047]	18	1	_	Covered
bin auto $[2048:3071]$	15	1	_	Covered
bin auto [3072:4095]	13	1	_	Covered
bin auto $[4096:5119]$	13	1	_	Covered
bin auto $[5120:6143]$	14	1	_	Covered
bin auto $[6144:7167]$	13	1	_	Covered
bin auto [7168:8191]	18	1	_	Covered
bin auto [8192:9215]	18	1	_	Covered
bin auto [9216:10239]	16	1	_	Covered
bin auto [10240:11263]	14	1	_	Covered
bin auto [11264:12287]	10	1	_	Covered
bin auto [12288:13311]	14	1	_	Covered
bin auto [13312:14335]	19	1	_	Covered
bin auto [14336:15359]	14	1	_	Covered
bin auto [15360:16383]	18	1	_	Covered
bin auto [16384:17407]	21	1	_	Covered
bin auto [17408:18431]	15	1	_	Covered
bin auto [18432:19455]	16	1	_	Covered
bin auto [19456:20479]	11	1	_	Covered
bin auto [20480:21503]	18	1	_	Covered
bin auto [21504:22527]	15	1	_	Covered
bin auto $[22528:23551]$	15	1	_	Covered
bin auto [23552:24575]	$\frac{1}{2}$	1	_	Covered
bin auto [24576:25599]	13	1	_	Covered
bin auto [25600:26623]	10	1	_	Covered
bin auto [26624:27647]	19	1	_	Covered
bin auto [27648:28671]	17	1	_	Covered
bin auto [28672:29695]	17	1	_	Covered
bin auto [29696:30719]	17	1	_	Covered
bin auto [30720:31743]	9	1	_	Covered
bin auto [31744:32767]	18	1	_	Covered
bin auto [32768:33791]	15		_	Covered
· ·		1	_	
bin auto [33792:34815]	$\frac{12}{20}$	1	_	Covered
bin auto [34816:35839]	20	1	_	Covered
bin auto [35840:36863]	11	1	_	Covered
bin auto [36864:37887]	9	1	_	Covered
bin auto [37888:38911]	13	1	_	Covered
bin auto [38912:39935]	19	1	_	Covered
bin auto $[39936:40959]$	19	1	_	Covered
bin auto [40960:41983]	10	1	_	Covered
bin auto $[41984:43007]$	21	1	_	Covered
bin auto $[43008:44031]$	23	1	_	Covered
${ m bin~auto}[44032{:}45055]$	15	1	_	$\operatorname{Covered}$
bin auto $[45056:46079]$	21	1	_	$\operatorname{Covered}$
bin auto $[46080:47103]$	15	1	_	Covered
bin auto [47104:48127]	12	1	_	Covered
bin auto [48128:49151]	19	1	_	Covered
bin auto $[49152:50175]$	7	1	_	Covered
bin auto $[50176:51199]$	18	1	_	Covered
bin auto $[51200:52223]$	20	1	_	Covered
bin auto $[52224:53247]$	13	1	_	Covered
bin auto $[53248:54271]$	19	1	_	Covered
bin auto $[54272:55295]$	24	1	_	Covered
bin auto [55296:56319]	17	1	_	Covered
bin auto [56320:57343]	15	1	_	Covered
bin auto [57344:58367]	20	1	_	Covered
bin auto [58368:59391]	20	1	_	Covered
bin auto [59392:60415]	16	1	_	Covered
bin auto [60416:61439]	11	1	_	Covered
bin auto [61440:62463]	15	1	_	Covered
bin auto [62464:63487]	10	1	_	Covered
bin auto [63488:64511]	12	1	_	Covered
bin auto [64512:65535]	19	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100^{-}	_	
bin auto [0]	675	1	_	Covered
bin auto[1]	333	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	$\overline{0}$	$\stackrel{-}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	329	1	_	Covered
bin auto[1]	679	1	_	Covered
Coverpoint data_out_cp	95.31%	100	_	Uncovered
covered/total bins:	61	64	_	5 , 01 Ou
missing/total bins:	3	64	_	
% Hit:	95.31%	100	_	
bin auto [0:1023]	$\frac{95.51}{516}$	100	_	Covered
bin auto $[0.1023]$ bin auto $[1024:2047]$	6	1	_	Covered
bin auto $[2048:3071]$	10	1	_	Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$	4	1	_	Covered
			_	
bin auto [4096:5119]	4	1	_	Covered
bin auto [5120:6143]	8	1	_	Covered
bin auto [6144:7167]	0	1	_	ZERO
bin auto [7168:8191]	10	1	_	Covered
bin auto [8192:9215]	17	1	_	Covered

1. [0010.1000]	10	4		G 1
bin auto [9216:10239]	12	1	_	Covered
bin auto $[10240:11263]$	4	1	_	Covered
bin auto [11264:12287]	19	1	_	Covered
bin auto [12288:13311]	3	1	_	Covered
bin auto [13312:14335]	15	1	_	Covered
bin auto [14336:15359]	9	1	_	Covered
bin auto $[15360:16383]$	8	1	_	Covered
bin auto [16384:17407]	9	1	_	Covered
bin auto [17408:18431]	8	1	_	Covered
bin auto [18432:19455]	14	1		Covered
			_	
bin auto $[19456:20479]$	5	1	_	Covered
bin auto [20480:21503]	21	1	_	Covered
bin auto [21504:22527]	1	1	_	Covered
bin auto [22528:23551]	9	1	_	Covered
			_	
bin auto $[23552:24575]$	8	1	_	Covered
bin auto $[24576:25599]$	0	1	_	ZERO
bin auto [25600:26623]	4	1	_	Covered
bin auto $[26624:27647]$	9	1	_	Covered
bin auto $[27648:28671]$	6	1	_	Covered
bin auto [28672:29695]	9	1	_	Covered
bin auto [29696:30719]	8	1	_	Covered
bin auto $[30720:31743]$	8	1	_	Covered
bin auto $[31744:32767]$	7	1	_	$\operatorname{Covered}$
bin auto $[32768:33791]$	8	1	_	Covered
bin auto [33792:34815]	2	1	_	Covered
	14	1		Covered
bin auto [34816:35839]			_	
bin auto $[35840:36863]$	3	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	8	1	_	Covered
bin auto [37888:38911]	8	1	_	Covered
bin auto [38912:39935]	$\frac{14}{7}$	1	_	Covered
bin auto $[39936:40959]$	7	1	_	Covered
bin auto [40960:41983]	1	1	_	Covered
bin auto [41984:43007]	7	1	_	Covered
bin auto [43008:44031]	10	1	_	Covered
bin auto $[44032:45055]$	4	1	_	$\operatorname{Covered}$
bin auto $[45056:46079]$	6	1	_	Covered
bin auto [46080:47103]	0	1	_	ZERO
,	ŭ .	1		
bin auto [47104:48127]	9	1	_	Covered
bin auto [48128:49151]	9	1	_	$\operatorname{Covered}$
bin auto [49152:50175]	6	1	_	Covered
bin auto [50176:51199]	3	1	_	Covered
bin auto $[51200:52223]$	9	1	_	Covered
bin auto $[52224:53247]$	23	1	_	Covered
bin auto $[53248:54271]$	10	1	_	Covered
bin auto [54272:55295]	16	1	_	Covered
		_		
$\operatorname{bin} \ \operatorname{auto} \left[55296 \!:\! 56319 \right]$	5	1	_	Covered
bin auto $[56320:57343]$	17	1	_	$\operatorname{Covered}$
bin auto [57344:58367]	8	1	_	Covered
bin auto [58368:59391]	5	1		Covered
		_	_	
$\operatorname{bin} \ \operatorname{auto} \left[59392 \!:\! 60415 \right]$	7	1	_	Covered
bin auto $[60416:61439]$	3	1	_	$\operatorname{Covered}$
bin auto [61440:62463]	5	1	_	Covered
bin auto [62464:63487]	1	1		Covered
	1		_	
bin auto $[63488:64511]$	1	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	8	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2		Covered
			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	449	1	_	Covered
bin auto[1]	559	1		Covered
			_	
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100^{-}	_	
bin auto [0]	976	1		Covered
			_	
bin auto[1]	32	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
			_	
% Hit:	100.00%	100	_	
bin auto [0]	810	1	_	Covered
bin auto[1]	198	1	_	Covered
Coverpoint empty_cp	100.00%	100		Covered
			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	769	1	_	Covered
			_	
bin auto[1]	239	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{2}{2}$		
	-		_	
% Hit:	100.00%	100	_	~
$ \text{bin auto} \left[0 \right]$	820	1	_	Covered
bin auto[1]	188	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
				Jovereu
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	619	1	_	Covered
	019	1	_	
	900	1		
bin auto[1]	389	1	_	Covered
Coverpoint underflow_cp	$389 \\ 100.00\%$	$1\\100$	_ _	Covered Covered

covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	919	1	_	Covered
bin auto[1]	89	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right] >$	188	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	38	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]\!>$	371	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[0 ight] >$	82	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	107	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	222	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	93	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	50	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	192	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	86	1	_	Covered
bin $\langle auto[1], auto[0] \rangle$ bin $\langle auto[0], auto[1], auto[0] \rangle$	360	1	_	Covered
bin $\langle auto[0], auto[1], auto[0] \rangle$	172	1	_	Covered
Illegal and Ignore Bins:	112	1	_	Covered
	21			Occurred
ignore_bin r_en_actv_wr_full			_	
ignore_bin w_en_r_en_allactv_full	34	100	_	Occurred
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] >$	34	1	_	Covered
bin < auto[1], auto[0], auto[1] >	57	1	_	Covered
bin < auto[1], auto[1], auto[0] >	192	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [1], \operatorname{auto} [0] >$	393	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	50	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] >$	134	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	148		_	Occurred
-8				
Cross almostfull cross	100.00%	100	_	Covered
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_ _ _	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins:</pre>	8 0	8 8	_ _ _	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins: % Hit:</pre>	8	8	- - -	Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</pre>	$\begin{array}{c} 8 \\ 0 \\ 100.00\% \end{array}$	8 8 100	_ _ _	
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></pre>	$egin{array}{c} 8 \\ 0 \\ 100.00\% \\ 44 \end{array}$	8 8 100	_ _ _	Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></pre>	$\begin{array}{c} 8 \\ 0 \\ 100.00\% \\ \end{array}$	$ \begin{array}{c} 8 \\ 8 \\ 100 \\ \hline 1 \\ 1 \end{array} $	- - -	Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8 \\ 0 \\ 100.00\% \\ \hline 44 \\ 71 \\ 23 \end{array} $	8 8 100 1 1 1	- - - -	Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[1],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \hline 44 \\ 71 \\ 23 \\ 50 \end{array} $	8 8 100 1 1 1 1	- - - - -	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \hline 44 \\ 71 \\ 23 \\ 50 \\ 182 \end{array} $	8 8 100 1 1 1 1 1	- - - - - -	Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \hline 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ \end{array} $	8 8 100 1 1 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{r} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \end{array} $	8 8 100 1 1 1 1 1 1 1	- - - - - - - -	Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \hline 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ \end{array} $	8 8 100 1 1 1 1 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{r} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ 100.00\% \\ \end{array} $	8 8 100 1 1 1 1 1 1 1 1 1 100	- - - - - - - -	Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins:</auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{r} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ 100.00\% \\ 8 \end{array} $	8 8 100 1 1 1 1 1 1 1 1 100 8	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins:</auto[1],></auto[1],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{r} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ 100.00\% \\ 8 \\ 0 $	8 8 100 1 1 1 1 1 1 1 1 100 8 8	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit:</auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{r} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{r} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ 100.00\% \\ 8 \end{array} $	8 8 100 1 1 1 1 1 1 1 1 100 8	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\% \end{array} $	8 8 100 1 1 1 1 1 1 1 100 8 8 100	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8 \\ 0 \\ 100.00\% \\ \end{array} $ $ \begin{array}{c} 44 \\ 71 \\ 23 \\ 50 \\ 182 \\ 382 \\ 84 \\ 172 \\ 100.00\% \\ 8 \\ 0 \\ 100.00\% \\ \end{array} $	8 8 100 1 1 1 1 1 1 1 100 8 8 100	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]="" auto[1],=""> </auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147 \end{array} $	8 8 100 1 1 1 1 1 1 1 1 100 8 8 100	- - - - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered
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<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> cross overflow_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: </auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147\\ 34\\ 83\\ 101\\ 306\\ 73\\ 139\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\$	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147\\ 34\\ 83\\ 101\\ 306\\ 73\\ 139\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 7\\ 219\\ 25\\ 428\\ 107\\ 222\\ 0\\ 100.00\%\\ 6\\ 0\\ 0 \end{array} $	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins:</auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></pre>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147\\ 34\\ 83\\ 101\\ 306\\ 73\\ 139\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 6\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\ 0\\$	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> cross overflow_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147\\ 34\\ 83\\ 101\\ 306\\ 73\\ 139\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 7\\ 219\\ 25\\ 428\\ 107\\ 222\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%$	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> cross overflow_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack cross underflow_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	8 0 100.00% 44 71 23 50 182 382 84 172 100.00% 8 0 100.00% 125 147 34 83 101 306 73 139 100.00% 6 0 100.00% 7 219 25 428 107 222 0 100.00% 6 0 100.00% 6 6 0 100.00% 6 6 6 6 7 6 6 7 6 7 6 7 6 7 6 7 6 7 6	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross overflow_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack cross underflow_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	$ \begin{array}{c} 8\\ 0\\ 100.00\%\\ 44\\ 71\\ 23\\ 50\\ 182\\ 382\\ 84\\ 172\\ 100.00\%\\ 8\\ 0\\ 100.00\%\\ 125\\ 147\\ 34\\ 83\\ 101\\ 306\\ 73\\ 139\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 7\\ 219\\ 25\\ 428\\ 107\\ 222\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%\\ 6\\ 0\\ 100.00\%$	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> cross overflow_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack cross underflow_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	8 0 100.00% 44 71 23 50 182 382 84 172 100.00% 8 0 100.00% 125 147 34 83 101 306 73 139 100.00% 6 0 100.00% 7 219 25 428 107 222 0 100.00% 6 0 100.00% 6 6 0 100.00% 6 6 6 6 7 6 6 7 6 7 6 7 6 7 6 7 6 7 6	8 8 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

$\begin{array}{l} \text{bin } < \text{auto} \left[0\right] \text{, auto} \left[1\right] \text{, auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right] \text{, auto} \left[0\right] \text{, auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right] \text{, auto} \left[0\right] \text{, auto} \left[0\right] > \end{array}$	$453 \\ 81 \\ 222$	1 1 1	_ _ _	Covered Covered Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

COVERGROUP COVERAGE:

overgroup	Metric	Goal	Bins	Status
YPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100		Uncovered
covered/total bins:	191	194	_	0-1-0-0 (0-1-0-0
missing/total bins:	3	194	_	
% Hit:	98.45%	100	_	C 1
Coverpoint rst_n_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	$\frac{2}{2}$		
% Hit:	100.00%	100	_	
bin auto[0]	161	1	_	Covered
bin auto[1]	847	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$64 \\ 100$	_	
bin auto $[0:1023]$	18	1		Covered
bin auto [1024:2047]	18	1	_	Covered
bin auto [2048:3071]	15	1	_	Covered
bin auto [3072:4095]	13	1	_	Covered
bin auto $[4096:5119]$	13	1	_	$\operatorname{Covered}$
bin auto [5120:6143]	14	1	_	Covered
bin auto [6144:7167]	$\begin{array}{c} 13 \\ 18 \end{array}$	1	_	Covered Covered
bin auto [7168:8191] bin auto [8192:9215]	18	1 1	_	Covered
bin auto [9216:10239]	16	1	_	Covered
bin auto [10240:11263]	14	1	_	Covered
bin auto [11264:12287]	10	1	_	Covered
bin auto [12288:13311]	14	1	_	Covered
bin auto $[13312:14335]$	19	1	_	$\operatorname{Covered}$
bin auto [14336:15359]	14	1	_	Covered
bin auto [15360:16383]	18	1	_	Covered
bin auto [16384:17407]	21	1	_	Covered
bin auto [17408:18431] bin auto [18432:19455]	$\frac{15}{16}$	1 1	_	Covered Covered
bin auto [19456:20479]	11	1	_	Covered
bin auto $[20480:21503]$	18	1	_	Covered
bin auto $[21504:22527]$	15	1	_	Covered
bin auto [22528:23551]	15	1	_	Covered
bin auto $[23552:24575]$	22	1	_	Covered
bin auto [24576:25599]	13	1	_	Covered
bin auto [25600:26623]	10	1	_	Covered
bin auto [26624:27647]	19	1	_	Covered
bin auto $[27648:28671]$ bin auto $[28672:29695]$	17 17	1	_	Covered Covered
bin auto [29696:30719]	17	1	_	Covered
bin auto [30720:31743]	9	1	_	Covered
bin auto [31744:32767]	18	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[32768 \colon\! 33791 \right]$	15	1	_	$\operatorname{Covered}$
bin auto [33792:34815]	$\frac{12}{2}$	1	_	Covered
bin auto [34816:35839]	20	1	_	Covered
bin auto [35840:36863]	$\begin{array}{c} 11 \\ 9 \end{array}$	1	_	Covered Covered
bin auto [36864:37887] bin auto [37888:38911]	13	1	_	Covered
bin auto [38912:39935]	19	1	_	Covered
bin auto [39936:40959]	19	1	_	Covered
bin auto [40960:41983]	10	1	_	Covered
bin auto [41984:43007]	21	1	_	Covered
bin auto $[43008:44031]$	23	1	_	$\operatorname{Covered}$
bin auto [44032:45055]	15	1	_	Covered
bin auto [45056:46079]	21	1	_	Covered
bin auto [46080:47103] bin auto [47104:48127]	$\frac{15}{12}$	1	_	Covered Covered
bin auto [48128:49151]	19	1	_	Covered
bin auto [49152:50175]	7	1	_	Covered
bin auto [50176:51199]	18	1	_	Covered
bin auto [51200:52223]	20	1	_	Covered
bin auto [52224:53247]	13	1	_	Covered
bin auto [53248:54271]	19	1	_	Covered
bin auto [54272:55295]	24	1	_	Covered
bin auto [55296:56319]	17	1	_	Covered
bin auto [56320:57343]	15	1	_	Covered
bin auto [57344:58367]	20	1	_	Covered
bin auto [58368:59391] bin auto [59392:60415]	$\begin{array}{c} 20 \\ 16 \end{array}$	1 1	_	Covered Covered
bin auto $[60416:61439]$	10	1	_	Covered
bin auto $[61440:62463]$	15	1	_	Covered
bin auto $[62464:63487]$	10	1	_	Covered
bin auto [63488:64511]	12	1	_	Covered
bin auto [64512:65535]	19	1	_	Covered
Coverpoint r_en_cp covered/total bins:	100.00%	$100 \\ 2$	_	$\operatorname{Covered}$

O4	100.000	100		
% Hit: bin auto [0]	100.00% 675	$100\\1$	_	Covered
bin auto [1]	333	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0\\100.00\%$	$\begin{array}{c} 2 \\ 100 \end{array}$	_	
bin auto $[0]$	329	100	_	Covered
bin auto[1]	679	1	_	Covered
Coverpoint data_out_cp	95.31%	100	_	Uncovered
covered/total bins:	61	64	_	
missing/total bins: % Hit:	$\begin{array}{c} 3\\95.31\%\end{array}$	$64 \\ 100$	_	
bin auto [0:1023]	516	1	_	Covered
bin auto [1024:2047]	6	1	_	Covered
bin auto [2048:3071]	10	1	_	Covered
bin auto [3072:4095] bin auto [4096:5119]	$rac{4}{4}$	1 1	_	Covered Covered
bin auto [5120:6143]	8	1	_	Covered
bin auto [6144:7167]	0	1	_	ZERO
bin auto [7168:8191]	10	1	_	Covered
$\begin{array}{ll} \text{bin auto} [8192:9215] \\ \text{bin auto} [9216:10239] \end{array}$	17 12	1 1	_	Covered Covered
bin auto $[10240:11263]$	4	1	_	Covered
bin auto [11264:12287]	19	1	_	Covered
bin auto [12288:13311]	3	1	_	Covered
bin auto [13312:14335]	15	1	_	Covered
bin auto [14336:15359] bin auto [15360:16383]	$\frac{9}{8}$	1 1	_	Covered Covered
bin auto [16384:17407]	9	1	_	Covered
bin auto [17408:18431]	8	1	_	Covered
bin auto [18432:19455]	14	1	_	Covered
$egin{array}{ll} { m bin } & { m auto} \left[19456{:}20479 ight] \ { m bin } & { m auto} \left[20480{:}21503 ight] \end{array}$	$5\\21$	1	_	Covered Covered
bin auto $[21504:21505]$	1	1	_	Covered
bin auto [22528:23551]	9	1	_	Covered
bin auto [23552:24575]	8	1	_	Covered
bin auto [24576:25599]	0	1	_	ZERO
$egin{array}{ll} { m bin } & { m auto} \left[25600; 26623 ight] \ { m bin } & { m auto} \left[26624; 27647 ight] \end{array}$	$rac{4}{9}$	1 1	_	Covered Covered
bin auto [27648:28671]	6	1		Covered
bin auto [28672:29695]	9	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \big[29696 \colon\! 30719 \big]$	8	1	_	Covered
bin auto [30720:31743]	8	1	_	Covered
bin auto $[31744:32767]$ bin auto $[32768:33791]$	8	1	_	Covered Covered
bin auto [33792:34815]	$\frac{3}{2}$	1		Covered
bin auto [34816:35839]	$\frac{1}{4}$	1	_	Covered
bin auto $[35840:36863]$	3	1	_	Covered
bin auto [36864:37887]	8	1	_	Covered
bin auto [37888:38911] bin auto [38912:39935]	$\frac{8}{14}$	1	_	Covered Covered
bin auto [39936:40959]	7	1	_	Covered
bin auto [40960:41983]	1	1	_	Covered
bin auto [41984:43007]	7	1	_	Covered
$egin{array}{ll} { m bin \ auto} [43008;44031] \ { m bin \ auto} [44032;45055] \end{array}$	10 4	1	_	Covered Covered
bin auto [45056:46079]	6	1	_	Covered
bin auto [46080:47103]	0	1	_	ZERO
bin auto [47104:48127]	9	1	_	Covered
$egin{array}{lll} { m bin } & { m auto} \left[48128; 49151 ight] \ { m bin } & { m auto} \left[49152; 50175 ight] \end{array}$	9	1	_	Covered Covered
bin auto [49132:30175] bin auto [50176:51199]	3	1	_	Covered
bin auto [51200:52223]	9	1	_	Covered
bin auto [52224:53247]	23	1	_	Covered
bin auto $[53248:54271]$ bin auto $[54272:55295]$	10	1	_	Covered Covered
bin auto $[54272:55295]$ bin auto $[55296:56319]$	16 5	1 1	_	Covered Covered
bin auto [56320:57343]	17	1	_	Covered
bin auto [57344:58367]	8	1	_	Covered
bin auto [58368:59391]	5	1	_	Covered
$egin{array}{ll} { m bin \ auto} [59392\!:\!60415] \ { m bin \ auto} [60416\!:\!61439] \end{array}$	$7 \\ 3$	1	_	Covered Covered
bin auto $[61440:62463]$	5 5	1	_	Covered
bin auto [62464:63487]	1	1	_	Covered
bin auto [63488:64511]	1	1	_	Covered
bin auto [64512:65535]	100.00%	1	_	Covered
Coverpoint wr_ack_cp covered/total bins:	100.00%	$\frac{100}{2}$	_	Covered
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100	_	-
bin auto[0]	449	1	_	Covered
bin auto[1] Coverpoint overflow_cp	$\frac{559}{100.00\%}$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
covered/total bins:	$\frac{100.00\%}{2}$	$\frac{100}{2}$	_	Covered
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	976 32	1	_	Covered Covered
bin auto[1] Coverpoint full_cp	$\frac{32}{100.00\%}$	$1\\100$	_	Covered Covered
covered/total bins:	2	2	_	· · · · · · · · · · · · · · · · · · ·
missing/total bins:	0	2	_	

% Hit:	100.00%	100	_	
bin auto [0]	810	1	_	Covered
bin auto[1]	198	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	769	1	_	Covered
bin auto [1]	239	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	820	1	_	Covered
bin auto $[1]$	188	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	619	1	_	Covered
bin auto[1]	389	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	919	1	_	Covered
bin auto $[1]$	89	1		Covered
Cross wr_ack_cross	100.00%	100		Covered
		6	_	Covered
covered/total bins:	6 0	_	_	
missing/total bins:		6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	1.00	1		C 1
bin < auto[1], auto[1], auto[1] >	188	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	38	1	_	Covered
bin < auto[0], auto[1], auto[1] >	371	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	82	1	_	Covered
$\texttt{bin} \ < \texttt{auto} \ [1] \ , \ \texttt{auto} \ [0] \ , \ \texttt{auto} \ [0] >$	107	1	_	Covered
${\rm bin}\ <\!{\rm auto}[0]\ , {\rm auto}[0]\ , {\rm auto}[0] >$	222	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[1], \operatorname{auto}[1] >$	93	1	_	Covered
	33	-		Covered
	50	1	_	Covered
bin <auto [0],="" [1]="" auto=""> bin <auto [0]="" [1],="" auto=""></auto></auto>			_	
$\begin{array}{ll} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \end{array}$	$50 \\ 192$	1	_ _ _	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
$\begin{array}{ll} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \end{array}$	$50 \\ 192 \\ 86$	1 1	_ _ _ _	Covered Covered Covered
$\begin{array}{ll} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \end{array}$	$50 \\ 192 \\ 86 \\ 360$	1 1 1	- - - -	Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$50 \\ 192 \\ 86$	1 1 1 1	- - - -	Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172	1 1 1 1	- - - -	Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172	1 1 1 1	- - - - -	Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34	1 1 1 1	- - - - -	Covered Covered Covered Covered Covered Occurred
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$	1 1 1 1 1	- - - - -	Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6	1 1 1 1 1 100 6	- - - - - -	Covered Covered Covered Covered Covered Occurred
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0	1 1 1 1 1 100 6 6	- - - - - - -	Covered Covered Covered Covered Covered Occurred
<pre>bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></pre>	50 192 86 360 172 21 34 $100.00%$ 6	1 1 1 1 1 100 6	- - - - - - - -	Covered Covered Covered Covered Covered Occurred
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 100 6 6 100	- - - - - - -	Covered Covered Covered Covered Covered Covered Occurred Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 100 6 6 100	- - - - - - - -	Covered Covered Covered Covered Occurred Occurred Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57	1 1 1 1 1 1 100 6 6 100		Covered Covered Covered Covered Occurred Occurred Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192	1 1 1 1 1 1 100 6 6 100		Covered Covered Covered Covered Occurred Occurred Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393	1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> </auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50	1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393	1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134	1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148	1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
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bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - -	Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lillegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - -	Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> lillegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins:</auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - -	Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore-bin r_en_actv_wr_full ignore-bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - -	Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - - - - -	Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - - - - -	Covered
bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" auto=""> bin <auto ,="" [0]="" auto=""> bin <auto ,="" [0]="" auto=""> lillegal and Ignore Bins:</auto></auto></auto></auto></auto></auto>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - - - - - -	Covered
bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" [1]="" auto=""> bin <auto ,="" [0]="" auto=""> bin <auto ,="" [0]="" auto=""> bin <auto ,="" [0]="" auto=""> lillegal and Ignore Bins:</auto></auto></auto></auto></auto></auto>	50 192 86 360 172 21 34 $100.00%$ 6 0 $100.00%$ 34 57 192 393 50 134 148 $100.00%$ 8 0 $100.00%$ 44 71 23 50 182 382 84 172 $100.00%$ 8 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- - - - - - - - -	Covered
bin <auto ,="" [0]="" [1]="" auto=""></auto>	50 192 86 360 172 21 34 100.00% 6 0 100.00% 34 57 192 393 50 134 148 100.00% 8 0 100.00% 44 71 23 50 182 382 84 172 100.00% 8 0 100.00%	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto ,="" [0]="" [1]="" auto=""></auto>	50 192 86 360 172 21 34 100.00% 6 0 100.00% 34 57 192 393 50 134 148 100.00% 8 0 100.00% 44 71 23 50 182 382 84 172 100.00% 8 0 100.00%	1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto ,="" [0]="" [1]="" auto=""></auto>	50 192 86 360 172 21 34 100.00% 6 0 100.00% 34 57 192 393 50 134 148 100.00% 8 0 100.00% 44 71 23 50 182 382 84 172 100.00% 8 0 100.00%	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

bin < auto[0], auto[0], auto[0] >	139	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	7	1	_	Covered
bin < auto[1], $auto[1]$, $auto[0] >$	219	1	_	Covered
bin < auto[0], $auto[1]$, $auto[1] >$	25	1	_	Covered
bin < auto[0], auto[1], auto[0] >	428	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0] >$	107	1	_	Covered
bin < auto[0], auto[0], auto[0] >	222	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} < \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight] >$	63	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight]$, $\operatorname{auto}\left[0 ight]$, $\operatorname{auto}\left[1 ight]>$	26	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight]$, $\operatorname{auto}\left[1 ight]$, $\operatorname{auto}\left[0 ight]>$	163	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight]$, $\operatorname{auto}\left[1 ight]$, $\operatorname{auto}\left[0 ight]>$	453	1	_	Covered
${\rm bin}\ {<} {\rm auto}\left[1\right], {\rm auto}\left[0\right], {\rm auto}\left[0\right] >$	81	1	_	Covered
${\rm bin}\ {<} {\rm auto} \left[0 \right], {\rm auto} \left[0 \right], {\rm auto} \left[0 \right] >$	222	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 99.75% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.75%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Typ
/FIFO_top/dut/cov	SVA	1	Off	847	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	847	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	847	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	2	1	Unli	1	100%		V	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	19	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	187	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	23	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	32	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	194	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	58	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	20	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	473	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	161	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 1: SVA "Seed1"

4.2 Functional Coverage "seed2" Report

Coverage Report by instance with details

_____Instance. /FIFO coverage plan

Instance: /FIFO_coverage_pkg
Design Unit: work.FIFO_coverage_pkg

Covergroup Coverage:

 Covergroups
 1
 na
 na
 99.83%

 Coverpoints/Crosses
 19
 na
 na
 na

 Covergroup Bins
 194
 192
 2
 98.96%

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100		Uncovered
covered/total bins:	192	194	_	
missing/total bins:	2	194	_	
% Hit:	98.96%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	156	1	_	Covered
bin auto [1]	852	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	22	1	_	Covered
bin auto $[1024:2047]$	15	1	_	Covered
bin auto [2048:3071]	12	1	_	Covered
bin auto $[3072:4095]$	16	1	_	Covered
bin auto $[4096:5119]$	18	1	_	Covered
bin auto $[5120:6143]$	11	1	_	Covered
bin auto [6144:7167]	20	1	_	Covered
bin auto [7168:8191]	16	1	_	Covered
bin auto [8192:9215]	24	1	_	Covered
bin auto $[9216:10239]$	19	1	_	Covered
bin auto $[10240:11263]$	17	1	_	Covered
bin auto $[11264:12287]$	10	1	_	Covered
bin auto [12288:13311]	9	1	_	Covered

bin auto [13312:14335]				
	13	1	_	Covered
bin auto $[14336:15359]$	13	1	_	Covered
bin auto [15360:16383]	17	1	_	Covered
bin auto [16384:17407]	15	1	_	Covered
bin auto [17408:18431]	21	1	_	Covered
bin auto [18432:19455]	13	1	_	Covered
bin auto [19456:20479]	19	1	_	Covered
bin auto [20480:21503]	8	1		Covered
			_	
bin auto $[21504:22527]$	11	1	_	Covered
bin auto $[22528:23551]$	11	1	_	Covered
bin auto $[23552:24575]$	12	1	_	Covered
bin auto $[24576:25599]$	13	1	_	Covered
bin auto [25600:26623]	8	1	_	Covered
bin auto [26624:27647]	12	1	_	Covered
bin auto [27648:28671]	17	1	_	Covered
bin auto [28672:29695]	10	1	_	Covered
bin auto [29696:30719]	20	1	_	Covered
bin auto [30720:31743]	20	1	_	Covered
bin auto $[31744:32767]$	20	1	_	Covered
bin auto $[32768:33791]$	13	1	_	Covered
bin auto [33792:34815]	21	1	_	Covered
bin auto [34816:35839]	14	1	_	Covered
bin auto [35840:36863]	18	1	_	Covered
bin auto [36864:37887]	18	1	_	Covered
	14	1		Covered
bin auto [37888:38911]			_	
bin auto [38912:39935]	17	1	_	Covered
bin auto $[39936:40959]$	15	1	_	Covered
bin auto $[40960:41983]$	15	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	14	1	_	$\operatorname{Covered}$
bin auto [43008:44031]	16	1	_	Covered
bin auto [44032:45055]	12	1	_	Covered
bin auto [45056:46079]	$\frac{12}{22}$	1	_	Covered
bin auto $[46080:470073]$	17	1	_	Covered
bin auto [47104:48127]	14	1	_	Covered
bin auto $[48128:49151]$	17	1	_	Covered
bin auto $[49152:50175]$	15	1	_	$\operatorname{Covered}$
bin auto $[50176:51199]$	13	1	_	$\operatorname{Covered}$
bin auto [51200:52223]	16	1	_	Covered
bin auto [52224:53247]	24	1	_	Covered
bin auto [53248:54271]	17	1	_	Covered
bin auto $[54272:55295]$	18	1	_	Covered
		1		
bin auto [55296:56319]	18	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[56320 \colon 57343 \right]$	15	1	_	$\operatorname{Covered}$
bin auto $[57344:58367]$	19	1	_	$\operatorname{Covered}$
bin auto [58368:59391]	15	1	_	Covered
bin auto [59392:60415]	14	1	_	Covered
bin auto [60416:61439]	17	1	_	Covered
bin auto [61440:62463]	12	1	_	Covered
	16	1		
bin auto $[62464:63487]$	10	1	_	Covered
1: (00400 04511)	0.4	4		$\operatorname{Covered}$
bin auto [63488:64511]	24	1	_	
bin auto [64512:65535]	16	1 1	_	Covered
		$\begin{matrix}1\\1\\100\end{matrix}$		
bin auto [64512:65535]	16	_		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins:	$16\\100.00\%$	100		Covered
$egin{array}{lll} { m bin auto} \left[64512 {:} 65535 ight] \ { m Coverpoint r_en_cp} \ { m covered/total bins:} \ { m missing/total bins:} \end{array}$	$16 \\ 100.00\% \\ 2 \\ 0$	100 2 2		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit:	$16 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\%$	100 2 2 100		Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0]	$16 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 731$	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $		Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1]	16 $100.00%$ 2 0 $100.00%$ 731 277	100 2 2 100 1 1		Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp	$16 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 731 \\ 277 \\ 100.00\%$	100 2 2 100 1 1 100		Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins:	$16 \\ 100.00\%$ $2 \\ 0 \\ 100.00\%$ $731 \\ 277 \\ 100.00\%$ 2	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 100 \\ 2 \end{array} $		Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \end{array} $		Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 100 \\ 2 \end{array} $		Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \end{array} $		Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100	 	Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717	100 2 2 100 1 1 100 2 2 100 1 1 1	 	Covered Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$	100 2 2 100 1 1 100 2 2 100 1	 	Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62	100 2 2 100 1 1 100 2 2 100 1 1 100 64	 	Covered Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64	 	Covered Covered Covered Covered Covered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100		Covered Covered Covered Covered Covered Uncovered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins:	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [8192:9215] bin auto [8192:9215] bin auto [9216:10239]	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Uncovered Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [64512:65535] Coverpoint r_en_cp	16 $100.00%$ 2 0 $100.00%$ 731 277 $100.00%$ 2 0 $100.00%$ 291 717 $96.87%$ 62 2 $96.87%$ 557 2 7 15 8 5 32 19 12 2 2 11 1 1 1 1 1 1 1 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

bin auto $[25600:26623]$	21	1	_	Covered
bin auto $[26624:27647]$	2	1	_	Covered
bin auto $[27648:28671]$	1	1	_	Covered
bin auto [28672:29695]	8	1	_	Covered
bin auto [29696:30719]	5	1	_	Covered
bin auto [30720:31743]	6	1	_	Covered
· J	13			Covered
bin auto [31744:32767]		1	_	
bin auto [32768:33791]	1	1	_	Covered
bin auto [33792:34815]	17	1	_	Covered
bin auto [34816:35839]	9	1	_	Covered
bin auto [35840:36863]	10	1	_	Covered
bin auto [36864:37887]	2	1	_	Covered
bin auto [37888:38911]	3	1		Covered
			_	
bin auto [38912:39935]	11	1	_	Covered
${ m bin \ auto} [39936{:}40959]$	2	1	_	Covered
bin auto $[40960:41983]$	0	1	_	ZERO
bin auto [41984:43007]	4	1	_	Covered
bin auto $[43008:44031]$	14	1	_	Covered
bin auto [44032:45055]	8	1		Covered
i i			_	
bin auto [45056:46079]	9	1	_	Covered
bin auto $[46080:47103]$	15	1	_	$\operatorname{Covered}$
bin auto [47104:48127]	5	1	_	Covered
bin auto [48128:49151]	11	1	_	Covered
bin auto [49152:50175]	$\overline{2}$	1	_	Covered
bin auto [50176:51199]	6	1		Covered
			_	
bin auto [51200:52223]	9	1	_	Covered
bin auto $[52224:53247]$	0	1	_	ZERO
bin auto $[53248:54271]$	8	1	_	Covered
bin auto [54272:55295]	6	1	_	Covered
bin auto [55296:56319]	10	1	_	Covered
	10	1		Covered
bin auto [56320:57343]			_	
$\operatorname{bin} \ \operatorname{auto} \left[57344 \!:\! 58367 \right]$	4	1	_	Covered
bin auto $[58368:59391]$	5	1	_	$\operatorname{Covered}$
bin auto [59392:60415]	2	1	_	Covered
bin auto [60416:61439]	10	1	_	Covered
bin auto $[61440:62463]$	$\frac{10}{2}$	1		Covered
		1	_	
bin auto $[62464:63487]$	3	1	_	Covered
bin auto $[63488:64511]$	15	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	9	1	_	$\operatorname{Covered}$
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	-			
	100.00%	100	_	~ .
bin auto [0]	447	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} [1]$	561	1	_	$\operatorname{Covered}$
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$		
	-			
% Hit:	100.00%	100	_	~ ,
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	942	1	_	$\operatorname{Covered}$
bin auto[1]	66	1	_	$\operatorname{Covered}$
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$		
% Hit:	100.00%	100		
			_	C 1
bin auto [0]	937	1	_	Covered
bin auto[1]	71	1	_	$\operatorname{Covered}$
Coverpoint empty_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
				Carranad
bin auto[0]	784	1	_	Covered
bin auto[1]	224	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	933	1	_	Covered
bin auto[1]	75	1	_	Covered
Coverpoint almostempty_cp	100.00%			Covered
	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	805	1	_	Covered
bin auto [1]	203	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:		2		55 v 51 6 G
,	2		_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	949	1	_	Covered
bin auto [1]	59	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
		6		SSVSIGU
covered/total bins:	6		_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	145	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	56	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	416	1	_	Covered
	100	1	•	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$				
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	76	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[0]\;,\mathrm{auto}[0]>$	215	1	_	Covered

overgroup	Metric	Goal	$_{ m Bins}$	Status
VERGROUP COVERAGE:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
Illegal and Ignore Bins:				
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [0] > \end{aligned} \ \ egin{aligned} ext{bin} & < ext{auto} [0] \ , ext{auto} [0] \ , ext{auto} [0] > \end{aligned}$	$54 \\ 215$	1 1	_	$egin{array}{c} { m Covered} \end{array}$
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	516	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	164	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] > \end{aligned}$	$\begin{array}{c} 37 \\ 22 \end{array}$	1 1		$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
Auto, Default and User Defined Bins:				~
missing/total bins: % Hit:	$0\\100.00\%$	$6 \\ 100$	_	
covered/total bins:	6	6	_	
Cross underflow_cross	100.00%	100	_	Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack	0		_	ZERO
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	215	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$\frac{477}{76}$	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\frac{39}{477}$	1 1	_	$egin{array}{c} { m Covered} \end{array}$
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[0] >$	174	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right] >$	27	1	_	Covered
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
missing/total bins:	0 100 00%	6 100	_	
covered/total bins:	6	6	_	22.0104
$ ext{bin } < ext{auto} \left[0\right], ext{auto} \left[0\right], ext{auto} \left[0\right] > \\ ext{Cross } ext{overflow_cross}$	$179\\100.00\%$	$1\\100$	_	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	69 170	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	417	1	_	Covered
bin $<$ auto [0], auto [0], auto [1] $>$ bin $<$ auto [1], auto [1], auto [0] $>$	140	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \end{aligned}$	$\begin{array}{c} 7 \\ 36 \end{array}$	1 1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right] >$	99	1	_	Covered
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	61	1	_	Covered
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
missing/total bins:	100.00%	8	_	
covered/total bins:	8	8	_	
$\begin{array}{c} \text{bin } < \text{auto} \left[0 \right], \text{auto} \left[0 \right], \text{auto} \left[0 \right] > \\ \text{Cross } \text{almostempty_cross} \end{array}$	100.00%	100	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$70 \\ 202$	1 1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	496	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	165	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] > \ & ext{bin } < ext{auto} [0] \ , ext{auto} [0] \ , ext{auto} [1] > \end{aligned}$	$\begin{array}{c} 6 \\ 13 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	20	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} [1] \ , \\ \mathrm{auto} [1] \ , \\ \mathrm{auto} [1] >$	36	1	_	Covered
Auto, Default and User Defined Bins:	100.0070	100	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$\begin{matrix} 8 \\ 100 \end{matrix}$	_	
covered/total bins:	8	8	_	
Cross almostfull_cross	100.00%	100	_	Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty	140		_	Occurred
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	143	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	33	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{160}{448}$	1	_	Covered Covered
$egin{aligned} & ext{bin } < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] > \ & ext{bin } < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] > \end{aligned}$	$43 \\ 160$	1 1	_	Covered Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[1]\;,\mathrm{auto}[1]>$	41	1	_	Covered
Auto, Default and User Defined Bins:	100.0070	100	_	
missing/total bins: % Hit:	$0\\100.00\%$	$6 \\ 100$	_	
covered/total bins:	6	6	_	
Cross empty_cross	100.00%	100	_	Covered
ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full	0		_	ZERO ZERO
Illegal and Ignore Bins:	~			MDD C
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	206	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{76}{454}$	1	_	Covered Covered
$\begin{array}{l} \mathrm{bin} < \mathrm{auto}\left[1\right], \mathrm{auto}\left[1\right], \mathrm{auto}\left[0\right] > \\ \mathrm{bin} < \mathrm{auto}\left[1\right], \mathrm{auto}\left[0\right], \mathrm{auto}\left[0\right] > \end{array}$	$\begin{array}{c} 201 \\ 76 \end{array}$	1 1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	9	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	62	1	_	Covered
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
missing/total bins:	100.00%	6	_	
covered/total bins:	6	6	_	
Cross full_cross	100.00%	100	_	Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Illogal and Ignore Ding.				

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Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100		Uncovered
covered/total bins:	192	194	_	
missing/total bins:	2	194	_	
% Hit:	98.96%	100	_	
$\operatorname{Coverpoint} \operatorname{rst_n_cp}$	100.00%	100	_	Covered

covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	~
$egin{array}{ll} egin{array}{ll} egi$	$\frac{156}{852}$	1 1	_	Covered Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	Covered
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	G 1
$egin{array}{lll} { m bin } & { m auto} [0\!:\!1023] \ { m bin } & { m auto} [1024\!:\!2047] \end{array}$	$\frac{22}{15}$	1 1	_	Covered Covered
bin auto [2048:3071]	$\frac{13}{12}$	1	_	Covered
bin auto [3072:4095]	16	1	_	Covered
bin auto [4096:5119]	18	1	_	Covered
bin auto [5120:6143] bin auto [6144:7167]	$\begin{array}{c} 11 \\ 20 \end{array}$	1 1	_	Covered Covered
bin auto [7168:8191]	16	1	_	Covered
bin auto [8192:9215]	24	1	_	Covered
bin auto [9216:10239]	19	1	_	Covered
bin auto [10240:11263] bin auto [11264:12287]	17 10	1 1	_	Covered Covered
bin auto [12288:13311]	9	1	_	Covered
bin auto [13312:14335]	13	1	_	Covered
bin auto [14336:15359]	13	1	_	Covered
bin auto [15360:16383] bin auto [16384:17407]	17 15	1 1	_	Covered Covered
bin auto [17408:18431]	$\frac{15}{21}$	1	_	Covered
bin auto [18432:19455]	13	1	_	Covered
bin auto [19456:20479]	19	1	_	Covered
$\begin{array}{ll} \text{bin } \text{ auto} \left[20480 \text{:} 21503 \right] \\ \text{bin } \text{ auto} \left[21504 \text{:} 22527 \right] \end{array}$	8 11	1 1	_	Covered Covered
bin auto $[21504:22527]$	11	1	_	Covered
bin auto [23552:24575]	12	1	_	Covered
bin auto $[24576:25599]$	13	1	_	Covered
bin auto [25600:26623]	$\begin{matrix} 8 \\ 12 \end{matrix}$	1 1	_	Covered Covered
bin auto $[26624:27647]$ bin auto $[27648:28671]$	$\frac{12}{17}$	1	_	Covered
bin auto [28672:29695]	10	1	_	Covered
bin auto [29696:30719]	20	1	_	Covered
bin auto $[30720:31743]$ bin auto $[31744:32767]$	$\frac{20}{20}$	1 1	_	Covered Covered
bin auto [32768:33791]	$\frac{20}{13}$	1	_	Covered
bin auto [33792:34815]	21	1	_	Covered
bin auto [34816:35839]	14	1	_	Covered
bin auto [35840:36863]	18	1	_	Covered
bin auto [36864:37887] bin auto [37888:38911]	$\frac{18}{14}$	1 1	_	Covered Covered
bin auto [38912:39935]	17	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[39936 \!:\! 40959 \right]$	15	1	_	Covered
bin auto [40960:41983]	15	1	_	Covered
bin auto [41984:43007] bin auto [43008:44031]	$\frac{14}{16}$	1 1	_	Covered Covered
bin auto [44032:45055]	12	1	_	Covered
bin auto $[45056:46079]$	22	1	_	Covered
bin auto [46080:47103]	$\begin{array}{c} 17 \\ 14 \end{array}$	1	_	Covered Covered
bin auto [47104:48127] bin auto [48128:49151]	$\frac{14}{17}$	1 1	_	Covered
bin auto [49152:50175]	15	1	_	Covered
bin auto [50176:51199]	13	1	_	Covered
bin auto [51200:52223] bin auto [52224:53247]	$\frac{16}{24}$	1 1	_	Covered Covered
bin auto $[52224.53247]$	17	1	_	Covered
bin auto [54272:55295]	18	1	_	Covered
bin auto [55296:56319]	18	1	_	Covered
bin auto [56320:57343] bin auto [57344:58367]	$\begin{array}{c} 15 \\ 19 \end{array}$	1 1	_	Covered Covered
bin auto $[57344:58367]$	$\frac{19}{15}$	1	_	Covered
bin auto [59392:60415]	14	1	_	Covered
bin auto [60416:61439]	17	1	_	Covered
bin auto [61440:62463] bin auto [62464:63487]	$\frac{12}{16}$	1 1	_	Covered Covered
bin auto [63488:64511]	$\frac{10}{24}$	1	_	Covered
bin auto $[64512:65535]$	16	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	$\frac{2}{0}$	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	731	1	_	Covered
bin auto[1]	277	1	_	Covered
Coverpoint w_en_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	-
bin auto [0]	291 717	1	_	Covered
bin auto[1] Coverpoint data_out_cp	$717\\96.87\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Uncovered
covered/total bins:	62	64	_	SHOOTOLOU
missing/total bins:	2	64	_	
% Hit:	96.87%	100	_	01
bin auto [0:1023] bin auto [1024:2047]	$\frac{557}{2}$	1 1	_	Covered Covered
bin auto $[1024:2047]$ bin auto $[2048:3071]$	7	1	_	Covered
•				

1.1 [0.0 = 0.40.0 ×]				G 1
bin auto [3072:4095]	15	1	_	Covered
bin auto [4096:5119]	8	1	_	Covered
bin auto [5120:6143]	5	1	_	Covered
bin auto [6144:7167]	32	1	_	Covered
bin auto [7168:8191]	19	1	_	Covered
bin auto[8192:9215]	12			Covered
		1	_	
bin auto [9216:10239]	2	1	_	Covered
bin auto $[10240:11263]$	2	1	_	Covered
bin auto [11264:12287]	11	1	_	Covered
bin auto [12288:13311]	1	1	_	Covered
bin auto [13312:14335]	11	1	_	Covered
1				
bin auto [14336:15359]	8	1	_	Covered
bin auto $[15360:16383]$	7	1	_	Covered
bin auto [16384:17407]	2	1	_	Covered
bin auto [17408:18431]	5	1	_	Covered
bin auto [18432:19455]	1	1	_	Covered
,				
bin auto [19456:20479]	8	1	_	Covered
bin auto $[20480:21503]$	7	1	_	$\operatorname{Covered}$
bin auto $[21504:22527]$	1	1	_	Covered
bin auto [22528:23551]	1	1	_	Covered
bin auto $[23552:24575]$	3	1	_	Covered
bin auto $[24576:25599]$	3	1	_	Covered
${ m bin \ auto} [2 5 6 0 0 : 2 6 6 2 3]$	21	1	_	Covered
bin auto $[26624:27647]$	2	1	_	Covered
bin auto [27648:28671]	1	1	_	Covered
bin auto $[28672:29695]$	8	1	_	Covered
,				
bin auto [29696:30719]	5	1	_	Covered
bin auto $[30720:31743]$	6	1	_	Covered
bin auto $[31744:32767]$	13	1	_	$\operatorname{Covered}$
bin auto [32768:33791]	1	1	_	Covered
bin auto[33792:34815]	17	1	_	Covered
bin auto [34816:35839]	9	1	_	Covered
bin auto $[35840:36863]$	10	1	_	Covered
bin auto [36864:37887]	2	1	_	$\operatorname{Covered}$
bin auto [37888:38911]	3	1	_	Covered
bin auto [38912:39935]	11	1	_	Covered
	$\frac{11}{2}$	1		Covered
bin auto [39936:40959]		1	_	
bin auto $[40960:41983]$	0	1	_	ZERO
bin auto [41984:43007]	4	1	_	Covered
bin auto [43008:44031]	14	1	_	Covered
bin auto $[44032:45055]$	8	1	_	Covered
bin auto $[45056:46079]$	9	1	_	Covered
	_			
bin auto [46080:47103]	15	1	_	Covered
bin auto $[47104:48127]$	5	1	_	$\operatorname{Covered}$
bin auto $[48128:49151]$	11	1	_	Covered
bin auto [49152:50175]	2	1	_	Covered
bin auto [50176:51199]	6	1		Covered
bin auto [51200:52223]	9	1	_	Covered
bin auto $[52224:53247]$	0	1	_	ZERO
bin auto [53248:54271]	8	1	_	Covered
bin auto [54272:55295]	6	1	_	Covered
bin auto [55296:56319]	10	1		Covered
			_	
bin auto [56320:57343]	10	1	_	Covered
bin auto $[57344:58367]$	4	1	_	Covered
${ m bin \ auto} [58368{:}59391]$	5	1	_	Covered
bin auto [59392:60415]	2	1	_	Covered
bin auto [60416:61439]	10	1	_	Covered
bin auto $[61440:62463]$	$\frac{10}{2}$	1		Covered
			_	
bin auto $[62464:63487]$	3	1	_	Covered
bin auto $[63488:64511]$	15	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	9	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{1}{2}$	_	
		$\frac{2}{2}$		
missing/total bins:	0		_	
% Hit:	100.00%	100	_	~
$ \text{bin } \text{ auto} \left[0 \right]$	447	1	_	Covered
bin auto[1]	561	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
	0	$\frac{2}{2}$		
missing/total bins:			_	
% Hit:	100.00%	100	_	
bin auto [0]	942	1	_	$\operatorname{Covered}$
bin auto[1]	66	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2		Covered
,				
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	937	1	_	Covered
bin auto [1]	71	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
1 1 1 1			_	Oovered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	784	1	_	Covered
bin auto[1]	$\frac{701}{224}$	1	_	Covered
	100.00%	100		Covered
Coverpoint almostfull_cp			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	933	1	_	Covered
bin auto[0]	75	1		Covered
	100.00%	100	_	Covered
${\bf Coverpoint~almost empty_cp}$	100.00%	100	_	Covered

covered/total bins:	2	2	_
missing/total bins: % Hit:	$0 \\ 100.00\%$	2	_
bin auto $[0]$	805	$100 \\ 1$	– – Covered
bin auto[0]	203	1	- Covered
Coverpoint underflow-cp	100.00%	100	- Covered
covered/total bins:	2	2	_
missing/total bins:	0	2	_
% Hit:	100.00%	100	_
bin auto [0]	949	1	- Covered
bin auto[1]	59	1	- Covered
Cross wr_ack_cross	100.00%	100	- Covered
covered/total bins:	6	6	_
missing/total bins: % Hit:	$0\\100.00\%$	$6 \\ 100$	_
Auto, Default and User Defined Bins:	100.0070	100	_
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	145	1	- Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	56	1	- Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	416	1	- Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right]$, $\operatorname{auto} \left[1\right]$, $\operatorname{auto} \left[0\right] >$	100	1	- Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	76	1	- Covered
$ \text{bin } < \text{auto} \left[0 \right] \text{ , auto} \left[0 \right] \text{ , auto} \left[0 \right] >$	215	1	- Covered
Illegal and Ignore Bins:			ZED O
ignore_bin w_en_nactv_wr_ack	100.00%	100	- ZERO
Cross full_cross covered/total bins:	100.00%	100 6	- Covered
missing/total bins:	0	6	_
% Hit:	100.00%	100	_
Auto, Default and User Defined Bins:	100.0070	100	
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[1], \operatorname{auto}[1] >$	62	1	- Covered
bin <auto [0],="" [1]="" auto=""></auto>	9	1	- Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	201	1	- Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	76	1	- Covered
bin < auto[0], auto[1], auto[0] >	454	1	- Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$	206	1	- Covered
Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full	0		– ZERO
ignore_bin w_en_r_en_allactv_full	0		– ZERO – ZERO
Cross empty_cross	100.00%	100	- Covered
covered/total bins:	6	6	_
missing/total bins:	0	6	_
% Hit:	100.00%	100	_
Auto, Default and User Defined Bins:	4.4		
bin <auto [1]="" [1],="" auto=""></auto>	41	1	- Covered
$egin{aligned} ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ \end{aligned}$	43 160	1 1	$egin{array}{ll} - & \operatorname{Covered} \ - & \operatorname{Covered} \end{array}$
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	448	1	- Covered
bin $\langle auto[0], auto[0] \rangle$	33	1	- Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	143	1	- Covered
Illegal and Ignore Bins:			
ignore_bin read_nactv_empty	140		- Occurred
Cross almostfull_cross	100.00%	100	- Covered
covered/total bins:	8	8	_
missing/total bins:	$0\\100.00\%$	8	_
% Hit: Auto, Default and User Defined Bins:	100.0070	100	_
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	36	1	- Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	$\frac{30}{20}$	1	- Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	6	1	- Covered
bin < auto[0], auto[0], auto[1] >	13	1	- Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\ ,\mathrm{auto}[1]\ ,\mathrm{auto}[0]\!>$	165	1	- Covered
$ \text{bin } < \text{auto} \left[0 \right] \text{ , auto} \left[1 \right] \text{ , auto} \left[0 \right] >$	496	1	C
			- Covered
bin < auto [1], auto [0], auto [0] >	70	1	- Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	202	1	- Covered $-$ Covered
$\begin{array}{c} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Cross } \text{almostempty_cross} \end{array}$	$\frac{202}{100.00\%}$	$\begin{matrix} 1 \\ 100 \end{matrix}$	- Covered
$\begin{array}{c} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Cross almostempty_cross} \\ \text{covered/total bins:} \end{array}$	$202 \\ 100.00\% \\ 8$	$1\\100\\8$	- Covered $-$ Covered
$\begin{array}{c} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Cross } \text{almostempty_cross} \end{array}$	$\frac{202}{100.00\%}$	$\begin{matrix} 1 \\ 100 \end{matrix}$	- Covered $-$ Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins:</auto[0],>	$202 \\ 100.00\% \\ 8 \\ 0$	1 100 8 8	- Covered $-$ Covered
<pre>bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit:</auto[0],></pre>	202 $100.00%$ 8 0 $100.00%$	1 100 8 8	 Covered Covered Covered — — — — Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],>	$202 \\ 100.00\% \\ 8 \\ 0 \\ 100.00\%$	$ \begin{array}{c} 1 \\ 100 \\ 8 \\ 8 \\ 100 \end{array} $	 Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7	1 100 8 8 100	 Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36	1 100 8 8 100 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140	1 100 8 8 100 1 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417	1 100 8 8 100 1 1 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69	1 100 8 8 100 1 1 1 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179	1 100 8 8 100 1 1 1 1 1 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69	1 100 8 8 100 1 1 1 1 1 1	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0	1 100 8 8 100 1 1 1 1 1 1 1 1 1 100 6 6	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6	1 100 8 8 100 1 1 1 1 1 1 1 1 1 100 6	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$	1 100 8 8 100 1 1 1 1 1 1 1 100 6 6 6 100	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[1],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$	1 100 8 8 100 1 1 1 1 1 1 1 1 100 6 6 6 100	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$	1 100 8 8 100 1 1 1 1 1 1 100 6 6 100	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39	1 100 8 8 100 1 1 1 1 1 1 100 6 6 100	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39 477	1 100 8 8 100 1 1 1 1 1 1 100 6 6 100	 Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> covered total auto[0], auto[0], auto[0] > bin <auto[1], auto[0]="" auto[0],=""> covered total auto[0], auto[</auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39	1 100 8 8 8 100 1 1 1 1 1 1 100 6 6 6 100	- Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39 477 76	1 100 8 8 8 100 1 1 1 1 1 1 100 6 6 100	- Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39 477 76 215	1 100 8 8 100 1 1 1 1 1 1 100 6 6 6 100	- Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross</auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39 477 76 215 0 $100.00%$	1 100 8 8 8 100 1 1 1 1 1 100 6 6 100 1 1 1 1 1	- Covered
bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	202 $100.00%$ 8 0 $100.00%$ 61 99 7 36 140 417 69 179 $100.00%$ 6 0 $100.00%$ 27 174 39 477 76 215	1 100 8 8 100 1 1 1 1 1 1 100 6 6 6 100	- Covered

▼ Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov	SVA	1	Off	853	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	853	1	Unli	1	100%		√	0	0	0 ns	. 0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	V	Off	853	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	2	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	23	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	159	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	67	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	62	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	191	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	44	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	28	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	472	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	156	1	Unli	1	100%		V	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 2: SVA "Seed2"

98.96%

rered
rered
O

TOTAL COVERGROUP COVERAGE: 99.83% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.83%

4.3 Functional Coverage "seed3" Report

Coverage Report by instance with details

Covergroup Bins

192

194

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100		Uncovered
covered/total bins:	192	194	_	
missing/total bins:	2	194	_	
% Hit:	98.96%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	143	1	_	$\operatorname{Covered}$
bin auto[1]	865	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	19	1	_	Covered
bin auto [1024:2047]	12	1	_	Covered
bin auto [2048:3071]	14	1	_	Covered
bin auto [3072:4095]	11	1	_	$\operatorname{Covered}$
bin auto [4096:5119]	16	1	_	$\operatorname{Covered}$
bin auto [5120:6143]	15	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	9	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	12	1	_	Covered
bin auto [8192:9215]	16	1	_	$\operatorname{Covered}$
bin auto [9216:10239]	11	1	_	$\operatorname{Covered}$
bin auto [10240:11263]	16	1	_	$\operatorname{Covered}$
bin auto [11264:12287]	19	1	_	$\operatorname{Covered}$
bin auto [12288:13311]	22	1	_	$\operatorname{Covered}$
bin auto [13312:14335]	17	1	_	$\operatorname{Covered}$
bin auto [14336:15359]	15	1	_	$\operatorname{Covered}$
bin auto [15360:16383]	20	1	_	Covered
bin auto $[16384:17407]$	19	1	_	Covered
bin auto [17408:18431]	13	1	_	Covered
bin auto $[18432:19455]$	10	1	_	Covered
bin auto $[19456:20479]$	20	1	_	Covered
bin auto [20480:21503]	17	1	_	Covered
bin auto $[21504:22527]$	26	1	_	$\operatorname{Covered}$
bin auto [22528:23551]	12	1	_	Covered
bin auto [23552:24575]	11	1	_	Covered
bin auto [24576:25599]	15	1	_	Covered
bin auto [25600:26623]	23	1	_	Covered
bin auto [26624:27647]	12	1	_	Covered
bin auto [27648:28671]	15	1	_	Covered

bin auto $[28672:29695]$	15	1	_	Covered
bin auto [29696:30719]	16	1	_	Covered
bin auto [30720:31743]	14	1	_	Covered
bin auto [31744:32767]	18	1	_	Covered
bin auto [32768:33791]	10	1	_	Covered
bin auto [33792:34815]	11	1	_	Covered
bin auto [34816:35839]	14	1	_	$\operatorname{Covered}$
bin auto [35840:36863]	15	1	_	Covered
bin auto [36864:37887]	12	1	_	Covered
	13			
bin auto [37888:38911]		1	_	Covered
bin auto [38912:39935]	22	1	_	$\operatorname{Covered}$
bin auto [39936:40959]	18	1	_	Covered
bin auto [40960:41983]	14	1	_	Covered
bin auto [41984:43007]	22	1	_	Covered
bin auto [43008:44031]	22	1	_	Covered
bin auto $[44032;45055]$	14	1	_	$\operatorname{Covered}$
bin auto $[45056:46079]$	19	1	_	$\operatorname{Covered}$
bin auto [46080:47103]	18	1	_	Covered
bin auto [47104:48127]	18	1	_	Covered
,				
bin auto [48128:49151]	12	1	_	Covered
bin auto $[49152:50175]$	14	1	_	$\operatorname{Covered}$
bin auto [50176:51199]	14	1	_	$\operatorname{Covered}$
bin auto [51200:52223]	20	1	_	Covered
bin auto [52224:53247]	$\frac{20}{21}$	1	_	Covered
,				
bin auto [53248:54271]	13	1	_	Covered
bin auto $[54272:55295]$	12	1	_	$\operatorname{Covered}$
bin auto $[55296:56319]$	16	1	_	Covered
bin auto $[56320:57343]$	15	1	_	Covered
bin auto [57344:58367]	19	1	_	Covered
bin auto $[58368:59391]$	14	1	_	$\operatorname{Covered}$
bin auto $[59392:60415]$	18	1	_	$\operatorname{Covered}$
bin auto [60416:61439]	19	1	_	Covered
bin auto $[61440:62463]$	15	1	_	Covered
		_		
bin auto $[62464:63487]$	20	1	_	Covered
bin auto $[63488:64511]$	12	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	12	1	_	$\operatorname{Covered}$
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2		00,0104
,			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	716	1	_	$\operatorname{Covered}$
bin auto[1]	292	1	_	Covered
Coverpoint w_en_cp	100.00%	100		Covered
			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
	100.00%	100	_	
% Hit:	100.00%	100	_	Covered
% Hit: bin auto[0]	285	1		Covered
% Hit: bin auto[0] bin auto[1]	$\begin{array}{c} 285 \\ 723 \end{array}$	1 1	_ _ _	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp	$285 \\ 723 \\ 96.87\%$	$\begin{matrix}1\\1\\100\end{matrix}$	_ _ _ _	
% Hit: bin auto[0] bin auto[1]	$\begin{array}{c} 285 \\ 723 \end{array}$	1 1	_ _ _ _	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins:	$285 \\ 723 \\ 96.87\% \\ 62$	$1\\1\\100\\64$	- - - -	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins:	$285 \\ 723 \\ 96.87\% \\ 62 \\ 2$	$1\\1\\100\\64\\64$	- - - -	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit:	$285 \\ 723 \\ 96.87\% \\ 62 \\ 2 \\ 96.87\%$	$1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100$	- - - - -	Covered Uncovered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023]	285 723 $96.87%$ 62 2 $96.87%$ 502	$egin{array}{c} 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \end{array}$	- - - - - -	Covered Uncovered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	$285 \\ 723 \\ 96.87\% \\ 62 \\ 2 \\ 96.87\%$	$1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100$	- - - - - - -	Covered Covered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023]	285 723 $96.87%$ 62 2 $96.87%$ 502	$egin{array}{c} 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \end{array}$		Covered Uncovered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \end{array}$	_	Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]</pre>	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$	_ _ _	Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119]</pre>	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$	_ _ _ _	Covered Uncovered Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143]</pre>	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\$	_ _ _ _	Covered Uncovered Covered Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167]</pre>	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$	_ _ _ _	Covered Uncovered Covered Covered Covered Covered Covered Covered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3	$egin{array}{c} 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\$	_ _ _ _	Covered Uncovered Covered Covered Covered Covered Covered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7	$ \begin{array}{c} 1\\ 1\\ 100\\ 64\\ 64\\ 100\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1 \end{array} $	_ _ _ _ _	Covered Uncovered Covered Covered Covered Covered Covered Covered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5	1 100 64 64 100 1 1 1 1 1 1 1		Covered Uncovered Covered Covered Covered Covered Covered Covered Covered Covered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5 4	1 100 64 64 100 1 1 1 1 1 1 1 1	- - - - - -	Covered Uncovered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5 4 11	1 100 64 64 100 1 1 1 1 1 1 1 1 1 1	- - - - - - -	Covered Uncovered Covered
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% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263] bin auto [12288:13311] bin auto [13312:14335] bin auto [1336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [19456:20479] bin auto [19456:20479] bin auto [20480:21503] bin auto [21504:22527]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5 4 11 25 7 4 4 10 11 10 6 22 1 9	1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Uncovered Covered
% Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [1264:12287] bin auto [1264:12287] bin auto [13312:14335] bin auto [14336:15359] bin auto [14384:17407] bin auto [17408:18431] bin auto [19456:20479] bin auto [29480:21503] bin auto [20480:21503] bin auto [21504:22527] bin auto [22528:23551]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5 4 11 25 7 4 4 10 11 10 6 22 1 9 3	1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Uncovered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[7168:8191] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[10240:11263] bin auto[12288:13311] bin auto[12288:13311] bin auto[13312:14335] bin auto[14336:15359] bin auto[14360:16383] bin auto[14384:17407] bin auto[17408:18431] bin auto[17408:18431] bin auto[19456:20479] bin auto[20480:21503] bin auto[2528:23551] bin auto[22528:23551] bin auto[23552:24575]	285 723 $96.87%$ 62 2 $96.87%$ 502 4 7 3 3 3 7 6 5 4 11 25 7 4 4 10 11 10 6 22 1 9 3 0	1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Uncovered Covered
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bin auto [46080:47103]	3	1	_	Covered
bin auto [47104:48127]	1	1	_	Covered
bin auto [48128:49151]	$\frac{1}{2}$	1	_	Covered
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bin auto [50176:51199]	1	1	_	Covered
bin auto $[51200:52223]$	15	1	_	Covered
bin auto $[52224:53247]$	21	1	_	Covered
bin auto [53248:54271]	6	1	_	Covered
bin auto $[54272:55295]$	0	1	_	ZERO
bin auto [55296:56319]	$\overset{\circ}{6}$	1	_	Covered
· ·				
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bin auto $[57344:58367]$	25	1	_	Covered
bin auto [58368:59391]	7	1	_	Covered
bin auto [59392:60415]	6	1	_	Covered
bin auto [60416:61439]	4	1	_	Covered
bin auto [61440:62463]	20	1	_	Covered
bin auto [62464:63487]	8	1	_	Covered
bin auto $[63488:64511]$	3	1	_	Covered
bin auto $[64512:65535]$	10	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	C 1
bin auto $[0]$	432	1	_	Covered
bin auto[1]	576	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100		
			_	C 1
$\mathrm{bin} \ \mathrm{auto} \left[0 \right]$	957	1	_	Covered
bin auto[1]	51	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
				Correnad
bin auto [0]	927	1	_	Covered
${\rm bin \ \ auto} [1]$	81	1	_	$\operatorname{Covered}$
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
				Correnad
bin auto [0]	795	1	_	Covered
${\rm bin \ \ auto} [1]$	213	1	_	$\operatorname{Covered}$
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
				Command
bin auto [0]	955	1	_	Covered
${\rm bin \ \ auto} [1]$	53	1	_	Covered
$\operatorname{Coverpoint}$ $\operatorname{almostempty_cp}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	791	1		Covered
. ,		_		
bin auto[1]	217	1	_	Covered
$\operatorname{Coverpoint}$ $\operatorname{underflow_cp}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	943	1	_	Covered
bin auto[1]	65	1	_	Covered
Cross wr_ack_cross	100.00%	100		Covered
			_	Sovered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	172	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	42	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	404	1		Covered
			_	
bin < auto [0], auto [1], auto [0] >	105	1	_	Covered
bin < auto[1], auto[0], auto[0] >	78	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] >$	207	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6		55,516d
			_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right] >$	59	1	_	Covered
bin < auto[0], auto[0], auto[1] >	22	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	214	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	78	1	_	Covered
	450	1		Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$			_	
bin < auto[0], auto[0], auto[0] >	185	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO

ignore_bin w_en_r_en_allactv_full	0	100	_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6 0	6	_	
missing/total bins: % Hit:	100.00%	$6 \\ 100$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	33	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	39	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	181	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	437	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0] \rangle$	39	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	138	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	141		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				~ .
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	20	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	17	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	8	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	8	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	$194 \\ 492$	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\begin{array}{c} 492 \\ 70 \end{array}$	1 1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	199	1	_	Covered
Cross almostempty_cross	100.00%	100		Covered
covered/total bins:	8	8	_	Covered
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	79	1	_	Covered
bin < auto[0], auto[1], auto[1] >	91	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [1], \operatorname{auto} [0], \operatorname{auto} [1] >$	11	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0],\mathrm{auto}[0],\mathrm{auto}[1]>$	36	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1],\mathrm{auto}[1],\mathrm{auto}[0]\!>$	135	1	_	Covered
$\mathrm{bin} < \mathrm{auto}\left[0 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[0 ight] >$	418	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ < \operatorname{auto} \left[1 ight], \operatorname{auto} \left[0 ight], \operatorname{auto} \left[0 ight] >$	67	1	_	Covered
bin < auto[0], auto[0], auto[0] >	171	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6\\100$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	12	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	$\frac{12}{202}$	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	39	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	470	1	_	Covered
bin < auto[1], auto[0], auto[0] >	78	1	_	Covered
bin < auto[0], auto[0], auto[0] >	207	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	4.5	4		C 1
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	45	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	20	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{169}{509}$	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\frac{509}{58}$	1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	$\begin{array}{c} 58 \\ 207 \end{array}$	1	_	Covered Covered
Illegal and Ignore Bins:	201	1	_	Covered
ignore_bin_r_en_nactv_wr_ack	0		_	ZERO
-0	· ·			

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100		Uncovered
covered/total bins:	192	194	_	
missing/total bins:	2	194	_	
% Hit:	98.96%	100	_	
$Coverpoint rst_n_cp$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	143	1	_	Covered
bin auto [1]	865	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	19	1	_	Covered
bin auto [1024:2047]	12	1	_	Covered
bin auto [2048:3071]	14	1	_	Covered
bin auto 3072:4095	11	1	_	Covered
bin auto [4096:5119]	16	1	_	Covered
bin auto [5120:6143]	15	1	_	Covered

bin auto [6144:7167]	9	1	_	Covered
bin auto [7168:8191]	12	1	_	Covered
bin auto [8192:9215]	16	1	_	Covered
bin auto [9216:10239]	11	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
	19			Covered
bin auto [11264:12287]		1	_	
bin auto [12288:13311]	22	1	_	Covered
bin auto [13312:14335]	17	1	_	Covered
bin auto [14336:15359]	15	1	_	Covered
bin auto $[15360:16383]$	20	1	_	Covered
bin auto [16384:17407]	19	1	_	Covered
bin auto [17408:18431]	13	1	_	Covered
bin auto [18432:19455]	10	1	_	Covered
bin auto [19456:20479]	20	1	_	Covered
bin auto[13430.20473]	17	1		Covered
			_	
bin auto [21504:22527]	26	1	_	Covered
bin auto [22528:23551]	12	1	_	Covered
${ m bin \ auto} [23552{:}24575]$	11	1	_	Covered
${ m bin \ auto} [24576 \hbox{:} 25599]$	15	1	_	Covered
bin auto $[25600:26623]$	23	1	_	Covered
bin auto [26624:27647]	12	1	_	Covered
bin auto [27648:28671]	15	1	_	Covered
bin auto [28672:29695]	15	1	_	Covered
bin auto [29696:30719]	16	1		Covered
			_	
bin auto [30720:31743]	14	1	_	Covered
bin auto [31744:32767]	18	1	_	Covered
bin auto $[32768:33791]$	10	1	_	Covered
bin auto $[33792:34815]$	11	1	_	$\operatorname{Covered}$
bin auto $[34816:35839]$	14	1	_	Covered
bin auto [35840:36863]	15	1	_	Covered
bin auto [36864:37887]	12	1	_	Covered
bin auto [37888:38911]	13	1	_	Covered
bin auto[38912:39935]	$\frac{13}{22}$	1	_	Covered
		1		Covered
bin auto [39936:40959]	18	_	_	
bin auto [40960:41983]	14	1	_	Covered
bin auto $[41984:43007]$	22	1	_	Covered
bin auto $[43008:44031]$	22	1	_	$\operatorname{Covered}$
bin auto [44032:45055]	14	1	_	Covered
bin auto $[45056:46079]$	19	1	_	Covered
bin auto [46080:47103]	18	1	_	Covered
bin auto [47104:48127]	18	1	_	Covered
bin auto [48128:49151]	12	1	_	Covered
bin auto [49152:50175]	14	1	_	Covered
bin auto [50176:51199]	14	1		Covered
			_	
bin auto [51200:52223]	20	1	_	Covered
bin auto [52224:53247]	21	1	_	Covered
bin auto $[53248:54271]$	13	1	_	$\operatorname{Covered}$
${ m bin \ auto} [54272 \!:\! 55295]$	12	1	_	$\operatorname{Covered}$
bin auto [55296:56319]	16	1	_	Covered
bin auto $[56320:57343]$	15	1	_	Covered
bin auto [57344:58367]	19	1	_	Covered
bin auto [58368:59391]	14	1	_	Covered
bin auto [59392:60415]	18	1	_	Covered
bin auto [60416:61439]	19	1	_	Covered
	15	1		Covered
bin auto [61440:62463]				
bin auto [62464:63487]	20	1	_	Covered
bin auto [63488:64511]	12	1	_	Covered
bin auto $[64512\!:\!65535]$	12	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	716	1	_	Covered
bin auto[1]	$\frac{710}{292}$	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{100.007_{0}}{2}$	$\frac{100}{2}$	_	Covered
missing/total bins:	$0 \frac{2}{0}$	$\frac{2}{2}$	_	
missing/total bins: % Hit:	100.00%	$\frac{2}{100}$	_	
			_	C 1
bin auto [0]	285	1	_	Covered
bin auto[1]	723	1	_	Covered
Coverpoint data_out_cp	96.87%	100	_	${ m Uncovered}$
covered/total bins:	62	64	_	
missing/total bins:	2	64	_	
% Hit:	96.87%	100	_	
bin auto [0:1023]	502	1	_	Covered
bin auto [1024:2047]	4	1	_	Covered
bin auto[1024.2047] bin auto[2048:3071]	7	1	_	Covered
bin auto $[2048.3071]$ bin auto $[3072:4095]$	3	1		Covered
			_	
bin auto [4096:5119]	3	1	_	Covered
bin auto [5120:6143]	3	1	_	Covered
bin auto [6144:7167]	7	1	_	Covered
bin auto [7168:8191]	6	1	_	Covered
bin auto [8192:9215]	5	1	_	Covered
bin auto [9216:10239]	4	1	_	Covered
bin auto [10240:11263]	11	1	_	Covered
bin auto [11264:12287]	$\frac{11}{25}$	1	_	Covered
bin auto[12288:13311]	20	1	_	Covered
	7	1	_	Covered
	7 4			Covered
bin auto [13312:14335]	4	1	_	Covered
bin auto [13312:14335] bin auto [14336:15359]	4 4	1 1	_	Covered
bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383]	$\begin{array}{c} 4\\4\\10\end{array}$	1 1 1	_ _	Covered Covered
bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407]	$egin{array}{c} 4 \\ 4 \\ 10 \\ 11 \end{array}$	1 1 1 1	_	Covered Covered Covered
bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383]	$\begin{array}{c} 4\\4\\10\end{array}$	1 1 1	_ _	Covered Covered

bin auto [18432:19455]	6	1	_	Covered
bin auto $[19456:20479]$	22	1	_	Covered
bin auto [20480:21503]	1	1	_	Covered
bin auto [21504:22527]	9	1	_	Covered
bin auto [22528:23551]	3	1	_	Covered
bin auto $[23552:24575]$	0	1	_	ZERO
bin auto [24576:25599]	7	1	_	Covered
	7			
bin auto [25600:26623]	7	1	_	Covered
bin auto $[26624:27647]$	15	1	_	Covered
bin auto $[27648:28671]$	6	1	_	Covered
bin auto [28672:29695]	4	1	_	Covered
bin auto [29696:30719]	8	1	_	Covered
bin auto [30720:31743]	13	1	_	Covered
bin auto [31744:32767]	8	1	_	Covered
bin auto [32768:33791]	8	1		Covered
			_	
bin auto [33792:34815]	4	1	_	Covered
bin auto $[34816:35839]$	3	1	_	Covered
bin auto $[35840:36863]$	3	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	10	1	_	Covered
bin auto [37888:38911]	7	1	_	Covered
bin auto [38912:39935]	7	1	_	Covered
bin auto [39936:40959]	18	1	_	Covered
bin auto [40960:41983]	12	1	_	Covered
bin auto $[41984:43007]$	16	1	_	Covered
bin auto $[43008:44031]$	8	1	_	$\operatorname{Covered}$
bin auto $[44032:45055]$	9	1	_	Covered
bin auto $[45056:46079]$	6	1	_	Covered
bin auto [46080:47103]	3	1	_	Covered
bin auto [47104:48127]	1	1	_	Covered
bin auto [48128:49151]	$\frac{2}{7}$	1	_	Covered
bin auto [49152:50175]	7	1	_	Covered
bin auto $[50176:51199]$	1	1	_	Covered
${ m bin \ auto} [51200 \!:\! 52223]$	15	1	_	$\operatorname{Covered}$
bin auto $[52224:53247]$	21	1	_	Covered
bin auto [53248:54271]	6	1	_	Covered
bin auto [54272:55295]	0	1	_	ZERO
	6	1		Covered
bin auto [55296:56319]	17	1	_	
bin auto $[56320:57343]$	17	1	_	Covered
bin auto [57344:58367]	25	1	_	$\operatorname{Covered}$
bin auto $[58368:59391]$	7	1	_	Covered
bin auto $[59392:60415]$	6	1	_	Covered
bin auto [60416:61439]	4	1	_	Covered
bin auto [61440:62463]	20	1	_	Covered
bin auto $[62464:63487]$	8	1		Covered
			_	
bin auto [63488:64511]	3	1	_	Covered
bin auto $[64512:65535]$	10	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	432	1	_	Covered
bin auto[1]	576	1		Covered
		_	_	
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	957	1	_	Covered
bin auto[1]	51	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{2}{2}$		
% Hit:	100.00%	100	_	
			_	G 1
bin auto[0]	927	1	_	Covered
bin auto[1]	81	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	795	1	_	Covered
bin auto[1]	213	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
	100.0070	100	_	Oovered
covered/total bins:	<i>Z</i>	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	~
			_	Covered
bin auto [0]	955	1		
$egin{array}{ll} egin{array}{ll} egi$		1 1	_	Covered
	955		_ _	
bin auto[1] Coverpoint almostempty_cp	955 53	1	_ _ _	Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins:	$955 \\ 53 \\ 100.00\%$	$1\\100\\2$	_ _ _ _	Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins:	$955 \\ 53 \\ 100.00\% \\ 2 \\ 0$	$1\\100\\2\\2$	- - - -	Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit:	$955 \\ 53 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\%$	$ \begin{array}{c} 1 \\ 100 \\ 2 \\ 2 \\ 100 \end{array} $	- - - -	Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0]	$955 \\ 53 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 791$	$1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1$	- - - -	Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	955 53 $100.00%$ 2 0 $100.00%$ 791 217	$egin{array}{c} 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \end{array}$	- - - - -	Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$	$1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100$	- - - - - -	Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2	$ \begin{array}{c} 1\\100\\2\\2\\100\\1\\1\\100\\2 \end{array} $	- - - - - -	Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2 \end{array} $	 	Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2	$ \begin{array}{c} 1\\100\\2\\2\\100\\1\\1\\100\\2 \end{array} $	 	Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2 \end{array} $	 	Covered Covered Covered
bin auto [1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto [0]	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2\\ 100 \end{array} $	 	Covered Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943 65	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1 \end{array} $	 	Covered Covered Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943 65 $100.00%$	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100 \end{array} $	 	Covered Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943 65 $100.00%$ 6	1 100 2 2 2 100 1 1 100 2 2 100 1 1 100 6		Covered Covered Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943 65 $100.00%$ 6 0	$ \begin{array}{c} 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 6\\ 6\\ 6 \end{array} $		Covered Covered Covered Covered Covered
bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins:	955 53 $100.00%$ 2 0 $100.00%$ 791 217 $100.00%$ 2 0 $100.00%$ 943 65 $100.00%$ 6	1 100 2 2 2 100 1 1 100 2 2 100 1 1 100 6		Covered Covered Covered Covered Covered

Auto Default and Hear Defined Bing.				
Auto, Default and User Defined Bins: bin $<$ auto[1], auto[1], auto[1]>	172	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	42	1	_	Covered
bin $<$ auto [0], auto [1], auto [1]>	404	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	105	1	_	Covered
bin < auto[1], auto[0], auto[0] >	78	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	207	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO
Cross full_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	6 0	$\frac{6}{6}$	_	
% Hit:	100.00%	100		
Auto, Default and User Defined Bins:	100.0070	100		
bin < auto[0], auto[1], auto[1] >	59	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	22	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	214	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	78	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight]>$	450	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > 1$	185	1	_	Covered
Illegal and Ignore Bins:	0			ZEDO
ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full	0		_	ZERO ZERO
Cross empty_cross	100.00%	100		Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]\!>$	33	1	_	$\operatorname{Covered}$
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight]>$	39	1	_	Covered
bin < auto[1], auto[1], auto[0] >	181	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	437	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$\begin{array}{c} 39 \\ 138 \end{array}$	1 1	_	Covered Covered
$ ext{bin } < ext{auto} [0] , ext{auto} [0] , ext{auto} [0] > \\ ext{Illegal and Ignore Bins:}$	130	1	_	Covered
ignore_bin read_nactv_empty	141		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] >$	20	1	_	Covered
	17	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	8	1	_	Covered Covered
$egin{aligned} ext{bin } < & ext{auto} \left[0 ight], & ext{auto} \left[1 ight] > \ ext{bin } < & ext{auto} \left[1 ight], & ext{auto} \left[0 ight] > \end{aligned}$	$8\\194$	1 1	_	Covered Covered
bin $<$ auto[1], auto[1], auto[0]>	492	1	_	Covered
bin $<$ auto [1], auto [0], auto [0]>	70	1	_	Covered
bin $<$ auto [0], auto [0], auto [0]>	199	1	_	Covered
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	70	1		Command
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \end{aligned}$	79 91	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	11	1	_	Covered
bin $<$ auto [0], auto [0], auto [1]>	36	1	_	Covered
bin < auto[1], auto[1], auto[0] >	135	1	_	Covered
bin < auto[0], auto[1], auto[0] >	418	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	67	1	_	Covered
$\mathrm{bin} <\! \mathrm{auto} [0] , \mathrm{auto} [0] , \mathrm{auto} [0] >$	171	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	100.00%	6	_	
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
bin $<$ auto [1], auto [1] $>$	12	1	_	Covered
bin $<$ auto[1], auto[1], auto[0]>	202	1	_	Covered
bin $<$ auto [0], auto [1], auto [1]>	39	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	470	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	78	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	207	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0	1.00	_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	6 0	$\frac{6}{6}$	_	
missing/total bins: % Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	45	1	_	Covered
bin $<$ auto [1], auto [0], auto [1]>	20	1	_	Covered
$\operatorname{bin} < \operatorname{auto}\left[1\right], \operatorname{auto}\left[1\right], \operatorname{auto}\left[0\right] >$	169	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	509	1	_	Covered
bin < auto[1], auto[0], auto[0] >	58	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	207	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0			ZERO

TOTAL COVERGROUP COVERAGE: 99.83% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.83%

▼ Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Ty
/FIFO_top/dut/cov	SVA	1	Off	866	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	866	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	866	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	3	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	24	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	183	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	49	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	72	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	189	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	49	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	✓	Off	28	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	484	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	√	Off	143	1	Unli	1	100%		I ✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 3: SVA "Seed3"

${\bf 4.4}\quad {\bf Functional~Coverage~"seed 4"~Report}$

Coverage Report by instance with details

== Instance: /FIFO_coverage_pk == Design Unit: work.FIFO_cove					
Covergroup Coverage:					
$\operatorname{Covergroups}$	1	na	na	99.75%	
$\operatorname{Coverpoints}/\operatorname{Crosses}$	19	$^{\mathrm{na}}$	na	na	
Carranana Pina	104	1.0.1	2	00 4507	

Covergroup Bins	19 na 194 191	$^{ m na}_3$	$^{\mathrm{na}}_{98.45\%}$		
Covergroup		Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_co	overage/fifo_cg	99.75%	100		Uncovered
covered/total bins:		191	194	_	
missing/total bins:		3	194	_	
% Hit:		98.45%	100	_	
$Coverpoint rst_n_cp$		100.00%	100	_	$\operatorname{Covered}$
covered/total bins:		2	2	_	
missing/total bins:		0	2	_	
% Hit:		100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$		159	1	_	$\operatorname{Covered}$
$ \text{bin } \ \text{auto} [1]$		849	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp		100.00%	100	_	$\operatorname{Covered}$
covered/total bins:		64	64	_	
missing/total bins:		0	64	_	
% Hit:		100.00%	100	_	
bin auto [0:1023]		18	1	_	$\operatorname{Covered}$
bin auto $[1024:2047]$		17	1	_	$\operatorname{Covered}$
bin auto [2048:3071]		10	1	_	$\operatorname{Covered}$
bin auto [3072:4095]		18	1	_	$\operatorname{Covered}$
bin auto [4096:5119]		18	1	_	$\operatorname{Covered}$
bin auto [5120:6143]		14	1	_	$\operatorname{Covered}$
bin auto $[6144:7167]$		16	1	_	Covered
bin auto [7168:8191]		26	1	_	Covered
bin auto [8192:9215]		15	1	_	Covered
bin auto [9216:10239]		15	1	_	Covered
bin auto [10240:11263]		12	1	_	Covered
bin auto [11264:11268]		18	1	_	Covered
bin auto [12288:13311]		15	1	_	Covered
bin auto [13312:14335]		13	1	_	Covered
bin auto [13312:14333] bin auto [14336:15359]		19	1	_	Covered
bin auto [15360:16383]		16	1		Covered
bin auto [16384:17407]		13	1	_	Covered
bin auto [17408:18431]		13 17	1	_	Covered
bin auto $[17408:18431]$ bin auto $[18432:19455]$			1	_	Covered
		17	1	_	
bin auto [19456:20479]		21	1	_	Covered
bin auto [20480:21503]		17	1	_	Covered
bin auto [21504:22527]		13	1	_	Covered
bin auto [22528:23551]		13	1	_	Covered
bin auto [23552:24575]		18	1	_	Covered
bin auto [24576:25599]		18	1	_	Covered
bin auto [25600:26623]		16	1	_	Covered
bin auto [26624:27647]		21	1	_	Covered
bin auto $[27648:28671]$		15	1	_	Covered
$\mathrm{bin} \ \mathrm{auto} \left[28672 \colon\! 29695 \right]$		19	1	_	$\operatorname{Covered}$
bin auto $[29696:30719]$		16	1	_	$\operatorname{Covered}$
bin auto $[30720:31743]$		11	1	_	$\operatorname{Covered}$
bin auto $[31744:32767]$		18	1	_	$\operatorname{Covered}$
bin auto [32768:33791]		11	1	_	$\operatorname{Covered}$
bin auto [33792:34815]		19	1	_	$\operatorname{Covered}$
bin auto [34816:35839]		12	1	_	$\operatorname{Covered}$
bin auto [35840:36863]		12	1	_	Covered
bin auto [36864:37887]		12	1	_	Covered
bin auto [37888:38911]		12	1	_	Covered
bin auto [38912:39935]		10	1	_	Covered
bin auto [39936:40959]		13	1	_	Covered
bin auto [40960:41983]		15	1	_	Covered
bin auto $[41984:43007]$		9	1	_	Covered
bin auto [43008:44031]		18	1	_	Covered
bin auto [44032:45055]		14	1	_	Covered
bin auto [45056:46079]		16	1	_	Covered
2111 WW.O [10000. 100 0]		10	1		00.0104

bin auto [46080:47103]	13	1	_	Covered
bin auto [47104:48127]	15	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto [49152:50175]	16	1	_	Covered
bin auto [50176:51199]	13	1	_	Covered
bin auto [51200:52223]	21	1	_	Covered
bin auto [52224:53247]	11	1	_	Covered
bin auto [53248:54271]	10	1	_	Covered
bin auto [54272:55295]	18	1		Covered
bin auto [55296:56319]	18	1		Covered
bin auto [56320:57343]	$\frac{13}{23}$	1		Covered
bin auto [57344:58367]	15	1	_	Covered
			_	
bin auto [58368:59391]	18	1	_	Covered
bin auto [59392:60415]	19	1	_	Covered
bin auto [60416:61439]	16	1	_	Covered
bin auto [61440:62463]	19	1	_	Covered
bin auto $[62464:63487]$	20	1	_	Covered
bin auto $[63488:64511]$	15	1	_	Covered
bin auto $[64512:65535]$	15	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	709	1	_	Covered
bin auto[1]	299	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	315	1	_	Covered
bin auto[1]	693	1	_	Covered
Coverpoint data_out_cp	95.31%	100	_	Uncovered Uncovered
			_	Uncovered
covered/total bins:	61	64	_	
missing/total bins:	3	64	_	
% Hit:	95.31%	100	_	
bin auto [0:1023]	541	1	_	Covered
bin auto $[1024:2047]$	5	1	_	Covered
bin auto $[2048:3071]$	5	1	_	Covered
bin auto $[3072:4095]$	6	1	_	Covered
bin auto $[4096:5119]$	9	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[5120 \colon 6143\right]$	8	1	_	Covered
bin auto [6144:7167]	4	1	_	Covered
bin auto [7168:8191]	17	1	_	Covered
bin auto [8192:9215]	18	1	_	Covered
bin auto [9216:10239]	9	1	_	Covered
bin auto [10240:11263]	5	1	_	Covered
bin auto [11264:12287]	3	1	_	Covered
bin auto[12288:13311]	9	1	_	Covered
bin auto [13312:14335]	$\frac{3}{14}$	1	_	Covered
bin auto [14336:15359]	5	1	_	Covered
· ·				
bin auto [15360:16383]	9	1	_	Covered
bin auto [16384:17407]	8	1	_	Covered
bin auto [17408:18431]	15	1	_	Covered
bin auto [18432:19455]	0	1	_	ZERO
bin auto $[19456:20479]$	3	1	_	Covered
bin auto [20480:21503]	8	1	_	Covered
bin auto $[21504:22527]$	0	1	_	ZERO
$\operatorname{bin} \ \operatorname{auto} \left[22528 \colon\! 23551 \right]$	5	1	_	Covered
${ m bin \ auto} [23552{:}24575]$	11	1	_	$\operatorname{Covered}$
bin auto $[24576:25599]$	9	1	_	Covered
${ m bin \ auto} [25600{:}26623]$	4	1	_	Covered
bin auto [26624:27647]	9	1	_	Covered
bin auto [27648:28671]	9	1	_	Covered
bin auto [28672:29695]	9	1	_	Covered
bin auto [29696:30719]	3	1	_	Covered
bin auto [30720:31743]	5	1	_	Covered
bin auto [31744:32767]	9	1	_	Covered
bin auto [32768:33791]	6	1	_	Covered
bin auto [33792:34815]	10	1	_	Covered
bin auto [34816:35839]	2	1	_	Covered
bin auto [35840:36863]	$\frac{2}{4}$	1	_	Covered
bin auto [36864:37887]	12	1	_	Covered
bin auto [37888:38911]	6	1		Covered
bin auto[37888:38911] bin auto[38912:39935]	$\frac{6}{3}$	1		Covered
bin auto[38912:39935] bin auto[39936:40959]	3 6	1	_	Covered
bin auto[39930:40959] bin auto[40960:41983]		1	_	Covered
i j	8		_	
bin auto [41984:43007]	1	1	_	Covered
bin auto [43008:44031]	29	1	_	Covered
bin auto [44032:45055]	7	1	_	Covered
bin auto [45056:46079]	0	1	_	ZERO
bin auto [46080:47103]	6	1	_	Covered
bin auto [47104:48127]	15	1	_	Covered
bin auto [48128:49151]	5	1	_	Covered
bin auto $[49152:50175]$	2	1	_	Covered
bin auto $[50176:51199]$	4	1	_	Covered
bin auto [51200:52223]	12	1	_	Covered
bin auto [52224:53247]	12	1	_	Covered
bin auto [53248:54271]	7	1	_	Covered
bin auto [54272:55295]	2	1	_	Covered
bin auto [55296:56319]	5	1	_	Covered
bin auto [56320:57343]	18	1	_	Covered
bin auto [57344:58367]	6	1	_	Covered
	Ÿ	-		

bin auto [58368:59391]	_			
1: [[[[[[[[[[[[[[[[[[[8	1	_	Covered
bin auto [59392:60415]	2	1	_	Covered
bin auto [60416:61439]	1	1	_	Covered
bin auto [61440:62463]	11	1	_	Covered
bin auto [62464:63487]	7	1	_	Covered
bin auto [63488:64511]	9	1	_	Covered
bin auto [64512:65535]	8	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	443	1	_	Covered
bin auto [1]	565	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	$\overset{2}{2}$		
% Hit:	100.00%	100	_	
bin auto [0]	977	1		Covered
bin auto [1]	31	1		Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{100.0076}{2}$	$\frac{100}{2}$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
	972		_	Covered
bin auto[0]		1	_	
bin auto[1]	36	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 ight]$	772	1	_	Covered
bin auto [1]	236	1	_	$\operatorname{Covered}$
Coverpoint almostfull_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	958	1	_	Covered
bin auto[1]	50	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	790	1	_	Covered
bin auto [1]	218	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2		Covered
missing/total bins:	0 = 0	$\frac{2}{2}$	_	
- ·	100.00%		_	
% Hit:		100	_	C 1
bin auto[0]	939	1	_	Covered
bin auto[1]	69	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	6	6	_	
missing/total bins:		6		
A	0		_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.00%		_	
Auto, Default and User Defined Bins: bin $<$ auto[1], auto[1], auto[1]>	100.00% 155	100	_ _ _	Covered
$\begin{array}{c} \text{Auto},\;\; \text{Default}\;\; \text{and}\;\; \text{User}\;\; \text{Defined}\;\; \text{Bins} \colon\\ \text{bin}\;\; < \text{auto}[1]\;, \text{auto}[1]\;, \text{auto}[1]\;,\\ \text{bin}\;\; < \text{auto}[1]\;, \text{auto}[1]\;, \text{auto}[0]\;> \end{array}$	100.00% 155 43		_ _ _	Covered
Auto, Default and User Defined Bins: bin $<$ auto[1], auto[1], auto[1]> bin $<$ auto[1], auto[1], auto[0]> bin $<$ auto[0], auto[1], auto[1]>	100.00% 155 43 410	1	_ _ _ _	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
Auto, Default and User Defined Bins: $\begin{array}{l} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \end{array}$	100.00% 155 43 410 85	1		Covered Covered Covered
Auto, Default and User Defined Bins: $\begin{array}{c} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \end{array}$	100.00% 155 43 410 85 101	1 1 1	_	Covered Covered Covered Covered
Auto, Default and User Defined Bins: $\begin{array}{l} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \end{array}$	100.00% 155 43 410 85	1 1 1	_ _	Covered Covered Covered
Auto, Default and User Defined Bins: $\begin{array}{c} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \end{array}$	100.00% 155 43 410 85 101	1 1 1 1	_ _ _	Covered Covered Covered Covered
Auto, Default and User Defined Bins: $\begin{array}{l} \text{bin } < \text{auto} [1] , \text{auto} [1] , \text{auto} [1] > \\ \text{bin } < \text{auto} [1] , \text{auto} [1] , \text{auto} [0] > \\ \text{bin } < \text{auto} [0] , \text{auto} [1] , \text{auto} [1] > \\ \text{bin } < \text{auto} [0] , \text{auto} [1] , \text{auto} [0] > \\ \text{bin } < \text{auto} [1] , \text{auto} [0] , \text{auto} [0] > \\ \text{bin } < \text{auto} [0] , \text{auto} [0] , \text{auto} [0] > \\ \end{array}$	100.00% 155 43 410 85 101	1 1 1 1	_ _ _	Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	100.00% 155 43 410 85 101 214	1 1 1 1	_ _ _	Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	100.00% 155 43 410 85 101 214	1 1 1 1 1	_ _ _	Covered Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$	1 1 1 1 1 1	_ _ _	Covered Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6	1 1 1 1 1 1 100 6	_ _ _	Covered Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0	1 1 1 1 1 1 100 6 6	_ _ _	Covered Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0	1 1 1 1 1 1 100 6 6	_ _ _	Covered Covered Covered Covered Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 1 100 6 6 6 100	_ _ _	Covered Covered Covered Covered ZERO Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$ 32 4	1 1 1 1 1 1 1 100 6 6 100	_ _ _	Covered Covered Covered Covered Covered ZERO Covered Covered
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Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$ 32 4 198 101 463 210 0 0	1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered ZERO Covered Covered Covered Covered Covered Covered Covered Covered Covered Covered Covered Covered Covered Covered
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Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$ 32 4 198 101 463 210 0 0 $100.00%$ 6 0 $100.00%$ $100.00%$ $100.00%$ $100.00%$ $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins:</auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$ 32 4 198 101 463 210 0 $100.00%$ 6 0 $100.00%$ 6 0 $100.00%$ $100.00%$ 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	100.00% 155 43 410 85 101 214 0 $100.00%$ 6 0 $100.00%$ 32 4 198 101 463 210 0 0 $100.00%$ 6 0 $100.00%$ $100.00%$ $100.00%$ $100.00%$ $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	17	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	19	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	5	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	9	1	_	Covered
bin $<$ auto [1], auto [1], auto [0]>	181	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	476	1	_	Covered
bin $\langle auto[0], auto[1], auto[0] \rangle$	96	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	205	1		Covered
Cross almostempty_cross	100.00%	100	_	Covered
- *			_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]\!>$	71	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[1]\;,\mathrm{auto}[1]>$	97	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[0 ight] , \mathrm{auto} \left[1 ight] > $	12	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight] >$	38	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right] >$	127	1	_	Covered
bin < auto[0], auto[1], auto[0] >	398	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	89	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	176	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	14	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	184	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	17	1		Covered
	478	1		Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$			_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	101	1	_	
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > 0$	214	1	_	Covered
Illegal and Ignore Bins:				ZED O
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight]\!>$	45	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ <\! \mathrm{auto} \left[1 ight], \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight]\!>$	24	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right] >$	153	1	_	Covered
bin < auto[0], auto[1], auto[0] >	495	1	_	Covered
bin < auto[1], auto[0], auto[0] >	77	1	_	Covered
bin $\langle auto[0], auto[0], auto[0] \rangle$	214	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
9				

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100		Uncovered
covered/total bins:	191	194	_	
missing/total bins:	3	194	_	
% Hit:	98.45%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	159	1	_	Covered
bin auto[1]	849	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	18	1	_	Covered
bin auto [1024:2047]	17	1	_	Covered
bin auto $\begin{bmatrix} 2048:3071 \end{bmatrix}$	10	1	_	Covered
bin auto [3072:4095]	18	1	_	Covered
bin auto $[4096:5119]$	18	1	_	Covered
bin auto [5120:6143]	14	1	_	Covered
bin auto [6144:7167]	16	1	_	Covered
bin auto [7168:8191]	26	1	_	Covered
bin auto [8192:9215]	15	1	_	Covered
bin auto [9216:10239]	15	1	_	Covered
bin auto [10240:11263]	12	1	_	Covered
bin auto [11264:12287]	18	1	_	Covered
bin auto [12288:13311]	15	1	_	Covered
bin auto [13312:14335]	13	1	_	Covered
bin auto [14336:15359]	19	1	_	Covered
bin auto [15360:16383]	16	1	_	Covered
bin auto [16384:17407]	13	1	_	Covered
bin auto [17408:18431]	17	1	_	Covered
bin auto [18432:19455]	17	1	_	Covered
bin auto [19456:20479]	21	1	_	Covered
bin auto [20480:21503]	17	1	_	Covered
bin auto [21504:22527]	13	1	_	Covered
bin auto [22528:23551]	13	1	_	Covered

bin auto [23552:24575]				
DIII auto [23332.24373]	18	1	_	$\operatorname{Covered}$
bin auto [24576:25599]	18	1	_	Covered
$\mathrm{bin} \ \ \mathrm{auto} \left[25600 \colon\! 26623 \right]$	16	1	_	Covered
bin auto [26624:27647]	21	1	_	Covered
bin auto [27648:28671]	15	1	_	Covered
<u>.</u>				Covered
bin auto [28672:29695]	19	1	_	
bin auto $[29696:30719]$	16	1	_	Covered
bin auto [30720:31743]	11	1	_	Covered
				Covered
bin auto [31744:32767]	18	1	_	
bin auto [32768:33791]	11	1	_	Covered
bin auto [33792:34815]	19	1	_	Covered
bin auto [34816:35839]				Covered
	12	1	_	
bin auto [35840:36863]	12	1	_	Covered
bin auto [36864:37887]	12	1	_	Covered
bin auto [37888:38911]	12	1	_	Covered
bin auto [38912:39935]	10	1	_	Covered
bin auto [39936:40959]	13	1	_	Covered
bin auto $[40960:41983]$	15	1	_	Covered
bin auto $[41984:43007]$	9	1	_	$\operatorname{Covered}$
bin auto [43008:44031]	18	1	_	Covered
${\rm bin \ \ auto} [44032\!:\!45055]$	14	1	_	Covered
bin auto [45056:46079]	16	1	_	$\operatorname{Covered}$
bin auto [46080:47103]	13	1	_	Covered
bin auto [47104:48127]	15	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto [49152:50175]	16	1	_	Covered
$\mathrm{bin} \ \ \mathrm{auto} \left[50176 {:} 51199 \right]$	13	1	_	Covered
bin auto $[51200:52223]$	21	1	_	$\operatorname{Covered}$
bin auto [52224:53247]	11	1	_	Covered
bin auto [53248:54271]	10	1	_	Covered
bin auto $[54272:55295]$	18	1	_	Covered
bin auto [55296:56319]	18	1	_	Covered
	$\frac{13}{23}$	1		Covered
$\mathrm{bin} \ \ \mathrm{auto} \left[56320 \colon 57343 \right]$			_	
bin auto $[57344:58367]$	15	1	_	$\operatorname{Covered}$
bin auto [58368:59391]	18	1	_	Covered
bin auto $[59392:60415]$	19	1	_	Covered
bin auto $[60416:61439]$	16	1	_	$\operatorname{Covered}$
bin auto [61440:62463]	19	1		Covered
		_		
bin auto $[62464:63487]$	20	1	_	Covered
bin auto $[63488:64511]$	15	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	15	1	_	Covered
		_		
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
	_	_		
% Hit:	100.00%	100	_	
bin auto $[0]$	709	1	_	$\operatorname{Covered}$
hin auto[1]	200	1		Covered
bin auto[1]	299	1	_	Covered
Coverpoint w_en_cp	$\frac{299}{100.00\%}$	$1\\100$	_	Covered Covered
Coverpoint w_en_cp			_ _ _	
Coverpoint w_en_cp covered/total bins:	$\frac{100.00\%}{2}$	$100 \\ 2$	_ _ _	
Coverpoint w_en_cp covered/total bins: missing/total bins:	$100.00\% \ 2 \ 0$	$100 \\ 2 \\ 2$	_ _ _ _	
Coverpoint w_en_cp covered/total bins:	$\frac{100.00\%}{2}$	$100 \\ 2$	_ _ _ _	
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit:	$100.00\% \ 2 \ 0 \ 100.00\%$	$100 \\ 2 \\ 2$	- - - -	
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0]	100.00% 2 0 $100.00%$ 315	$100 \\ 2 \\ 2 \\ 100 \\ 1$	- - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 315 693	100 2 2 100 1 1	- - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$	100 2 2 100 1 1 100	- - - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp	100.00% 2 0 $100.00%$ 315 693	100 2 2 100 1 1	- - - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins:	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61	100 2 2 100 1 1 100 64	- - - - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3	100 2 2 100 1 1 100 64 64	- - - - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit:	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$	100 2 2 100 1 1 100 64 64 100	- - - - - - - -	Covered Covered Uncovered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3	100 2 2 100 1 1 100 64 64	- - - - - - - -	Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541	100 2 2 100 1 1 100 64 64 100 1	_ _ _ _	Covered Covered Uncovered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5	100 2 2 100 1 1 100 64 64 100 1 1	- - - - -	Covered Covered Uncovered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5	100 2 2 100 1 1 100 64 64 100 1 1 1	_ _ _ _ _	Covered Covered Uncovered Covered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5	100 2 2 100 1 1 100 64 64 100 1 1	- - - - -	Covered Covered Uncovered Covered Covered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5	100 2 2 100 1 1 100 64 64 100 1 1 1	- - - - - -	Covered Covered Uncovered Covered Covered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8	100 2 2 100 1 1 100 64 64 100 1 1 1 1	- - - - - - - -	Covered Covered Uncovered Covered Covered Covered Covered Covered Covered Covered
Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[0:4:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167]	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4	100 2 2 100 1 1 100 64 64 100 1 1 1 1	- - - - - - -	Covered Covered Uncovered Covered Covered Covered Covered Covered Covered Covered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8	100 2 2 100 1 1 100 64 64 100 1 1 1 1	- - - - - - - -	Covered Covered Uncovered Covered Covered Covered Covered Covered Covered Covered Covered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17	100 2 2 100 1 1 100 64 64 100 1 1 1 1	- - - - - - - -	Covered Covered Uncovered Covered Covered Covered Covered Covered Covered Covered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1	- - - - - - - - - -	Covered Covered Uncovered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1	- - - - - - - - - -	Covered Covered Uncovered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 315 693 $95.31%$ 61 3 $95.31%$ 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11 9 4 9 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11 9 4 9 9 9 9 9 9 9 9 9	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11 9 4 9 9 9 9 9 9 9 6	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00% 2 0 100.00% 315 693 95.31% 61 3 95.31% 541 5 6 9 8 4 17 18 9 5 3 9 14 5 9 8 15 0 3 8 0 5 11 9 4 9 9 9 9 9 9 9 6	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint w_en_cp	100.00%	100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

bin auto [35840:36863]		1		C 1
	4	1	_	Covered
bin auto [36864:37887]	12	1	_	Covered
bin auto [37888:38911]	6	1	_	Covered
bin auto [38912:39935]	3	1	_	Covered
bin auto [39936:40959]	6	1	_	Covered
bin auto $[40960:41983]$	8	1	_	Covered
bin auto [41984:43007]	1	1	_	Covered
bin auto $[43008:44031]$	29	1	_	Covered
bin auto $[44032:45055]$	7	1	_	Covered
bin auto $[45056:46079]$	0	1	_	ZERO
bin auto [46080:47103]	6	1	_	Covered
bin auto [47104:48127]	15	1	_	Covered
bin auto [48128:49151]	5	1	_	Covered
bin auto [49152:50175]	$\frac{1}{2}$	1	_	Covered
bin auto [50176:51199]	$\frac{2}{4}$	1	_	Covered
bin auto [51200:52223]	12	1	_	Covered
bin auto [52224:53247]	12	1	_	Covered
· ·				
bin auto [53248:54271]	7	1	_	Covered
bin auto [54272:55295]	2	1	_	Covered
$\texttt{bin auto} \left[55296 \colon 56319\right]$	5	1	_	Covered
bin auto $[56320:57343]$	18	1	_	Covered
bin auto $[57344:58367]$	6	1	_	Covered
bin auto $[58368:59391]$	8	1	_	Covered
bin auto $[59392:60415]$	2	1	_	Covered
bin auto [60416:61439]	1	1	_	Covered
bin auto [61440:62463]	11	1	_	Covered
bin auto $[62464:63487]$	7	1	_	Covered
bin auto [63488:64511]	9	1	_	Covered
bin auto [64512:65535]	8	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
			_	Covered
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$	443	1	_	$\operatorname{Covered}$
bin auto[1]	565	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	977	1	_	Covered
bin auto[1]	31	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$		Covered
			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$	972	1	_	Covered
bin auto[1]	36	1	_	$\operatorname{Covered}$
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	772	1	_	Covered
bin auto[1]	236	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{100.0076}{2}$	$\frac{100}{2}$		Covered
			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	~ .
bin auto $[0]$	958	1	_	$\widehat{\text{Covered}}$
bin auto [1]	50	1	_	Covered
$\operatorname{Coverpoint}$ almostempty_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2		
:	2	2	_	
missing/total bins:	0	$\frac{2}{2}$	_	
missing/total bins: % Hit:			_ _ _	
	0	2	_ _ _ _	Covered
% Hit:	$0 \\ 100.00\%$	$\begin{matrix}2\\100\end{matrix}$	_ _ _ _	Covered Covered
% Hit: bin auto[0] bin auto[1]	$0 \\ 100.00\% \\ 790 \\ 218$	$\begin{matrix}2\\100\\1\\1\end{matrix}$	_ _ _ _	
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp	$0 \\ 100.00\% \\ 790$	$\begin{matrix}2\\100\\1\end{matrix}$	- - - - -	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins:	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\%$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \end{array}$	- - - - -	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins:	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \end{array} $	- - - - -	Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit:	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\%$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \end{array} $	- - - - - -	Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0]</pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939$	$ \begin{array}{c} 2\\100\\ 1\\ 1\\ 100\\ 2\\ 2\\ 100\\ 1 \end{array} $	- - - - - - -	Covered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69$	2 100 1 1 100 2 2 2 100 1	- - - - - - -	Covered Covered Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\%$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ \end{array}$	- - - - - - - -	Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins:</pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\% \\ 6$	2 100 1 1 100 2 2 100 1 1 100 6	- - - - - - - - -	Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins:</pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\% \\ 6 \\ 0$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 6 \\ 6 \end{array}$	- - - - - - - - - -	Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit:</pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\% \\ 6$	2 100 1 1 100 2 2 100 1 1 100 6	- - - - - - - - - - - - -	Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\% \\ 6 \\ 0 \\ 100.00\%$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100		Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 6 100		Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""></auto[1],></pre>	$0 \\ 100.00\% \\ 790 \\ 218 \\ 100.00\% \\ 2 \\ 0 \\ 100.00\% \\ 939 \\ 69 \\ 100.00\% \\ 6 \\ 0 \\ 100.00\%$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100		Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 6 100		Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 6 100		Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100		Covered Covered Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85$	2 100 1 1 100 2 2 100 1 1 100 6 6 100		Covered Covered Covered Covered Covered Covered Covered Covered Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100		Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100		Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 6 100		Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\%$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 6 100		Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100 1 1 1 1 1		Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6 \ 0 \ 0$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100 1 1 1 1 1		Covered
% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: % Hit:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6$	2 100 1 1 100 2 2 2 100 1 1 100 6 6 100 1 1 1 1 1		Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ $	2 100 1 1 100 2 2 100 1 1 100 6 6 100 1 1 1 1 1 1 1 1 1		Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 32$	2 100 1 1 100 2 2 100 1 1 100 6 6 100 1 1 1 1 1 1 1 1 1 1		Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> </auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 939 \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 32 \ 4$	2 100 1 1 1 100 2 2 100 1 1 1 100 6 6 100 1 1 1 1 1 1 1 1		Covered
<pre>% Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross full_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	$0 \ 100.00\% \ 790 \ 218 \ 100.00\% \ 2 \ 0 \ 100.00\% \ 69 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 155 \ 43 \ 410 \ 85 \ 101 \ 214 \ 0 \ 100.00\% \ 6 \ 0 \ 100.00\% \ 32$	2 100 1 1 100 2 2 100 1 1 100 6 6 100 1 1 1 1 1 1 1 1 1 1		Covered

$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	101	1	_	Covered
bin < auto[0], auto[1], auto[0] >	463	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0]$	210	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: $\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	34	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	50	1		Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	164	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	421	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	51	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	136	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight] >$	17	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right] >$	19	1	_	Covered
bin < auto[1], auto[0], auto[1] >	5	1	_	Covered
bin < auto [0], auto [0], auto [1] >	9	1	_	Covered
bin < auto[1], auto[1], auto[0] >	181	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	476	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] > \\ \operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > $	$\frac{96}{205}$	1 1	_	$egin{array}{c} { m Covered} \\ { m Covered} \end{array}$
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	8	8		Covered
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
$\operatorname{bin} = \operatorname{auto}[1], \operatorname{auto}[1] > 1$	71	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	97	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	12	1	_	Covered
bin < auto[0], auto[0], auto[1] >	38	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[1]\;,\mathrm{auto}[0]\!>$	127	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[1]\;,\mathrm{auto}[0]\!>$	398	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[0]\;,\mathrm{auto}[0]>$	89	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]>$	176	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	14	1		Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ \end{aligned}$	$\frac{14}{184}$	1 1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	17	1		Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	478	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	101	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	214	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto} \left[1 ight], \operatorname{auto} \left[1 ight], \operatorname{auto} \left[1 ight] >$	45	1	_	$\widetilde{\text{Covered}}$
	24	1	_	Covered
bin < auto[1], auto[1], auto[0] >	153	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	495	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	77	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ >	214	1	_	Covered
Illegal and Ignore Bins:	0			ZERO
ignore_bin r_en_nactv_wr_ack	0		_	ZERU

TOTAL COVERGROUP COVERAGE: 99.75% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.75%

▼ Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov	SVA	1	Off	850	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	850	1	Unli	1	100%		V	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	850	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	V	Off	1	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	21	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	181	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	43	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	29	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	197	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	55	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	9	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	484	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov	SVA	1	Off	159	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 4: SVA "Seed4"

4.5 Functional Coverage "seed5" Report

Coverage Report by instance with details

Instance: /FIFO_coverage_pkg
Design Unit: work.FIFO_coverage_pkg

besign Unit: work.FIFO_coverage_pkg

Covergroup Coverage:

 Covergroups
 1
 na
 na
 99.91%

 Coverpoints/Crosses
 19
 na
 na
 na

 Covergroup Bins
 194
 193
 1
 99.48%

Covergroup Bins 194 193	1 99.	48%		
overgroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.91%	100		Uncovered
covered/total bins:	193	194	_	
missing/total bins:	1	194	_	
% Hit:	99.48%	100	_	C 1
Coverpoint rst_n_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	162	1	_	Covered
bin auto[1]	846	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	C1
$egin{array}{ll} { m bin \ auto} [0\!:\!1023] \ { m bin \ auto} [1024\!:\!2047] \end{array}$	$\frac{18}{12}$	1 1	_	Covered Covered
bin auto [$2048:3071$]	21	1	_	Covered
bin auto $[3072:4095]$	$\frac{21}{14}$	1	_	Covered
bin auto [4096:5119]	19	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[5120 \!:\! 6143 \right]$	17	1	_	Covered
bin auto [6144:7167]	12	1	_	Covered
bin auto [7168:8191]	16	1	_	Covered
bin auto [8192:9215]	9	1	_	Covered
bin auto [9216:10239]	10	1	_	Covered
bin auto [10240:11263] bin auto [11264:12287]	$\frac{16}{21}$	1 1	_	Covered Covered
bin auto [12288:13311]	16	1	_	Covered
bin auto [13312:14335]	9	1	_	Covered
bin auto [14336:15359]	16	1	_	Covered
bin auto [15360:16383]	14	1	_	Covered
bin auto [16384:17407]	21	1	_	Covered
bin auto [17408:18431]	18	1	_	$\operatorname{Covered}$
bin auto [18432:19455]	18	1	_	Covered
bin auto [19456:20479]	19	1	_	Covered
$egin{array}{ll} ext{bin} & ext{auto} \left[20480 {:} 21503 ight] \ ext{bin} & ext{auto} \left[21504 {:} 22527 ight] \end{array}$	16	1	_	Covered
bin auto $[21504:22527]$	$14 \\ 17$	1	_	Covered Covered
bin auto $[23552:24575]$	17	1	_	Covered
bin auto [24576:25599]	16	1	_	Covered
bin auto $[25600:26623]$	25	1	_	Covered
bin auto [26624:27647]	14	1	_	Covered
bin auto $[27648:28671]$	15	1	_	Covered
bin auto [28672:29695]	18	1	_	Covered
bin auto [29696:30719]	10	1	_	Covered
bin auto [30720:31743]	18	1	_	Covered
bin auto [31744:32767] bin auto [32768:33791]	10 19	1	_	Covered Covered
bin auto [32708.33791] bin auto [33792:34815]	19 17	1	_	Covered
bin auto [34816:35839]	21	1	_	Covered
bin auto [35840:36863]	11	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	20	1	_	Covered
bin auto [37888:38911]	17	1	_	Covered
bin auto [38912:39935]	19	1	_	$\widetilde{\text{Covered}}$
bin auto [39936:40959]	18	1	_	Covered
bin auto [40960:41983]	16	1	_	Covered
bin auto [41984:43007] bin auto [43008:44031]	$\begin{array}{c} 21 \\ 13 \end{array}$	1	_	Covered Covered
bin auto $[44032:45051]$	10	1	_	Covered
bin auto [45056:46079]	11	1	_	Covered
bin auto [46080:47103]	9	1	_	Covered
bin auto [47104:48127]	12	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[49152 {:} 50175 \right]$	21	1	_	Covered
bin auto [50176:51199]	16	1	_	Covered
bin auto [51200:52223]	13	1	_	Covered
bin auto [52224:53247]	21	1	_	Covered
bin auto [53248:54271]	15	1	_	Covered
bin auto [54272:55295]	13 13	1	_	Covered
bin auto [55296:56319] bin auto [56320:57343]	13 15	1 1	_	Covered Covered
bin auto $[57344:58367]$	15 14	1	_	Covered Covered
bin auto[57344.38367] bin auto[58368:59391]	13	1	_	Covered
bin auto[59392:60415]	14	1	_	Covered
		-		
bin auto [60416:61439]	19	1	_	$\operatorname{Covered}$

bin auto [62464:63487]	12	1	_	Covered
bin auto [63488:64511]	17	1	_	Covered
bin auto [64512:65535]	16	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	$\frac{2}{0}$	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	713	1	_	Covered
bin auto[1]	295	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	297	1	_	Covered
bin auto[1]	711	1	_	Covered
Coverpoint data_out_cp	98.43%	100	_	Uncovered
covered/total bins:	63	64	_	
missing/total bins:	1	$64 \\ 100$	_	
% Hit: bin auto[0:1023]	$\frac{98.43\%}{506}$	100	_	Covered
bin auto [1024:2047]	3	1		Covered
bin auto [2048:3071]	18	1	_	Covered
bin auto [3072:4095]	1	1	_	Covered
bin auto [4096:5119]	10	1	_	Covered
bin auto [5120:6143]	9	1	_	Covered
bin auto [6144:7167]	13	1	_	Covered
bin auto [7168:8191]	8	1	_	Covered
bin auto [8192:9215]	2	1	_	Covered
bin auto [9216:10239]	1	1	_	Covered
bin auto [10240:11263]	7	1	_	Covered
bin auto [11264:12287]	8	1	_	$\widehat{\text{Covered}}$
bin auto [12288:13311]	13	1	_	Covered
bin auto [13312:14335]	2	1	_	Covered
bin auto [14336:15359] bin auto [15360:16383]	$\frac{12}{5}$	1	_	Covered Covered
bin auto [16384:17407]	$5\\30$	1 1	_	Covered
bin auto [17408:18431]	5 5	1	_	Covered
bin auto [18432:19455]	7	1		Covered
bin auto $[19456:20479]$	10	1	_	Covered
bin auto [20480:21503]	13	1	_	Covered
bin auto [21504:22527]	$\frac{1}{2}$	1	_	Covered
bin auto [22528:23551]	5	1	_	Covered
bin auto [23552:24575]	9	1	_	Covered
bin auto [24576:25599]	7	1	_	Covered
bin auto $[25600:26623]$	5	1	_	Covered
bin auto $[26624:27647]$	4	1	_	Covered
bin auto $[27648:28671]$	11	1	_	Covered
bin auto $[28672:29695]$	15	1	_	$\widehat{\text{Covered}}$
bin auto [29696:30719]	2	1	_	Covered
bin auto [30720:31743]	0	1	_	ZERO
bin auto [31744:32767]	$\frac{3}{5}$	1 1	_	Covered Covered
bin auto [32768:33791] bin auto [33792:34815]	$\frac{3}{13}$	1	_	Covered
bin auto [34816:35839]	$\frac{13}{22}$	1		Covered
bin auto [35840:36863]	2	1	_	Covered
bin auto [36864:37887]	3	1	_	Covered
bin auto [37888:38911]	14	1	_	Covered
bin auto [38912:39935]	6	1	_	Covered
bin auto [39936:40959]	6	1	_	Covered
bin auto $[40960:41983]$	5	1	_	Covered
bin auto $[41984:43007]$	26	1	_	Covered
bin auto [43008:44031]	4	1	_	Covered
bin auto [44032:45055]	13	1	_	Covered
bin auto [45056:46079]	$\frac{2}{2}$	1	_	Covered
bin auto $[46080:47103]$ bin auto $[47104:48127]$	$rac{3}{4}$	1 1	_	Covered Covered
bin auto $[47104:48127]$ bin auto $[48128:49151]$	8	1	_	Covered
bin auto $[49152:50175]$	23	1	_	Covered
bin auto [50176:51199]	13	1	_	Covered
bin auto [51200:52223]	13	1	_	Covered
bin auto [52224:53247]	3	1	_	Covered
bin auto [53248:54271]	3	1	_	Covered
bin auto [54272:55295]	18	1	_	Covered
bin auto $[55296:56319]$	2	1	_	Covered
bin auto [56320:57343]	7	1	_	Covered
bin auto [57344:58367]	3	1	_	Covered
bin auto [58368:59391]	4	1	_	Covered
$egin{array}{lll} { m bin } & { m auto} [59392\!:\!60415] \ { m bin } & { m auto} [60416\!:\!61439] \end{array}$	1 11	1 1	_	Covered Covered
bin auto $[60416:61439]$ bin auto $[61440:62463]$	$\frac{11}{2}$	1	_	Covered
bin auto $[62464:63487]$	$\frac{2}{3}$	1	_	Covered
bin auto $[63488:64511]$	$\frac{3}{12}$	1	_	Covered
bin auto [64512:65535]	8	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	433	1	_	Covered
bin auto[1]	575	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{0}$	$\frac{2}{2}$	_	
missing/total bins:	U	۷	_	

% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	959	1	- Cove	ered
bin auto [1]	49	1	- Cove	ered
Coverpoint full_cp	100.00%	100	- Cove	ered
covered/total bins:	2	2	_	
missing/total bins:	0	2		
% Hit:	100.00%	100	_	
			_	,
$ \text{bin } \text{ auto} \left[0 \right]$	949	1	- Cove	
bin auto [1]	59	1	- Cove	
Coverpoint empty_cp	100.00%	100	Cove	$_{ m ered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	1
bin auto [0]	780	1	- Cove	
bin auto[1]	228	1	- Cove	
Coverpoint almostfull_cp	100.00%	100	– Cove	$_{ m ered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	953	1	- Cove	rod
t 3				
bin auto[1]	55	1	- Cove	
${\bf Coverpoint~almost empty_cp}$	100.00%	100	- Cove	ered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	777	1	- Cove	ered
bin auto[1]	231	1	- Cove	
Coverpoint underflow_cp	100.00%	100	– Cove	теа
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	950	1	- Cove	ered
bin auto [1]	58	1	- Cove	
£ 3	100.00%			
Cross wr_ack_cross		100	- Cove	erea
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1]>	168	1	- Cove	ered
bin $\langle auto[1], auto[1], auto[0] \rangle$	32	1	- Cove	
	$\frac{32}{407}$	_		
bin < auto[0], auto[1], auto[1] >		1	- Cove	
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight] >$	104	1	- Cove	
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[0 ight] , \mathrm{auto} \left[0 ight] > $	95	1	- Cove	$_{ m ered}$
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	202	1	- Cove	ered
Illegal and Ignore Bins:				
ignore_bin_w_en_nactv_wr_ack	0		ZERO	,
_	100.00%	100		a al
Cross full_cross	100.00%	100	– ZERO – Cove	ered
Cross full_cross covered/total bins:		100 6		ered
Cross full_cross covered/total bins:	100.00%			ered
Cross full_cross	100.00%	6		ered
Cross full_cross covered/total bins: missing/total bins: % Hit:	$100.00\% \\ 6 \\ 0$	6 6		ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:	100.00% 6 0 $100.00%$	$\begin{matrix} 6 \\ 6 \\ 100 \end{matrix}$	- Cove - - -	
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""></auto[0],>	100.00% 6 0 $100.00%$ 48	6 6 100	- Cove 	ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- Cove Cove - Cove	ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- Cove Cove - Cove - Cove	ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95	6 6 100 1 1 1 1	- Cove - Cove - Cove - Cove - Cove - Cove	ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- Cove	ered ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95	6 6 100 1 1 1 1	- Cove - Cove - Cove - Cove - Cove - Cove	ered ered ered ered
Cross full_cross	100.00% 6 0 $100.00%$ 48 11 200 95 463	6 6 100 1 1 1 1 1	- Cove	ered ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191	6 6 100 1 1 1 1	- Cove	ered ered ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191	6 6 100 1 1 1 1	- Cove	ered ered ered ered ered
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Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191 0 0 $100.00%$	6 6 100 1 1 1 1 1 1	- Cove	ered ered ered ered ered
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Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191 0 0 $100.00%$ 6 0 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- Cove	ered ered ered ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191 0 0 $100.00%$ 6 0 $100.00%$ 23 53	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- Cove	ered ered ered ered ered ered ered
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Cross full_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: wise thit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: with: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191 0 0 $100.00%$ 6 0 $100.00%$ 23 53 177 435 42 126 152 $100.00%$ 8 0 $100.00%$ 24 22 1 8 176 489 94 194 $100.00%$ 8 0 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- Cove	ered ered ered ered ered ered ered ered
Cross full_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> line <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	100.00% 6 0 $100.00%$ 48 11 200 95 463 191 0 0 $100.00%$ 6 0 $100.00%$ 23 53 177 435 42 126 152 $100.00%$ 8 0 $100.00%$ 24 22 1 8 176 489 94 194 $100.00%$ 8 0	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- Cove	ered ered ered ered ered ered ered ered

1 [0] . [1] . [4].	100	1		0 1
$\begin{array}{ll} \text{bin } < \text{auto} \left[0 \right], \text{auto} \left[1 \right], \text{auto} \left[1 \right] > \end{array}$	103	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[1\right]\!>$	6	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	40	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight]>$	118	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] \! > \!$	408	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[0]\;,\mathrm{auto}[0]>$	89	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	162	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	15	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [1], \text{auto} [0] \rangle$	185	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	34	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	477	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	95	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	202	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	41	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	17	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	159	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	511	1	_	Covered
bin < auto[1], auto[0], auto[0] >	78	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	202	1	_	Covered
Illegal and Ignore Bins:		-		30.0200
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
-0	· ·			

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.91%	100		Uncovered
covered/total bins:	193	194	_	
missing/total bins:	1	194	_	
% Hit:	99.48%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$	162	1	_	$\operatorname{Covered}$
bin auto[1]	846	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	18	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[1024 {:} 2047 \right]$	12	1	_	$\operatorname{Covered}$
bin auto [2048:3071]	21	1	_	Covered
bin auto [3072:4095]	14	1	_	Covered
bin auto [4096:5119]	19	1	_	Covered
bin auto [5120:6143]	17	1	_	Covered
bin auto [6144:7167]	12	1	_	Covered
bin auto [7168:8191]	16	1	_	Covered
bin auto [8192:9215]	9	1	_	Covered
bin auto [9216:10239]	10	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
bin auto [11264:12287]	21	1	_	Covered
bin auto [12288:13311]	$\begin{array}{c} 16 \\ 9 \end{array}$	1	_	Covered Covered
bin auto [13312:14335] bin auto [14336:15359]	16	1 1	_	Covered
bin auto [14336:13339] bin auto [15360:16383]	14	1	_	Covered
bin auto [15360:16383]	$\frac{14}{21}$	1	_	Covered
bin auto [17408:18431]	18	1	_	Covered
bin auto [17403.18431]	18	1		Covered
bin auto [19456:20479]	19	1	_	Covered
bin auto [20480:21503]	16	1	_	Covered
bin auto [21504:22527]	14	1	_	Covered
bin auto [22528:23551]	17	1	_	Covered
bin auto [23552:24575]	17	1	_	Covered
bin auto [24576:25599]	16	1	_	Covered
bin auto [25600:26623]	$\frac{10}{25}$	1	_	Covered
bin auto [26624:27647]	$\frac{26}{14}$	1	_	Covered
bin auto [27648:28671]	15	1	_	Covered
bin auto [28672:29695]	18	1	_	Covered
bin auto [29696:30719]	10	1	_	Covered
bin auto [30720:31743]	18	1	_	Covered
bin auto [31744:32767]	10	1	_	Covered
bin auto [32768:33791]	19	1	_	Covered
bin auto [33792:34815]	17	1	_	Covered
bin auto [34816:35839]	21	1	_	Covered
bin auto [35840:36863]	11	1	_	Covered
bin auto [36864:37887]	20	1	_	Covered
bin auto [37888:38911]	17	1	_	Covered
bin auto [38912:39935]	19	1	_	Covered

bin auto [39936:40959]	18	1	_	Covered
bin auto [40960:41983]	16	1	_	Covered
bin auto [41984:43007]	21	1	_	Covered
bin auto [43008:44031]	13	1	_	Covered
bin auto $[44032:45055]$	10	1	_	Covered
bin auto [45056:46079]	11	1	_	Covered
bin auto [46080:47103]	9	1	_	Covered
bin auto $[47104:48127]$	12	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto [49152:50175]	21	1	_	Covered
bin auto [50176:51199]	16	1		Covered
			_	
bin auto [51200:52223]	13	1	_	Covered
bin auto [52224:53247]	21	1	_	Covered
bin auto [53248:54271]	15	1	_	Covered
bin auto [54272:55295]	13	1	_	Covered
bin auto $[55296:56319]$	13	1	_	Covered
bin auto $[56320:57343]$	15	1	_	Covered
bin auto $[57344:58367]$	14	1	_	Covered
bin auto $[58368:59391]$	13	1	_	Covered
bin auto [59392:60415]	14	1	_	Covered
bin auto [60416:61439]	19	1	_	Covered
bin auto [61440:62463]	19	1	_	Covered
bin auto [62464:63487]	12	1	_	Covered
bin auto [63488:64511]	17	1	_	Covered
bin auto [64512:65535]	16	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	covered
missing/total bins:	0	$\overset{2}{2}$		
% Hit:	100.00%	100	_	
			_	C 1
bin auto [0]	713	1	_	Covered
bin auto[1]	295	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	297	1	_	Covered
bin auto [1]	711	1	_	Covered
Coverpoint data_out_cp	98.43%	100	_	Uncovered
covered/total bins:	63	64	_	
missing/total bins:	1	64	_	
% Hit:	98.43%	100	_	
bin auto [0:1023]	506	1	_	Covered
bin auto [1024:2047]	3	1	_	Covered
bin auto $[2048:3071]$	18	1	_	Covered
bin auto [3072:4095]	1	1		Covered
,	10			Covered
bin auto [4096:5119]		1	_	
bin auto [5120:6143]	9	1	_	Covered
bin auto [6144:7167]	13	1	_	Covered
bin auto [7168:8191]	8	1	_	Covered
bin auto [8192:9215]	2	1	_	Covered
bin auto $[9216:10239]$	1	1	_	$\operatorname{Covered}$
bin auto $[10240:11263]$	7	1	_	$\operatorname{Covered}$
bin auto $[11264:12287]$	8	1	_	$\operatorname{Covered}$
bin auto [12288:13311]	13	1	_	Covered
bin auto [13312:14335]	2	1	_	Covered
bin auto [14336:15359]	12	1	_	Covered
bin auto [15360:16383]	5	1	_	Covered
bin auto [16384:17407]	30	1	_	Covered
bin auto [17408:18431]	5	1	_	Covered
bin auto [18432:19455]	7	1	_	Covered
bin auto [19456:20479]	10	1	_	Covered
bin auto [20480:21503]	13	1	_	Covered
bin auto $[20480.21303]$	$\frac{13}{2}$	1	_	Covered
bin auto $[21304:22327]$	5	1	_	Covered
bin auto $[22328:23331]$	9	1	_	Covered
bin auto $[23552:24575]$	9 7	1	_	Covered Covered
bin auto $[24576:25599]$ bin auto $[25600:26623]$	7 5	1	_	Covered Covered
bin auto [26624:27647]	4	1	_	Covered
bin auto [27648:28671]	11	1	_	Covered
bin auto [28672:29695]	15	1	_	Covered
bin auto [29696:30719]	2	1	_	Covered
bin auto [30720:31743]	0	1	_	ZERO
bin auto [31744:32767]	3	1	_	Covered
bin auto [32768:33791]	5	1	_	Covered
bin auto [33792:34815]	13	1	_	Covered
bin auto $[34816:35839]$		1	_	Covered
bin auto $[35840:36863]$	22	4	_	Covered
bin auto [36864:37887]	2	1		Covered
	$\frac{2}{3}$	1	_	
bin auto [37888:38911]	$\begin{matrix}2\\3\\14\end{matrix}$			Covered
	$\frac{2}{3}$	1		
bin auto [37888:38911]	$\begin{matrix}2\\3\\14\end{matrix}$	1 1	_	Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959]	$\begin{array}{c} 2 \\ 3 \\ 14 \\ 6 \end{array}$	1 1 1	_ _	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983]	$\begin{array}{c} 2\\ 3\\ 14\\ 6\\ 6\\ 5\\ \end{array}$	1 1 1 1	_ _ _	Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007]	$egin{array}{c} 2 \\ 3 \\ 14 \\ 6 \\ 6 \\ 5 \\ 26 \\ \end{array}$	1 1 1 1 1	_ _ _ _	Covered Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031]	$ \begin{array}{c} 2\\ 3\\ 14\\ 6\\ 6\\ 5\\ 26\\ 4 \end{array} $	1 1 1 1 1 1	- - - - -	Covered Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055]	2 3 14 6 6 5 26 4 13	1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079]	2 3 14 6 6 5 26 4 13 2	1 1 1 1 1 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103]	2 3 14 6 6 5 26 4 13 2 3	1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103] bin auto [47104:48127]	2 3 14 6 6 5 26 4 13 2 3 4	1 1 1 1 1 1 1 1 1	 	Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103] bin auto [47104:48127] bin auto [48128:49151]	2 3 14 6 6 5 26 4 13 2 3 4 8	1 1 1 1 1 1 1 1 1 1	 	Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103] bin auto [47104:48127] bin auto [48128:49151] bin auto [49152:50175]	2 3 14 6 6 5 26 4 13 2 3 4 8 23	1 1 1 1 1 1 1 1 1 1 1	 	Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103] bin auto [47104:48127] bin auto [48128:49151] bin auto [49152:50175] bin auto [50176:51199]	2 3 14 6 6 5 26 4 13 2 3 4 8 23 13	1 1 1 1 1 1 1 1 1 1 1 1	 	Covered
bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [41984:43007] bin auto [43008:44031] bin auto [44032:45055] bin auto [45056:46079] bin auto [46080:47103] bin auto [47104:48127] bin auto [48128:49151] bin auto [49152:50175]	2 3 14 6 6 5 26 4 13 2 3 4 8 23	1 1 1 1 1 1 1 1 1 1 1	 	Covered

bin auto $[52224:53247]$	3	1	_	Covered
bin auto [53248:54271]	3	1	_	Covered
bin auto [54272:55295]	18	1	_	Covered
bin auto $[55296:56319]$	2	1	_	Covered
bin auto [56320:57343]	7	1	_	Covered
bin auto [57344:58367]	3	1	_	Covered
bin auto [58368:59391]	4	1	_	Covered
bin auto [59392:60415]	1	1	_	Covered
bin auto [60416:61439]	11	1	_	Covered
bin auto [61440:62463]	2	1	_	Covered
bin auto [62464:63487]	3	1	_	Covered
bin auto [63488:64511]	12	1	_	Covered
bin auto [64512:65535]	8	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	433	1	_	Covered
bin auto[1]	575	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	959	1	_	Covered
bin auto[1]	49	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	949	1	_	Covered
bin auto[1]	59	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{1}{2}$	_	00.0100
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	780	1	_	Covered
bin auto[1]	228	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$	_	covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	953	1	_	Covered
bin auto[1]	55	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{100.0070}{2}$	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$		
% Hit:	100.00%	100		
bin auto $[0]$	777	1		Covered
bin auto $[0]$	231	1		Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$		Covered
missing/total bins:	0	$\frac{2}{2}$		
% Hit:	100.00%	100		
bin auto[0]	950	1		Covered
bin auto[0]	58	1		Covered
Cross wr_ack_cross	100.00%	100		Covered
covered/total bins:	6	6		Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100		
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto[1], auto[1]=""></auto[1],>	168	1	_	Covered
	$\frac{100}{32}$		_	Covered
$egin{aligned} ext{bin } <& ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] > \ & ext{bin } <& ext{auto} [0] \ , ext{auto} [1] \ , ext{auto} [1] > \end{aligned}$	$\frac{32}{407}$	1 1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	104	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	95	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	202	1	_	Covered
Illegal and Ignore Bins:	202	1		Sovereu
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Sovereu
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	200		
bin $<$ auto [0], auto [1], auto [1]>	48	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	11	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1] \rangle$	200	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	95	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	463	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	191	1	_	Covered
Illegal and Ignore Bins:	101	-		, , , , , , , , , , , , , , , , , , ,
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	55 v 51 6 tr
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	_ 0 0 . 0 0 / 0			
bin <auto[1], auto[1]=""></auto[1],>	23	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	53	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	177	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	435	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	42	1	_	Covered

bin < auto[0], auto[0], auto[0] >	126	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]>$	24	1	_	Covered
$\mathrm{bin} < \mathrm{auto}\left[0 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight]>$	22	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	1	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	8	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right] >$	176	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	489	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	94	1	_	Covered
bin < auto[0], auto[0], auto[0] >	194	1	_	Covered
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	0.0	4		C 1
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	82	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	103	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	6	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	40	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	$\begin{array}{c} 118 \\ 408 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	89	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} [1], ext{auto} [0], ext{auto} [0] > \ ext{bin} & < ext{auto} [0], ext{auto} [0] > \end{aligned}$	162	1	_	Covered
Cross overflow_cross	100.00%	100		Covered
covered/total bins:	6	6		Covered
missing/total bins:	0	6		
% Hit:	100.00%	100		
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	15	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	185	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	34	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	477	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	95	1	_	Covered
bin < auto[0], auto[0], auto[0] >	202	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] >$	41	1	_	Covered
$\mathrm{bin} < \mathrm{auto}\left[1 ight], \mathrm{auto}\left[0 ight], \mathrm{auto}\left[1 ight] >$	17	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\! >$	159	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]>$	511	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	78	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	202	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 99.91% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.91%

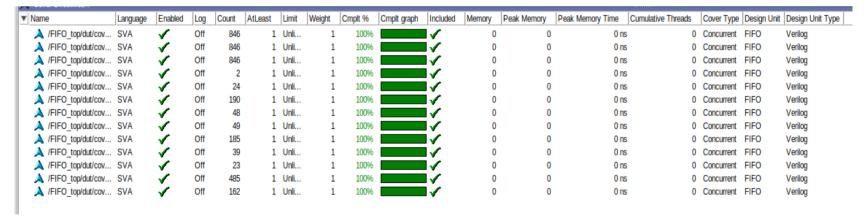


Figure 5: SVA "Seed5"

5 Code Coverage Report

5.1 Code Coverage "seed1" Report

 $\label{eq:coverage_coverage} Coverage \ Report \ by \ DU \ with \ details$

— Design Un	iit: work.FIFO					
Assertion Cov Assertions	9	13	13	0	100.00%	
Name	File (Line)			Failure Count	Pass Count	

```
work.FIFO::assert__counter_threshold
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
work.FIFO::assert_read_ptr_threshold
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
work.FIFO::assert_write_ptr_threshold
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
work.FIFO::assert__read_ptr_wraparound
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
work.FIFO::assert_write_ptr_wraparound
                      /home/tare/Desktop/syn-fifo/sv-verification/FIFO_v1.0.0.sv(151)
work.FIFO::assert_almost_empty_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
work.FIFO::assert__almost_full_check
                      /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(149)
work.FIFO::assert__full_flag_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO::assert_empty_flag_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_-overflow_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO:: assert\_\_reset\_behavior
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Branch Coverage:
    Enabled Coverage
                                   Bins
                                              Hits
                                                      Misses
                                                              Coverage
    Branches
                                     25
                                                25
                                                           0
                                                               100.00\%
                                =Branch Details=
Branch Coverage for Design Unit work.FIFO
NOTE: The modification timestamp for source file '/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv' has been altered since con
    Line
                 Item
                                             Count
                                                       Source
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
    13
                                              1135
                                                       Count coming in to IF
    13
                    1
                                               289
                                                          if (!fifo_intf.rst_n) begin
                                               559
    18
                    1
                                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
                                                          else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                     -IF Branch-
    25
                                               287
                                                       Count coming in to IF
                                                                  if (fifo_intf.full & fifo_intf.wr_en)
    25
                    1
                                               ^{26}
Branch totals: 2 hits of 2 branches = 100.00%
                                     -IF Branch-
    33
                                              1135
                                                       Count coming in to IF
    33
                    1
                                               289
                                                          if (!fifo_intf.rst_n) begin
                                                          else if (fifo_intf.rd_en && count != 0) begin
    38
                    1
                                               213
                                               633
Branch totals: 3 hits of 3 branches = 100.00\%
                                     \operatorname{-IF} Branch-
    43
                                               633
                                                       Count coming in to IF
                                                                  if (fifo_intf.empty & fifo_intf.rd_en)
                    1
    43
                                               65
    45
                    1
                                               568
Branch totals: 2 hits of 2 branches = 100.00\%
                                   ----IF Branch---
    51
                                              1045
                                                       Count coming in to IF
    51
                    1
                                              279
                                                          if (!fifo_intf.rst_n) begin
                    1
                                               766
    54
                                                          else begin
Branch totals: 2 hits of 2 branches = 100.00%
                                   —IF Branch—
    55
                                               766
                                                       Count coming in to IF
                    1
                                               371
                                                                           ((\{fifo_intf.wr_en, fifo_intf.rd_en\} = 2'b10) \&\& !fifo_intf.fu
    55
                                                                  i f
                    1
                                               66
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    57
                                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                    1
                                                4
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                                                45
                                               280
                                                       All False Count
```

—IF Branch-

```
856
                                                                                                 Count coming in to IF
                                                                                                 assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
       66
                                    1
                                                                                  255
                                                                                                 assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                                                                                  601
                                    2
Branch totals: 2 hits of 2 branches = 100.00\%
                                                              —IF Branch-
                                                                                  856
                                                                                                 Count coming in to IF
       67
                                                                                  386
                                    1
                                                                                                 assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
       67
                                    2
                                                                                  470
                                                                                                 assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
       67
Branch totals: 2 hits of 2 branches = 100.00\%
                                                              ——IF Branch-
                                                                                                 Count coming in to IF
                                                                                  856
       68
                                    1
                                                                                  261
                                                                                                 assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
       68
                                                                                                 assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                                    2
                                                                                  595
Branch totals: 2 hits of 2 branches = 100.00\%
                                                                -{
m IF} Branch-
       69
                                                                                                 Count coming in to IF
                                                                                  856
                                                                                  389
       69
                                    1
                                                                                                 assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                                    2
                                                                                  467
                                                                                                 assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
       Enabled Coverage
                                                                                               Misses Coverage
                                                              _{\mathrm{Bins}}
                                                                           Covered
        Conditions
                                                                 28
                                                                                                        2
                                                                                                                 92.85\%
                                                                                    ^{26}
                                                          Condition Details=
Condition Coverage for Design Unit work.FIFO —
NOTE: \ The \ modification \ timestamp \ for \ source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of the source \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ constraints of \ file \ '/home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ file \ '/home/tare/Desktop/syn\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ file \ '/home/tare/Desktop/syn\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ file \ '/home/tare/Desktop/syn\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ file \ '/home/tare/Desktop/syn\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ since \ file \ '/home/tare/Desktop/syn\_verification/FIFO\_v1.0.0.sv' \ has \ been \ altered \ has \ file \ has \ f
    File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                           -{
m Focused} Condition View-
                    18 Item
                                    1 (fifo_intf.wr_en && (count < 8))
Line
Condition totals: 2 of 2 input terms covered = 100.00%
                                    Covered Reason for no coverage
             Input Term
                                                                                                  _{
m Hint}
    fifo_intf.wr_en
                                               Y
           (count < 8)
                                               Y
         Rows:
                               Hits FEC Target
                                                                                  Non-masking condition(s)
                                         fifo_intf.wr_en_0
   Row
               1:
   Row
                                    1
                                          fifo_intf.wr_en_1
                                                                                  (count < 8)
                                          (count < 8)_{-0}
                                                                                  fifo_intf.wr_en
   Row
               3:
                                    1
                                          (count < 8)_{-1}
                                                                                  fifo_intf.wr_en
   Row
              4:
                                    1
                             -Focused Condition View-
                    25 Item
                                    1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
             Input Term
                                    Covered Reason for no coverage
                                                                                                  _{
m Hint}
     fifo_intf.full
                                               Ν
                                                     ^{\prime}_{-0} or not hit
                                                                                                  Hit '_0'
    fifo_intf.wr_en
                                               Y
         Rows:
                               Hits FEC Target
                                                                                  Non-masking condition(s)
                                          fifo_intf.full_0
   Row
                                                                                  fifo_intf.wr_en
   Row
               2:
                                    1
                                          fifo_intf.full_1
                                                                                  fifo_intf.wr_en
   Row
               3:
                                    1
                                          fifo_intf.wr_en_0
                                                                                  fifo_intf.full
                                          fifo_intf.wr_en_1
   Row
               4:
                                    1
                                                                                  fifo_intf.full
                             -Focused Condition View-
                    38 Item 1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00\%
             Input Term
                                    Covered Reason for no coverage
                                                                                                  Hint
    fifo_intf.rd_en
                                               Υ
         (count != 0)
                                               Y
                               Hits FEC Target
                                                                                  Non-masking condition(s)
         Rows:
   Row
               1:
                                          fifo_intf.rd_en_0
               2:
                                          fifo_intf.rd_en_1
                                                                                  (count != 0)
   Row
               3:
                                                                                  fifo_intf.rd_en
   Row
                                          (count != 0)_{-0}
                                    1
                                          (count != 0)_{-1}
   Row
               4:
                                    1
                                                                                  fifo_intf.rd_en
                             -Focused Condition View-
Line
                                       1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
                                   Covered Reason for no coverage
             Input Term
                                                                                                  Hint
```

'_0' not hit Hit '_0' fifo_intf.empty fifo_intf.rd_en Rows: $_{
m Hits}$ FEC Target Non-masking condition(s) Row 1: ***0*** fifo_intf.empty_0 fifo_intf.rd_en 2: fifo_intf.empty_1 Row 1 fifo_intf.rd_en fifo_intf.rd_en_0 Row 3: 1 fifo_intf.empty fifo_intf.rd_en_1 Row 4:1 fifo_intf.empty -Focused Condition View-1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full) 55 Item Line Condition totals: 3 of 3 input terms covered = 100.00%Input Term Covered Reason for no coverage Hint Y fifo_intf.rd_en fifo_intf.wr_en Y Y fifo_intf.full Rows:Non-masking condition(s) $_{
m Hits}$ FEC Target 1 $fifo_intf.rd_{en_0}$ (~fifo_intf.full && fifo_intf.wr_en) Row 1: Row 2: fifo_intf.rd_en_1 1 \tilde{f} if o_intf.rd_en Row 3: fifo_intf.wr_en_0 -1 (~fifo_intf.full && ~fifo_intf.rd_en) Row $fifo_intf.wr_en_1$ 4:1 fifo_intf.full_0 (~fifo_intf.rd_en && fifo_intf.wr_en) Row 5: 1 fifo_intf.full_1 6: (~fifo_intf.rd_en && fifo_intf.wr_en) Row 1 -Focused Condition View-Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty) Condition totals: 3 of 3 input terms covered = 100.00% Input Term Reason for no coverage Covered Hint fifo_intf.rd_en Y $fifo_intf.wr_en$ Y fifo_intf.empty Y Rows: HitsFEC Target Non-masking condition(s) Row 1: 1 fifo_intf.rd_en_0 Row 2: fifo_intf.rd_en_1 (~fifo_intf.empty && ~fifo_intf.wr_en) Row 3: fifo_intf.wr_en_0 (~fifo_intf.empty && fifo_intf.rd_en) fifo_intf.wr_en_1 fifo_intf.rd_en Row 4: Row 5:fifo_intf.empty_0 (fifo_intf.rd_en && ~fifo_intf.wr_en) (fifo_intf.rd_en && ~fifo_intf.wr_en) Row 6: fifo_intf.empty_1 -Focused Condition View-1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full) Condition totals: 3 of 3 input terms covered = 100.00% Covered Reason for no coverage Input Term Hint fifo_intf.rd_en Y fifo_intf.wr_en Y fifo_intf.full Y Rows: FEC Target Non-masking condition(s) $_{
m Hits}$ Row 1: fifo_intf.rd_en_0 2: fifo_intf.rd_en_1 (fifo_intf.full && fifo_intf.wr_en) Row 3: fifo_intf.wr_en_0 fifo_intf.rd_en Row 4: fifo_intf.wr_en_1 (fifo_intf.full && fifo_intf.rd_en) Row Row 5: fifo_intf.full_0 (fifo_intf.rd_en && fifo_intf.wr_en) fifo_intf.full_1 Row 6: (fifo_intf.rd_en && fifo_intf.wr_en) $\operatorname{Focused}$ Condition View-Line 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty) Condition totals: 3 of 3 input terms covered = 100.00% Input Term Covered Reason for no coverage fifo_intf.rd_en Y fifo_intf.wr_en Υ Y fifo_intf.empty Hits FEC Target Non-masking condition(s) Rows: 1 fifo_intf.rd_en_0 Row 1: 2:fifo_intf.rd_en_1 (fifo_intf.empty && fifo_intf.wr_en) Row 1 Row 3: 1 $fifo_intf.wr_en_0$ fifo_intf.rd_en 4: $fifo_intf.wr_en_1$ (fifo_intf.empty && fifo_intf.rd_en) Row 1 (fifo_intf.rd_en && fifo_intf.wr_en) 5:fifo_intf.empty_0 Row 1 (fifo_intf.rd_en && fifo_intf.wr_en) 6: Row 1 fifo_intf.empty_1 -Focused Condition View-1 ((count == 8) || ~fifo_intf.rst_n) Line 66 Item Condition totals: 2 of 2 input terms covered = 100.00% Input Term Covered Reason for no coverage Hint

```
Y
      (count = 8)
                             Y
   fifo_intf.rst_n
                   Hits FEC Target
                                                  Non-masking condition(s)
     Rows:
                          (count = 8)_{-0}
  Row
         1:
                      1
                                                  fifo_intf.rst_n
  Row
         2:
                          (count = 8)_{-1}
                          fifo_intf.rst_n_0
                                                   \tilde{} (count == 8)
  Row
         3:
                          fifo_intf.rst_n_1
                                                   \sim (count == 8)
  Row
         4:
                 -Focused Condition View-
            67 Item
                      1 \quad ((count == 0) \mid | \quad \tilde{fifo}_i ntf.rst_n)
Line
Condition totals: 2 of 2 input terms covered = 100.00%
        Input Term
                      Covered Reason for no coverage
                                                            Hint
                             Y
      (count = 0)
  fifo_intf.rst_n
                             Y
     Rows:
                   Hits FEC Target
                                                  Non-masking condition(s)
                          (count = 0)_{-}0
                                                  fifo_intf.rst_n
  Row
         1:
                      1
                          (count = 0)_{-1}
  Row
         2:
  Row
         3:
                          fifo_intf.rst_n_0
                                                  \tilde{} (count == 0)
  Row
         4:
                          fifo_intf.rst_n_1
                                                   \tilde{} (count == 0)
                 -Focused Condition View-
            68 Item
                      1 \quad ((count = (8 - 1)) \mid | \quad \tilde{fifo}_{intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
           Input Term
                          Covered Reason for no coverage
                                                                Hint
  (count = (8 - 1))
                                Y
      fifo_intf.rst_n
                                Y
     Rows:
                   Hits
                         FEC Target
                                                  Non-masking condition(s)
                                                  fifo_intf.rst_n
                          (count = (8 - 1))_{-0}
  Row
         1:
                      1
                          (count = (8 - 1))_{-1}
  Row
         2:
                          fifo_intf.rst_n_0
                                                  (count = (8 - 1))
  Row
         3:
  Row
         4:
                          fifo_intf.rst_n_1
                                                  \tilde{\ } (count == (8 - 1))
                  -Focused Condition View-
                      1 ((count == 1) \mid | \tilde{fifo_intf.rst_n})
            69 Item
Condition totals: 2 of 2 input terms covered = 100.00%
        Input Term
                      Covered Reason for no coverage
                                                            Hint
                             \mathbf{Y}
      (count = 1)
  fifo_intf.rst_n
                             Y
     Rows:
                   Hits FEC Target
                                                  Non-masking condition(s)
  Row
         1:
                      1
                          (count = 1)_{-0}
                                                  fifo_intf.rst_n
  Row
                          (count = 1)_{-1}
                                                  \tilde{} (count == 1)
  Row
         3:
                          fifo_intf.rst_n_0
  Row
         4:
                          fifo_intf.rst_n_1
                                                   \tilde{} (count == 1)
Directive Coverage:
     Directives
                                        13
                                                   13
                                                                    100.00\%
DIRECTIVE COVERAGE:
```

Name	Design Unit	Design UnitType		File (Line) Hits Status
work.FIFO::cover_counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 847 Covered
work.FIFO::cover_read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 847 Covered
work.FIFO::cover_write_ptr_threshold	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)\\847\ Covered$
$work.FIFO:: cover__read_ptr_wrap around$	FIFO	Verilog	SVA	$/\text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} \\ \text{2 Covered}$
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	$/ home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)\\ 19~Covered$
$work.FIFO::cover_almost_empty_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164) 187 Covered
work.FIFO::coveralmost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 23 Covered
work.FIFO::coverfull_flag_check	FIFO	Verilog	SVA	$/ \text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} \\ 100 \\ 200 \\$
$work.FIFO::cover_empty_flag_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 194 Covered
work.FIFO::cover_underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 58 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 20 Covered
work.FIFO::cover_write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 473 Covered

Enabled Coverage	$_{ m Bins}$	Hits	Misses	Coverage
Statements	28	28	0	100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

NOTE: The modification timestamp for source file '/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv' has been altered since con

Line	${\bf Item}$	Count	Source
	me/tare/Desktop/s	yn_fifo/sv_verification	
$\frac{1}{2}$			module FIFO(FIFO_IF.DUT fifo_intf); parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4 5			$localparam max_fifo_addr = $clog2(FIFO_DEPTH);$
6 7 8			$\label{eq:reg_fif} \text{reg} \hspace{0.2cm} \text{[FIFO-WIDTH-1:0]} \hspace{0.2cm} \text{mem} \hspace{0.2cm} \text{[FIFO-DEPTH-1:0]}; \hspace{0.2cm} // \hspace{0.2cm} 1 -\hspace{-0.2cm} \text{D} \hspace{0.2cm} \text{Array}$
8 9			$\operatorname{reg} \ [\operatorname{max_fifo_addr} -1{:}0] \ \operatorname{wr_ptr}, \ \operatorname{rd_ptr};$
10			reg [max_fifo_addr:0] count;
$\frac{11}{12}$	1	1135	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13	1	200	if (!fifo_intf.rst_n) begin
$14 \\ 15$	1	$\frac{289}{289}$	$wr_ptr \le 0;$ $fifo_intf.wr_ack \le 0;$
16	1	289	fifo_intf.overflow <= 0;
$\frac{17}{18}$			end else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	559	mem[wr_ptr] <= fifo_intf.data_in;
20	1	559	$fifo_intf.wr_ack <= 1;$
$\frac{21}{22}$	1	559	$wr_ptr \le wr_ptr + 1;$
23			else begin
$\frac{24}{25}$	1	287	<pre>fifo_intf.wr_ack <= 0; if (fifo_intf.full & fifo_intf.wr_en)</pre>
$\frac{25}{26}$	1	26	$fifo_intf.verflow <= 1;$
27	1	261	else
$\frac{28}{29}$	1	261	<pre>fifo_intf.overflow <= 0; end</pre>
30			end
$\frac{31}{32}$	1	1135	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33	1	1100	if (!fifo_intf.rst_n) begin
$\frac{34}{25}$	1	289	$rd_ptr \le 0;$
$\frac{35}{36}$	1 1	$\frac{289}{289}$	<pre>fifo_intf.underflow <= 0; fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};</pre>
37			end
$\frac{38}{39}$	1	213	else if (fifo_intf.rd_en && count != 0) begin fifo_intf.data_out <= mem[rd_ptr];
40	1	213	$rd_ptr \ll rd_ptr + 1;$
$\frac{41}{42}$			end else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	65	fifo_intf.underflow <= 1;
45 46	1	568	else fifo_intf.underflow <= 0;
47			end
$48 \\ 49$			end
50	1	1045	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51 52	1	070	if (!fifo_intf.rst_n) begin
$\frac{52}{53}$	1	279	$\operatorname{count} <= 0;$ end
54			else begin
55	1	371	if ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu count <= count + 1;
57	1		else if (({fifo_intf.wr_en, fifo_intf.rd_en} $\Longrightarrow 2$ 'b01) && !fifo_intf.em
58 50	1	66	$count \le count - 1;$
$\frac{59}{60}$	1	4	else if ($\{fifo_intf.wr_en, fifo_intf.rd_en\} == 2'b11$) && fifo_intf.ful count <= count - 1;
61			else if (({fifo_intf.wr_en, fifo_intf.rd_en} $= 2$ 'bll) && fifo_intf.emp
62 63	1	45	$\operatorname{count} <= \operatorname{count} + 1;$
64			end
$\frac{65}{66}$	1	857	assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67	1	857 857	assign fifo_intf.empty = $(count = 0 \mid !fifo_intf.rst_n)? 1 : 0;$
68 60	1	857 857	assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69	1	857	assign fifo_intf.almostempty = $(count == 1)$? 1 : 0;
oggle Cov Enable	verage: d Coverage	Bins Hits	Misses Coverage
Toggle	S	20 20	0 - 100.00%

Toggle Details———

	Node	1H->0L	0L->1H	"Coverage"
count[[0-3]	1	1	100.00
rd_ptr[[0-2]	1	1	100.00
wr_ptr	0-2	1	1	100.00

Toggle~Coverage~=~100.00%~(20~of~20~bins)

DIRECTIVE COVERAGE:

Name	Design Unit	$\begin{array}{c} \text{Design} \\ \text{UnitType} \end{array}$	0	File (Line) Hits Status
$work.FIFO:: cover_counter_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 847 Covered
work . FIFO:: $\operatorname{cover_read_ptr_threshold}$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 847 Covered
$work.FIFO::cover_write_ptr_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167) 847 Covered
$work.FIFO:: cover__read_ptr_wrap around$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166) 2 Covered
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165) 19 Covered
$work.FIFO::cover_almost_empty_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164) 187 Covered
$work.FIFO::cover__almost_full_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 23 Covered
work.FIFO::coverfull_flag_check	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)\\ 32~Covered$
$work.FIFO::cover_empty_flag_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 194 Covered
$work.FIFO::cover_underflow_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 58 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 20 Covered
$work.FIFO::cover_write_ack_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 473 Covered
$work.FIFO::cover_reset_behavior$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157) 161 Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	${ m File}({ m Line})$	Failure Count	$\begin{array}{c} {\rm Pass} \\ {\rm Count} \end{array}$	
work.FIFO:: ass	sert_counter_threshold			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$ an / ext{FIFO}_{ ext{-}} ext{v1.0.0.sv}$	(15)
work . FIFO : : ass	sert_read_ptr_threshold /home/tare/Desktop/s	yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(15
work . FIFO : : ass	sertwrite_ptr_threshold	Ü	1	
., 01111110111011	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(15
work.FIFO::ass	sert_read_ptr_wraparound		-	
	/home/tare/Desktop/s	yn_fifo/sv_verifica	$tion/FIFO_v1.0.0.sv$	(15)
work . FIFO : : ass	sert_write_ptr_wraparound	O	1	
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(15
work.FIFO::ass	sert_almost_empty_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(15)
work.FIFO:: ass	$sert_almost_full_check$			
	/home/tare/Desktop/s	yn_fifo/sv_verifica 0	$ an / FIFO_v1.0.0.sv$	(14
work.FIFO:: as:	sertfull_flag_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$ an / FIFO_v1.0.0.sv$	(14)
work.FIFO::ass	sert_empty_flag_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$ an / ext{FIFO_v1.0.0.sv}$	(14)
work.FIFO:: ass	sert_underflow_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica	,	(14
work FIFO	sertoverflow_check	U	1	
work.riro ass	/home/tare/Desktop/s	yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(14
work FIFO	ant write oak shock	0	1	
work.fifU:: ass	sert_write_ack_check /home/tare/Desktop/s	yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(14
work FIFO · · ass	sert_reset_behavior	U	1	
work.rr ask	/home/tare/Desktop/s	vn fifo/sy verifica	tion/FIFO v1 0 0 gv	(14

1

0

5.2 Code Coverage "seed2" Report

Coverage Report by DU with details

```
= Design Unit: work.FIFO
Assertion Coverage:
    Assertions
                                                              100.00\%
                                    13
                                               13
Name
                     File (Line)
                                                   Failure
                                                                Pass
                                                   Count
                                                                Count
work.FIFO::assert_counter_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
work.FIFO::assert_read_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
work.FIFO::assert_write_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
work.FIFO::assert_read_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
work.FIFO::assert_write_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
work.FIFO::assert_almost_empty_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
work.FIFO:: assert\_almost\_full\_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
work.FIFO::assert__full_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO:: assert\_\_empty\_flag\_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(143)
Branch Coverage:
    Enabled Coverage
                                                     Misses
                                  Bins
                                             Hits
                                                             Coverage
    Branches
                                    25
                                               25
                                                          0
                                                              100.00\%
                               =Branch Details=
```

Branch Coverage for Design Unit work.FIFO

Line	${\rm Item}$	Count	Source
File /ho	ome/tare/Desktop/syr	n_fifo/sv_verification,	$/\text{FIFO}_{\text{-v}1.0.0.sv}$
1.0		IF Branch	
13		1140	Count coming in to IF
13	1	288	if (!fifo_intf.rst_n) begin
18	1	562	else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
23	1	290	else begin
Branch to	tals: 3 hits of 3 br	canches = 100.00%	
		IF Branch	
25		290	Count coming in to IF
25	1	47	if (fifo_intf.full & fifo_intf.wr_en)
27	1	243	else
Branch to	tals: 2 hits of 2 br	ranches = 100.00%	
		IF Branch	
33		1140	Count coming in to IF
33	1	288	if (!fifo_intf.rst_n) begin
38	1	$\frac{170}{170}$	else if (fifo_intf.rd_en && count != 0) begin
42	1	682	else begin
	tals: 3 hits of 3 br		0100 00811
		IF Branch	
43		682	Count coming in to IF
43	1	53	if (fifo_intf.empty & fifo_intf.rd_en)

```
Branch totals: 2 hits of 2 branches = 100.00\%
                                     -{
m IF} -{
m Branch}
                                                        Count coming in to IF
   51
                                              1057
                                                           if (!fifo_intf.rst_n) begin
                    1
                                               277
   51
                    1
                                               780
                                                           else begin
   54
Branch totals: 2 hits of 2 branches = 100.00%
                                     \operatorname{-IF} Branch-
                                                        Count coming in to IF
                                               780
    55
                                                                          (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10\} \&\& !fifo\_intf.fu
                    1
    55
                                               416
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
    57
                    1
                                                41
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
                                                15
    59
                    1
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                32
    61
                    1
                                                        All False Count
                                               276
Branch totals: 5 hits of 5 branches = 100.00\%
                                    —IF Branch-
    66
                                               627
                                                        Count coming in to IF
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                    1
                                                30
    66
                    2
                                               597
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                   —IF Branch—
                                               891
                                                        Count coming in to IF
    67
                    1
                                               395
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
   67
                    2
                                               496
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
                                   ---IF Branch-
                                                        Count coming in to IF
                                               627
    68
                    1
                                                41
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                    2
                                               586
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
                                     -{
m IF}~{
m Branch}-
    69
                                               627
                                                        Count coming in to IF
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                    1
                                               138
                    2
                                               489
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
    Enabled Coverage
                                           Covered
                                                       Misses Coverage
                                    _{\mathrm{Bins}}
    Conditions
                                      25
                                                            2
                                                                 92.00\%
                                                23
                                 =Condition Details=
Condition Coverage for Design Unit work.FIFO —
 File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
Line
           18 Item
                    1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                    Covered Reason for no coverage
                           Y
  fifo_intf.wr_en
      (count < 8)
                           Y
                 Hits FEC Target
     Rows:
                                               Non-masking condition(s)
 Row
                        fifo_intf.wr_en_0
 Row
        2:
                        fifo_intf.wr_en_1
                                               (count < 8)
 Row
        3:
                        (count < 8)_{-0}
                                               fifo_intf.wr_en
                                               fifo_intf.wr_en
 Row
        4:
                        (count < 8)_{-1}
                -Focused Condition View---
           25 Item 1 (fifo_intf.full & fifo_intf.wr_en)
Line
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
   fifo_intf.full
                                                         Hit '_0'
                              ^{\prime}_{-0} or not hit
                           Ν
  fifo_intf.wr_en
                 Hits FEC Target
     Rows:
                                               Non-masking condition(s)
                        fifo_intf.full_0
               ***0***
                                               fifo_intf.wr_en
 Row
        1:
 Row
        2:
                        fifo_intf.full_1
                                               fifo_intf.wr_en
        3:
                        fifo_intf.wr_en_0
                                               fifo_intf.full
 Row
                     1
                        fifo_intf.wr_en_1
                                               fifo_intf.full
 Row
        4:
                     1
                -Focused Condition View-
                     1 (fifo_intf.rd_en && (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00%
                    Covered Reason for no coverage
       Input Term
                                                         Hint
  fifo_intf.rd_en
                           Y
```

629

else

45

1

```
Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                     1
                        fifo_intf.rd_en_0
  Row
        2:
                     1
                        fifo_intf.rd_en_1
                                                (count != 0)
        3:
                        (count != 0)_{-0}
                                                fifo_intf.rd_en
  Row
                     1
                        (count != 0)_{-1}
  Row
        4:
                     1
                                                fifo_intf.rd_en
                -Focused Condition View-
           43 Item
Line
                      1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered
                              Reason for no coverage
                                                         Hint
                                                         Hit '_0'
  fifo_intf.empty
                           Ν
                               '_0 not hit
                           Y
  fifo_intf.rd_en
                        FEC Target
     Rows:
                  _{
m Hits}
                                                Non-masking condition(s)
        1:
               ***0***
                        fifo_intf.empty_0
                                                fifo_intf.rd_en
  Row
                                                fifo_intf.rd_en
        2:
                        fifo_intf.empty_1
  Row
                     1
        3:
                        fifo_intf.rd_{en_0}
                                                fifo_intf.empty
  Row
                     1
                        fifo_intf.rd_en_1
  Row
        4:
                     1
                                                fifo_intf.empty
                -Focused Condition View-
           55 Item
Line
                      1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                              Reason for no coverage
                                                         Hint
                     Covered
  fifo_intf.rd_en
                           Y
                           Y
  fifo_intf.wr_en
                           Y
   fifo_intf.full
     Rows:
                        FEC Target
                                                Non-masking condition(s)
                  Hits
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                                                (~fifo_intf.full && fifo_intf.wr_en)
                        fifo_intf.rd_{en_1}
  Row
        2:
  Row
        3:
                        fifo_intf.wr_en_0
                                                ~ fifo_intf.rd_en
  Row
        4:
                        fifo_intf.wr_en_1
                                                (~fifo_intf.full && ~fifo_intf.rd_en)
                        fifo_intf.full_0
  Row
        5:
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                        fifo_intf.full_1
                 \hbox{-}Focused \quad Condition \quad View-
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Line
           57 Item
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
  fifo_intf.empty
                           Y
     Rows:
                        FEC Target
                                                Non-masking condition(s)
                  Hits
                        fifo_intf.rd_en_0
  Row
        1:
        2:
                        fifo_intf.rd_en_1
                                                (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
  Row
        3:
                        fifo_intf.wr_en_0
                                                (~fifo_intf.empty && fifo_intf.rd_en)
  Row
        4:
                        fifo_intf.wr_en_1
                                                fifo_intf.rd_en
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                        fifo_intf.empty_0
  Row
        6:
                        fifo_intf.empty_1
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
                 -Focused Condition View-
Line
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered
                              Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
   fifo_intf.full
                           Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition (s)
  Row
        1:
                     1
                        fifo_intf.rd_en_0
  Row
        2:
                     1
                        fifo_intf.rd_en_1
                                                (fifo_intf.full && fifo_intf.wr_en)
        3:
                        fifo_intf.wr_en_0
                                                fifo_intf.rd_en
  Row
                     1
                        fifo_intf.wr_en_1
                                                (fifo_intf.full && fifo_intf.rd_en)
  Row
        4:
        5:
                        fifo_intf.full_0
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
        6:
                        fifo_intf.full_1
  Row
                     1
                 -Focused Condition View-
           61 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.rd_en
                           Y
                           Y
  fifo_intf.wr_en
                           Y
  fifo_intf.empty
```

Y

(count != 0)

```
Row
        1:
                    1
                        fifo_intf.rd_en_0
  Row
        2:
                     1
                        fifo_intf.rd_en_1
                                               (fifo_intf.empty && fifo_intf.wr_en)
                        fifo_intf.wr_en_0
  Row
        3:
                    1
                                               fifo_intf.rd_en
                                               (fifo_intf.empty && fifo_intf.rd_en)
  Row
        4:
                     1
                        fifo_intf.wr_en_1
                                               (fifo_intf.rd_en && fifo_intf.wr_en)
                        fifo_intf.empty_0
  Row
        5:
                     1
                        fifo_intf.empty_1
  Row
                    1
                                               (fifo_intf.rd_en && fifo_intf.wr_en)
                -Focused Condition View-
           66 Item
Line
                     1 \quad (count == 8)
Condition totals: 1 of 1 input term covered = 100.00\%
                  Covered Reason for no coverage
    Input Term
  (count == 8)
                       Y
                  Hits FEC Target
                                               Non-masking condition(s)
     Rows:
        1:
                        (count = 8)_{-0}
 Row
                    1
 Row
        2:
                        (count = 8)_{-1}
                     1
                -Focused Condition View-
           67 Item
                     1 \quad ((count == 0) \mid | \quad \tilde{fifo_intf.rst_n})
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
     (count = 0)
                           Y
  fifo_intf.rst_n
                           Y
                  Hits FEC Target
     Rows:
                                               Non-masking condition(s)
  Row
        1:
                    1
                        (count = 0)_{-}0
                                               fifo_intf.rst_n
  Row
        2:
                        (count = 0)_{-1}
                     1
  Row
        3:
                        fifo_intf.rst_n_0
                                               \tilde{} (count == 0)
                    1
                        fifo_intf.rst_n_1
                                               \tilde{} (count == 0)
  Row
        4:
                    1
                -Focused Condition View—
           68 Item
                     1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
                        Covered Reason for no coverage
  (count = (8 - 1))
                              Y
     Rows:
                  _{
m Hits}
                       FEC Target
                                               Non-masking condition(s)
                        (count = (8 - 1))_{-0}
 Row
        1:
                        (count = (8 - 1))_{-1}
 Row
                -Focused Condition View-
           69 Item
                      1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                        Y
  (count == 1)
     Rows:
                  _{
m Hits}
                      FEC Target
                                               Non-masking condition(s)
  Row
        1:
                    1
                        (count = 1)_{-0}
                        (count = 1)_{-1}
  Row
Directive Coverage:
                                                                100.00\%
    Directives
                                     13
                                                13
DIRECTIVE COVERAGE:
Name
                                           Design Design
                                                           Lang File (Line)
                                                                                  Hits Status
                                           Unit UnitType
                                           FIFO
                                                           SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)
work.FIFO::cover_counter_threshold
                                                  Verilog
                                                                                   853 Covered
work.FIFO::cover_read_ptr_threshold
                                           FIFO
                                                  Verilog
                                                           SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)
                                                                                   853 Covered
work.FIFO::cover_write_ptr_threshold
                                           FIFO
                                                  Verilog
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)
                                                                                   853 Covered
                                           FIFO
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
work.FIFO::cover_read_ptr_wraparound
                                                  Verilog
                                                                                     2 Covered
                                           FIFO
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
work.FIFO::cover_write_ptr_wraparound
                                                  Verilog
                                                                                    23 Covered
work.FIFO::cover_almost_empty_check
                                           FIFO
                                                  Verilog
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
                                                                                   159 Covered
                                           FIFO
work.FIFO::cover__almost_full_check
                                                  Verilog
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
                                                                                    67 Covered
work.FIFO::cover_full_flag_check
                                           FIFO
                                                  Verilog
                                                           SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                                    62 Covered
                                           FIFO
work.FIFO::cover_empty_flag_check
                                                           SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                  Verilog
                                                                                   191 Covered
```

Non-masking condition(s)

Hits FEC Target

Rows:

```
SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                 Verilog
work.FIFO::cover_underflow_check
                                          FIFO
                                                                                   44 Covered
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
work.FIFO::cover_overflow_check
                                          FIFO
                                                 Verilog
                                                          SVA
                                                                                   28 Covered
work.FIFO::cover_write_ack_check
                                          FIFO
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                 Verilog
                                                                                  472 Covered
work.FIFO::cover_reset_behavior
                                          FIFO
                                                 Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                                  156 Covered
Statement Coverage:
                                                      Misses
    Enabled Coverage
                                   _{\mathrm{Bins}}
                                             Hits
                                                              Coverage
```

100.00%

0

28

28

Statement Coverage for Design Unit work.FIFO —

Statements

Enabled Coverage

Bins

Hits

```
Line
                  Item
                                               Count
                                                          Source
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                                          module FIFO(FIFO_IF.DUT fifo_intf);
    ^{2}
                                                          parameter FIFO_WIDTH = 16;
    3
                                                          parameter FIFO_DEPTH = 8;
    4
                                                          localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
    6
                                                          reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
    7
    8
    9
                                                              [max_fifo_addr -1:0] wr_ptr, rd_ptr;
                                                          reg [max_fifo_addr:0] count;
    10
    11
                     1
                                                1140
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    12
                                                             if (!fifo_intf.rst_n) begin
    13
                     1
                                                 288
    14
                                                                      wr_ptr \le 0;
                     1
                                                 288
                                                                      fifo_intf.wr_ack \le 0;
    15
                     1
                                                 288
                                                                      fifo_intf.overflow <= 0;
    16
    17
                                                             end
                                                             else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                     1
                                                 562
                                                                      mem[wr_ptr] <= fifo_intf.data_in;
    19
    20
                     1
                                                 562
                                                                      fifo_intf.wr_ack \ll 1;
    21
                     1
                                                 562
                                                                      wr_ptr \le wr_ptr + 1;
    22
                                                             _{\mathrm{end}}
    23
                                                             else begin
    24
                     1
                                                 290
                                                                      fifo_intf.wr_ack \ll 0;
    25
                                                                      if (fifo_intf.full & fifo_intf.wr_en)
    ^{26}
                     1
                                                  47
                                                                               fifo_intf.overflow <= 1;
    27
                                                                      else
    28
                     1
                                                 243
                                                                               fifo_intf.overflow \ll 0;
    ^{29}
                                                             _{\mathrm{end}}
    30
                                                          end
    31
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    32
                     1
                                                1140
                                                             if (!fifo_intf.rst_n) begin
    33
    34
                     1
                                                 288
                                                                      rd_ptr \ll 0;
                                                                      fifo_intf.underflow <= 0;
    35
                     1
                                                 288
    36
                     1
                                                 288
                                                                      fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    37
                                                             \operatorname{end}
                                                             else if (fifo_intf.rd_en && count != 0) begin
    38
    39
                     1
                                                 170
                                                                      fifo_intf.data_out <= mem[rd_ptr];
                     1
                                                 170
                                                                      rd_ptr \ll rd_ptr + 1;
    40
    41
                                                             _{
m end}
                                                             else begin
    42
                                                                      if (fifo_intf.empty & fifo_intf.rd_en)
    43
                     1
                                                                               fifo_intf.underflow \ll 1;
    44
                                                  53
    45
                                                                      else
    46
                     1
                                                 629
                                                                               fifo_intf.underflow \le 0;
    47
                                                             end
    48
                                                          end
    49
                     1
                                                1057
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    51
                                                             if (!fifo_intf.rst_n) begin
    52
                     1
                                                 277
                                                                      count \ll 0;
                                                             end
                                                             else begin
    54
                                                                               ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    55
                                                 416
    56
                     1
                                                                               count \ll count + 1;
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    57
                     1
    58
                                                  41
                                                                               count \ll count - 1;
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                     1
                                                                               count \le count - 1;
    60
                                                  15
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
    62
                     1
                                                  32
                                                                               count \ll count + 1;
    63
                                                             \operatorname{end}
                                                          end
    64
    65
                     1
                                                 628
                                                          assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
    67
                     1
                                                 892
                                                          assign fifo_intf.empty = (count == 0 \mid \mid !fifo_intf.rst_n)? 1 : 0;
                     1
                                                 628
                                                          assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                                                          assign fifo_intf.almostempty = (count = 1)? 1 : 0;
    69
                                                 628
Toggle Coverage:
```

Misses Coverage

Toggles 20 20 0 100.00%

Toggle Details=

Toggle Coverage for Design Unit work.FIFO

Toggle Coverage = 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	$\begin{array}{c} \text{Design} \\ \text{UnitType} \end{array}$	_	File (Line) Hits Status
$work.FIFO:: cover_counter_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 853 Covered
$work.FIFO::cover_read_ptr_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 853 Covered
work.FIFO::coverwrite_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167) 853 Covered
$work.FIFO::cover__read_ptr_wraparound$	FIFO	Verilog	SVA	$/ \text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} \\ \text{2 Covered}$
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	$/\text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} \\ 10.0 - \text{volume} \\ 10.0$
$work.FIFO::cover_almost_empty_check$	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)\\ 159~Covered$
$work.FIFO::cover_almost_full_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 67 Covered
work.FIFO::coverfull_flag_check	FIFO	Verilog	SVA	$/\text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} \\ 62 \text{ Covered}$
work.FIFO::coverempty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 191 Covered
$work.FIFO::cover_underflow_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 44 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 28 Covered
work.FIFO::coverwrite_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 472 Covered
work.FIFO::cover_reset_behavior	FIFO	Verilog	SVA	$/ \text{home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv} (157) \\ 156 \text{ Covered}$

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File (Line)	Failure Count	Pass Count
work.FIFO:: a	ssert_counter_threshold		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{syn}$	a_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(15
work . FIFO : : a	ssert_read_ptr_threshold	O .	1
	/home/tare/Desktop/syr	n_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
	// · ···· · / = · · · · · · · · · · · · ·	0	1
work . FIFO : : a	ssertwrite_ptr_threshold	· ·	_
	/home/tare/Desktop/syr	n_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(15
	, , , , , , , , , , , , , , , , , , , ,	0	1
work . FIFO : : a	ssertread_ptr_wraparound		
	/home/tare/Desktop/syr	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
	, , ,	0	1
work . FIFO : : a	ssert_write_ptr_wraparound		
	/home/tare/Desktop/syr	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(15
	, , , , , , , , , , , , , , , , , , , ,	0	1
work . FIFO : : a	ssertalmost_empty_check		
	/home/tare/Desktop/syr	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(15
		0	1
work.FIFO:: a	$ssert_almost_full_check$		
	/home/tare/Desktop/syr	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(14
		0	1
work.FIFO:: a	ssertfull_flag_check		
	/home/tare/Desktop/syr	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(14
		0	1
$\operatorname{work}.\operatorname{FIFO}::a$	$ssert_empty_flag_check$		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{syr}$	n_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(14
		0	1
work.FIFO:: a	ssertunderflow_check		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{syr}$	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(14
		0	1
$\operatorname{work}.\operatorname{FIFO}::\operatorname{a}$	ssertoverflow_check		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{syr}$	a_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(14
		0	1

```
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Total Coverage By Design Unit (filtered view): 98.66%
     Code Coverage "seed3" Report
5.3
Coverage Report by DU with details
 = Design Unit: work.FIFO
Assertion Coverage:
    Assertions
                                                              100.00\%
                     File (Line)
                                                   Failure
Name
                                                                Pass
                                                   Count
                                                                Count
work.FIFO::assert_counter_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
work.FIFO::assert__read_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
work.FIFO::assert_write_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
work.FIFO::assert_read_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
work.FIFO::assert_write_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
work.FIFO::assert_almost_empty_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
work.FIFO::assert_almost_full_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
work.FIFO::assert__full_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO::assert_empty_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Branch Coverage:
    Enabled Coverage
                                  Bins
                                             Hits
                                                     Misses
                                                             Coverage
    Branches
                                    25
                                               25
                                                          0
                                                              100.00\%
                                =Branch Details=
Branch Coverage for Design Unit work.FIFO
    Line
                 Item
                                            Count
                                                      Source
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                    -IF Branch
   13
                                             1132
                                                      Count coming in to IF
   13
                    1
                                              267
                                                         if (!fifo_intf.rst_n) begin
                                                         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                    1
                                              577
    23
                                              288
                                                         else begin
Branch totals: 3 hits of 3 branches = 100.00%
    25
                                              288
                                                      Count coming in to IF
                    1
    25
                                              42
                                                                 if (fifo_intf.full & fifo_intf.wr_en)
    27
                    1
                                              246
                                                                 else
Branch totals: 2 hits of 2 branches = 100.00\%
    33
                                             1132
                                                      Count coming in to IF
    33
                    1
                                              267
                                                         if (!fifo_intf.rst_n) begin
                                                         else if (fifo_intf.rd_en && count != 0) begin
                                              192
    38
                    1
    42
                                              673
                                                         else begin
```

```
—IF Branch-
                                                673
                                                         Count coming in to IF
                                                                    if (fifo_intf.empty & fifo_intf.rd_en)
    43
                     1
                                                 56
    45
                     1
                                                617
Branch totals: 2 hits of 2 branches = 100.00%
                                    ---IF Branch
                                                         Count coming in to IF
                                               1068
    51
                                                261
                     1
                                                            if (!fifo_intf.rst_n) begin
    51
                     1
                                                807
    54
                                                            else begin
Branch totals: 2 hits of 2 branches = 100.00%
                                    —IF Branch-
                                                         Count coming in to IF
                                                807
                     1
                                                405
                                                                             (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
    55
                                                                     i f
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                                                 52
    57
                     1
                     1
                                                  9
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                                                 41
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                     1
    61
                                                300
                                                         All False Count
Branch totals: 5 hits of 5 branches = 100.00%
                                      \operatorname{-IF} Branch-
    66
                                                626
                                                         Count coming in to IF
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                     1
                                                 ^{26}
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     2
                                                600
    66
Branch totals: 2 hits of 2 branches = 100.00%
                                      \operatorname{-IF} Branch-
    67
                                                874
                                                         Count coming in to IF
                                                         assign \ fifo\_intf.empty = (count == 0 \ || \ !fifo\_intf.rst\_n)? \ 1 \ : \ 0;
    67
                     1
                                                380
                     2
                                                494
                                                         assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} Branch{
m \cdot}
    68
                                                626
                                                         Count coming in to IF
                     1
                                                 34
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     2
                                                592
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} {
m Branch}{
m -}
    69
                                                626
                                                         Count coming in to IF
    69
                     1
                                                143
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                     ^{2}
                                                483
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                            Covered
                                                        Misses
                                                                Coverage
    Conditions
                                      25
                                                             2
                                                                  92.00\%
                                 =Condition Details=
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                -{
m Focused} Condition View-
Line
           18 Item
                     1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
  fifo_intf.wr_en
                           Y
      (count < 8)
                           Y
                  Hits FEC Target
     Rows:
                                                Non-masking condition(s)
                        fifo_intf.wr_en_0
  Row
                        fifo_intf.wr_en_1
                                                (count < 8)
  Row
        3:
                        (count < 8)_{-0}
                                                fifo_intf.wr_en
  Row
                                                 fifo_intf.wr_en
                        (count < 8)_{-1}
                 -Focused Condition View-
Line
                     1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                                                          Hit '_0'
   fifo_intf.full
                               ^{\prime}_{-0} or not hit
                           Ν
                           Y
  fifo_intf.wr_en
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
               ***0***
                        fifo_intf.full_0
 Row
        1:
                                                fifo_intf.wr_en
        2:
 Row
                        fifo_intf.full_1
                                                fifo_intf.wr_en
  Row
        3:
                        fifo_intf.wr_en_0
                                                fifo_intf.full
                     1
                        fifo_intf.wr_en_1
 Row
        4:
                     1
                                                fifo_intf.full
                -Focused Condition View-
                      1 (fifo_intf.rd_en && (count != 0))
Line
```

```
Input Term
                     Covered Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
     (count != 0)
     Rows:
                  _{
m Hits}
                        FEC Target
                                               Non-masking condition(s)
  Row
                        fifo_intf.rd_en_0
        1:
                     1
        2:
                        fifo_intf.rd_en_1
                                               (count != 0)
  Row
        3:
                        (count != 0)_{-0}
                                                fifo_intf.rd_en
  Row
                     1
                        (count != 0)_{-1}
  Row
        4:
                                                fifo_intf.rd_en
                -Focused Condition View-
           43 Item
                      1 (fifo_intf.empty & fifo_intf.rd_en)
Line
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
                                                         Hit '_0'
  fifo_intf.empty
                           Ν
                              ^{\prime}_{-0} or not hit
  fifo_intf.rd_en
                           Y
                  Hits
     Rows:
                        FEC Target
                                               Non-masking condition(s)
               ***0***
                        fifo_intf.empty_0
                                                fifo_intf.rd_en
  Row
        1:
                        fifo_intf.empty_1
                                               fifo_intf.rd_en
  Row
        2:
                     1
                                               fifo_intf.empty
                        fifo_intf.rd_en_0
  Row
        3:
                    1
                        fifo_intf.rd_en_1
  Row
        4:
                    1
                                               fifo_intf.empty
                -Focused Condition View-
           55 Item
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
   fifo_intf.full
     Rows:
                  Hits
                        FEC Target
                                               Non-masking condition(s)
  Row
        1:
                    1
                        fifo_intf.rd_en_0
                                               (~fifo_intf.full && fifo_intf.wr_en)
  Row
        2:
                        fifo_intf.rd_en_1
                                               ~ fifo_intf.rd_en
  Row
        3:
                        fifo_intf.wr_en_0
                                               (~fifo_intf.full && ~fifo_intf.rd_en)
  Row
        4:
                        fifo_intf.wr_en_1
  Row
        5:
                        fifo_intf.full_0
                                               (~fifo_intf.rd_en && fifo_intf.wr_en)
                        fifo_intf.full_1
  Row
        6:
                                               (~fifo_intf.rd_en && fifo_intf.wr_en)
                 Focused Condition View-
Line
           57 Item
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                              Reason for no coverage
                     Covered
                                                         Hint
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
                           Y
  fifo_intf.empty
     Rows:
                        FEC Target
                                               Non-masking condition(s)
                  _{
m Hits}
  Row
        1:
                        fifo_intf.rd_en_0
        2:
                        fifo_intf.rd_en_1
                                               (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
 Row
                                                (~fifo_intf.empty && fifo_intf.rd_en)
        3:
                        fifo_intf.wr_en_0
        4:
                        fifo_intf.wr_en_1
                                                fifo_intf.rd_en
  Row
                                               (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                        fifo_intf.empty_0
  Row
        6:
                        fifo_intf.empty_1
                                               (fifo_intf.rd_en && ~fifo_intf.wr_en)
                 Focused Condition View-
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Line
           59 Item
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term Covered Reason for no coverage
                           Υ
  fifo_intf.rd_en
  fifo_intf.wr_en
                           Y
                           Y
   fifo_intf.full
                       FEC Target
                                               Non-masking condition(s)
     Rows:
                  _{
m Hits}
                        fifo_intf.rd_en_0
  Row
        1:
                     1
                                               (fifo_intf.full && fifo_intf.wr_en)
  Row
        2:
                     1
                        fifo_intf.rd_en_1
        3:
                        fifo_intf.wr_en_0
                                               fifo_intf.rd_en
  Row
                     1
                        fifo_intf.wr_en_1
                                               (fifo_intf.full && fifo_intf.rd_en)
        4:
  Row
                     1
                        fifo_intf.full_0
                                               (fifo_intf.rd_en && fifo_intf.wr_en)
        5:
                     1
  Row
                        fifo_intf.full_1
        6:
                                               (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                     1
                -Focused Condition View-
                      1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
```

Input Term Covered Reason for no coverage Hint

```
Y
  fifo_intf.wr_en
  fifo_intf.empty
                           Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                        fifo_intf.rd_en_1
                                                (fifo_intf.empty && fifo_intf.wr_en)
  Row
        2:
                                                fifo_intf.rd_en
  Row
        3:
                        fifo_intf.wr_en_0
                     1
                                                (fifo_intf.empty && fifo_intf.rd_en)
                        fifo_intf.wr_en_1
  Row
        4:
                     1
                        fifo_intf.empty_0
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
                     1
  Row
        6:
                     1
                        fifo_intf.empty_1
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
                \operatorname{-Focused} Condition View-
           66 Item
                     1 \quad (count == 8)
Line
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                      Hint
  (count == 8)
                        Y
                  Hits FEC Target
                                               Non-masking condition(s)
     Rows:
  Row
        1:
                     1
                        (count = 8)_{-}0
  Row
        2:
                        (count = 8)_{-1}
                     1
                -Focused Condition View-
           67 Item
                     1 \quad ((count == 0) \mid | \quad \tilde{fifo}_{intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
                     Covered Reason for no coverage
       Input Term
                                                         Hint
     (count = 0)
                           Y
  fifo_intf.rst_n
                           Y
                  _{
m Hits}
                       FEC Target
     Rows:
                                               Non-masking condition(s)
  Row
        1:
                     1
                        (count = 0)_{-}0
                                                fifo_intf.rst_n
  Row
        2:
                        (count = 0)_{-1}
                     1
                                                \tilde{} (count == 0)
  Row
        3:
                        fifo_intf.rst_n_0
                                                \tilde{} (count == 0)
  Row
                        fifo_intf.rst_n_1
                -Focused Condition View-
           68 Item
                     1 (count = (8 - 1))
Line
Condition totals: 1 of 1 input term covered = 100.00%
          Input Term
                        Covered Reason for no coverage
  (count = (8 - 1))
                              Y
                  Hits
                        FEC Target
                                               Non-masking condition(s)
     Rows:
  Row
        1:
                        (count = (8 - 1))_{-0}
  Row
                        (count = (8 - 1))_{-1}
                 -Focused Condition View-
           69 Item
                     1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                      Hint
                        Y
  (count == 1)
     Rows:
                  Hits FEC Target
                                               Non-masking condition(s)
  Row
        1:
                     1
                        (count = 1)_{-0}
  Row
        2:
                        (count = 1)_{-1}
Directive Coverage:
                                                13
                                                          0 100.00\%
    Directives
DIRECTIVE COVERAGE:
Name
                                           Design Design
                                                            Lang File (Line)
                                                                                   Hits Status
                                                   UnitType
                                           Unit
                                                            SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)
work.FIFO::cover_counter_threshold
                                           FIFO
                                                   Verilog
                                                                                    866 Covered
work.FIFO::cover_read_ptr_threshold
                                           FIFO
                                                   Verilog
                                                            SVA
                                                                 /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)
                                                                                    866 Covered
                                           FIFO
                                                   Verilog
                                                                 /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)
work.FIFO::cover_write_ptr_threshold
                                                            SVA
                                                                                    866 Covered
                                           FIFO
                                                   Verilog
                                                                 /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
work.FIFO::cover_read_ptr_wraparound
                                                            SVA
                                                                                      3 Covered
work.FIFO::cover_write_ptr_wraparound
                                           FIFO
                                                   Verilog
                                                            SVA
                                                                 /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
                                                                                     24 Covered
                                                                 /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
                                           FIFO
work.FIFO::cover_almost_empty_check
                                                   Verilog
                                                            SVA
                                                                                    183 Covered
```

Y

fifo_intf.rd_en

work.FIFO::cover__almost_full_check

/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)

FIFO

Verilog

SVA

```
49 Covered
work.FIFO::cover_full_flag_check
                                         FIFO
                                                Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                                72 Covered
work.FIFO::cover_empty_flag_check
                                         FIFO
                                                         SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                Verilog
                                                                               189 Covered
                                                         SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
work.FIFO::cover_underflow_check
                                         FIFO
                                                Verilog
                                                                                49 Covered
                                                             /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
work.FIFO::cover__overflow_check
                                         FIFO
                                                        SVA
                                                Verilog
                                                                                28 Covered
work.FIFO::cover_write_ack_check
                                         FIFO
                                                        SVA
                                                             /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                Verilog
                                                                               484 Covered
work.FIFO::cover_reset_behavior
                                         FIFO
                                                Verilog SVA
                                                             /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                               143 Covered
Statement Coverage:
```

Enabled Coverage Bins Hits Coverage Misses Statements 0 100.00%2828

=Statement Details=

Statement Coverage for Design Unit work.FIFO —

67

```
Line
                Item
                                             Count
                                                        Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                                        module FIFO(FIFO_IF.DUT fifo_intf);
 -1
 2
                                                        parameter FIFO_WIDTH = 16;
                                                        parameter FIFO_DEPTH = 8;
 3
 4
                                                        localparam max_fifo_addr = $clog2(FIFO_DEPTH);
 5
  6
                                                        reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
 7
  8
                                                        reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
 9
  10
                                                        reg [max_fifo_addr:0] count;
  11
                   1
                                              1132
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  12
                                                           if (!fifo_intf.rst_n) begin
  13
                   1
                                               267
                                                                   wr_ptr \ll 0;
  14
  15
                   1
                                               267
                                                                    fifo_intf.wr_ack \ll 0;
  16
                   1
                                               267
                                                                    fifo_intf.overflow <= 0;
  17
                                                           _{\mathrm{end}}
                                                           else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
  18
                                                                   mem[wr_ptr] <= fifo_intf.data_in;
  19
                   1
                                               577
  20
                   1
                                               577
                                                                   fifo_intf.wr_ack \ll 1;
  21
                   1
                                               577
                                                                    wr_ptr \le wr_ptr + 1;
  22
                                                           _{\mathrm{end}}
  23
                                                           else begin
  24
                   1
                                               288
                                                                    fifo_intf.wr_ack \le 0;
                                                                    if (fifo_intf.full & fifo_intf.wr_en)
  25
  ^{26}
                   1
                                                42
                                                                             fifo_intf.overflow <= 1;
  27
                                                                    else
                   1
                                               246
                                                                             fifo_intf.overflow \ll 0;
  28
  29
                                                           end
                                                        end
  30
  31
                                              1132
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  32
                   1
  33
                                                           if (!fifo_intf.rst_n) begin
  34
                   1
                                               267
                                                                   rd_ptr \ll 0;
  35
                   1
                                               267
                                                                    fifo_intf.underflow \ll 0;
                                                                    fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
  36
                   1
                                               267
  37
  38
                                                           else if (fifo_intf.rd_en && count != 0) begin
  39
                   1
                                               192
                                                                    fifo_intf.data_out <= mem[rd_ptr];
  40
                   1
                                               192
                                                                    rd_ptr \ll rd_ptr + 1;
  41
                                                           end
  42
                                                           else begin
  43
                                                                    if (fifo_intf.empty & fifo_intf.rd_en)
                                                                             fifo_intf.underflow <= 1;
  44
                   1
                                                56
                                                                    else
  46
                   1
                                               617
                                                                             fifo_intf.underflow \le 0;
  47
                                                           end
  48
  49
                                              1068
  50
                   1
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  51
                                                           if (!fifo_intf.rst_n) begin
  52
                   1
                                               261
                                                                   count \ll 0;
  53
                                                           \operatorname{end}
  54
                                                           else begin
                                                                            (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
  55
                                                                    i f
                   1
  56
                                               405
                                                                            count \ll count + 1;
  57
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
                   1
  58
                                                52
                                                                            count \ll count - 1;
                                                                    else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
  59
                   1
                                                 9
  60
                                                                            count \le count - 1;
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
  61
  62
                   1
                                                41
                                                                            count \ll count + 1;
  63
                                                           _{\mathrm{end}}
  64
                                                        end
  65
                   1
                                               627
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
  66
                   1
                                                        assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
                                               875
```

68	1	627	assign	fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69	1	627	assign	$fifo_intf.almostempty = (count == 1)? 1 : 0;$

Toggle Coverage:

Enabled Coverage	$_{ m Bins}$	$_{ m Hits}$	Misses	Coverage
Toggles	20	20	0	100.00%

Toggle Details———

 $Toggle\ Coverage\ for\ Design\ Unit\ work.FIFO$

	Node	1H—>0L	0L->1H	"Coverage"
count	[0-3]	1	1	100.00
rd_ptr	[0-2]	1	1	100.00
wr_ptr	[0-2]	1	1	100.00

 $\begin{array}{lll} {\rm Total~Node~Count} & = & 10 \\ {\rm Toggled~Node~Count} & = & 10 \\ {\rm Untoggled~Node~Count} & = & 0 \end{array}$

Toggle Coverage = 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	$\begin{array}{c} \text{Design} \\ \text{UnitType} \end{array}$	_	File (Line) Hits Status
work.FIFO::cover_counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 866 Covered
$work.FIFO::cover_read_ptr_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 866 Covered
work.FIFO::cover_write_ptr_threshold	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)\\866~Covered$
work.FIFO::cover_read_ptr_wraparound	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)\\ 3~Covered$
$work.FIFO::cover_write_ptr_wraparound$	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)\\ 24~Covered$
work.FIFO::cover_almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164) 183 Covered
$work.FIFO::cover_almost_full_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 49 Covered
work.FIFO::coverfull_flag_check	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)\\72~Covered$
$work.FIFO::cover_empty_flag_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 189 Covered
$work.FIFO::cover_underflow_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 49 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 28 Covered
work.FIFO::coverwrite_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 484 Covered
$work.FIFO::cover_reset_behavior$	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)\\ 143~Covered$

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	${ m File}({ m Line})$	Failure Count	$egin{array}{c} { m Pass} \\ { m Count} \end{array}$
work.FIFO:: asse	ert_counter_threshold		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
		0	1
work . FIFO : : asse	ertread_ptr_threshold		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(1
work . FIFO : : asse	ert_write_ptr_threshold		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	vn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(1 1
work . FIFO : : asse	ert_read_ptr_wraparound		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
		0	1
work . FIFO $:: asset$	ert_write_ptr_wraparound		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(1
work . FIFO : : asse	ert_almost_empty_check		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
		0	1
work.FIFO::asse	ertalmost_full_check		
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
		0	1
work.FIFO::ass	ertfull_flag_check		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(1 1
work . FIFO : : asse	ert_empty_flag_check		
	/home/tare/Desktop/sy	vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(1
		0	1
work FIFO · · asse	ert_underflow_check		

```
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Total Coverage By Design Unit (filtered view): 98.66%
5.4 Code Coverage "seed4" Report
Coverage Report by DU with details
 — Design Unit: work.FIFO
Assertion Coverage:
    Assertions
                                     13
                                               13
                                                              100.00\%
                                                                Pass
Name
                     File (Line)
                                                   Failure
                                                   Count
                                                                 Count
work.FIFO::assert_counter_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
work.FIFO::assert_read_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
work.FIFO::assert_write_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
work.FIFO::assert_read_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
work.FIFO:: assert\_\_write\_ptr\_wrap around
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
work.FIFO::assert__almost_empty_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
work.FIFO:: assert\_almost\_full\_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
work.FIFO::assert__full_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO::assert__empty_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO:: assert\_reset\_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Branch Coverage:
    Enabled Coverage
                                                             Coverage
                                   Bins
                                             Hits
                                                     Misses
    Branches
                                     25
                                               25
                                                          0
                                                              100.00\%
                                =Branch Details=
Branch Coverage for Design Unit work.FIFO
    Line
                 Item
                                            Count
                                                      Source
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                  ---IF Branch-
                                                      Count coming in to IF
    13
                                             1135
    13
                    1
                                              286
                                                         if (!fifo_intf.rst_n) begin
    18
                    1
                                              566
                                                         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23
                    1
                                              283
                                                         else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                    -IF Branch
    25
                                                      Count coming in to IF
    25
                    1
                                                                  if (fifo_intf.full & fifo_intf.wr_en)
                                               20
                    1
                                              263
    27
Branch totals: 2 hits of 2 branches = 100.00%
```

/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)

```
-{
m IF} -{
m Branch}
    33
                                                1135
                                                          Count coming in to IF
    33
                     1
                                                 286
                                                             if (!fifo_intf.rst_n) begin
                                                             else if (fifo_intf.rd_en && count != 0) begin
    38
                     1
                                                 193
    42
                     1
                                                 656
                                                             else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                       -IF Branch
    43
                                                 656
                                                          Count coming in to IF
                                                                      if (fifo_intf.empty & fifo_intf.rd_en)
    43
                     1
                                                  61
                     1
                                                 595
    45
Branch totals: 2 hits of 2 branches = 100.00%
                                       -IF Branch
                                                          Count coming in to IF
    51
                                                1071
                     1
    51
                                                 277
                                                             if (!fifo_intf.rst_n) begin
                     1
                                                 794
    54
                                                             else begin
Branch totals: 2 hits of 2 branches = 100.00%
                                       -IF Branch-
    55
                                                 794
                                                          Count coming in to IF
                     1
                                                                              (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10) \&\& !fifo\_intf.fu
    55
                                                 410
                                                                      i f
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                     1
                                                  71
    57
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                     1
                                                   9
    61
                                                  43
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                     1
                                                          All False Count
                                                 261
Branch totals: 5 hits of 5 branches = 100.00\%
                                     \operatorname{---IF} Branch-
    66
                                                 653
                                                          Count coming in to IF
                                                  21
                                                          assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     1
    66
                                                          assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     2
                                                 632
    66
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} {
m Branch}{
m -}
    67
                                                 907
                                                          Count coming in to IF
                     1
                                                 394
                                                          assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                     2
                                                 513
                                                          assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                     -\!\!-\!\!\operatorname{IF} Branch-
    68
                                                 653
                                                          Count coming in to IF
                                                          assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     1
                                                  33
                                                          assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                                                 620
Branch totals: 2 hits of 2 branches = 100.00%
                                     -\!\!-\!\!\operatorname{IF} Branch-
    69
                                                 653
                                                          Count coming in to IF
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                     1
                                                 152
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
                                                                 Coverage
    Enabled Coverage
                                     Bins
                                             Covered
                                                         Misses
    Conditions
                                       25
                                                              ^{2}
                                                                   92.00\%
                                 ---Condition Details---
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                 \operatorname{-Focused} Condition View—
Line
                     1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
                     Covered Reason for no coverage
       Input Term
  fifo_intf.wr_en
                            Y
                            Y
      (count < 8)
                  Hits FEC Target
                                                 Non-masking \ condition \, (\, s \, )
  Row
                         fifo_intf.wr_en_0
        2:
                         fifo_intf.wr_en_1
  Row
                                                 (count < 8)
  Row
        3:
                         (count < 8)_{-0}
                                                 fifo_intf.wr_en
        4:
                         (count < 8)_{-1}
                                                 fifo_intf.wr_en
  Row
                     1
                 -Focused Condition View—
                       1 (fifo_intf.full & fifo_intf.wr_en)
Line
Condition totals: 1 of 2 input terms covered = 50.00%
                     Covered Reason for no coverage
       Input Term
                                                           Hint
                               ^{\prime}_{-0} on not hit
   fifo_intf.full
                                                           Hit '_0'
                            Ν
                            Y
  fifo_intf.wr_en
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
                         fifo_intf.full_0
                                                 fifo_intf.wr_en
               ***0***
```

fifo_intf.wr_en

Row

Row

1: 2:

fifo_intf.full_1

1

```
Row
                        fifo_intf.wr_en_0
                                                fifo_intf.full
                        fifo_intf.wr_en_1
  Row
                                                fifo_intf.full
                -Focused Condition View-
           38 Item
                     1 (fifo_intf.rd_en && (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
       Input Term
                     Covered
                              Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
     (count != 0)
     Rows:
                  Hits
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        fifo_intf.rd_en_0
        2:
                                                (count != 0)
  Row
                        fifo_intf.rd_{en_1}
                        (count != 0)_{-0}
                                                fifo_intf.rd_en
  Row
        3:
                     1
                        (count != 0)_{-1}
                                                fifo_intf.rd_en
  Row
        4:
                     1
                 -Focused Condition View-
Line
           43 Item
                      1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered
                              Reason for no coverage
                                                         Hint
  fifo_intf.empty
                           Ν
                               ^{\prime}_{-0} , not hit
                                                         Hit '_0'
  fifo_intf.rd_en
                           Y
                                                Non-masking \ condition \, (\, s \, )
                  _{
m Hits}
                        FEC Target
     Rows:
               ***0***
                                                fifo_intf.rd_en
  Row
        1:
                        fifo_intf.empty_0
                        fifo_intf.empty_1
  Row
        2:
                                                fifo_intf.rd_en
                     1
                        fifo_intf.rd_en_0
                                                fifo_intf.empty
  Row
        3:
                     1
  Row
        4:
                        fifo_intf.rd_en_1
                                                fifo_intf.empty
                     1
                 Focused Condition View-
           55 Item
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
                              Reason for no coverage
       Input Term
                     Covered
                                                         Hint
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
                           Y
   fifo_intf.full
     Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                                                (~fifo_intf.full && fifo_intf.wr_en)
                        fifo_intf.rd_{en_1}
  Row
        2:
                        fifo_intf.wr_en_0
                                                ~fifo_intf.rd_en
  Row
        3:
  Row
        4:
                        fifo_intf.wr_en_1
                                                (~fifo_intf.full && ~fifo_intf.rd_en)
                        fifo_intf.full_0
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
                        fifo_intf.full_1
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 Focused Condition View-
           57 Item
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                           Y
  fifo_intf.rd_en
  fifo_intf.wr_en
                           \mathbf{Y}
                           Y
  fifo_intf.empty
     Rows:
                  Hits
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                                                (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
        2:
                        fifo_intf.rd_en_1
  Row
        3:
                        fifo_intf.wr_en_0
                                                (~fifo_intf.empty && fifo_intf.rd_en)
                                                fifo_intf.rd_en
  Row
        4:
                        fifo_intf.wr_en_1
                        fifo_intf.empty_0
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
  Row
        6:
                        fifo_intf.empty_1
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
                 -Focused Condition View-
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Line
           59 Item
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         _{
m Hint}
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
   fifo_intf.full
                           Y
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
                        fifo_intf.rd_en_0
  Row
        1:
                     1
                                                (fifo_intf.full && fifo_intf.wr_en)
        2:
  Row
                     1
                        fifo_intf.rd_en_1
  Row
        3:
                     1
                        fifo_intf.wr_en_0
                                                fifo_intf.rd_en
                                                (fifo_intf.full && fifo_intf.rd_en)
  Row
        4:
                     1
                        fifo_intf.wr_en_1
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
                        fifo_intf.full_0
  Row
        5:
                     1
                        fifo_intf.full_1
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
        6:
  Row
```

```
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                            Y
  fifo_intf.rd_en
                            \mathbf{Y}
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                  Hits
                        FEC Target
                                                Non-masking condition(s)
     Rows:
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
                                                 (fifo_intf.empty && fifo_intf.wr_en)
  Row
         2:
                     1
                         fifo_intf.wr_en_0
                                                 fifo_intf.rd_en
  Row
         3:
                                                 (fifo_intf.empty && fifo_intf.rd_en)
                         fifo_intf.wr_en_1
  Row
         4:
                     1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                         fifo_intf.empty_0
        5:
                     1
                         fifo_intf.empty_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                     1
                 -Focused Condition View-
Line
           66 Item
                      1 \quad (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                       _{
m Hint}
  (count == 8)
                        Y
                  _{
m Hits}
                       FEC Target
                                                Non-masking condition(s)
     Rows:
  Row
        1:
                     1
                        (count = 8)_{-}0
  Row
        2:
                         (count = 8)_{-1}
                     1
                 -Focused Condition View-
            67 Item
                     1 \quad ((count = 0) \mid | \quad fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                            Y
     (count = 0)
  fifo_intf.rst_n
                            Y
                       FEC Target
     Rows:
                  _{
m Hits}
                                                Non-masking condition(s)
                        (count = 0)_{-0}
                                                 fifo_intf.rst_n
  Row
        1:
                     1
                         (count = 0)_{-1}
  Row
         2:
                     1
  Row
        3:
                         fifo_intf.rst_n_0
                                                 \tilde{} (count == 0)
  Row
        4:
                     1
                         fifo_intf.rst_n_1
                                                 \tilde{} (count == 0)
                 -Focused Condition View-
           68 Item
                     1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
                        Covered Reason for no coverage
  (count = (8 - 1))
                               Y
                  Hits
                        FEC Target
                                                Non-masking condition(s)
     Rows:
                        (count = (8 - 1))_{-0}
  Row
         1:
  Row
         2:
                        (count = (8 - 1))_{-1}
                 \operatorname{-Focused} Condition View\operatorname{-}
Line
            69 Item
                       1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                        Y
  (count == 1)
     Rows:
                  Hits FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        (count = 1)_{-0}
  Row
                         (count = 1)_{-1}
Directive Coverage:
                                       13
                                                 13
                                                                 100.00\%
    Directives
DIRECTIVE COVERAGE:
                                                             Lang File (Line)
Name
                                            Design Design
                                                                                    Hits Status
                                            Unit
                                                    UnitType
work.FIFO::cover_counter_threshold
                                            FIFO
                                                            SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)
                                                    Verilog
                                                                                     850 Covered
work.FIFO::cover_read_ptr_threshold
                                            FIFO
                                                             SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)
                                                    Verilog
                                                                                     850 Covered
work.FIFO::cover_write_ptr_threshold
                                            FIFO
                                                             SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)
                                                    Verilog
                                                                                     850 Covered
                                            FIFO
                                                    Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
work.FIFO::cover_read_ptr_wraparound
                                                                                        1 Covered
```

-Focused Condition View—

1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)

61 Item

```
work.FIFO::cover_write_ptr_wraparound
                                                         SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
                                         FIFO
                                                 Verilog
                                                                                 21 Covered
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
work.FIFO::cover_almost_empty_check
                                         FIFO
                                                 Verilog
                                                          SVA
                                                                                181 Covered
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
work.FIFO::cover__almost_full_check
                                                          SVA
                                         FIFO
                                                 Verilog
                                                                                 43 Covered
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
work.FIFO::cover__full_flag_check
                                         FIFO
                                                 Verilog
                                                          SVA
                                                                                 29 Covered
work.FIFO::cover_empty_flag_check
                                         FIFO
                                                 Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                                                197 Covered
work.FIFO::cover_underflow_check
                                         FIFO
                                                 Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                                                 55 Covered
                                         FIFO
work.FIFO::cover_overflow_check
                                                 Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
                                                                                   9 Covered
                                         FIFO
                                                 Verilog
work.FIFO::cover_write_ack_check
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                                                484 Covered
work.FIFO::cover_reset_behavior
                                         FIFO
                                                         SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                 Verilog
                                                                                159 Covered
Statement Coverage:
                                                             Coverage
    Enabled Coverage
                                  Bins
                                             Hits
                                                     Misses
                                    28
                                               28
                                                          0
                                                              100.00\%
    Statements
```

=Statement Details=

Statement Coverage for Design Unit work.FIFO —

```
Line
                Item
                                             Count
                                                        Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                                        module FIFO(FIFO_IF.DUT fifo_intf);
                                                        parameter FIFO_WIDTH = 16;
 2
 3
                                                        parameter FIFO_DEPTH = 8;
 4
 5
                                                        localparam max_fifo_addr = $clog2(FIFO_DEPTH);
 6
                                                        reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
 7
 8
                                                            [max_fifo_addr -1:0] wr_ptr, rd_ptr;
 9
 10
                                                        reg [max_fifo_addr:0] count;
  11
  12
                   1
                                              1135
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
                                                            if (!fifo_intf.rst_n) begin
  13
                                                                     wr_ptr \ll 0;
                   1
                                               286
  14
  15
                   1
                                               286
                                                                     fifo_intf.wr_ack \ll 0;
  16
                   1
                                               286
                                                                     fifo_intf.overflow <= 0;
  17
                                                           _{\mathrm{end}}
                                                            else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
  18
  19
                   1
                                               566
                                                                    mem[wr_ptr] <= fifo_intf.data_in;
  20
                   1
                                               566
                                                                     fifo_intf.wr_ack \ll 1;
  21
                                               566
                                                                     wr_ptr \ll wr_ptr + 1;
  22
                                                           \operatorname{end}
  23
                                                            else begin
                                               283
  24
                   1
                                                                     fifo_intf.wr_ack \ll 0;
                                                                     if (fifo_intf.full & fifo_intf.wr_en)
  25
  ^{26}
                   1
                                                 20
                                                                              fifo_intf.overflow <= 1;
  27
                                                                     else
                   1
                                               263
                                                                              fifo_intf.overflow \ll 0;
  28
  29
                                                           _{\mathrm{end}}
                                                        end
  30
  31
                   1
                                              1135
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  32
                                                            if (!fifo_intf.rst_n) begin
  33
                   1
                                               286
  34
                                                                     rd_ptr \le 0;
                                                                     fifo_intf.underflow \le 0;
  35
                   1
                                               286
  36
                   1
                                               286
                                                                     fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
  37
  38
                                                            else if (fifo_intf.rd_en && count != 0) begin
                                                                     fifo_intf.data_out <= mem[rd_ptr];
  39
                   1
                                               193
                   1
                                               193
                                                                     rd_ptr \ll rd_ptr + 1;
  41
                                                           _{\mathrm{end}}
  42
                                                            else begin
                                                                     if (fifo_intf.empty & fifo_intf.rd_en)
  43
                                                61
  44
                   1
                                                                              fifo_intf.underflow \ll 1;
  45
                                                                     else
                   1
                                               595
                                                                              fifo_intf.underflow \ll 0;
  46
  47
                                                           \operatorname{end}
  48
                                                        end
  49
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
                   1
                                              1071
  50
  51
                                                            if (!fifo_intf.rst_n) begin
  52
                   1
                                               277
                                                                     count \ll 0;
 53
                                                           \operatorname{end}
                                                            else begin
 54
                                                                              (\{fifo_intf.wr_en, fifo_intf.rd_en\} = 2'b10\} \&\& !fifo_intf.fu
 55
                                                                     i f
                   1
                                               410
                                                                              count \le count + 1;
 56
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
 57
                   1
                                                71
 58
                                                                              count \le count - 1;
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
 59
                                                 9
                   1
 60
                                                                              count \le count - 1;
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
 61
                   1
                                                43
 62
                                                                              count \le count + 1;
```

```
63
                                                               end
    64
                                                            \quad \text{end} \quad
    65
                                                            assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                      1
                                                   654
                      1
                                                   908
                                                            assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
    67
                                                   654
                                                            assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                      1
                                                   654
                                                            assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                      1
Toggle Coverage:
    Enabled Coverage
                                      _{\rm Bins}
                                                 _{
m Hits}
                                                           Misses
                                                                   Coverage
    Toggles
                                        20
                                                    20
                                                                0
                                                                    100.00\%
```

Toggle Coverage for Design Unit work.FIFO

=Toggle Details=

0L->1H "Coverage" Node 1H->0L $\operatorname{count}\left[0-3\right]$ 100.00 1 1 100.00 $rd_ptr[0-2]$ 1 1 $wr_ptr[0-2]$ 1 1 100.00

Total Node Count 10 Toggled Node Count = 10 ${\rm Untoggled\ Node\ Count}\,=\,$ 0

Toggle Coverage 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	$\begin{array}{c} \text{Design} \\ \text{UnitType} \end{array}$	_	File (Line) Hits Status
work.FIFO::cover_counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 850 Covered
$work.FIFO::cover_read_ptr_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 850 Covered
work.FIFO::coverwrite_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167) 850 Covered
$work.FIFO::cover__read_ptr_wrap around$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166) 1 Covered
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165) 21 Covered
$work.FIFO::cover_almost_empty_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164) 181 Covered
$work.FIFO::cover_almost_full_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 43 Covered
$work.FIFO::cover__full_flag_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162) 29 Covered
$work.FIFO::cover_empty_flag_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 197 Covered
$work.FIFO::cover_underflow_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 55 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 9 Covered
work.FIFO::cover_write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 484 Covered
$work.FIFO::cover_reset_behavior$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157) 159 Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File (Line)	Failure Count	$egin{array}{c} { m Pass} \\ { m Count} \end{array}$
work . FIFO : : a	assertcounter_threshold		
		yn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(15
work . FIFO : : a	assert_read_ptr_threshold		
	-	yn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(154
work . FIFO : : a	assertwrite_ptr_threshold		
		vn fifo/sv verifica	tion/FIFO_v1.0.0.sv(15
	/ nome/ tare/ Besittop/ s	0	1
work.FIFO:: a	assert_read_ptr_wraparound	Ü	1
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv(155
work . FIFO : : a	assertwrite_ptr_wraparound		
		vn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(15
	/ /	0	1
work FIFO :: a	assert_almost_empty_check	_	_
		vn fifo/sv verifica	tion/FIFO_v1.0.0.sv(150
	/ Home/ tare/ Besktop/ s	0	1
work FIFO · · a	assert_almost_full_check	O	1
WOIR.111 O o		vn fifo/sv verifica	tion/FIFO_v1.0.0.sv(149
	/ nome/ tare/ besktop/ s	y 11 _ 11 11 0 / 5 v _ v C 1 11 1 C a	1
work . FIFO : : a	assertfull_flag_check	U	1
		yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv(148

```
0
                                                                   1
work.FIFO::assert_empty_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert_write_ack_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Total Coverage By Design Unit (filtered view): 98.66%
    Code Coverage "seed5" Report
Coverage Report by DU with details
```

5.5

```
— Design Unit: work.FIFO
Assertion Coverage:
    Assertions
                                               13
                                                              100.00\%
                                                   Failure
Name
                     File (Line)
                                                                Pass
                                                   Count
                                                                Count
work.FIFO::assert_counter_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
work.FIFO::assert_read_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
work.FIFO::assert_write_ptr_threshold
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
work.FIFO::assert_read_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
work.FIFO::assert_write_ptr_wraparound
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
work.FIFO::assert_almost_empty_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
work.FIFO::assert_almost_full_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
work.FIFO::assert_full_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO::assert_empty_flag_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO:: assert\_\_write\_ack\_check
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Branch Coverage:
                                  Bins
                                             Hits
    Enabled Coverage
                                                     _{
m Misses}
                                                            Coverage
   Branches
                                    25
                                               25
                                                          0
                                                              100.00\%
                                Branch Details=
```

Branch Coverage for Design Unit work.FIFO

Lin	e Item	Count	Source			
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv						
		—IF Branch———				
13		1139	Count coming in to IF			
13	1	294	if (!fifo_intf.rst_n) begin			
18	1	575	else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin			
23	1	270	else begin			
Branch totals: 3 hits of 3 branches = 100.00%						

-IF Branch-

```
25
                                                270
                                                         Count coming in to IF
    25
                     1
                                                 37
                                                                     if (fifo_intf.full & fifo_intf.wr_en)
    27
                     1
                                                233
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -\mathrm{IF} Branch-
    33
                                                         Count coming in to IF
                                               1139
    33
                     1
                                                294
                                                            if (!fifo_intf.rst_n) begin
                                                203
    38
                     1
                                                            else if (fifo_intf.rd_en && count != 0) begin
                                                642
                     1
                                                            else begin
Branch totals: 3 hits of 3 branches = 100.00%
                                    —IF Branch-
                                                642
    43
                                                         Count coming in to IF
                                                                     if (fifo_intf.empty & fifo_intf.rd_en)
                     1
                                                49
    43
                     1
                                                593
    45
                                                                     else
Branch totals: 2 hits of 2 branches = 100.00%
                                     -\!\!-\!\!\operatorname{IF} Branch-
                                               1065
    51
                                                         Count coming in to IF
                     1
                                                281
    51
                                                            if (!fifo_intf.rst_n) begin
                     1
                                                784
                                                            else begin
    54
Branch totals: 2 hits of 2 branches = 100.00%
                                    --IF Branch-
                                                784
                                                         Count coming in to IF
                     1
                                                                           (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} == 2'b10) \&\& !fifo\_intf.fu
    55
                                                407
                                                                     i f
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                                                 61
    57
                     1
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                     1
                                                  9
                                                 35
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                     1
                                                272
                                                         All False Count
Branch totals: 5 hits of 5 branches = 100.00\%
                                      {
m -IF} {
m Branch}{
m -}
    66
                                                632
                                                         Count coming in to IF
                     1
                                                 20
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     2
                                                612
    66
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -IF \operatorname{Branch}-
    67
                                                893
                                                         Count coming in to IF
                                                         assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                     1
                                                400
                                                         assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
                     ^{2}
                                                493
Branch totals: 2 hits of 2 branches = 100.00%
                                      {
m -IF} Branch-
    68
                                                632
                                                         Count coming in to IF
                     1
                                                 32
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     ^{2}
                                                600
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -IF \operatorname{Branch}-
                                                632
                                                         Count coming in to IF
                     1
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                                                144
                     2
                                                488
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                            Covered
                                                        _{
m Misses}
                                                                Coverage
    Conditions
                                      25
                                                 23
                                                             ^{2}
                                                                  92.00\%
                                ==Condition Details=
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
Line
           18 Item 1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term Covered Reason for no coverage Hint
                           Υ
  fifo_intf.wr_en
                           Y
      (count < 8)
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
                        fifo_intf.wr_en_0
 Row
        1:
        2:
                                                (count < 8)
 Row
                        fifo_intf.wr_en_1
  Row
        3:
                        (count < 8)_{-0}
                                                fifo_intf.wr_en
        4:
                        (count < 8)_{-1}
                                                fifo_intf.wr_en
 Row
                     1
                -Focused Condition View-
                     1 (fifo_intf.full & fifo_intf.wr_en)
Line
Condition totals: 1 of 2 input terms covered = 50.00%
                     Covered Reason for no coverage
       Input Term
                                                          Hint
```

Hit '_0'

 $^{\prime}_{-0}$ on not hit

Ν

Y

fifo_intf.full

 $fifo_intf.wr_en$

```
Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
               ***0***
                        fifo_intf.full_0
                                                fifo_intf.wr_en
                        fifo_intf.full_1
  Row
        2:
                     1
                                                fifo_intf.wr_en
                        fifo_intf.wr_en_0
                                                fifo_intf.full
  Row
        3:
                     1
                        fifo_intf.wr_en_1
                                                fifo_intf.full
 Row
        4:
                     1
                -Focused Condition View-
           38 Item
                      1 (fifo_intf.rd_en \&\& (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Y
  fifo_intf.rd_en
     (count != 0)
                           Y
                  _{
m Hits}
                        FEC Target
     Rows:
                                                Non-masking condition(s)
                        fifo_intf.rd_en_0
 Row
        1:
                     1
                        fifo_intf.rd_{en_1}
  Row
        2:
                                                (count != 0)
                     1
                        (count != 0)_{-0}
                                                fifo_intf.rd_en
  Row
        3:
                     1
                        (count != 0)_{-1}
                                                fifo_intf.rd_en
 Row
        4:
                     1
                 -Focused Condition View-
           43 Item
                      1 (fifo_intf.empty & fifo_intf.rd_en)
Line
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Ν
                               '_0' not hit
                                                          Hit '_0'
  fifo_intf.empty
                           Y
  fifo_intf.rd_en
                        FEC Target
     Rows:
                                                Non-masking condition(s)
                  _{
m Hits}
  Row
        1:
               ***0***
                        fifo_intf.empty_0
                                                fifo_intf.rd_en
  Row
        2:
                        fifo_intf.empty_1
                                                fifo_intf.rd_en
                     1
  Row
        3:
                        fifo_intf.rd_en_0
                                                fifo_intf.empty
                     1
                                                fifo_intf.empty
        4:
                        fifo_intf.rd_en_1
  Row
                     1
                 -Focused Condition View-
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Line
           55 Item
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
   fifo_intf.full
     Rows:
                  _{
m Hits}
                        FEC Target
                                                Non-masking condition(s)
                                                (~fifo_intf.full && fifo_intf.wr_en)
  Row
        1:
                        fifo_intf.rd_en_0
                        fifo_intf.rd_en_1
  Row
                        fifo_intf.wr_en_0
  Row
        3:
                                                ~ fifo_intf.rd_en
  Row
        4:
                        fifo_intf.wr_en_1
                                                (~fifo_intf.full && ~fifo_intf.rd_en)
                        fifo_intf.full_0
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
  Row
                        fifo_intf.full_1
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
                 \operatorname{-Focused} Condition View-
Line
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00\%
                              Reason for no coverage
       Input Term
                     Covered
                                                          Hint
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
                           Y
  fifo_intf.empty
     Rows:
                        FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        fifo_intf.rd_en_0
  Row
                        fifo_intf.rd_en_1
                                                (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
        3:
                        fifo_intf.wr_en_0
                                                (~fifo_intf.empty && fifo_intf.rd_en)
  Row
        4:
                        fifo_intf.wr_en_1
                                                fifo_intf.rd_en
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                     1
                        fifo_intf.empty_0
  Row
        6:
                     1
                        fifo_intf.empty_1
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
                 -Focused Condition View-
           59 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
   fifo_intf.full
                        FEC Target
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
        1:
                     1
                        fifo_intf.rd_en_0
                                                (fifo_intf.full && fifo_intf.wr_en)
        2:
 Row
                     1
                        fifo_intf.rd_en_1
```

```
(fifo_intf.full && fifo_intf.rd_en)
  Row
                        fifo_intf.wr_en_1
  Row
                         fifo_intf.full_0
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
                        fifo_intf.full_1
  Row
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
                 -Focused Condition View-
            61 Item
                      1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
  fifo_intf.empty
                            Y
                  _{
m Hits}
                        FEC Target
     Rows:
                                                Non-masking condition(s)
                        fifo_intf.rd_en_0
  Row
        1:
                     1
                                                (fifo_intf.empty && fifo_intf.wr_en)
  Row
         2:
                        fifo_intf.rd_en_1
                        fifo_intf.wr_en_0
                                                fifo_intf.rd_en
  Row
         3:
                     1
                        fifo_intf.wr_en_1
                                                (fifo_intf.empty && fifo_intf.rd_en)
  Row
         4:
                     1
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                        fifo_intf.empty_0
        5:
                     1
                                                (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
         6:
                     1
                        fifo_intf.empty_1
                 -Focused Condition View-
            66 Item
                     1 \quad (count == 8)
Line
Condition totals: 1 of 1 input term covered = 100.00\%
    Input Term
                  Covered Reason for no coverage
                                                      _{
m Hint}
  (count == 8)
                        Y
                        FEC Target
     Rows:
                  Hits
                                                Non-masking condition(s)
  Row
        1:
                     1
                        (count = 8)_{-0}
         2:
                        (count = 8)_{-1}
  Row
                     1
                 -Focused Condition View-
                     1 ((count == 0) \mid | \tilde{fifo_intf.rst_n})
Line
            67 Item
Condition totals: 2 of 2 input terms covered = 100.00%
                     Covered Reason for no coverage
       Input Term
                                                          _{
m Hint}
     (count = 0)
                           Y
                            Y
  fifo_intf.rst_n
                  _{
m Hits}
                        FEC Target
     Rows:
                                                Non-masking condition(s)
                        (count = 0)_{-0}
  Row
         1:
                     1
                                                fifo_intf.rst_n
                        (count = 0)_{-1}
  Row
         2:
  Row
        3:
                        fifo_intf.rst_n_0
                                                \tilde{} (count == 0)
                        fifo_intf.rst_n_1
                                                \tilde{} (count == 0)
  Row
                 Focused Condition View-
Line
            68 Item
                       1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
           Input Term
                        Covered Reason for no coverage
  (count = (8 - 1))
                               Y
     Rows:
                  Hits
                        FEC Target
                                                Non-masking condition(s)
                        (count = (8 - 1))_{-0}
  Row
         1:
  Row
         2:
                        (count = (8 - 1))_{-1}
                 Focused Condition View—
Line
            69 Item
                      1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
                  Covered Reason for no coverage
    Input Term
                                                Non-masking condition(s)
     Rows:
                  Hits FEC Target
  Row
        1:
                     1
                        (count = 1)_{-0}
         2:
                        (count = 1)_{-1}
  Row
                     1
Directive Coverage:
                                      13
                                                 13
                                                                 100.00\%
    Directives
DIRECTIVE COVERAGE:
                                                             Lang File (Line)
                                                                                    Hits Status
Name
                                            Design Design
                                                   UnitType
                                            Unit
                                                                  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)
work.FIFO::cover_counter_threshold
                                            FIFO
                                                   Verilog
                                                             SVA
                                                                                     846 Covered
                                                            SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)
                                            FIFO
work.FIFO::cover_read_ptr_threshold
                                                   Verilog
```

fifo_intf.rd_en

fifo_intf.wr_en_0

Row

162 Covered

Statement Coverage:

Enabled Coverage	$_{ m Bins}$	$_{ m Hits}$	Misses	Coverage
Statements	28	28	0	100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

```
Line
                                              Count
                                                         Source
                Item
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                                         module FIFO(FIFO_IF.DUT fifo_intf);
 1
                                                         parameter FIFO_WIDTH = 16;
 ^{2}
 3
                                                         parameter FIFO_DEPTH = 8;
 4
                                                         localparam max_fifo_addr = $clog2(FIFO_DEPTH);
 5
  6
                                                         reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
  7
  8
                                                         reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
  9
                                                         reg [max_fifo_addr:0] count;
  10
  11
                                                         always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  12
                   1
                                               1139
  13
                                                            if (!fifo_intf.rst_n) begin
                    1
                                                294
                                                                      wr_ptr \le 0;
  14
  15
                    1
                                                294
                                                                      fifo_intf.wr_ack \ll 0;
  16
                    1
                                                294
                                                                      fifo_intf.overflow <= 0;
  17
                                                            \operatorname{end}
                                                             else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
  18
                                                                     mem[wr_ptr] <= fifo_intf.data_in;
  19
                    1
                                                575
  20
                    1
                                                575
                                                                     fifo_intf.wr_ack \ll 1;
  21
                                                575
                                                                      wr_ptr \ll wr_ptr + 1;
  22
                                                            \operatorname{end}
  23
                                                            else begin
  24
                    1
                                                270
                                                                      fifo_intf.wr_ack \ll 0;
  25
                                                                      if (fifo_intf.full & fifo_intf.wr_en)
  ^{26}
                    1
                                                 37
                                                                               fifo_intf.overflow <= 1;
  27
                                                                      else
  28
                    1
                                                233
                                                                               fifo_intf.overflow \ll 0;
  ^{29}
                                                            \operatorname{end}
  30
                                                         end
  31
  32
                    1
                                               1139
                                                         always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
                                                             if (!fifo_intf.rst_n) begin
  33
  34
                    1
                                                294
                                                                     rd_ptr \le 0;
  35
                    1
                                                294
                                                                      fifo_intf.underflow \ll 0;
                                                                      fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
  36
                    1
                                                294
  37
  38
                                                             else if (fifo_intf.rd_en && count != 0) begin
  39
                   1
                                                203
                                                                      fifo_intf.data_out <= mem[rd_ptr];
                    1
  40
                                                203
                                                                      rd_ptr \ll rd_ptr + 1;
  41
                                                            \operatorname{end}
  42
                                                            else begin
                                                                      if (fifo_intf.empty & fifo_intf.rd_en)
  43
                    1
  44
                                                 49
                                                                               fifo_intf.underflow <= 1;
  45
                                                                      else
                                                                               fifo_intf.underflow \le 0;
  46
                   1
                                                593
  47
                                                            \operatorname{end}
  48
                                                         end
  49
                    1
                                               1065
                                                         always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  50
  51
                                                             if (!fifo_intf.rst_n) begin
  52
                   1
                                                281
                                                                     count \ll 0;
  53
                                                            _{\mathrm{end}}
                                                             else begin
  54
                                                                               (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
  55
                                                                      i f
                   1
                                                407
                                                                               count \le count + 1;
  56
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
  57
```

```
61
                     1
    58
                                                                             count \ll count - 1;
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                                                  9
                                                                             count \ll count - 1;
                     1
    60
                                                                    else if ( (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.emp
    61
                     1
                                                 35
    62
                                                                             count \ll count + 1;
    63
                                                           end
                                                        end
    64
    65
                                                633
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                                                894
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                                                633
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     1
                                                633
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
Toggle Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                               Hits
                                                       Misses
                                                               Coverage
                                      20
                                                            0
                                                                100.00\%
    Toggles
                                                 20
```

Toggle Coverage for Design Unit work.FIFO

=Toggle Details=

Node	e 1H—>0L	0L->1H	"Coverage"
$\operatorname{count}\left[0-3\right]$] 1	1	100.00
$rd_ptr[0-2]$] 1	1	100.00
$wr_ptr[0-2]$	1	1	100.00

Toggle Coverage = 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	$\begin{array}{c} \mathrm{Design} \\ \mathrm{Unit} \end{array}$	$\begin{array}{c} {\rm Design} \\ {\rm UnitType} \end{array}$	_	File (Line) Hits Status
work.FIFO::covercounter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 846 Covered
$work.FIFO::cover_read_ptr_threshold$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 846 Covered
work.FIFO::coverwrite_ptr_threshold	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)\\846\ Covered$
$work.FIFO:: cover__read_ptr_wrap around$	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)\\ 2~Covered$
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)\\24~Covered$
$work.FIFO:: cover_almost_empty_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164) 190 Covered
$work.FIFO::cover_almost_full_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 48 Covered
work.FIFO::coverfull_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162) 49 Covered
work . FIFO:: $\operatorname{cover_empty_flag_check}$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) 185 Covered
$work.FIFO::cover_underflow_check$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 39 Covered
work.FIFO::coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 23 Covered
work.FIFO::coverwrite_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 485 Covered
work.FIFO::cover_reset_behavior	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)\\ 162~Covered$

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File (Line)	Failure Count	Pass Count	
work.FIFO:: ass	sert_counter_threshold			
	/home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0	. sv (155)
	, , , , , , , , , , , , , , , , , , , ,	, 0	1	`
work.FIFO:: ass	sert_read_ptr_threshold	· ·		
	/home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0	. sv (154
		0	1	
work.fifO:: as:	sertwrite_ptr_threshold /home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0	. sv (153
work FIFO ass	sert_read_ptr_wraparound	U	1	
work.Fif O ass	/home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0	. sv (152
	, , , , , , , , , , , , , , , , , , , ,	,	1	
work.FIFO:: ass	sert_write_ptr_wraparound			
	/home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0	. sv (151)
		0	1	
work.FIFO::ass	sert_almost_empty_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	tion/FIFO_v1.0.0 1	. sv (150)

```
work.FIFO:: assert\_almost\_full\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(149) \\ work.FIFO:: assert\_full\_flag\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(148) \\ 0 1 \\ work.FIFO:: assert\_empty\_flag\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(147) \\ work.FIFO:: assert\_underflow\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(146) \\ work.FIFO:: assert\_overflow\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(145) \\ work.FIFO:: assert\_write\_ack\_check \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(144) \\ work.FIFO:: assert\_reset\_behavior \\ /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(143) \\ 0 1 \\ \end{cases}
```

Total Coverage By Design Unit (filtered view): 98.66%

6 Waveform

3.1 Waveform & Transcript "seed1" Report

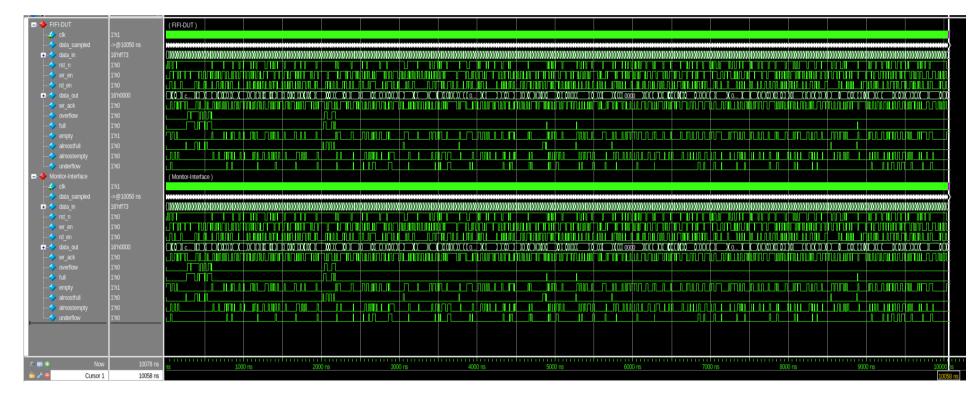


Figure 6: simulation waveform "seed1"

```
# Loading sv_std.std
 Loading work.Shared_pkg(fast)
 Loading work.Shared_pkg_sv_unit(fast)
 Loading work.FIFO_top(fast)
 Loading work.FIFO_IF(fast__1)
  Loading work.FIFO(fast)
  Loading work.FIFO_transaction_pkg(fast)
 Loading work.FIFO_tb(fast)
 Loading work.FIFO scoreboard pkg(fast)
 Loading work.FIFO coverage pkg(fast)
 Loading work.FIFO_monitor(fast)
 run -all
  Test Summary:
    Total Correct: 1008
    Total Errors: 0
    Coverage: 99.75%
                    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
  ** Note: $stop
     Time: 10078 ns Iteration: 0 Instance: /FIFO top/mon
 Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
 Stopped at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
  quit -f
# End time: 14:44:51 on May 01,2025, Elapsed time: 0:00:04
# Errors: 0, Warnings: 0
Running simulation with seed 1111
Reading pref.tcl
```

Figure 7: Transcript : all test cases passed "seed1"



Figure 8: simulation waveform "seed2"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIF0_seed1111.ucdb
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 1511
Reading pref.tcl
# Test Summary:
  Total Correct: 1008
  Total Errors: 0
  Coverage: 99.84%
*** Note: $stop : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
# Time: 10078 ns Iteration: 0 Instance: /FIFO_top/mon
# Break in Module FIFO monitor at /home/tare/Desktop/syn fifo/sv verification/FIFO monitor.sv line 66
```

Figure 9: Transcript : all test cases passed "seed2"

6.3 Waveform & Transcript "seed3" Report

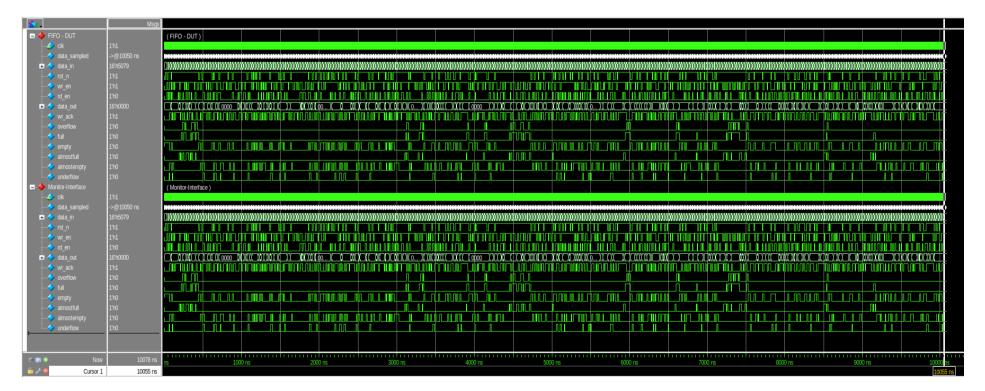


Figure 10: simulation waveform "seed3"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIF0_seed1111.ucdb
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIF0_seed1511.ucdb
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2515
Reading pref.tcl
# Test Summary:
  Total Correct: 1008
  Total Errors: 0
  Coverage: 99.84%
# ** Note: $stop : /home/tare/Desktop/syn fifo/sv verification/FIFO monitor.sv(66)
 Time: 10078 ns Iteration: 0 Instance: /FIFO_top/mon
# Break in Module FIFO monitor at /home/tare/Desktop/syn fifo/sv verification/FIFO monitor.sv line 66
```

Figure 11: Transcript : all test cases passed "seed3"

6.4 Waveform & Transcript "seed4" Report



Figure 12: simulation waveform "seed4"

```
Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIF0_seed1511.ucdb
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIF0_seed2515.ucdb
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2236
Reading pref.tcl
Test Summary:
 Total Correct: 1008
 Total Errors: 0
 Coverage: 99.75%
** Note: $stop : /home/tare/Desktop/syn fifo/sv verification/FIFO monitor.sv(66)
  Time: 10078 ns Iteration: 0 Instance: /FIFO_top/mon
Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
```

Figure 13: Transcript : all test cases passed "seed4"

6.5 Waveform & Transcript "seed5" Report



Figure 14: simulation waveform "seed5"

```
Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIF0_seed2515.ucdb
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2236
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:01:48 on May 01,2025
vcover report FIFO_seed2236.ucdb -details -annotate -all -output code_coverage_rpt_seed2236.txt -du=FIFO
End time: 15:01:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:01:48 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2236.txt FIF0_seed2236.ucdb
End time: 15:01:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 5215
Reading pref.tcl
Test Summary:
 Total Correct: 1008
 Total Errors: 0
 Coverage: 99.92%
** Note: $stop : /home/tare/Desktop/syn fifo/sv verification/FIFO monitor.sv(66)
 Time: 10078 ns Iteration: 0 Instance: /FIFO_top/mon
Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv verification/FIFO monitor.sv line 66
```

Figure 15: Transcript : all test cases passed "seed5"

7 Merged Coverage

```
Merging coverage from all seed runs
vcover merge merged.ucdb FIFO_seed*.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:15 on May 01,2025
vcover merge merged.ucdb FIF0_seed1111.ucdb FIF0_seed1511.ucdb FIF0_seed2236.ucdb FIF0_seed2515.ucdb FIF0_seed5215.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Merging file FIFO_seed1111.ucdb
Merging file FIFO_seed1511.ucdb
Merging file FIFO_seed2236.ucdb
Merging file FIFO_seed2515.ucdb
Merging file FIFO_seed5215.ucdb
Writing merged result to merged.ucdb
End time: 15:09:15 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
Reading pref.tcl
# 2021.2_1
# coverage open merged.ucdb
# coverage read -dataset merged merged.ucdb
# merged.ucdb opened as coverage dataset "merged"
# coverage report -output merged_coverage_report.txt -srcfile=* -detail
# quit -1
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:17 on May 01,2025
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
End time: 15:09:17 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:17 on May 01,2025
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
Errors: 0, Warnings: 0
Coverage merged to merged.ucdb and reports saved
```

Figure 16: Merge seed

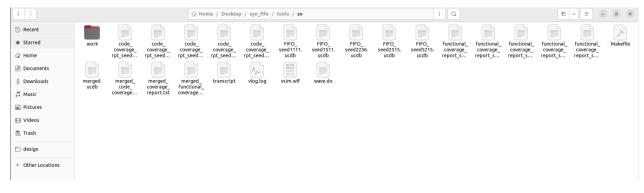


Figure 17: generated files *.ucdb

7.1 Functional Coverage "Merged" Report

Coverage Report by instance with details

Instance: /FIFO_coverage_pkg
Design Unit: work.FIFO_coverage_pkg

Covergroup Coverage:

Covergroups1nana100.00%Coverpoints/Crosses19nananaCovergroup Bins1941940100.00%

overgroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100		Covered
covered/total bins:	100.00% 194	$100 \\ 194$	_	Covered
missing/total bins:	0	194	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	781	1	_	Covered
bin auto[1]	4259	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	00,0104
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	95	1	_	Covered
bin auto [1024:2047]	74	1	_	Covered
bin auto [2048:3071]	72	1	_	Covered
bin auto $[3072:4095]$	$\frac{72}{72}$	1	_	Covered
bin auto [4096:5119]	84	1	_	Covered
bin auto [5120:6143]	71	1	_	Covered
bin auto $[6144:7167]$	70	1	_	Covered
bin auto [7168:8191]	88	1		Covered
bin auto $[8192:9215]$	82	1	_	Covered
bin auto $[8192:9215]$ bin auto $[9216:10239]$	71	1	_	Covered
bin auto [10240:11263]	$\frac{71}{75}$	1		Covered
bin auto $[11264:11263]$	73 78	1	_	Covered
bin auto [12288:13311]	76	1	_	Covered
bin auto [13312:14335]	70	1	_	Covered
	77	1	_	Covered
bin auto [14336:15359]			_	
bin auto [15360:16383]	85	1	_	Covered
bin auto [16384:17407]	89	1	_	Covered
bin auto [17408:18431]	84	1	_	Covered
bin auto [18432:19455]	74	1	_	Covered
bin auto $[19456:20479]$	90	1	_	Covered
bin auto [20480:21503]	76 70	1	_	Covered
bin auto [21504:22527]	79	1	_	Covered
bin auto $[22528:23551]$	68	1	_	Covered
bin auto [23552:24575]	80	1	_	Covered
bin auto $[24576:25599]$	75	1	_	$\operatorname{Covered}$
${\rm bin \;\; auto} [25600 \colon\! 26623]$	82	1	_	$\operatorname{Covered}$
bin auto $[26624:27647]$	78	1	_	$\operatorname{Covered}$
bin auto [27648:28671]	79	1	_	$\operatorname{Covered}$
bin auto $[28672:29695]$	79	1	_	$\operatorname{Covered}$
bin auto $[29696:30719]$	79	1	_	$\operatorname{Covered}$
bin auto $[30720:31743]$	72	1	_	$\operatorname{Covered}$
bin auto $[31744:32767]$	84	1	_	$\operatorname{Covered}$
bin auto $[32768:33791]$	68	1	_	$\operatorname{Covered}$
bin auto [33792:34815]	80	1	_	$\operatorname{Covered}$
bin auto [34816:35839]	81	1	_	Covered
bin auto [35840:36863]	67	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	71	1	_	Covered
bin auto [37888:38911]	69	1	_	$\operatorname{Covered}$
bin auto [38912:39935]	87	1	_	Covered
bin auto [39936:40959]	83	1	_	Covered
bin auto [40960:41983]	70	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	87	1	_	Covered
bin auto [43008:44031]	92	1	_	$\operatorname{Covered}$
bin auto [44032:45055]	65	1	_	Covered
bin auto $[45056:46079]$	89	1	_	Covered
bin auto [46080:47103]	72	1	_	$\operatorname{Covered}$
bin auto [47104:48127]	71	1	_	Covered
bin auto [48128:49151]	82	1	_	Covered
bin auto [49152:50175]	73	1	_	Covered
bin auto [50176:51199]	74	1	_	Covered
bin auto $[51200:52223]$	90	1	_	Covered
bin auto [52224:53247]	90	1	_	Covered
bin auto $[53248:54271]$	74	1	_	Covered
bin auto $[54272:55295]$	85			Covered
bin auto $[54272:55295]$ bin auto $[55296:56319]$		1	_	
	82	1	_	Covered
bin auto [56320:57343]	83	1	_	Covered
bin auto [57344:58367]	87	1	_	Covered
bin auto [58368:59391]	80	1	_	Covered
bin auto [59392:60415]	81	1	_	Covered
bin auto $[60416:61439]$ bin auto $[61440:62463]$	82 80	1	_	Covered Covered
		1		(11

bin auto $[62464:63487]$	78	1	_	Covered
bin auto [63488:64511]	80	1	_	Covered
bin auto [64512:65535]	78	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	100	_	
bin auto [0]	3544	1	_	Covered
bin auto[1]	1496	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	1517	1	_	Covered
bin auto[1]	3523	1	_	Covered
Coverpoint data_out_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	100.0007	64	_	
% Hit: bin auto[0:1023]	$100.00\% \ 2622$	$100\\1$	_	Covered
bin auto $[1024:2047]$	2022	1	_	Covered
bin auto [2048:3071]	47	1	_	Covered
bin auto [3072:4095]	29	1	_	Covered
bin auto [4096:5119]	34	1	_	Covered
bin auto [5120:6143]	33	1	_	Covered
bin auto [6144:7167]	56	1	_	Covered
bin auto [7168:8191]	60	1	_	Covered
bin auto [8192:9215]	54	1	_	Covered
bin auto [9216:10239]	28	1	_	Covered
bin auto [10240:11263]	29	1	_	Covered
bin auto [11264:12287]	66	1	_	Covered
bin auto [12288:13311]	33	1	_	Covered
bin auto [13312:14335] bin auto [14336:15359]	$\frac{46}{38}$	1 1	_	Covered Covered
bin auto [15360:16383]	39	1	_	Covered
bin auto [16384:17407]	60	1		Covered
bin auto [17408:18431]	43	1	_	Covered
bin auto [18432:19455]	28	1	_	Covered
bin auto [19456:20479]	48	1	_	Covered
bin auto $[20480:21503]$	50	1	_	Covered
bin auto [21504:22527]	13	1	_	Covered
bin auto [22528:23551]	23	1	_	Covered
${ m bin \ auto} [23552{:}24575]$	31	1	_	Covered
bin auto $[24576:25599]$	26	1	_	Covered
bin auto $[25600:26623]$	41	1	_	Covered
bin auto [26624:27647]	39	1	_	Covered
bin auto [27648:28671]	33	1	_	Covered
bin auto [28672:29695]	45	1	_	Covered
bin auto $[29696:30719]$ bin auto $[30720:31743]$	$\frac{26}{32}$	1 1	_	Covered Covered
bin auto $[31744:32767]$	$\frac{32}{40}$	1	_	Covered
bin auto [32768:33791]	28	1	_	Covered
bin auto [33792:34815]	46	1	_	Covered
bin auto [34816:35839]	50	1	_	Covered
bin auto [35840:36863]	22	1	_	Covered
bin auto [36864:37887]	35	1	_	Covered
bin auto [37888:38911]	38	1	_	Covered
bin auto [38912:39935]	41	1	_	Covered
bin auto $[39936:40959]$	39	1	_	Covered
bin auto [40960:41983]	26	1	_	Covered
bin auto [41984:43007]	$\frac{54}{65}$	1 1	_	Covered Covered
$egin{array}{lll} ext{bin} & ext{auto} [43008;44031] \ ext{bin} & ext{auto} [44032;45055] \end{array}$	41	1	_	Covered
bin auto $[45056:46079]$	23	1	_	Covered
bin auto [46080:47103]	27 27	1	_	Covered
bin auto [47104:48127]	34	1	_	Covered
bin auto [48128:49151]	35	1	_	Covered
bin auto $[49152:50175]$	40	1	_	Covered
bin auto [50176:51199]	27	1	_	Covered
bin auto [51200:52223]	58	1	_	Covered
bin auto [52224:53247]	59	1	_	Covered
bin auto [53248:54271]	$\frac{34}{42}$	1	_	Covered
bin auto [54272:55295] bin auto [55296:56319]	$\begin{array}{c} 42 \\ 28 \end{array}$	1	_	Covered Covered
bin auto $[563296:56319]$	28 69	1 1	_	Covered
bin auto [57344:58367]	46	1	_	Covered
bin auto [58368:59391]	29	1	_	Covered
bin auto [59392:60415]	18	1	_	Covered
bin auto [60416:61439]	29	1	_	Covered
bin auto [61440:62463]	40	1	_	Covered
bin auto [62464:63487]	22	1	_	Covered
bin auto [63488:64511]	40	1	_	Covered
bin_auto [64512:65535]	43	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	100	_	
% Hit: bin auto $[0]$	100.00% 2204	$100\\1$	_	Covered
bin auto[0]	$\begin{array}{c} 2204 \\ 2836 \end{array}$	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	

% Hit:	100.00%	100		
bin auto[0]	4811	1	- Covere	$^{\mathrm{d}}$
bin auto [1]	229	1	- Covere	$^{\mathrm{ed}}$
Coverpoint full_cp	100.00%	100	- Covere	d
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
	4756		- Covere	1
bin auto[0]		1		
bin auto[1]	284	1	- Covere	
Coverpoint empty_cp	100.00%	100	- Covere	d
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	3900	1	- Covere	d
bin auto[1]	1140	1	- Covere	
Coverpoint almostfull_cp	100.00%	100	- Covere	
			– Covere	·u
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	4780	1	- Covere	$^{\circ}$ d
bin auto[1]	260	1	- Covere	$^{\mathrm{d}}$
Coverpoint almostempty_cp	100.00%	100	- Covere	$^{\mathrm{ed}}$
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
	3943	1	- Covere	1
bin auto[0]				
bin auto[1]	1097	1	- Covere	
$\operatorname{Coverpoint}$ $\operatorname{underflow_cp}$	100.00%	100	- Covere	d
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	4700	1	- Covere	d
bin auto[1]	340	1	- Covere	
Cross wr_ack_cross	100.00%	100	- Covere	
			– Covere	·u
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	828	1	- Covere	$\cdot \mathbf{d}$
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	211	1	- Covere	$^{\mathrm{d}}$
bin < auto[0], auto[1], auto[1] >	2008	1	- Covere	$^{\mathrm{ed}}$
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	476	1	- Covere	$^{\mathrm{ed}}$
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	457	1	- Covere	
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	1060	1	- Covere	
	1000	1	- Covere	·u
Illegal and Ignore Bins:	0		ZEDO	
ignore_bin w_en_nactv_wr_ack	0		– ZERO	
Cross full_cross	100.00%	100	- Covere	ea
covered/total bins:	100.00%	6	– Covere	ea
covered/total bins:			_ Covered	ea
<pre>covered/total bins: missing/total bins:</pre>	6 0	6 6	- Covere	ea
<pre>covered/total bins: missing/total bins: % Hit:</pre>	6	6	- Covered	ea
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</pre>	$6\\0\\100.00\%$	6 6 100	_ _ _	
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""></auto[0],></pre>	$6 \\ 0 \\ 100.00\%$	6 6 100	_ _ _ _ Covere	ed
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[0]<="" pre=""></auto[0],></auto[0],></pre>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \end{array}$	$ \begin{array}{c} 6 \\ 6 \\ 100 \end{array} $	– – – Covere – Covere	$_{ m ed}$
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[0],></auto[0],></pre>	$ \begin{array}{r} 6 \\ 0 \\ 100.00\% \\ \hline 234 \\ 50 \\ 1039 \\ \end{array} $	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- Covere - Covere - Covere	ed ed
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[0],></pre>	$ \begin{array}{r} 6 \\ 0 \\ 100.00\% \\ \hline 234 \\ 50 \\ 1039 \\ 457 \\ \end{array} $	6 6 100 1 1 1 1	- Covered Cove	ed ed ed
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></pre>	$ \begin{array}{c} 6 \\ 0 \\ 100.00\% \end{array} $ $ \begin{array}{c} 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \end{array} $	6 6 100 1 1 1 1	- Covered Cove	ed ed ed ed
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></pre>	$ \begin{array}{r} 6 \\ 0 \\ 100.00\% \\ \hline 234 \\ 50 \\ 1039 \\ 457 \\ \end{array} $	6 6 100 1 1 1 1	- Covered Cove	ed ed ed ed
<pre>covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></pre>	$ \begin{array}{c} 6 \\ 0 \\ 100.00\% \end{array} $ $ \begin{array}{c} 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \end{array} $	6 6 100 1 1 1 1	- Covered Cove	ed ed ed ed
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covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> linegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> linegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 222 \\ 42 \\ 932 \\ 2395 \\ \end{array}$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostful_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 101.00\% \\ \\ 107 \\ 89 \\ 22 \\ 42 \\ 932 \\ 2395 \\ 435 \\ 1018 \\ \\ \end{array}$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> cross almostempty_cross</auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 107 \\ 89 \\ 22 \\ 42 \\ 932 \\ 2395 \\ 435 \\ 1018 \\ 100.00\% \\ \\ \end{array}$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 100.00\% \\ \\ 8 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin v_en_ren_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins:</auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lillegal and Ignore Bins: ignore_bin w_en_r_en_allactv_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0],="" auto[1]=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 100.00\% \\ \\ 8 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Cross almostempty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ \\ 107 \\ 89 \\ 22 \\ 42 \\ 932 \\ 2395 \\ 435 \\ 1018 \\ 100.00\% \\ \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ \end{array}$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e
covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lillegal and Ignore Bins: ignore_bin w_en_r_en_allactv_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> cross almostempty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],>	$\begin{array}{c} 6 \\ 0 \\ 100.00\% \\ \\ 234 \\ 50 \\ 1039 \\ 457 \\ 2250 \\ 1010 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 165 \\ 242 \\ 874 \\ 2134 \\ 215 \\ 677 \\ \\ \\ 733 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 100.00\% \\ \\ 8 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Covered Covere	ed e

bin <auto[0], auto[1]="" auto[1],=""></auto[0],>	477	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	49	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [1] \rangle$	187	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	655	1	_	Covered
bin < auto[0], auto[1], auto[0] >	2007	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	408	1	_	Covered
bin < auto[0], auto[0], auto[0] >	873	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	75	1	_	Covered
bin < auto[1], auto[1], auto[0] >	964	1	_	Covered
bin < auto[0], auto[1], auto[1] >	154	1	_	Covered
bin < auto[0], auto[1], auto[0] >	2330	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0] >$	457	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0]$	1060	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] > $	231	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[0]\;,\mathrm{auto}[1]\!>$	109	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}[1]\ ,\mathrm{auto}[1]\ ,\mathrm{auto}[0]\!>$	808	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[0 ight]$, $\mathrm{auto} \left[1 ight]$, $\mathrm{auto} \left[0 ight] > 0$	2484	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[1 ight]$, $\mathrm{auto} \left[0 ight]$, $\mathrm{auto} \left[0 ight] > 0$	348	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight] , \mathrm{auto} \left[0 ight] , \mathrm{auto} \left[0 ight] > $	1060	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	$_{ m Bins}$	Status
	100.00%	100		Covered
covered/total bins:	194	194	_	
missing/total bins:	0	194	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$	781	1	_	$\operatorname{Covered}$
bin auto[1]	4259	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	95	1	_	$\operatorname{Covered}$
bin auto $[1024:2047]$	74	1	_	$\operatorname{Covered}$
bin auto [2048:3071]	72	1	_	$\operatorname{Covered}$
bin auto $[3072:4095]$	72	1	_	$\operatorname{Covered}$
bin auto $[4096:5119]$	84	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[5120 \colon\! 6143\right]$	71	1	_	$\operatorname{Covered}$
bin auto $[6144:7167]$	70	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	88	1	_	$\operatorname{Covered}$
bin auto [8192:9215]	82	1	_	$\operatorname{Covered}$
bin auto [9216:10239]	71	1	_	$\operatorname{Covered}$
bin auto $[10240:11263]$	75	1	_	$\operatorname{Covered}$
bin auto $[11264:12287]$	78	1	_	$\operatorname{Covered}$
bin auto $[12288:13311]$	76	1	_	$\operatorname{Covered}$
bin auto [13312:14335]	71	1	_	$\operatorname{Covered}$
bin auto $[14336:15359]$	77	1	_	$\operatorname{Covered}$
bin auto $[15360:16383]$	85	1	_	$\operatorname{Covered}$
bin auto $[16384:17407]$	89	1	_	$\operatorname{Covered}$
bin auto $[17408:18431]$	84	1	_	$\operatorname{Covered}$
bin auto [18432:19455]	74	1	_	$\operatorname{Covered}$
bin auto $[19456:20479]$	90	1	_	$\operatorname{Covered}$
bin auto $[20480:21503]$	76	1	_	$\operatorname{Covered}$
bin auto $[21504:22527]$	79	1	_	$\operatorname{Covered}$
bin auto $[22528:23551]$	68	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ \mathrm{auto} \left[23552{:}24575 \right]$	80	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[24576 \colon\! 25599\right]$	75	1	_	$\operatorname{Covered}$
${\rm bin \;\; auto} [25600 \colon\! 26623]$	82	1	_	$\operatorname{Covered}$
bin auto $[26624:27647]$	78	1	_	$\operatorname{Covered}$
bin auto $[27648:28671]$	79	1	_	Covered
${\rm bin \ \ auto} [28672 \hbox{:} 29695]$	79	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[29696 \hspace{-0.05cm}:\hspace{-0.05cm} 30719 \right]$	79	1	_	Covered
bin auto [30720:31743]	72	1	_	Covered
bin auto $[31744:32767]$	84	1	_	Covered
bin auto [32768:33791]	68	1	_	Covered
bin auto $[33792:34815]$	80	1	_	Covered
bin auto $[34816:35839]$	81	1	_	Covered
bin auto $[35840:36863]$	67	1	_	Covered
bin auto $[36864:37887]$	71	1	_	Covered
bin auto [37888:38911]	69	1	_	Covered
bin auto [38912:39935]	87	1	_	Covered

bin auto [39936:40959]	83	1	_	Covered
bin auto [40960:41983]	70	1	_	Covered
bin auto [41984:43007]	87	1	_	Covered
bin auto $[43008:44031]$	92	1	_	Covered
bin auto $[44032:45055]$	65	1	_	Covered
bin auto [45056:46079]	89	1	_	Covered
bin auto [46080:47103]	72	1	_	Covered
bin auto [47104:48127]	71	1	_	Covered
bin auto [48128:49151]	82	1	_	Covered
bin auto [49152:50175]	73	1	_	Covered
bin auto [50176:51199]	74	1	_	Covered
bin auto $[51200:52223]$	90	1	_	Covered
bin auto $[52224:53247]$	90	1	_	Covered
bin auto [53248:54271]	74	1	_	Covered
bin auto $[54272:55295]$	85	1	_	Covered
bin auto [55296:56319]	82	1	_	Covered
bin auto $[56320:57343]$	83	1	_	Covered
bin auto [57344:58367]	87	1	_	Covered
bin auto [58368:59391]	80	1	_	Covered
· ·				
bin auto [59392:60415]	81	1	_	Covered
bin auto $[60416:61439]$	82	1	_	Covered
bin auto $[61440:62463]$	80	1	_	Covered
bin auto $[62464:63487]$	78	1	_	Covered
bin auto [63488:64511]	80	1	_	Covered
bin auto $[64512 : 65535]$	78	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
,				
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	3544	1	_	Covered
bin auto[1]	1496	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing / total bins:	0	2	_	
% Hit:	100.00%	100		
			_	
$ \text{bin auto} \left[0 \right]$	1517	1	_	Covered
$\operatorname{bin} \operatorname{auto}[1]$	3523	1	_	Covered
Coverpoint data_out_cp	100.00%	100	_	Covered
covered/total bins:	64	64		Covered
			_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto $[0:1023]$	2622	1	_	Covered
bin auto [1024:2047]	20	1	_	Covered
bin auto [2048:3071]	47	1	_	Covered
bin auto $[3072:4095]$	29	1	_	Covered
bin auto [4096:5119]	34	1	_	Covered
bin auto [5120:6143]	33	1	_	Covered
bin auto $[6144:7167]$	56	1	_	Covered
bin auto $[7168:8191]$	60	1	_	Covered
bin auto [8192:9215]	54	1	_	Covered
bin auto [9216:10239]	28	1	_	Covered
bin auto $[10240:11263]$	29	1	_	Covered
bin auto $[11264:12287]$	66	1	_	Covered
bin auto [12288:13311]	33	1	_	Covered
bin auto [13312:14335]	46	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[14336{:}15359\right]$	38	1	_	Covered
bin auto $[15360:16383]$	39	1	_	Covered
bin auto [16384:17407]	60	1	_	Covered
bin auto [17408:18431]	43	1	_	Covered
bin auto [18432:19455]	28	1	_	Covered
bin auto [19456:20479]	48	1	_	Covered
bin auto $[20480:21503]$	50	1	_	Covered
bin auto [21504:22527]	13	1	_	Covered
bin auto [22528:23551]	$\frac{1}{23}$	1	_	Covered
bin auto [2252:23551] bin auto [23552:24575]	31	1		Covered
bin auto $[24576:25599]$	26	1	_	Covered
$bin \ \ auto \ [25600:26623]$	41	1	_	Covered
bin auto [26624:27647]	39	1	_	Covered
bin auto $[27648:28671]$	33	1	_	Covered
bin auto [28672:29695]	45	1	_	Covered
bin auto $[29696:30719]$	26	1	_	Covered
bin auto [30720:31743]	32	1	_	Covered
bin auto [31744:32767]	40	1	_	Covered
bin auto [32768:33791]	28	1	_	Covered
bin auto [33792:34815]	46	1	_	Covered
bin auto [34816:35839]	50	1	_	Covered
bin auto [35840:36863]	$\frac{3}{2}$	1	_	Covered
bin auto [36864:37887]	35	1	_	Covered
bin auto [37888:38911]	38	1	_	Covered
bin auto 38912:39935	41	1	_	Covered
bin auto [39936:40959]	39	1	_	Covered
bin auto [40960:41983]	26	1	_	Covered
bin auto $[41984:43007]$	54	1	_	Covered
bin auto [43008:44031]	65	1	_	Covered
bin auto [44032:45055]	41	1	_	Covered
bin auto [45056:46079]	23	1	_	Covered
bin auto $[46080:47103]$	27	1	_	Covered
bin auto [47104:48127]	34	1	_	Covered
bin auto [48128:49151]	35	1	_	Covered
				Covered
bin auto [49152:50175]	40	1	_	
bin auto [50176:51199]	27	1	_	Covered
bin auto $[51200:52223]$	58	1	_	Covered

bin auto $[52224:53247]$	59	1	_	Covered
bin auto [53248:54271]	34	1	_	Covered
bin auto [54272:55295]	42	1	_	Covered
bin auto [55296:56319]	28	1	_	Covered
bin auto [56320:57343]	69	1	_	Covered
bin auto [57344:58367]	46	1	_	Covered
bin auto [58368:59391]	29	1	_	Covered
bin auto [59392:60415]	18	1	_	Covered
bin auto [60416:61439]	29	1	_	Covered
bin auto [61440:62463]	40	1	_	Covered
bin auto [62464:63487]	22	1	_	Covered
bin auto $[63488:64511]$	40	1	_	Covered
bin auto $[64512:65535]$	43	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	00,0104
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	2204	1	_	Covered
bin auto[1]	2836	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	00,0104
missing/total bins:	0	$\frac{-}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	4811	1	_	Covered
bin auto[1]	229	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	4756	1		Covered
bin auto[0]	284	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{100.00\%}{2}$	$\frac{100}{2}$	_	Covered
,	0	$\frac{2}{2}$	_	
missing/total bins:	_		_	
% Hit:	100.00%	100	_	C 1
bin auto [0]	3900	1	_	Covered
bin auto[1]	1140	100	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	4780	1	_	Covered
bin auto[1]	260	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	3943	1	_	Covered
$ \text{bin } \text{ auto} \left[1 \right]$	1097	1	_	$\operatorname{Covered}$
$\operatorname{Coverpoint}$ $\operatorname{underflow_cp}$	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	4700	1	_	$\operatorname{Covered}$
bin auto [1]	340	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
$\operatorname{covered}/\operatorname{total}$ bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]>$	828	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[0 ight] >$	211	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight] >$	2008	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] \! > \!$	476	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight], \mathrm{auto} \left[0 ight], \mathrm{auto} \left[0 ight] >$	457	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[0 ight], \mathrm{auto} \left[0 ight] >$	1060	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]>$	234	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right]\!>$	50	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	1039	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\ ,\mathrm{auto}[0]\ ,\mathrm{auto}[0]>$	457	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[0 ight] >$	2250	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\ ,\mathrm{auto}[0]\ ,\mathrm{auto}[0] >$	1010	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
$Cross\ empty_cross$	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]\!>$	165	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right]\!>$	242	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	874	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	2134	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\ ,\mathrm{auto}[0]\ ,\mathrm{auto}[0]>$	215	1	_	Covered

$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0]$	677	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	733		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right] >$	107	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight]>$	89	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight] >$	22	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	42	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	932	1	_	$\overline{\text{Covered}}$
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	2395	1	_	Covered
bin < auto[1], auto[0], auto[0] >	435	1	_	Covered
bin < auto[0], auto[0], auto[0] >	1018	1	_	Covered
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	20.4	1		C 1
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	384	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	477	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	$49 \\ 187$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	655	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{033}{2007}$	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	408	1	_	Covered
$egin{aligned} ext{bin } < & ext{auto} [1] \ , & ext{auto} [0] \ , & ext{auto} [0] > \end{aligned} \ \ egin{aligned} ext{bin } < & ext{auto} [0] \ , & ext{auto} [0] > \end{aligned}$	873	1	_	Covered
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6		Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin $<$ auto [1], auto [1] $>$	75	1	_	Covered
bin $<$ auto [1], auto [1], auto [0] $>$	964	1	_	Covered
bin $<$ auto [0], auto [1], auto [1]>	154	1	_	Covered
bin $<$ auto [0], auto [1], auto [0] $>$	2330	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	457	1	_	Covered
bin < auto[0], auto[0], auto[0] >	1060	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right]>$	231	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	109	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	808	1	_	$\operatorname{Covered}$
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	2484	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	348	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [0], \operatorname{auto} [0] >$	1060	1	_	$\operatorname{Covered}$
Illegal and Ignore Bins:	_			FIDE C
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%

$7.2 \quad {\bf Code} \ {\bf Coverage} \ "{\bf Merged}" \ {\bf Report}$

Coverage Report by DU with details

— Design Unit:	work . FIFO					
Assertion Covera	ge:					
Assertions		13	13	0	100.00%	
Jame	File (Line)			Failure Count	Pass Count	
vork.FIFO:: asser	tcounter_thresh					
	/home/tare/D	Oesktop/sy	n_fifo/	sv_verific 0	ation/FIF0 5	O_v1.0.0.sv (15
vork.FIFO::asser	t_read_ptr_thresl					
	$/\mathrm{home}/\mathrm{tare}/\mathrm{D}$	esktop/sy	n_fifo/	_		$O_{-}v1.0.0.sv(15)$
vork FIFO :: asser	t_write_ptr_thres	shold		0	5	
, 0111.111 0			n_fifo/	sv_verific	ation/FIF(O_v1.0.0.sv(15
	, , , , ,	1, 0	,	0	5	`
vork.FIFO::asser	tread_ptr_wrapar	ound				
	/home/tare/D	Oesktop/sy	n_fifo/	sv_verific	ation/FIF0 5	$O_{-}v1.0.0.sv(15)$
vork FIFO · · asser	twrite_ptr_wrapa	round		U	9	
VOIR.III O abbei			n_fifo/	sv_verific	ation/FIF(O_v1.0.0.sv(15
	,,, -	P/-J		0	5	
vork.FIFO::asser	t_almost_empty_cl	heck				
	$/\mathrm{home}/\mathrm{tare}/\mathrm{D}$	Oesktop/sy	n_fifo/	sv_verific	ation/FIFO	O_v1.0.0.sv(15

```
work.FIFO:: assert\_\_full\_flag\_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
work.FIFO::assert__empty_flag_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
work.FIFO::assert_underflow_check
                      /home/tare/Desktop/syn\_fifo/sv\_verification/FIFO\_v1.0.0.sv(146)
work.FIFO::assert_overflow_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
work.FIFO::assert__write_ack_check
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
work.FIFO::assert_reset_behavior
                      /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
Branch Coverage:
    Enabled Coverage
                                    _{\rm Bins}
                                               Hits
                                                        Misses
                                                                Coverage
    Branches
                                      25
                                                 25
                                                             0
                                                                 100.00\%
                                ==Branch Details==
Branch Coverage for Design Unit work.FIFO
    _{
m Line}
                                                         Source
                  Item
                                              Count
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                    ---IF Branch-
    13
                                               5681
                                                         Count coming in to IF
                     1
                                                            if (!fifo_intf.rst_n) begin
    13
                                               1424
                                               2839
    18
                     1
                                                            else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
                                               1418
                                                            else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                      -{
m IF}~{
m Branch}-
    25
                                               1418
                                                         Count coming in to IF
    25
                     1
                                                172
                                                                     if (fifo_intf.full & fifo_intf.wr_en)
                                               1246
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} {
m Branch}{
m -}
    33
                                               5681
                                                         Count coming in to IF
    33
                     1
                                               1424
                                                            if (!fifo_intf.rst_n) begin
                     1
                                                971
                                                            else if (fifo_intf.rd_en && count != 0) begin
                                               3286
                                                            else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                      {
m -IF} Branch-
    43
                                               3286
                                                         Count coming in to IF
    43
                     1
                                                284
                                                                     if (fifo_intf.empty & fifo_intf.rd_en)
                                               3002
                     1
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} Branch{
m -}
    51
                                               5306
                                                         Count coming in to IF
                     1
                                               1375
                                                            if (!fifo_intf.rst_n) begin
                     1
                                               3931
                                                            else begin
Branch totals: 2 hits of 2 branches = 100.00\%
                                      \operatorname{-IF} Branch\operatorname{--}
    55
                                               3931
                                                         Count coming in to IF
                                                                             (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
                     1
                                               2009
    57
                     1
                                                291
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                     1
                                                 46
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
                                                                     else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                196
                                                         All False Count
Branch totals: 5 hits of 5 branches = 100.00\%
                                      -IF Branch-
    66
                                               3141
                                                         Count coming in to IF
    66
                     1
                                                108
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     2
                                               3033
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -IF Branch-
    67
                                               4421
                                                         Count coming in to IF
                     1
                                                         assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
    67
                                               1955
                     2
                                               2466
    67
                                                         assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {	ext{-IF}} {	ext{Branch}}{	ext{-}}
    68
                                               3141
                                                         Count coming in to IF
                     1
    68
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                                                157
                     2
                                               2984
    68
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
```

/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)

work.FIFO::assert_almost_full_check

```
-IF Branch
    69
                                                3141
                                                          Count coming in to IF
    69
                     1
                                                 722
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                     2
                                                2419
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                     _{\mathrm{Bins}}
                                             Covered
                                                         Misses
                                                                 Coverage
                                                              2
                                                                    92.00\%
    Conditions
                                       25
                                                  23
                                  =Condition Details:
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                 -Focused Condition View-
           18 Item
Line
                      1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
                            Y
  fifo_intf.wr_en
      (count < 8)
                            Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
 Row
        1:
                     5
                         fifo_intf.wr_en_0
  Row
        2:
                         fifo_intf.wr_en_1
                                                 (count < 8)
                     5
                         (count < 8)_{-0}
  Row
        3:
                                                 fifo_intf.wr_en
                     5
                         (count < 8)_{-1}
                                                 fifo_intf.wr_en
  Row
        4:
                 -Focused Condition View-
Line
           25 Item
                       1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
                     Covered Reason for no coverage
       Input Term
                                                           Hint
   fifo_intf.full
                                                           Hit '_0'
                            Ν
                               ^{\prime}_{-0} or not hit
  fifo_intf.wr_en
                            Y
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
                         fifo_intf.full_0
  Row
        1:
               ***0***
                                                 fifo_intf.wr_en
  Row
        2:
                     5
                         fifo_intf.full_1
                                                 fifo_intf.wr_en
  Row
        3:
                         fifo_intf.wr_en_0
                                                 fifo_intf.full
                     5
  Row
        4:
                         fifo_intf.wr_en_1
                                                 fifo_intf.full
                 -Focused Condition View-
Line
           38 Item
                       1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
                     Covered Reason for no coverage
       Input Term
                                                           Hint
  fifo_intf.rd_en
                            Y
     (count != 0)
                            Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
  Row
                         fifo_intf.rd_en_0
  Row
        2:
                         fifo_intf.rd_en_1
                                                 (count != 0)
                         (count != 0)_{-0}
  Row
        3:
                                                 fifo_intf.rd_en
  Row
        4:
                         (count != 0)_{-1}
                                                 fifo_intf.rd_en
                 -Focused Condition View-
Line
                       1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered
                              Reason for no coverage
                                                           Hint
                               '_{-0}, not hit
  fifo_intf.empty
                            Ν
                                                           Hit '_0'
  fifo_intf.rd_en
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
        1:
               ***0***
                         fifo_intf.empty_0
                                                 fifo_intf.rd_en
        2:
                         fifo_intf.empty_1
                                                 fifo_intf.rd_en
  Row
                     5
                                                 fifo_intf.empty
        3:
                         fifo_intf.rd_en_0
  Row
                     5
        4:
                         fifo_intf.rd_en_1
                                                 fifo_intf.empty
 Row
                     5
                 \operatorname{-Focused} Condition View\operatorname{-}
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                           Hint
                            Y
  fifo_intf.rd_en
  fifo_intf.wr_en
                            \mathbf{Y}
                            Y
   fifo_intf.full
```

89

Non-masking condition(s)

Hits FEC Target

Rows:

```
Row
        1:
                         fifo_intf.rd_en_0
                                                 (~fifo_intf.full && fifo_intf.wr_en)
  Row
        2:
                     5
                         fifo_intf.rd_en_1
                         fifo_intf.wr_en_0
                                                 \sim fifo_intf.rd_en
  Row
        3:
                     5
                         fifo_intf.wr_en_1
                                                 (~fifo_intf.full && ~fifo_intf.rd_en)
  Row
        4:
                     5
                                                 (~fifo_intf.rd_en && fifo_intf.wr_en)
                         fifo_intf.full_0
  Row
        5:
                     5
        6:
                         fifo_intf.full_1
                                                 (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                     5
                 -Focused Condition View-
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
           57 Item
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                           Hint
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
                        FEC Target
                     5
                         fifo_intf.rd_en_0
  Row
        1:
                         fifo_intf.rd_en_1
                                                 (~fifo_intf.empty && ~fifo_intf.wr_en)
        2:
  Row
                     5
                         fifo_intf.wr_en_0
                                                 (~fifo_intf.empty && fifo_intf.rd_en)
  Row
        3:
                     5
                                                 fifo_intf.rd_en
  Row
        4:
                         fifo_intf.wr_en_1
                     5
                         fifo_intf.empty_0
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                     5
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
        6:
                         fifo_intf.empty_1
  Row
                     5
                 \hbox{-}Focused \hskip.05in \hbox{Condition}\hskip.05in \hbox{View-}
Line
           59 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                               Reason for no coverage
                      Covered
                                                           Hint
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
   fifo_intf.full
                            Y
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
        1:
                     5
                         fifo_intf.rd_en_0
  Row
         2:
                         fifo_intf.rd_en_1
                                                 (fifo_intf.full && fifo_intf.wr_en)
                     5
                                                 fifo_intf.rd_en
  Row
        3:
                         fifo_intf.wr_en_0
                     5
                                                 (fifo_intf.full && fifo_intf.rd_en)
  Row
        4:
                         fifo_intf.wr_en_1
                     5
                         fifo_intf.full_0
  Row
        5:
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
                     5
  Row
        6:
                         fifo_intf.full_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
                 \hbox{-}Focused \quad Condition \quad View-
Line
           61 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                           Hint
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
  fifo_intf.empty
                            Y
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
         1:
                     5
                         fifo_intf.rd_en_0
        2:
                         fifo_intf.rd_en_1
                                                 (fifo_intf.empty && fifo_intf.wr_en)
  Row
  Row
        3:
                         fifo_intf.wr_en_0
                                                 fifo_intf.rd_en
        4:
                         fifo_intf.wr_en_1
                                                 (fifo_intf.empty && fifo_intf.rd_en)
  Row
                         fifo_intf.empty_0
        5:
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                         fifo_intf.empty_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 -Focused Condition View-
Line
            66 Item
                       1 \quad (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered
                           Reason for no coverage
                                                       Hint
  (count == 8)
                        Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
                         (count = 8)_{-0}
  Row
        1:
                     5
 Row
        2:
                     5
                         (count = 8)_{-1}
                 -Focused Condition View-
                       1 ((count = 0) | | \tilde{fifo_intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
     (count = 0)
                            Y
                            Y
  fifo_intf.rst_n
                  Hits FEC Target
     Rows:
                                                 Non-masking condition(s)
                         (count = 0)_{-}0
  Row
        1:
                     5
                                                 fifo_intf.rst_n
                         (count = 0)_{-1}
        2:
  Row
                     5
        3:
                         fifo_intf.rst_n_0
                                                 \tilde{} (count == 0)
  Row
```

```
Row
                       fifo_intf.rst_n_1
                -Focused Condition View-
           68 Item
                      1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00\%
                                                           Hint
                       Covered Reason for no coverage
                             Y
  (count = (8 - 1))
                 Hits
     Rows:
                       FEC Target
                                              Non-masking condition(s)
                       (count = (8 - 1))_{-0}
  Row
        1:
                    5
        2:
                       (count = (8 - 1))_{-1}
  Row
                -Focused Condition View-
Line
           69 Item
                      1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                 Covered Reason for no coverage
                                                    Hint
                       Υ
  (count == 1)
                       FEC Target
     Rows:
                 _{
m Hits}
                                              Non-masking condition(s)
  Row
        1:
                       (count = 1)_{-0}
                    5
  Row
        2:
                       (count = 1)_{-1}
                    5
Directive Coverage:
                                     13
                                                               100.00\%
    Directives
                                               13
DIRECTIVE COVERAGE:
                                          Design Design
Name
                                                          Lang File (Line)
                                                                                Hits Status
                                          Unit
                                                 UnitType
work.FIFO::cover_counter_threshold
                                          FIFO
                                                  Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)
                                                                                4262 Covered
work.FIFO::cover_read_ptr_threshold
                                          FIFO
                                                  Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)
                                                                                4262 Covered
                                          FIFO
                                                  Verilog
work.FIFO::cover_write_ptr_threshold
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)
                                                                                4262 Covered
                                          FIFO
                                                  Verilog
                                                          SVA
work.FIFO::cover_read_ptr_wraparound
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
                                                                                   10 Covered
                                          FIFO
                                                  Verilog
                                                          SVA
work.FIFO::cover_write_ptr_wraparound
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
                                                                                  111 Covered
                                          FIFO
                                                  Verilog
                                                          SVA
work.FIFO::cover_almost_empty_check
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
                                                                                  900 Covered
work.FIFO::cover__almost_full_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
                                                                                  230 Covered
work.FIFO::cover_full_flag_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                                  244 Covered
work.FIFO::cover_empty_flag_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                                                  956 Covered
work.FIFO::cover_underflow_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                                                  245 Covered
work.FIFO::cover_overflow_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
                                                                                  108 Covered
work.FIFO::cover_write_ack_check
                                          FIFO
                                                  Verilog
                                                          SVA
                                                                /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                                                2398 Covered
work.FIFO::cover_reset_behavior
                                          FIFO
                                                  Verilog
                                                          SVA
                                                               /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                                  781 Covered
Statement Coverage:
    Enabled Coverage
                                                              Coverage
                                   Bins
                                             Hits
                                                      Misses
                                               28
                                                           0
                                                               100.00\%
    Statements
                                     28
                                =Statement Details
Statement Coverage for Design Unit work.FIFO —
    Line
                 Item
                                            Count
                                                       Source
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
                                                       module FIFO(FIFO_IF.DUT fifo_intf);
    2
                                                       parameter FIFO_WIDTH = 16;
    3
                                                       parameter FIFO_DEPTH = 8;
    4
                                                       localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
    6
                                                       reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
    7
    8
                                                       reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
    9
                                                       reg [max_fifo_addr:0] count;
    10
    11
                    1
                                             5681
                                                       always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    12
                                                          if (!fifo_intf.rst_n) begin
    13
                    1
                                                                  wr_ptr \le 0;
    14
                                             1424
```

 $\tilde{}$ (count == 0)

 $fifo_intf.wr_ack \le 0;$

fifo_intf.overflow <= 0;

1424

1424

15

16

1

1

```
17
                                                              \operatorname{end}
                                                               else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                                                                       mem[wr_ptr] <= fifo_intf.data_in;
    19
                      1
                                                 2839
                      1
                                                 2839
                                                                       fifo_intf.wr_ack <= 1;
    20
                      1
                                                 2839
                                                                        wr_ptr \le wr_ptr + 1;
    21
    22
                                                              \operatorname{end}
    23
                                                               else begin
                      1
                                                 1418
    24
                                                                        fifo_intf.wr_ack \le 0;
    25
                                                                        if (fifo_intf.full & fifo_intf.wr_en)
                      1
    26
                                                  172
                                                                                 fifo_intf.overflow <= 1;
    27
                                                                        else
                      1
                                                                                 fifo_intf.overflow \le 0;
                                                 1246
    28
    29
                                                              _{\mathrm{end}}
    30
                                                           end
    31
                      1
                                                 5681
                                                           always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    32
                                                               if (!fifo_intf.rst_n) begin
    33
                      1
                                                                        rd_ptr \le 0;
                                                 1424
    34
                                                 1424
                                                                        fifo_intf.underflow <= 0;
    35
                      1
                                                                        fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};</pre>
                      1
                                                 1424
    36
    37
                                                              \operatorname{end}
                                                               else if (fifo_intf.rd_en && count != 0) begin
    38
                      1
                                                  971
                                                                        fifo_intf.data_out <= mem[rd_ptr];
    39
                      1
                                                  971
                                                                        rd_ptr \ll rd_ptr + 1;
    40
                                                              _{\mathrm{end}}
    41
                                                               else begin
    42
                                                                        if (fifo_intf.empty & fifo_intf.rd_en)
    43
                      1
                                                  284
                                                                                 fifo_intf.underflow <= 1;
    44
    45
                                                                        else
    46
                      1
                                                 3002
                                                                                 fifo_intf.underflow \ll 0;
    47
                                                              _{\mathrm{end}}
                                                           end
    48
    49
                                                           always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    50
                      1
                                                 5306
    51
                                                               if (!fifo_intf.rst_n) begin
    52
                      1
                                                 1375
                                                                        count \ll 0;
    53
                                                              end
    54
                                                               else begin
                                                                                 (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10) \&\& !fifo\_intf.fu
    55
                                                                        i f
                                                 2009
    56
                      1
                                                                                count \ll count + 1;
                                                                        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    57
                      1
                                                  291
    58
                                                                                count \ll count - 1;
                                                                        else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
    59
                      1
                                                   46
                                                                                count \le count - 1;
    60
                                                                        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                                                                                count \le count + 1;
    62
                      1
                                                  196
    63
                                                              _{\mathrm{end}}
                                                           end
    64
    65
    66
                      1
                                                 3146
                                                           assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                                                           assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                      1
                                                 4426
    68
                      1
                                                 3146
                                                           assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    69
                                                 3146
                                                           assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Toggle Coverage:
    Enabled Coverage
                                      Bins
                                                 Hits
                                                          _{
m Misses}
                                                                   Coverage
                                                                    100.00\%
    Toggles
                                        20
                                                   20
                                                               0
```

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H–> $0L$	0L->1H	"Coverage"
$\operatorname{count}\left[0\!-\!3\right]$	5	5	100.00
$\mathrm{rd}_{-}\mathrm{ptr}\left[0-2\right]$	5	5	100.00
$\operatorname{wr-ptr}\left[0-2\right]$	5	5	100.00

Toggle Coverage = 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType		File (Line)	Hits Status
work.FIFO::cover_counter_threshold	FIFO	Verilog	SVA	' '	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 4262 Covered
$work.FIFO::cover_read_ptr_threshold$	FIFO	Verilog	SVA	' '	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 4262 Covered
$work.FIFO:: cover_write_ptr_threshold$	FIFO	Verilog	SVA	' '	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167) 4262 Covered
$work.FIFO:: cover__read_ptr_wrap around$	FIFO	Verilog	SVA	/home/tare/Deskto	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166) 10 Covered
$work.FIFO:: cover_write_ptr_wrap around$	FIFO	Verilog	SVA	' '	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165) 111 Covered
work.FIFO::cover_almost_empty_check	FIFO	Verilog	SVA	/home/tare/Deskto	op/syn_fifo/sy_verification/FIFO_v1.0.0.sy(164)

900 Covered $work.FIFO::cover_almost_full_check$ FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 230 Covered work.FIFO::cover_full_flag_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162) 244 Covered SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161) work.FIFO::cover_empty_flag_check FIFO Verilog 956 Covered $work.FIFO::cover_underflow_check$ FIFO SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) Verilog 245 Covered Verilog work.FIFO::cover_overflow_check FIFO SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 108 Covered FIFO Verilog $work.FIFO::cover_write_ack_check$ SVA/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 2398 Covered FIFO $work.FIFO::cover__reset_behavior$ Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157) 781 Covered TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13 ASSERTION RESULTS:

Name	File (Line)	Failure Count	Pass Count	
vork . FIFO : : as	ssert_counter_threshold			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	n_fifo/sv_verifica 0	tion/FIFO_v1.0.0.sv	(1
work . FIFO : : as	ssert_read_ptr_threshold			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssert_write_ptr_threshold			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssertread_ptr_wraparound			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssertwrite_ptr_wraparound			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssert_almost_empty_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	$ssert__almost_full_check$			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work.FIFO:: a	ssertfull_flag_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssertempty_flag_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssert_underflow_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssertoverflow_check			
	/home/tare/Desktop/sy	n_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
work . FIFO : : as	ssert_write_ack_check /home/tare/Desktop/sy	n_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(1
work . FIFO : : as	ssert_reset_behavior			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{sy}$	n_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(1

Total Coverage By Design Unit (filtered view): 98.66%

7.3 Coverage "Merged" Report

Coverage Report by file with details

atement Coverage: Enabled Coverage	Bins	$_{ m Hits}$	Misses	Coverage
Statements	1	1	0	100.00%
		ent Details=		
atement Coverage fo				verificat
atement Coverage fo				_verificat
		Desktop/sy		verificat:

Toggle Coverage for File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_IF.sv —

0L—>1H "Coverage" Line Node 1H->0L

Total Node Count Toggled Node Count Untoggled Node Count = 100.00% (86 of 86 bins) Toggle Coverage === File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_coverage_pkg.sv Statement Coverage: Enabled Coverage $_{\mathrm{Bins}}$ HitsMisses Coverage 100.00%Statements =Statement Details= = File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv Branch Coverage: Enabled Coverage $_{\mathrm{Bins}}$ HitsMissesCoverage 100.00%Branches =Branch Details= Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv — IF Branch Count coming in to IF All False Count Branch totals: 2 hits of 2 branches = 100.00%Statement Coverage: Enabled Coverage $_{\mathrm{Bins}}$ HitsMisses Coverage Statements 100.00%=Statement Details= Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv — File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv Branch Coverage: Enabled Coverage HitsBins MissesCoverage 48.48%Branches =Branch Details=

Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv —

31	——IF Branch——— 5040	Count coming in to IF
31 1	781	Count coming in to ir
44 1 Branch totals: 2 hits of 2 branch	4259	
Dianen totals. 2 litts of 2 brane	nes = 100.0070	
51	IF Branch	Count coming in to IF
51 1	2836	Count coming in to if
55 1 Branch totals: 2 hits of 2 branch	1423 thes = $100.00%$	
57	IF Branch	Count coming in to IF
57 1	172	004110 00411110 10 11
60 1 Branch totals: 2 hits of 2 branch	1251 ches = $100.00%$	
66	IF Branch	Count coming in to IF
66 1	969	004110 00411110 14 14
69 1 Branch totals: 2 hits of 2 branch	3290 ches = $100.00%$	
70	——IF Branch——— 3290	Count coming in to IF
70 1	284	8
73 1 Branch totals: 2 hits of 2 branch	3006 ches = $100.00%$	
79	IF Branch	Count coming in to IF
79 1	2008	S
82 1 85 1	$\begin{array}{c} 291 \\ 196 \end{array}$	
88 1	46	
Branch totals: 5 hits of 5 branch	1718 ches = $100.00%$	All False Count
108	IF Branch 5040	Count coming in to IF
108 1	5040	
117 1 Branch totals: 1 hit of 2 branch	***0*** nes = $50.00%$	
	IF Branch	
120	***0***	Count coming in to IF
120 1	***0*** ***0***	All False Count
D 1 4 4 1 0 1 4 6 9 1		All Paise Count
Branch totals: 0 hits of 2 branch	ches = 0.00%	
Branch totals: U hits of 2 branch		
121	IF Branch	Count coming in to IF
	IF Branch	
121	IF Branch ***0*** ***0***	Count coming in to IF All False Count
121 121 1	F Branch ***0*** ***0*** ches = 0.00%	
121 121 1 Branch totals: 0 hits of 2 brance		
121 121 1 Branch totals: 0 hits of 2 brance		All False Count
121 121 1 Branch totals: 0 hits of 2 brance	#**0*** ***0*** ***0*** ***0*** TF Branch ***0*** ***0*** ***0***	All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1	#**0*** ***0*** ***0*** ***0*** TF Branch ***0*** ***0*** ***0***	All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance	#**0*** ***0*** ***0*** *ches = 0.00% IF Branch ***0*** ***0*** ***0*** ***0*** The Branch ***0*** ***0***	All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 1 Branch totals: 0 hits of 2 brance	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00%	All False Count Count coming in to IF All False Count
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ***0*** ***0***	All False Count Count coming in to IF All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ***0*** ***0***	All False Count Count coming in to IF All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** **0*** **0*** The branch ***0*** ***0*** ***0*** ***0*** ***0***	All False Count Count coming in to IF All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0***	All False Count Count coming in to IF All False Count Count coming in to IF All False Count
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance	IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** ***0*** ches = 0.00% IF Branch ***0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0***	All False Count Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 Branch totals: 0 hits of 2 brance	#**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** #**0*** ### Discontinuous of the properties of the prope	Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 Branch totals: 0 hits of 2 brance	#**0*** ##*0*** ###0*** ###0** ####0** ####0** ####0** ####0**	All False Count Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 1 Branch totals: 0 hits of 2 brance 124 124 1 Branch totals: 0 hits of 2 brance 125 125 1	IF Branch ***0***	Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 Branch totals: 0 hits of 2 brance	IF Branch ***0***	All False Count Count coming in to IF
121 121 1	IF Branch ***0*** ***10** ***0*** *	Count coming in to IF All False Count
121 121 1 Branch totals: 0 hits of 2 brance 122 122 1 Branch totals: 0 hits of 2 brance 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 Branch totals: 0 hits of 2 brance 125 125 1	IF Branch ***0*** *	All False Count Count coming in to IF
121 121 1 1 Branch totals: 0 hits of 2 brance 122 122 1 1 Branch totals: 0 hits of 2 brance 123 123 1 1 Branch totals: 0 hits of 2 brance 124 124 124 1 1 Branch totals: 0 hits of 2 brance 125 125 1 1 Branch totals: 0 hits of 2 brance 126 126 1 1	IF Branch ***0***	Count coming in to IF All False Count
121 121 1	IF Branch ***0***	Count coming in to IF All False Count Count coming in to IF Count coming in to IF
121 121 121 121 121 122 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 1 Branch totals: 0 hits of 2 brance 125 125 1 Branch totals: 0 hits of 2 brance 126 126 126 1 Branch totals: 0 hits of 2 brance 127 128 129 129 120 120 120 120 120 121 120 120 120 120	### Branch #### ### ### ### ### ### ### ### ### #	Count coming in to IF All False Count
121 121 1	IF Branch ***0*** *	Count coming in to IF All False Count
121 121 121 121 121 122 122 122 122 1 Branch totals: 0 hits of 2 brance 123 123 123 1 Branch totals: 0 hits of 2 brance 124 124 124 1 1 Branch totals: 0 hits of 2 brance 125 125 1 Branch totals: 0 hits of 2 brance 126 126 126 1 Branch totals: 0 hits of 2 brance 127	### Branch #### ### ### ### ### ### ### ### ### #	Count coming in to IF All False Count

Condition Coverage:

```
Enabled Coverage
                                      Bins
                                              Covered
                                                           Misses Coverage
    Conditions
                                        36
                                                               18
                                                                      50.00\%
                                                    18
                                   =Condition Details:
Condition Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv —
                \operatorname{-\!--Focused} Condition View\operatorname{-\!--}
            51 Item 1 (F_{txn.wr_{en}} & (this.count < 8))
Condition totals: 2 of 2 input terms covered = 100.00\%
                —Focused Condition View-
            57 Item
                      1 (F_{txn.wr_en \&\& (this.count == 8)})
Condition totals: 1 of 2 input terms covered = 50.00%
          Input Term
                        Covered Reason for no coverage
                                                               Hint
                               Y
         F_{txn.wr_{en}}
  (this.count == 8)
                                  ^{\prime}_{-0} or not hit
                                                               Hit '_0'
                               Ν
                                                  Non-masking condition(s)
                   Hits FEC Target
     Rows:
 Row
         1:
                      5 \quad F_{txn.wr_{en_0}}
  Row
                      5 \quad F_{txn.wr_{en_1}}
                                                   (this.count == 8)
  Row
         3:
               ***0***
                         (this.count == 8)_{-0}
                                                  F_{txn.wr_{en}}
                         (this.count == 8)_{-1}
                                                  F_{txn.wr_{en}}
  Row
                      5
                -Focused Condition View-
            66 Item 1 (F_txn.rd_en && (this.count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
                 -Focused Condition View-
            70 Item
                      1 (F_{txn.rd_{en} \&\& (this.count == 0)})
Condition totals: 1 of 2 input terms covered = 50.00%
          Input Term
                       Covered Reason for no coverage
                                                               _{
m Hint}
         F_{txn.rd_{en}}
                               Y
                               N '_0' not hit
                                                               Hit '_0'
  (this.count == 0)
     Rows:
                   Hits FEC Target
                                                  Non-masking condition(s)
  Row
         1:
                      5 \quad F_{txn.rd_{en_0}}
                                                   (this.count == 0)
  Row
                      5 \quad F_{txn.rd_{en_1}}
                         (this.count == 0)_{-0}
  Row
         3:
                                                  F_{txn.rd_{en}}
 Row
                         (this.count == 0)_{-1}
                                                  F_{txn.rd_{en}}
                 \operatorname{-Focused} Condition View\operatorname{-}
            79 Item 1 (~F_txn.rd_en && F_txn.wr_en && ~this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
                  -Focused Condition View-
            82 Item 1 (F_txn.rd_en && ~F_txn.wr_en && ~this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
                 \operatorname{-Focused} Condition View\operatorname{-}
            85 Item 1 (F<sub>txn.wr_en</sub> && F<sub>txn.rd_en</sub> && this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
                 -Focused Condition View-
            88 Item 1 (F<sub>-</sub>txn.wr<sub>-</sub>en && F<sub>-</sub>txn.rd<sub>-</sub>en && this.full<sub>-</sub>ref)
Condition totals: 3 of 3 input terms covered = 100.00\%
                  \hbox{-}Focused \quad Condition \quad View-
                        1 ((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this.wr_ack_ref) && (F_txn.overflow == this.over
Condition totals: 0 of 8 input terms covered = 0.00\%
                                        Input Term Covered Reason for no coverage Hint
                                                                  ^{\prime}_{-0} , not hit
                                                                                              Hit '_0'
         (F_{txn.data_out} = this.data_out_ref)
                                                              Ν
                                                                  '_{-0}, not hit
                                                                                              Hit '_0'
             (F_{txn.wr_{ack}} = this.wr_{ack_{ref}})
                                                              Ν
                                                                  ^{\prime}_{-0} , not hit
                                                                                              Hit '_0'
         (F_txn.overflow === this.overflow_ref)
                                                              Ν
                                                                  , _0 ,
                                                                                              Hit '_0'
       (F_txn.underflow === this.underflow_ref)
                                                              Ν
                                                                       not hit
                                                                                              Hit '_0'
                  (F_{txn.full} = this.full_ref)
                                                                  , _0 ,
                                                              Ν
                                                                       not hit
                                                                  '_{-0}, not hit
               (F_{txn.empty} = this.empty_ref)
                                                                                              Hit '_0'
                                                              Ν
                                                                                              Hit '_0'
                                                                  ^{\prime}_{-0} or not hit
    (F_{txn.almostfull} = this.almostfull_ref)
                                                              Ν
                                                                  ^{\prime}_{-0}, not hit
  (F_{txn.almostempty} = this.almostempty_ref)
                                                              Ν
                                                                                              Hit '_0'
                   Hits FEC Target
                                                                                Non-masking condition(s)
     Rows:
               ***0***
                          (F_{txn.data_out} = this.data_out_ref)_0
  Row
         1:
         2:
  Row
                          (F_{txn.data_out} = this.data_out_ref)_1
                                                                                ((F_{txn.wr_{ack}} = this.wr_{ack_{ref}}) & ((F_{txn.overflow} = this.
         3:
                ***0***
                          (F_{txn.wr_{ack}} = this.wr_{ack_{ref}})_0
                                                                                (F_{txn.data_out} = this.data_out_ref)
  Row
                          (F_{txn.wr_{ack}} = this.wr_{ack_{ref}})_{1}
                                                                                ((F_txn.data_out === this.data_out_ref) && ((F_txn.overflow === t
         4:
  Row
               ***0***
 Row
                          (F_txn.overflow === this.overflow_ref)_0
         5:
                                                                                ((F_{txn.data_out} = this.data_out_ref) && (F_{txn.wr_ack} = this)
 Row
         6:
                         (F_{txn.overflow} = this.overflow_ref)_1
                                                                                ((F_{txn.data_out} = this.data_out_ref) && (F_{txn.wr_ack} = this)
                         (F_txn.underflow === this.underflow_ref)_0
                                                                                ((F_{txn.data_out} = this.data_out_ref) & (F_{txn.wr_ack} = this)
         7:
  Row
```

```
Row
                        (F_{txn.underflow} = this.underflow_ref)_1
                                                                             ((F_{txn.data_out} = this.data_out_ref) & (F_{txn.wr_ack} = this)
 Row
        9:
               ***0***
                        (F_{txn.full} = this.full_ref)_0
                                                                             ((F_txn.data_out === this.data_out_ref) && (F_txn.wr_ack === this
Row
       10:
                     5
                        (F_{txn.full} = this.full_ref)_1
                                                                             ((F_{txn.data_out} = this.data_out_ref) \&\& (F_{txn.wr_ack} = this)
                                                                             ((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row
       11:
               ***0***
                        (F_{txn.empty} = this.empty_ref)_0
                        (F_{txn.empty} = this.empty_ref)_1
                                                                             ((F_{txn.data_out} = this.data_out_ref) & (F_{txn.wr_ack} = this)
Row
       12:
                     5
                        (F_{txn.almostfull} = this.almostfull_ref)_0
                                                                             ((F_{txn.data_out} = this.data_out_ref) && (F_{txn.wr_ack} = this)
Row
       13:
               ***0***
                                                                            ((F_txn.data_out === this.data_out_ref) && (F_txn.wr_ack === this
                        (F_{txn.almostfull} = this.almostfull_ref)_1
Row
       14:
                     5
                        (F_txn.almostempty === this.almostempty_ref)_0
                                                                            ((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row
       15:
               ***0***
                        (F_txn.almostempty === this.almostempty_ref)_1
                                                                            ((F_{txn.data_out} = this.data_out_ref) && (F_{txn.wr_ack} = this)
Row
       16:
                 -Focused Condition View-
           120 Item
                      1 (F_txn.data_out !== this.data_out_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
                                              Covered Reason for no coverage
                                Input Term
                                                                                   \operatorname{Hint}
  (F_txn.data_out !== this.data_out_ref)
                                                                                   Hit ,0, and ,1,
                                                    N No hits
     Rows:
                  _{
m Hits}
                        FEC Target
                                                                      Non-masking condition(s)
        1:
               ***0***
                        (F_txn.data_out !== this.data_out_ref)_0
 Row
               ***0***
                        (F_txn.data_out !== this.data_out_ref)_1
 Row
        2:
                \operatorname{-Focused} Condition View\operatorname{--}
           121 Item 1 (F_{txn.wr_ack}!= this.wr_ack_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00%
                            Input Term
                                          Covered Reason for no coverage
                                                                              Hint
  (F_{txn.wr_{ack}}!== this.wr_{ack_{ref}})
                                                N No hits
                                                                              Hit '_0' and '_1'
                  _{
m Hits}
                       FEC Target
                                                                 Non-masking condition(s)
     Rows:
                        (F_txn.wr_ack !== this.wr_ack_ref)_0
 Row
        1:
               ***0***
  Row
        2:
               ***0***
                        (F_txn.wr_ack !== this.wr_ack_ref)_1
                 \operatorname{-Focused} Condition View\operatorname{--}
           122 Item
                      1 (F_txn.overflow !== this.overflow_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                Input Term
                                              Covered Reason for no coverage
                                                                                   _{
m Hint}
                                                                                   Hit '_{-0}' and '_{-1}'
  (F_txn.overflow !== this.overflow_ref)
                                                    N No hits
     Rows:
                  _{
m Hits}
                        FEC Target
                                                                      Non-masking condition(s)
 Row
        1:
                        (F_txn.overflow !== this.overflow_ref)_0
                        (F_txn.overflow !== this.overflow_ref)_1
 Row
               ***0***
                 Focused Condition View-
           123 Item
                       1 (F_txn.underflow !== this.underflow_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                  Input Term
                                                Covered
                                                          Reason for no coverage
  (F_txn.underflow !== this.underflow_ref)
                                                      N No hits
                                                                                     Hit '_0' and '_1'
     Rows:
                        FEC Target
                                                                        Non-masking condition(s)
                  _{
m Hits}
 Row
        1:
                        (F_txn.underflow !== this.underflow_ref)_0
 Row
        2:
                        (F_txn.underflow !== this.underflow_ref)_1
                 -Focused Condition View-
                        1 (F_{txn.full} !== this.full_ref)
           124 Item
Condition totals: 0 of 1 input term covered = 0.00%
                                     Covered Reason for no coverage
                                                                          _{
m Hint}
  (F_{txn.full} !== this.full_ref)
                                            N No hits
                                                                          Hit '_0' and '_1'
                                                             Non-masking condition(s)
     Rows:
                  Hits FEC Target
                       (F_{txn.full} !== this.full_ref)_0
                        (F_{txn.full} !== this.full_ref)_1 -
  Row
        2:
                \operatorname{-Focused} Condition View\operatorname{-}
           125 Item
Line
                       1 (F_{txn.empty} !== this.empty_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                         Input Term
                                       Covered Reason for no coverage
                                                                            \operatorname{Hint}
                                                                            Hit '_0' and '_1'
  (F<sub>txn</sub>.empty !== this.empty_ref)
                                              N No hits
                  Hits FEC Target
     Rows:
                                                               Non-masking condition(s)
                        (F_txn.empty !== this.empty_ref)_0
 Row
        1:
               ***0***
                        (F_txn.empty !== this.empty_ref)_1
 Row
        2:
               ***0***
                -Focused Condition View-
           126 Item 1 (F_txn.almostfull !== this.almostfull_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
```

```
Covered Reason for no coverage
                                   Input Term
                                                                                    Hint
  (F_txn.almostfull !== this.almostfull_ref)
                                                                                    Hit '_0' and '_1'
                                                      N No hits
                 Hits FEC Target
                                                                       Non-masking condition(s)
    Rows:
 Row
        1:
              ***0***
                       (F_txn.almostfull !== this.almostfull_ref)_0
                       (F_txn.almostfull !== this.almostfull_ref)_1
 Row
        2:
              ***0***
                -Focused Condition View-
          127 Item 1 (F_txn.almostempty !== this.almostempty_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00%
                                     Input Term
                                                  Covered Reason for no coverage
                                                                                      Hint
 (F_txn.almostempty !== this.almostempty_ref)
                                                        N No hits
                                                                                      Hit '_0' and '_1'
                 Hits FEC Target
    Rows:
                                                                         Non-masking condition(s)
 Row
        1:
              ***0***
                       (F_txn.almostempty !== this.almostempty_ref)_0
                       (F_txn.almostempty !== this.almostempty_ref)_1
 Row
        2:
              ***0***
Expression Coverage:
    Enabled Coverage
                                   _{\mathrm{Bins}}
                                          Covered
                                                             Coverage
                                                      _{
m Misses}
                                                               100.00\%
    Expressions
                                      4
                                                           0
                              ==Expression Details
Expression Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv —
               -Focused Expression View-
           95 Item
                    1 \quad (this.count == 0)
Expression totals: 1 of 1 input term covered = 100.00\%
                -Focused Expression View-
           96 Item 1 (this.count == 8)
Expression totals: 1 of 1 input term covered = 100.00%
                -Focused Expression View-
           97 Item 1 (this.count = (8 - 1))
Expression totals: 1 of 1 input term covered = 100.00%
                -Focused Expression View-
           98 Item 1 (this.count == 1)
Expression totals: 1 of 1 input term covered = 100.00%
Statement Coverage:
                                                             Coverage
    Enabled Coverage
                                   Bins
                                             Hits
                                                      _{
m Misses}
    Statements
                                     43
                                               33
                                                          10
                                                                76.74\%
                               ==Statement Details====
Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv —
    28
                    1
                                             5040
    32
                    1
                                              781
    33
                    1
                                              781
    34
                                              781
    35
    36
    37
    38
    39
                                              781
    40
                                              781
    41
                                              781
    43
                                              781
    52
                                              2836
                                              2836
    54
                    1
                                             2836
                                             1423
    56
                    1
    59
                    1
                                              172
    61
                                              1251
                    1
    67
                                              969
                                              969
    68
    72
                                              284
                    1
                                             3006
    74
                    1
                                             2008
    80
                    1
    83
                    1
                                              291
    87
                                              196
                                              46
    90
                                             5040
    95
                                             5040
    96
                                             5040
    97
    98
                                             5040
                    1
```

 $5040 \\ 5040$

0

104

116

118

1

1

```
120
    121
    122
    123
    124
    125
    126
    127
                      1
  = File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv
Branch Coverage:
                                                 Hits
                                                          Misses
    Enabled Coverage
                                      _{\mathrm{Bins}}
                                                                   Coverage
                                         2
    Branches
                                                     1
                                                                1
                                                                      50.00\%
                                   =Branch Details=
Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv —
                                        -IF Branch-
    41
                                                 5000
                                                            Count coming in to IF
                      1
    41
                                              ***0***
                                                 5000
                                                            All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
Statement Coverage:
    Enabled Coverage
                                      _{\mathrm{Bins}}
                                                 _{
m Hits}
                                                           _{
m Misses}
                                                                   Coverage
    Statements
                                                                      90.00\%
                                        30
                                                    27
                                                                3
                                   =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv —
    11
                      1
                                                     5
    14
                      1
    15
                      1
                                                     5
                                                     5
    18
    19
                                                     5
    20
                                                     5
    21
                                                     5
    24
                                                     5
    27
                                                    10
                                                    10
    27
    30
                                                    5
    32
                                                    10
    32
                                                    10
    35
                                                     5
    36
                                                     5
    39
    39
                                                 5000
    42
    43
                                              ***0***
                                                 5000
                                                 5000
    51
                                                 5000
                                                 5000
                                                 5000
                                                 5000
    61
                                                    25
    61
                                                    25
    62
    65
    65
  = File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_top.sv
Statement Coverage:
    Enabled Coverage
                                      _{\mathrm{Bins}}
                                                 Hits
                                                           _{
m Misses}
                                                                   Coverage
                                         4
                                                                0
                                                                    100.00\%
    Statements
                                   =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_top.sv —
                      1
                                                     5
    8
    9
                      1
                                                     5
    9
                      2
                                                10080
                                                10075
Toggle Coverage:
    Enabled Coverage
                                                           Misses Coverage
                                      _{
m Bins}
                                                 _{
m Hits}
                                         2
    Toggles
                                                                0
                                                                    100.00\%
                                   =Toggle Details=
```

Line Node 1H->0L0L—>1H "Coverage" Total Node Count Toggled Node Count 1 Untoggled Node Count = 0 100.00% (2 of 2 bins) Toggle Coverage = File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_transaction_pkg.sv Statement Coverage: $_{\rm Hits}$ Enabled Coverage Bins Misses Coverage 100.00%2 0 Statements =Statement Details= Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_transaction_pkg.sv — 44201 451 20 = File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv Branch Coverage: Enabled Coverage Bins HitsCoverage $_{
m Misses}$ Branches 25250 100.00%=Branch Details= Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv — $\operatorname{-IF}$ Branch-13 5681Count coming in to IF 131 1 18 Branch totals: 3 hits of 3 branches = 100.00%-IF Branch-251418 Count coming in to IF 251 1721246 1 Branch totals: 2 hits of 2 branches = 100.00\% 33 5681Count coming in to IF 33 1 14241 9713286Branch totals: 3 hits of 3 branches = 100.00% $-{
m IF}$ Branch-433286Count coming in to IF 431 Branch totals: 2 hits of 2 branches = 100.00\% -IF Branch— 515306Count coming in to IF 511 1375Branch totals: 2 hits of 2 branches = 100.00% -IF Branch-553931Count coming in to IF 2009 291575946611961389All False Count Branch totals: 5 hits of 5 branches = 100.00\% ----IF Branch 66Count coming in to IF 31411 66 108 2 3033 66Branch totals: 2 hits of 2 branches = 100.00% _____IF Branch___ 67Count coming in to IF 44211 671955672 2466Branch totals: 2 hits of 2 branches = 100.00% -----IF Branch-

```
68
                                               157
    68
                    2
                                              2984
Branch totals: 2 hits of 2 branches = 100.00\%
                                     -IF Branch
    69
                                              3141
                                                        Count coming in to IF
    69
                    1
                                               722
                    ^{2}
                                              2419
    69
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                   _{\mathrm{Bins}}
                                           Covered
                                                       _{\mathrm{Misses}}
                                                               Coverage
    Conditions
                                                            2
                                     25
                                                23
                                                                 92.00\%
                                 =Condition Details=
Condition Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv —
                -Focused Condition View-
           18 Item
Line
                     1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
                -Focused Condition View-
           25 Item
Line
                     1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00\%
                    Covered Reason for no coverage
       Input Term
                                                         Hint
                              ^{\prime}_{-0}, not hit
   fifo_intf.full
                                                         Hit '_0'
                           Ν
  fifo_intf.wr_en
                           Y
                       FEC Target
                                               Non-masking condition(s)
     Rows:
                 _{
m Hits}
                                               fifo_intf.wr_en
 Row
              ***0***
                        fifo_intf.full_0
        1:
                        fifo_intf.full_1
                                               fifo_intf.wr_en
 Row
        2:
                    5
 Row
                        fifo_intf.wr_en_0
                                               fifo_intf.full
        3:
                    5
 Row
                        fifo_intf.wr_en_1
                                               fifo_intf.full
                \operatorname{-Focused} Condition View\operatorname{--}
           38 Item
                    1 (fifo_intf.rd_en && (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
                -Focused Condition View-
                     1 (fifo_intf.empty & fifo_intf.rd_en)
Line
           43 Item
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                    Covered Reason for no coverage
                                                         _{
m Hint}
  fifo_intf.empty
                              '_0 not hit
                                                         Hit '_0'
  fifo_intf.rd_en
                           Y
                      FEC Target
                                               Non-masking condition(s)
     Rows:
                 _{
m Hits}
                                               fifo_intf.rd_en
 Row
        1:
                        fifo_intf.empty_0
                        fifo_intf.empty_1
                                               fifo_intf.rd_en
 Row
 Row
                        fifo_intf.rd_en_0
                                               fifo_intf.empty
 Row
                        fifo_intf.rd_{en_1}
                                               fifo_intf.empty
                -Focused Condition View-
                     1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
                -Focused Condition View-
Line
                      1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
                Focused Condition View—
Line
                     1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
                -Focused Condition View-
           61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
                -Focused Condition View-
           66 Item 1 (count == 8)
Line
Condition totals: 1 of 1 input term covered = 100.00%
                -Focused Condition View-
           67 Item 1 ((count == 0) || \tilde{fifo_intf.rst_n})
Condition totals: 2 of 2 input terms covered = 100.00%
               -Focused Condition View-
           68 Item 1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
                -Focused Condition View----
           69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00\%
```

3141

Count coming in to IF

68

Statement	Coverage:
Duatement	Coverage.

Enabled Coverage	Bins	Hits	Misses	${\bf Coverage}$
Statements	28	28	0	100.00%

Statement Details

Toggles		20	20	0	100.00%
gle Covera Enabled (ige: Coverage	Bins	Hits	Misses	Coverage
69	1		3146		
68	1		3146		
7	1		4426		
66	1		3146		
2	1		196		
0	1		46		
8	1		291		
i	1		2009		
2	1		1375		
)	1		5306		
6	1		3002		
4	1		284		
0.	1		971		
9	1		971		
6	1		1424		
5	1		1424		
4	1		1424		
32	1		5681		
8	1		1246		
26	1		172		
24	1		1418		
21	1		2839		
20	1		2839		
19	1		2839		
16	1		1424		
15	1		1424		
12 14	1 1		$5681 \\ 1424$		

0L—>1H "Coverage" Line Node1H -> 0L

Total Node Count 10 Toggled Node Count = 10 ${\rm Untoggled\ Node\ Count}\,=\,$

100.00% (20 of 20 bins) Toggle Coverage

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100		Covered
covered/total bins:	194	194	_	
missing/total bins:	0	194	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	781	1	_	Covered
bin auto [1]	4259	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	95	1	_	Covered
bin auto [1024:2047]	74	1	_	Covered
bin auto [2048:3071]	72	1	_	Covered
bin auto [3072:4095]	72	1	_	Covered
bin auto [4096:5119]	84	1	_	Covered
bin auto [5120:6143]	71	1	_	Covered
bin auto [6144:7167]	70	1	_	Covered
bin auto [7168:8191]	88	1	_	Covered
bin auto [8192:9215]	82	1	_	Covered
bin auto [9216:10239]	71	1	_	Covered
bin auto [10240:11263]	75	1	_	Covered
bin auto [11264:12287]	78	1	_	Covered
bin auto [12288:13311]	76	1	_	Covered
bin auto [13312:14335]	71	1	_	Covered
bin auto [14336:15359]	77	1	_	Covered
bin auto [15360:16383]	85	1	_	Covered

bin auto [16384:17407]				
bin auto[10304.17407]	89	1	_	Covered
bin auto[17408:18431]	84	1	_	Covered
bin auto [18432:19455]	74	1	_	Covered
bin auto [19456:20479]	90	1	_	Covered
bin auto [20480:21503]	76	1	_	Covered
bin auto $[21504:22527]$				
	79	1	_	Covered
bin auto [22528:23551]	68	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[23552 \colon\! 24575 \right]$	80	1	_	Covered
bin auto $[24576:25599]$	75	1	_	Covered
bin auto $[25600:26623]$	82	1	_	$\operatorname{Covered}$
bin auto [26624:27647]	78	1	_	Covered
bin auto [27648:28671]	79	1	_	Covered
bin auto [28672:29695]	79	1	_	Covered
bin auto [29696:30719]	79	1	_	Covered
bin auto [30720:31743]	73	1		Covered
· ·			_	
bin auto [31744:32767]	84	1	_	Covered
bin auto $[32768:33791]$	68	1	_	Covered
bin auto $[33792:34815]$	80	1	_	$\operatorname{Covered}$
bin auto [34816:35839]	81	1	_	$\operatorname{Covered}$
bin auto [35840:36863]	67	1	_	Covered
bin auto [36864:37887]	71	1	_	Covered
bin auto [37888:38911]	69	1	_	Covered
bin auto [38912:39935]	87	1	_	Covered
bin auto [39936:40959]	83	1	_	Covered
bin auto [40960:41983]	70	1	_	Covered
bin auto [41984:43007]	87	1	_	Covered
bin auto [43008:44031]	92	1	_	Covered
bin auto $[44032:45055]$	65	1	_	Covered
bin auto $[45056:46079]$	89	1	_	Covered
bin auto $[46080:47103]$	72	1	_	Covered
bin auto [47104:48127]	71	1	_	Covered
bin auto [48128:49151]	82	1	_	Covered
bin auto [49152:50175]	73	1	_	Covered
bin auto [50176:51199]	74	1	_	Covered
	90			Covered
bin auto [51200:52223]		1	_	
bin auto $[52224:53247]$	90	1	_	Covered
$bin auto \left[53248 \colon\! 54271\right]$	74	1	_	Covered
bin auto $[54272:55295]$	85	1	_	$\operatorname{Covered}$
bin auto $[55296:56319]$	82	1	_	$\operatorname{Covered}$
bin auto [56320:57343]	83	1	_	Covered
bin auto [57344:58367]	87	1	_	Covered
bin auto [58368:59391]	80	1	_	Covered
bin auto [59392:60415]	81	1	_	Covered
bin auto [60416:61439]	82	1	_	Covered
	80	1		Covered
bin auto [61440:62463]		1	_	
bin auto [62464:63487]	78	1	_	$\widehat{\text{Covered}}$
$\operatorname{bin} \ \operatorname{auto} \left[63488 \!:\! 64511 \right]$	80	1	_	Covered
bin auto $[64512:65535]$	78	1	_	$\operatorname{Covered}$
Coverpoint r_en_cp	100.00%	100	_	Covered
	100.00%	$\frac{100}{2}$	_	Covered
covered/total bins:			_ _ _	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins:</pre>	$\frac{2}{0}$	$\frac{2}{2}$	_ _ _ _	Covered
<pre>covered/total bins: missing/total bins: % Hit:</pre>	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \end{array}$	$\begin{matrix}2\\2\\100\end{matrix}$	_ _ _ _	
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0]</pre>	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \\ 3544 \end{array}$	$\begin{matrix}2\\2\\100\\1\end{matrix}$	_ _ _	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \end{array}$	_ _ _	Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp</pre>	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \\ 3544 \\ 1496 \\ 100.00\% \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \end{array}$	_ _ _	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins:</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \end{array}$	_ _ _	Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins:</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\end{array}$	$ \begin{array}{c} 2\\ 2\\ 100\\ 1\\ 1\\ 100\\ 2\\ 2 \end{array} $	_ _ _	Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit:</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\\100.00\%\end{array}$	$ \begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \end{array} $	_ _ _	Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0]</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517 \end{array}$	$ \begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $	_ _ _	Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \end{array}$	_ _ _	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0]</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517 \end{array}$	$ \begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $	_ _ _	Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \end{array}$	_ _ _	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins:</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\\100.00\%\\1517\\3523\\100.00\%\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ \end{array}$	_ _ _	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\\100.00\%\\1517\\3523\\100.00\%\\64\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \end{array}$	_ _ _	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit:</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\% \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 64 \end{array}$	_ _ _	Covered Covered Covered Covered
<pre>covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023]</pre>	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\\100.00\%\\1517\\3523\\100.00\%\\64\\0\\100.00\%\\2622\\\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \end{array}$	_ _ _	Covered Covered Covered Covered Covered Covered
covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	$\begin{array}{c} 2\\0\\100.00\%\\3544\\1496\\100.00\%\\2\\0\\100.00\%\\1517\\3523\\100.00\%\\64\\0\\100.00\%\\2622\\20\end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \end{array}$		Covered Covered Covered Covered Covered Covered Covered
covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 100.00\%\\ \\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \end{array}$		Covered Covered Covered Covered Covered Covered Covered Covered Covered
covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: bin auto[0:1023] bin auto[0:1024:2047] bin auto[2048:3071] bin auto[3072:4095]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 100.00\%\\ \\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29 \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$		Covered
covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[0:1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 100.00\%\\ \\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ \\ 20\\ 47\\ 29\\ 34\\ \end{array}$	$\begin{array}{c} 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 2 \\ 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$		Covered
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covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [2048:3071] bin auto [4096:5119] bin auto [4096:5119] bin auto [5120:6143] bin auto [7168:8191] bin auto [7168:8191] bin auto [8192:9215] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [1436:15359] bin auto [14384:17407] bin auto [18432:19455] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [21504:22527] bin auto [22528:23551]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 60\\ 54\\ 28\\ 29\\ 66\\ 63\\ 3\\ 3\\ 46\\ 38\\ 39\\ 60\\ 43\\ 28\\ 48\\ 50\\ 13\\ \end{array}$	2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [2048:3071] bin auto [4096:5119] bin auto [4096:5119] bin auto [5120:6143] bin auto [7168:8191] bin auto [7168:8191] bin auto [8192:9215] bin auto [10240:11263] bin auto [10240:11263] bin auto [12288:13311] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [1436:15359] bin auto [14384:17407] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 100.00\%\\ \\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 33\\ 46\\ 38\\ 39\\ 60\\ 43\\ 28\\ 48\\ 50\\ 13\\ 28\\ 48\\ 50\\ 13\\ 23\\ 31\\ \end{array}$	2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [3072:4095] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [7168:8191] bin auto [1228:1331] bin auto [12240:11263] bin auto [12288:13311] bin auto [12288:13311] bin auto [13312:14335] bin auto [1336:15359] bin auto [14336:15359] bin auto [14336:15359] bin auto [14336:15359] bin auto [14336:15359] bin auto [14384:17407] bin auto [14382:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [23552:24575] bin auto [24576:25599]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ \\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 63\\ 3\\ 3\\ 46\\ 38\\ 39\\ 60\\ 43\\ 28\\ 48\\ 50\\ 13\\ 28\\ 48\\ 50\\ 13\\ 23\\ 31\\ 26\\ \end{array}$	2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [3072:4095] bin auto [3072:4095] bin auto [4096:5119] bin auto [4120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [7168:8191] bin auto [10240:11263] bin auto [10240:11263] bin auto [10240:11263] bin auto [12288:13311] bin auto [13312:14335] bin auto [1336:15359] bin auto [14336:15359] bin auto [14336:15359] bin auto [1448:18431] bin auto [1448:18431] bin auto [19456:20479] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23555] bin auto [24576:25599] bin auto [24576:25599] bin auto [24576:25599] bin auto [25600:26623]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 63\\ 33\\ 46\\ 38\\ 39\\ 60\\ 43\\ 28\\ 48\\ 50\\ 13\\ 23\\ 31\\ 26\\ 41\\ \end{array}$	2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [3072:4095] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [7168:8191] bin auto [1226:10239] bin auto [12240:11263] bin auto [12288:13311] bin auto [12288:13311] bin auto [14336:15359] bin auto [14336:16383] bin auto [16384:17407] bin auto [16384:17407] bin auto [18432:19455] bin auto [19456:20479] bin auto [25228:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23555] bin auto [22528:23555] bin auto [24576:25599] bin auto [25600:26623] bin auto [26624:27647]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 60\\ 54\\ 28\\ 29\\ 66\\ 60\\ 54\\ 28\\ 29\\ 66\\ 60\\ 33\\ 46\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 38\\ 39\\ 60\\ 43\\ 33\\ 28\\ 48\\ 50\\ 13\\ 28\\ 48\\ 50\\ 13\\ 28\\ 48\\ 50\\ 13\\ 29\\ 31\\ 48\\ 33\\ 32\\ 46\\ 48\\ 33\\ 39\\ 60\\ 43\\ 33\\ 32\\ 46\\ 48\\ 33\\ 39\\ 60\\ 43\\ 33\\ 39\\ 60\\ 43\\ 33\\ 39\\ 60\\ 43\\ 33\\ 39\\ 60\\ 43\\ 33\\ 39\\ 60\\ 44\\ 33\\ 39\\ 60\\ 44\\ 33\\ 39\\ 60\\ 44\\ 33\\ 39\\ 60\\ 43\\ 39\\ 48\\ 48\\ 50\\ 48\\ 48\\ 48\\ 50\\ 48\\ 48\\ 48\\ 50\\ 48\\ 48\\ 48\\ 50\\ 48\\ 48\\ 48\\ 48\\ 50\\ 48\\ 48\\ 48\\ 48\\ 48\\ 48\\ 48\\ 48\\ 48\\ 48$	2 2 100 1 1 100 2 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [0:1023] bin auto [1024:2047] bin auto [3072:4095] bin auto [3072:4095] bin auto [4096:5119] bin auto [4120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [7168:8191] bin auto [10240:11263] bin auto [10240:11263] bin auto [10240:11263] bin auto [12288:13311] bin auto [13312:14335] bin auto [1336:15359] bin auto [14336:15359] bin auto [14336:15359] bin auto [1448:18431] bin auto [1448:18431] bin auto [19456:20479] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23555] bin auto [24576:25599] bin auto [24576:25599] bin auto [24576:25599] bin auto [25600:26623]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 3544\\ 1496\\ 100.00\%\\ 2\\ 0\\ 100.00\%\\ 1517\\ 3523\\ 100.00\%\\ 64\\ 0\\ 100.00\%\\ 2622\\ 20\\ 47\\ 29\\ 34\\ 33\\ 56\\ 60\\ 54\\ 28\\ 29\\ 66\\ 63\\ 33\\ 46\\ 38\\ 39\\ 60\\ 43\\ 28\\ 48\\ 50\\ 13\\ 23\\ 31\\ 26\\ 41\\ \end{array}$	2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

	. ~			~ ·
bin auto [28672:29695]	45	1	_	Covered
bin auto [29696:30719]	26	1	_	Covered
bin auto $[30720:31743]$	32	1	_	Covered
bin auto [31744:32767]	40	1	_	Covered
bin auto [32768:33791]	28	1	_	Covered
bin auto [33792:34815]	46	1	_	Covered
bin auto [34816:35839]	50	1	_	Covered
bin auto [35840:36863]	22	1	_	Covered
bin auto [36864:37887]	35	1	_	Covered
bin auto [37888:38911]	38	1	_	Covered
bin auto [38912:39935]	41	1	_	Covered
bin auto [39936:40959]	39	1	_	Covered
bin auto [40960:41983]	$\frac{35}{26}$	1	_	Covered
bin auto [41984:43007]	54	1		Covered
bin auto [41304:43007] bin auto [43008:44031]	65	1	_	Covered
	41	1	_	
bin auto [44032:45055]			_	Covered
bin auto [45056:46079]	23	1	_	Covered
bin auto [46080:47103]	27	1	_	Covered
bin auto $[47104:48127]$	34	1	_	Covered
bin auto [48128:49151]	35	1	_	Covered
bin auto $[49152:50175]$	40	1	_	Covered
bin auto $[50176:51199]$	27	1	_	Covered
bin auto $[51200:52223]$	58	1	_	Covered
bin auto $[52224:53247]$	59	1	_	Covered
bin auto [53248:54271]	34	1	_	Covered
bin auto [54272:55295]	42	1	_	Covered
bin auto [55296:56319]	28	1	_	Covered
bin auto [56320:57343]	69	1	_	Covered
bin auto [57344:58367]	46	1	_	Covered
bin auto [58368:59391]	$\frac{10}{29}$	1	_	Covered
bin auto [59392:60415]	18	1	_	Covered
,				
bin auto [60416:61439]	29	1	_	Covered
bin auto [61440:62463]	40	1	_	Covered
bin auto [62464:63487]	22	1	_	Covered
bin auto $[63488:64511]$	40	1	_	Covered
${ m bin \ auto} [64512\!:\!65535]$	43	1	_	$\operatorname{Covered}$
Coverpoint wr_ack_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	2204	1	_	Covered
bin auto [1]	2836	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	00.0104
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100		
	4811		_	Covered
bin auto [0]		1	_	
bin auto[1]	229	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	4756	1	_	$\operatorname{Covered}$
bin auto [1]	284	1	_	$\operatorname{Covered}$
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	3900	1	_	Covered
bin auto[1]	1140	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	4780	1	_	Covered
bin auto[1]	260	1		Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	100.0070	2		Covered
·	0	$\frac{2}{2}$	_	
missing/total bins:		_	_	
% Hit:	$100.00\% \ 3943$	100 1	_	Covered
bin auto [0]			_	
bin auto[1]	1097	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins:		٠)	_	
% Hit:	0	2		
	100.00%	100	_	
bin auto[0]	$100.00\%\ 4700$	100 1	_	Covered
$egin{array}{ll} ext{bin auto} \left[0 ight] \ ext{bin auto} \left[1 ight] \end{array}$	$100.00\%\ 4700\ 340$	100 1 1	_ _ _	Covered
bin auto [0] bin auto [1] Cross wr_ack_cross	$100.00\% \ 4700 \ 340 \ 100.00\%$	$100 \\ 1 \\ 1 \\ 100$	_ _ _ _	
bin auto [0] bin auto [1] Cross wr_ack_cross covered/total bins:	$100.00\%\ 4700\ 340$	100 1 1	- - - -	Covered
bin auto [0] bin auto [1] Cross wr_ack_cross	$100.00\% \ 4700 \ 340 \ 100.00\%$	$100 \\ 1 \\ 1 \\ 100$	_ _ _ _ _	Covered
bin auto [0] bin auto [1] Cross wr_ack_cross covered/total bins:	$100.00\% \ 4700 \ 340 \ 100.00\% \ 6$	$100 \\ 1 \\ 1 \\ 100 \\ 6$	_ _ _ _ _	Covered
bin auto [0] bin auto [1] Cross wr_ack_cross covered/total bins: missing/total bins:	$100.00\% \ 4700 \ 340 \ 100.00\% \ 6 \ 0$	100 1 1 100 6 6		Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit:</pre>	$100.00\% \ 4700 \ 340 \ 100.00\% \ 6 \ 0$	100 1 1 100 6 6		Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], ,="" auto[1]=""></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$	100 1 1 100 6 6 100	- - - - - -	Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211	$ \begin{array}{c} 100 \\ 1 \\ 100 \\ 6 \\ 6 \\ 100 \\ \end{array} $	- - - - - -	Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008	100 1 1 100 6 6 100 1 1	- - - - - -	Covered Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476	100 1 1 100 6 6 100 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476 457	100 1 1 100 6 6 100 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476	100 1 1 100 6 6 100 1 1 1	- - - - - - - -	Covered Covered Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476 457 1060	100 1 1 100 6 6 100 1 1 1 1	- - - - - - - - -	Covered Covered Covered Covered Covered Covered Covered
bin auto [0] bin auto [1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto [1]="" [1],="" auto=""> bin <auto [0]="" [1],="" auto=""> bin <auto [0]="" [0],="" [1],="" auto=""> bin <auto [0]="" [0],="" [1],="" auto=""> bin <auto [0]="" [0],="" auto=""> bin <auto [0]="" [0],="" auto=""> lin <auto [0]="" [0],="" auto=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto></auto></auto></auto></auto></auto></auto>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476 457 1060	100 1 1 100 6 6 100 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered
<pre>bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></pre>	100.00% 4700 340 $100.00%$ 6 0 $100.00%$ 828 211 2008 476 457 1060	100 1 1 100 6 6 100 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered

covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
	234	1		Command
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$		1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0]$, $\operatorname{auto} [0]$, $\operatorname{auto} [1] >$	50	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	1039	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	457	1	_	Covered
bin < auto[0], auto[1], auto[0] >	2250	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	1010	1	_	Covered
Illegal and Ignore Bins:	1010	1		Covered
	0			ZEDO
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	200100,0	_ 0 0		
bin <auto[1], auto[1]=""></auto[1],>	165	1		Covered
		1	_	
$\operatorname{bin} < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight] >$	242	1	_	Covered
$\operatorname{bin} < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight] >$	874	1	_	$\operatorname{Covered}$
bin < auto[0], auto[1], auto[0] >	2134	1	_	$\operatorname{Covered}$
bin < auto[1], auto[0], auto[0] >	215	1	_	Covered
bin < auto[0], auto[0], auto[0] >	677	1	_	Covered
Illegal and Ignore Bins:	011	-		00,0104
	722			0 1
ignore_bin read_nactv_empty	733		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
	1.07	1		C 1
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] >$	107	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0],\mathrm{auto}[1],\mathrm{auto}[1]>$	89	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[1] >$	22	1	_	$\operatorname{Covered}$
bin < auto[0], auto[0], auto[1] >	42	1	_	Covered
bin < auto[1], auto[1], auto[0] >	932	1	_	Covered
bin $\langle auto[1], auto[1], auto[0] \rangle$	2395	1		Covered
			_	
$\verb bin < \verb auto[1] , \verb auto[0] , \verb auto[0] >$	435	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0],\mathrm{auto}[0],\mathrm{auto}[0]>$	1018	1	_	Covered
Cross almostempty_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	8	8	_	
missing/total bins:	0	8	_	
% Hit:	100.00%	100		
	100.0070	100	_	
Auto, Default and User Defined Bins:				~ .
$\mathrm{bin}\ <\!\mathrm{auto}[1],\mathrm{auto}[1],\mathrm{auto}[1]>$	384	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight] >$	477	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[1] >$	49	1	_	Covered
bin < auto[0], auto[0], auto[1] >	187	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	655	1	_	Covered
bin $\langle auto[1], auto[1], auto[0] \rangle$	2007	1		Covered
		_		
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	408	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] >$	873	1	_	Covered
Cross overflow_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	6	6	_	
missing / total bins:	0	6	_	
% Hit:	100.00%	100	_	
	100.0070	100		
Auto, Default and User Defined Bins:		1		0 1
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] >$	75	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] \! > \\$	964	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[1], \operatorname{auto}[1] >$			_	$\operatorname{Covered}$
bin < auto[0], auto[1], auto[0] >	154	1		~ 1
auvo+o+, $auvo+o+$, $auvo+o+$	154	1 1	_	Covered
	$\begin{array}{c} 154 \\ 2330 \end{array}$	1	_	Covered Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	$154 \\ 2330 \\ 457$	1 1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\begin{array}{c} 154 \\ 2330 \end{array}$	1	_ _ _	
$\begin{array}{c} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Illegal and Ignore Bins:} \end{array}$	$154 \\ 2330 \\ 457 \\ 1060$	1 1	_ _ _	Covered Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[1],></pre>	154 2330 457 1060	1 1	_ _ _	Covered Covered ZERO
$\begin{array}{c} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Illegal and Ignore Bins:} \end{array}$	$154 \\ 2330 \\ 457 \\ 1060$	1 1	_ _ _ _	Covered Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[1],></pre>	154 2330 457 1060	1 1 1	_ _ _ _ _	Covered Covered ZERO
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins:</auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$	1 1 1	- - - - -	Covered Covered ZERO
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins:</auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0	1 1 1 100 6 6	- - - - -	Covered Covered ZERO
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit:</auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6	1 1 1 100 6	- - - - - -	Covered Covered ZERO
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$	1 1 1 100 6 6 100	- - - - - -	Covered Covered ZERO Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$	1 1 1 100 6 6	- - - - - -	Covered ZERO Covered Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$	1 1 1 100 6 6 100	- - - - - - -	Covered Covered ZERO Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109	1 1 1 100 6 6 100	- - - - - - -	Covered ZERO Covered Covered
<pre>bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[1],></pre>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808	1 1 1 1 100 6 6 100	- - - - - - -	Covered ZERO Covered Covered Covered Covered
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484	1 1 1 1 1 1 0 6 6 100	- - - - - - - - -	Covered Covered Covered Covered Covered Covered Covered
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484 348	1 1 1 1 1 1 0 6 6 6 100		Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], aut<="" auto[0],="" td=""><td>154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484</td><td>1 1 1 1 1 1 0 6 6 100</td><td></td><td>Covered Covered Covered Covered Covered Covered Covered</td></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484	1 1 1 1 1 1 0 6 6 100		Covered Covered Covered Covered Covered Covered Covered
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484 348 1060	1 1 1 1 1 1 0 6 6 6 100		Covered
bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], aut<="" auto[0],="" td=""><td>154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484 348</td><td>1 1 1 1 1 1 0 6 6 6 100</td><td></td><td>Covered Covered Covered Covered Covered Covered Covered Covered Covered</td></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],>	154 2330 457 1060 0 $100.00%$ 6 0 $100.00%$ 231 109 808 2484 348	1 1 1 1 1 1 0 6 6 6 100		Covered Covered Covered Covered Covered Covered Covered Covered Covered

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	0	File (Line)	Hits Status
/FIFO_top/dut/covercounter_threshold	FIFO	Verilog	SVA		op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169) 4262 Covered
/FIFO_top/dut/cover_read_ptr_threshold	FIFO	Verilog	SVA	, , ,	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168) 4262 Covered
/FIFO_top/dut/cover_write_ptr_threshold	FIFO	Verilog	SVA	, ,	op/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167) 4262 Covered

$/ {\rm FIFO_top/dut/cover_read_ptr_wraparound}$	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166) 10 Covered
/FIFO_top/dut/cover_write_ptr_wraparoun	d			
	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165) 111 Covered
/FIFO_top/dut/coveralmost_empty_check	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)\\900~Covered$
/FIFO_top/dut/coveralmost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163) 230 Covered
/FIFO_top/dut/coverfull_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162) 244 Covered
/FIFO_top/dut/coverempty_flag_check	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)\\956~Covered$
/FIFO_top/dut/coverunderflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160) 245 Covered
/FIFO_top/dut/coveroverflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159) 108 Covered
/FIFO_top/dut/coverwrite_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158) 2398 Covered
/FIFO_top/dut/coverreset_behavior	FIFO	Verilog	SVA	$/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)\\ 781~Covered$

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

Name	File (Line)	$\begin{array}{c} {\rm Failure} \\ {\rm Count} \end{array}$	$\begin{array}{c} {\rm Pass} \\ {\rm Count} \end{array}$	
/FIFO_top/dut	/assertcounter_threshold			
1 /	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica		(1
/FIFO top/dut	/assert_read_ptr_threshold	Ü	5	
/ 1 11 O _0 O P / d d 0	/home/tare/Desktop/s		·	(1
/FIFO top/dut	/assert_write_ptr_threshold	0	5	
/ 1 11 O _ 10 p / u u t	/home/tare/Desktop/s	yn_fifo/sv_verifica	tion/FIFO_v1.0.0.sv	(1
/FIFO_top/dut	/assert_read_ptr_wraparound	O	· ·	
,	/home/tare/Desktop/s	yn_fifo/sv_verifica	$tion/FIFO_v1.0.0.sv$	(1
/FIFO_top/dut	/assert_write_ptr_wraparoun	d	· ·	
,	/home/tare/Desktop/s		$tion/FIFO_v1.0.0.sv$	(1
/FIFO_top/dut	/assert_almost_empty_check			
	/home/tare/Desktop/s	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
$/\mathrm{FIFO}_{-\mathrm{top}}/\mathrm{dut}$	/assertalmost_full_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
$/\mathrm{FIFO_top}/\mathrm{dut}$	/assertfull_flag_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
$/\mathrm{FIFO_top}/\mathrm{dut}$	/assertempty_flag_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
/FIFO_top/dut	/assert_underflow_check		/FIFO 1 0 0	/ 4
	/home/tare/Desktop/s	yn_fifo/sv_verifica 0	5 tion/FIFO_v1.0.0.sv	(1
$/{ m FIFO_top/dut}$	/assertoverflow_check			
	/home/tare/Desktop/s	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
/FIFO_top/dut	/assertwrite_ack_check			
	$/\mathrm{home}/\mathrm{tare}/\mathrm{Desktop}/\mathrm{s}$	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1
/FIFO_top/dut	/assertreset_behavior			,
	/home/tare/Desktop/s	yn_fifo/sv_verifica 0	$tion/FIFO_v1.0.0.sv$	(1

Total Coverage By File (code coverage only, filtered view): 85.76%