SV Project

Digital Design Verification

Name: Mohamed Ahmed Sayed Ahmed

Contents

List of Tables 1

List of Figures 1

1 Synchronous FIFO 2
- 1.1 Shared package . . . 2
- 1.2 Top Module . . . 2
- 1.3 Transaction Package . . . 2
- 1.4 Coverage Package . . . 3
- 1.5 scoreboard Package . . . 3
- 1.6 Monitor Package . . . 5
- 1.7 Testbench . . . 6
- 1.8 Design With Bugs + SVA . . . 6
- 1.9 Corrected Design + SVA . . . 8

2 Bugs report 10

3 Makefile Contain Do File 10

4 Functional Coverage Report 11
- 4.1 Functional Coverage "seed1" Report . . . 11
- 4.2 Functional Coverage "seed2" Report . . . 18
- 4.3 Functional Coverage "seed3" Report . . . 25
- 4.4 Functional Coverage "seed4" Report . . . 31
- 4.5 Functional Coverage "seed5" Report . . . 38

5 Code Coverage Report 45
- 5.1 Code Coverage "seed1" Report . . . 45
- 5.2 Code Coverage "seed2" Report . . . 51
- 5.3 Code Coverage "seed3" Report . . . 57
- 5.4 Code Coverage "seed4" Report . . . 63
- 5.5 Code Coverage "seed5" Report . . . 69

6 Waveform 76
- 6.1 Waveform & Transcript "seed1" Report . . . 76
- 6.2 Waveform & Transcript "seed2" Report . . . 76
- 6.3 Waveform & Transcript "seed3" Report . . . 77
- 6.4 Waveform & Transcript "seed4" Report . . . 78
- 6.5 Waveform & Transcript "seed5" Report . . . 79

7 Merged Coverage 80
- 7.1 Functional Coverage "Merged" Report . . . 81
- 7.2 Code Coverage "Merged" Report . . . 87
- 7.3 Coverage "Merged" Report . . . 93

List of Tables

1 Bugs report . . . 10

List of Figures

1 SVA "Seed1" . . . 18
2 SVA "Seed2" . . . 24
3 SVA "Seed3" . . . 31
4 SVA "Seed4" . . . 38
5 SVA "Seed5" . . . 45
6 simulation waveform "seed1" . . . 76
7 Transcript : all test cases passed "seed1" . . . 76
8 simulation waveform "seed2" . . . 76
9 Transcript : all test cases passed "seed2" . . . 77
10 simulation waveform "seed3" . . . 77
11 Transcript : all test cases passed "seed3" . . . 78
12 simulation waveform "seed4" . . . 78
13 Transcript : all test cases passed "seed4" . . . 79
14 simulation waveform "seed5" . . . 79
15 Transcript : all test cases passed "seed5" . . . 80
16 Merge seed . . . 80
17 generated files *.ucdb . . . 80

1 Synchronous FIFO

1.1 Shared package

```
package Shared_pkg;
    // ===== Global parameter for Signal Declaration =====
    parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 8;

    // ===== Signals For Test Control ======
    // ===== #No of Randomization ======
    parameter TEST_COUNT = 1000;
    // ===== Counter For Failed and Successed Test Transactions ======
    int unsigned error_count = 0;
    int unsigned correct_count = 0;
    // ===== When eq 1 Trim Test =====
    bit test_finished = 0;
endpackage
```

1.2 Top Module

```
import Shared_pkg::*;

module FIFO_top;

    // ====== Generate Clock ======
    bit clk;
    initial begin
        clk = 0;
        forever #5 clk = ~clk;  // 200 MHZ
    end

    // ====== interface instance ======
    FIFO_IF fifo_intf (clk);

    // ====== Instantiate DUT ======
    FIFO #(
        .FIFO_WIDTH(FIFO_WIDTH),
        .FIFO_DEPTH(FIFO_DEPTH)
    ) dut (
        .fifo_intf(fifo_intf)
    );

    // ====== Instantiate testbench ======
    FIFO_tb tb (
        .fifo_intf(fifo_intf)
    );

    // ====== Instantiate monitor ======
    FIFO_monitor mon
    (
        .fifo_intf(fifo_intf)
    );

endmodule
```

1.3 Transaction Package

```
package FIFO_transaction_pkg;

import Shared_pkg::*;

class FIFO_transaction;

    // ====================================================
    // Transaction Distribution "Set to Default Values"
    // Variable For parametrized Class "Class Signature"
    // ====================================================
    int RD_EN_ON_DIST;
    int WR_EN_ON_DIST;

    // ==== input signals ====
    rand bit rst_n;
    rand bit [FIFO_WIDTH-1:0] data_in;
    rand bit wr_en;
    rand bit rd_en;

    // ==== output signals ====
    bit [FIFO_WIDTH-1:0] data_out;
    bit wr_ack, overflow;
    bit full, empty, almostfull, almostempty, underflow;

        // ====================================================
    // Dassert Reset "Asyn - Active Low" most of the times
    // ====================================================
        constraint rst_c { rst_n dist {0:/15 , 1:/85};}

    // ========================================================
    // Only, Enable Write Enable Signal During "WR_EN_ON_DIST"
    // ========================================================
    constraint wr_en_c { wr_en dist {1 := WR_EN_ON_DIST, 0 := 100-WR_EN_ON_DIST};}

    // ========================================================
    // Only, Enable Read Enable Signal During "RD_EN_ON_DIST"
    // ========================================================
    constraint rd_en_c { rd_en dist {1 := RD_EN_ON_DIST, 0 := 100-RD_EN_ON_DIST};}

    // ==================
```

```
    // Class Constructor
    // ==================
    function new (int rd_dist = 30 ,int wr_dist = 70);
        RD_EN_ON_DIST = rd_dist;
        WR_EN_ON_DIST = wr_dist;
    endfunction

endclass
endpackage
```

1.4 Coverage Package

```
package FIFO_coverage_pkg;

import FIFO_transaction_pkg::*;
import Shared_pkg::*;

class FIFO_coverage;

    // ===== create object =======
    FIFO_transaction F_cvg_txn;

        // ===== Cover Group =====
    covergroup fifo_cg;

        // ====== Cover I/O Ports ======
        rst_n_cp:   coverpoint F_cvg_txn.rst_n;
        data_in_cp:     coverpoint F_cvg_txn.data_in;
        r_en_cp:    coverpoint F_cvg_txn.rd_en;
        w_en_cp:    coverpoint F_cvg_txn.wr_en;
        data_out_cp:    coverpoint F_cvg_txn.data_out;
        wr_ack_cp:      coverpoint F_cvg_txn.wr_ack;
        overflow_cp:    coverpoint F_cvg_txn.overflow;
        full_cp:    coverpoint F_cvg_txn.full;
        empty_cp:       coverpoint F_cvg_txn.empty;
        almostfull_cp:  coverpoint F_cvg_txn.almostfull;
        almostempty_cp: coverpoint F_cvg_txn.almostempty;
        underflow_cp:   coverpoint F_cvg_txn.underflow;


        // ====== "7" Cross Coverage ======
        wr_ack_cross:     cross r_en_cp ,w_en_cp ,wr_ack_cp{
            ignore_bins w_en_nactv_wr_ack        = binsof(w_en_cp) intersect {1'b0} && binsof(wr_ack_cp) intersect {1'b1};
        }
        full_cross:        cross r_en_cp ,w_en_cp ,full_cp{
            // full not asserted when both read and write enabled
            ignore_bins w_en_r_en_allactv_full   = binsof(w_en_cp) intersect {1'b1} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
                intersect {1'b1};
            // full not asserted when read enabled
            ignore_bins r_en_actv_wr_full        = binsof(w_en_cp) intersect {1'b0} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
                intersect {1'b1};
        }

        empty_cross:       cross r_en_cp ,w_en_cp ,empty_cp{
            ignore_bins read_nactv_empty         = binsof(r_en_cp) intersect {1'b0} && binsof(empty_cp) intersect {1'b1};
        }

        almostfull_cross:  cross r_en_cp ,w_en_cp ,almostfull_cp;

        almostempty_cross: cross r_en_cp ,w_en_cp ,almostempty_cp;


        overflow_cross:    cross r_en_cp ,w_en_cp ,overflow_cp{
            ignore_bins w_en_nactv_wr_ack        = binsof(w_en_cp) intersect {1'b0} && binsof(overflow_cp) intersect {1'b1};
        }

        underflow_cross:   cross r_en_cp ,w_en_cp ,underflow_cp{
            ignore_bins r_en_nactv_wr_ack        = binsof(r_en_cp) intersect {1'b0} && binsof(underflow_cp) intersect {1'b1};
        }

    endgroup

    // ====== Constructor ======
    function new();
        fifo_cg = new();
        F_cvg_txn = new();
    endfunction

    // ====== Sample Data Method ======
    function void sample_data(FIFO_transaction F_txn);
    F_cvg_txn = F_txn;
    // === Trigger Sampling ===
    fifo_cg.sample();
    endfunction

endclass
endpackage
```

1.5 scoreboard Package

```
package FIFO_scoreboard_pkg;

  import FIFO_transaction_pkg::*;
  import Shared_pkg::*;

  class FIFO_scoreboard;
    // ========= Reference Model Signals =========
    bit [FIFO_WIDTH-1:0] data_out_ref;
```

```
    bit wr_ack_ref, overflow_ref;
    bit full_ref, empty_ref, almostfull_ref, almostempty_ref, underflow_ref;

    // ===== #No Of Location In FIFO =====
    localparam max_fifo_addr = $clog2(FIFO_DEPTH);

    // ========= Internal FIFO model =========
    bit [FIFO_WIDTH-1:0] FIFO [$];  // FIFO == Queue "first in - first out"
    bit [max_fifo_addr-1:0] write_ptr;
    bit [max_fifo_addr-1:0] read_ptr;
    int count;
    bit [FIFO_WIDTH-1:0] last_data_in;

    // ======== Create object =========
    FIFO_transaction F_txn = new();

    // ========= Reference model to calculate expected outputs =========
    function void reference_model(FIFO_transaction F_txn);
        // ========= Capture input =========
        last_data_in = F_txn.data_in;

        // ========= Handle reset: clear pointers, count, memory, and outputs =========
        if (F_txn.rst_n == 0) begin
            write_ptr      = 'b0;
            read_ptr       = 'b0;
            count          = 0;
            data_out_ref   = 'b0;
            wr_ack_ref     = 0;
            overflow_ref   = 0;
            underflow_ref  = 0;
            full_ref       = 0;
            empty_ref      = 1;
            almostfull_ref = 0;
            almostempty_ref= 0;
            FIFO.delete();
           end else begin

            // ===== Default outputs for non-reset =====
            //overflow_ref   = 0;
            //underflow_ref  = 0;

                // Case: Write Enable
                if (F_txn.wr_en && count < FIFO_DEPTH) begin
                FIFO.push_back(last_data_in);
                write_ptr = write_ptr + 'b1;
                wr_ack_ref = 1'b1;
               end else begin
                        wr_ack_ref = 1'b0;
                        if (F_txn.wr_en && count == FIFO_DEPTH) begin
                    // overflow when full
                    overflow_ref = 1'b1;
                end else begin
                    overflow_ref = 1'b0;
                end
                end

                // Case: Read Enable
                if (F_txn.rd_en && count != 0) begin
                  data_out_ref = FIFO.pop_front();
                  read_ptr = read_ptr + 'b1 ;
            end else begin
                    if (F_txn.rd_en && count == 0) begin
                      // underflow when empty
                      underflow_ref = 1'b1;
                end else begin
                      underflow_ref = 1'b0;
                end
            end

            // Case: write Enable and not Full
                    if (!F_txn.rd_en && F_txn.wr_en && !full_ref) begin
                                count++;
                        // Case: Read Enable and not Empty
                        end else if (F_txn.rd_en && !F_txn.wr_en && !empty_ref) begin
                            count--;
                    // Case: simultaneous read & write
                    end else if (F_txn.wr_en && F_txn.rd_en && empty_ref) begin
                            // empty: only write
                        count++;
                    end else if (F_txn.wr_en && F_txn.rd_en && full_ref) begin
                        // full: only read
                         count--;
                        end
                     end

            // ===== Update status flags =====
            empty_ref      = (count == 0);
            full_ref       = (count == FIFO_DEPTH);
            almostfull_ref = (count == FIFO_DEPTH-1);
            almostempty_ref= (count == 1);
        endfunction

        // ====== Function to check data by comparing actual outputs with reference model ======
        function void check_data(FIFO_transaction F_txn);
            // ====== Compute expected ======
            reference_model(F_txn);

            // ====== Compare ======
            // === Use Force Equality ===
            if (F_txn.data_out   === data_out_ref   &&
```

```
            F_txn.wr_ack     === wr_ack_ref     &&
            F_txn.overflow   === overflow_ref   &&
            F_txn.underflow  === underflow_ref  &&
            F_txn.full       === full_ref       &&
                F_txn.empty      === empty_ref      &&
            F_txn.almostfull === almostfull_ref &&
                F_txn.almostempty=== almostempty_ref) begin
                correct_count++;
        end else begin
                error_count++;
                $display("ERROR at time %0t:", $time);
                if (F_txn.data_out   !== data_out_ref)    $display("   data_out   : Exp=%h, Got=%h", data_out_ref, F_txn.data_out);
                if (F_txn.wr_ack     !== wr_ack_ref)      $display("   wr_ack     : Exp=%b, Got=%b", wr_ack_ref, F_txn.wr_ack);
                if (F_txn.overflow   !== overflow_ref)    $display("   overflow   : Exp=%b, Got=%b", overflow_ref, F_txn.overflow);
                if (F_txn.underflow  !== underflow_ref)   $display("   underflow  : Exp=%b, Got=%b", underflow_ref, F_txn.underflow);
                if (F_txn.full       !== full_ref)        $display("   full       : Exp=%b, Got=%b", full_ref, F_txn.full);
                if (F_txn.empty      !== empty_ref)       $display("   empty      : Exp=%b, Got=%b", empty_ref, F_txn.empty);
                if (F_txn.almostfull !== almostfull_ref)  $display("   almostfull : Exp=%b, Got=%b", almostfull_ref, F_txn.almostfull);
                if (F_txn.almostempty!== almostempty_ref) $display("   almostempty: Exp=%b, Got=%b", almostempty_ref, F_txn.almostempty);
        end
    endfunction

  endclass

endpackage
```

1.6 Monitor Package

```
import Shared_pkg::*;

module FIFO_monitor (FIFO_IF.MON fifo_intf);

  // ===== Import required packages =====
  import FIFO_transaction_pkg::*;
  import FIFO_coverage_pkg::*;
  import FIFO_scoreboard_pkg::*;
  import Shared_pkg::*;

  // ===== Create class objects ======
  FIFO_transaction fifo_txn;
  FIFO_scoreboard  fifo_scb;
  FIFO_coverage    fifo_cov;

  initial begin
    // ==== Create objects ====
    fifo_txn = new();
    fifo_scb = new();
    fifo_cov = new();

    // ==== Start monitoring ====
    forever begin
      // ==== Wait for negedge clock to sample data ====
      @(negedge fifo_intf.clk);

      // ==== Wait for sampling event from testbench ====
      fifo_intf.trigger_sample();

      // ==== Sample the interface and update transaction object ====
      // ==== Input =====
      fifo_txn.data_in = fifo_intf.data_in;
      fifo_txn.wr_en = fifo_intf.wr_en;
      fifo_txn.rd_en = fifo_intf.rd_en;
      fifo_txn.rst_n = fifo_intf.rst_n;
      // ==== Output =====
      fifo_txn.data_out = fifo_intf.data_out;
      fifo_txn.full = fifo_intf.full;
      fifo_txn.empty = fifo_intf.empty;
      fifo_txn.almostfull = fifo_intf.almostfull;
      fifo_txn.almostempty = fifo_intf.almostempty;
      fifo_txn.overflow = fifo_intf.overflow;
      fifo_txn.underflow = fifo_intf.underflow;
      fifo_txn.wr_ack = fifo_intf.wr_ack;

      // ==== Fork-join to run coverage and scoreboard in parallel ====
      fork
        // ==== Process 1: Sample coverage ====
        fifo_cov.sample_data(fifo_txn);
                begin
            // ==== Process 2: Check data with scoreboard ====
            @(posedge fifo_intf.clk);
            // ======= Wait Output To Be Stable =======
            #3;
            fifo_scb.check_data(fifo_txn);
        end
      join

      // Check if test is finished
      if (test_finished) begin
        // Display test summary
        $display("Test Summary:");
        $display("   Total Correct: %0d", correct_count);
        $display("   Total Errors: %0d", error_count);
        $display("   Coverage: %0.2f%%", fifo_cov.fifo_cg.get_coverage());
        $stop;
      end
    end
  end
endmodule
```

1.7 Testbench

```
module FIFO_tb(FIFO_IF.TB fifo_intf);

  import FIFO_transaction_pkg::*;
  import Shared_pkg::*;

  // ===== Create transaction object =====
  FIFO_transaction fifo_txn;

  initial begin
    // ===== Create transaction object =====
    fifo_txn = new();

    // ===== Disable randomization & constrain =====
    fifo_txn.rand_mode(0);
    fifo_txn.constraint_mode(0);

    // ===== Initialize fifo inputs =====
    fifo_intf.data_in = 0;
    fifo_intf.wr_en = 0;
    fifo_intf.rd_en = 0;
    fifo_intf.rst_n = 0;

    // ===== Trigger sample event for monitor =====
    fifo_intf.trigger_sample();

    // ===== Apply reset for a few cycles =====
    repeat(2) @(posedge fifo_intf.clk);

    // ===== Apply Release reset =====
    fifo_intf.rst_n = 1;

    repeat(2) @(posedge fifo_intf.clk);

    // ===== Enable randomization & constrain =====
    fifo_txn.rand_mode(1);
    fifo_txn.constraint_mode(1);

    // ===== Start Randomaize Test Tramsactions  =====
    for (int i = 0; i < TEST_COUNT; i++) begin
        // ===== Randomize transaction =====
        if (!fifo_txn.randomize()) begin
            $error("Randomization␣failed␣at␣iteration␣%0d", i);
            break;
        end

        // ===== Wait for negedge clock =====
        @(negedge fifo_intf.clk);

        // ===== Drive inputs from transaction =====
        fifo_intf.data_in = fifo_txn.data_in;
        fifo_intf.wr_en   = fifo_txn.wr_en;
        fifo_intf.rd_en   = fifo_txn.rd_en;
        fifo_intf.rst_n   = fifo_txn.rst_n;

        // ===== Trigger sample event for monitor =====
        fifo_intf.trigger_sample();

    end

    // ===== Signal end of test =====
    repeat(5) @(posedge fifo_intf.clk);
    test_finished = 1;

    // ===== Wait a few more cycles for monitor to process results =====
    repeat(5) @(posedge fifo_intf.clk);
  end

endmodule
```

1.8 Design With Bugs + SVA

```
module FIFO(FIFO_IF.DUT fifo_intf);
parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;

localparam max_fifo_addr = $clog2(FIFO_DEPTH);

reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];

reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        wr_ptr <= 0;
    end
    else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
        mem[wr_ptr] <= fifo_intf.data_in;
        fifo_intf.wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
    end
    else begin
        fifo_intf.wr_ack <= 0;
        if (fifo_intf.full & fifo_intf.wr_en)
            fifo_intf.overflow <= 1;
        else
            fifo_intf.overflow <= 0;
```

```
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        rd_ptr <= 0;
    end
    else if (fifo_intf.rd_en && count != 0) begin
        fifo_intf.data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        count <= 0;
    end
    else begin
        if  ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
            count <= count + 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
            count <= count - 1;
    end
end

assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0)? 1 : 0;
assign fifo_intf.underflow = (fifo_intf.empty && fifo_intf.rd_en)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-2)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;


// ========================================
// Assertions using conditional compilation
// ========================================
`ifdef SIM
    // ===== Reset behavior assertion =====
    property reset_behavior;
        @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=>  (count == 0 && rd_ptr == 0 && wr_ptr == 0
                    && !fifo_intf.wr_ack && !fifo_intf.overflow  && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
    endproperty

    // ===== Write acknowledge assertion =====
    property write_ack_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
    endproperty

    // ===== Overflow detection assertion =====
    property overflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
            fifo_intf.overflow;
    endproperty

    // ===== Underflow detection assertion =====
    property underflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
    endproperty

    // ===== Empty flag assertion =====
    property empty_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == 0) |-> fifo_intf.empty;
    endproperty

    // ===== Full flag assertion =====
    property full_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH) |-> fifo_intf.full;
    endproperty

    // ===== Almost full condition assertion =====
    property almost_full_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
    endproperty

    // ===== Almost empty condition assertion =====
    property almost_empty_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == 1) |-> fifo_intf.almostempty;
    endproperty

    // ===== Pointer wraparound assertion for write_ptr =====
    property write_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && wr_ptr == FIFO_DEPTH-1) |=>
            (wr_ptr == 0);
    endproperty

    // ===== Pointer wraparound assertion for read_ptr =====
    property read_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && rd_ptr == FIFO_DEPTH-1) |=>
            (rd_ptr == 0);
    endproperty

    // ===== Pointer threshold assertion for write_ptr =====
    property write_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (wr_ptr < FIFO_DEPTH);
    endproperty

    // ===== Pointer threshold assertion for read_ptr =====
    property read_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (rd_ptr < FIFO_DEPTH);
    endproperty

```

```
    // ===== Counter threshold assertion =====
    property counter_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count <= FIFO_DEPTH);
    endproperty

    // ===== Assert all the properties =====
    assert property (reset_behavior)       else $error("Reset behavior assertion failed!");
    assert property (write_ack_check)      else $error("Write acknowledge assertion failed!");
    assert property (overflow_check)       else $error("Overflow detection assertion failed!");
    assert property (underflow_check)      else $error("Underflow detection assertion failed!");
    assert property (empty_flag_check)     else $error("Empty flag assertion failed!");
    assert property (full_flag_check)      else $error("Full flag assertion failed!");
    assert property (almost_full_check)    else $error("Almost full condition assertion failed!");
    assert property (almost_empty_check)   else $error("Almost empty condition assertion failed!");
    assert property (write_ptr_wraparound) else $error("Write pointer wraparound assertion failed!");
    assert property (read_ptr_wraparound)  else $error("Read pointer wraparound assertion failed!");
    assert property (write_ptr_threshold)  else $error("Write pointer threshold assertion failed!");
    assert property (read_ptr_threshold)   else $error("Read pointer threshold assertion failed!");
    assert property (counter_threshold)    else $error("Counter threshold assertion failed!");

    cover property (reset_behavior);
    cover property (write_ack_check);
    cover property (overflow_check);
    cover property (underflow_check);
    cover property (empty_flag_check);
    cover property (full_flag_check);
    cover property (almost_full_check);
    cover property (almost_empty_check);
    cover property (write_ptr_wraparound);
    cover property (read_ptr_wraparound);
    cover property (write_ptr_threshold);
    cover property (read_ptr_threshold);
    cover property (counter_threshold);

`endif

endmodule
```

1.9 Corrected Design + SVA

```
module FIFO(FIFO_IF.DUT fifo_intf);
parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;

localparam max_fifo_addr = $clog2(FIFO_DEPTH);

reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];  // 1-D Array

reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        wr_ptr <= 0;
        fifo_intf.wr_ack <= 0;
        fifo_intf.overflow <= 0;
    end
    else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
        mem[wr_ptr] <= fifo_intf.data_in;
        fifo_intf.wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
    end
    else begin
        fifo_intf.wr_ack <= 0;
        if (fifo_intf.full & fifo_intf.wr_en)
            fifo_intf.overflow <= 1;
        else
            fifo_intf.overflow <= 0;
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        rd_ptr <= 0;
        fifo_intf.underflow <= 0;
        fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    end
    else if (fifo_intf.rd_en && count != 0) begin
        fifo_intf.data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
    end
    else begin
        if (fifo_intf.empty & fifo_intf.rd_en)
            fifo_intf.underflow <= 1;
        else
            fifo_intf.underflow <= 0;
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        count <= 0;
    end
    else begin
        if  ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
            count <= count + 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
            count <= count - 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.full)
            count <= count - 1;
```

```
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.empty)
            count <= count + 1;
    end
end

assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;


// ========================================
// Assertions using conditional compilation
// ========================================
`ifdef SIM
    // ===== Reset behavior assertion =====
    property reset_behavior;
        @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=>  (count == 0 && rd_ptr == 0 && wr_ptr == 0
                    && !fifo_intf.wr_ack && !fifo_intf.overflow  && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
    endproperty

    // ===== Write acknowledge assertion =====
    property write_ack_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
    endproperty

    // ===== Overflow detection assertion =====
    property overflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
            fifo_intf.overflow;
    endproperty

    // ===== Underflow detection assertion =====
    property underflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
    endproperty

    // ===== Empty flag assertion =====
    property empty_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == 0) |-> fifo_intf.empty;
    endproperty

    // ===== Full flag assertion =====
    property full_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH) |-> fifo_intf.full;
    endproperty

    // ===== Almost full condition assertion =====
    property almost_full_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
    endproperty

    // ===== Almost empty condition assertion =====
    property almost_empty_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count == 1) |-> fifo_intf.almostempty;
    endproperty

    // ===== Pointer wraparound assertion for write_ptr =====
    property write_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && wr_ptr == FIFO_DEPTH-1) |=>
            (wr_ptr == 0);
    endproperty

    // ===== Pointer wraparound assertion for read_ptr =====
    property read_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && rd_ptr == FIFO_DEPTH-1) |=>
            (rd_ptr == 0);
    endproperty

    // ===== Pointer threshold assertion for write_ptr =====
    property write_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (wr_ptr < FIFO_DEPTH);
    endproperty

    // ===== Pointer threshold assertion for read_ptr =====
    property read_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (rd_ptr < FIFO_DEPTH);
    endproperty

    // ===== Counter threshold assertion =====
    property counter_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (count <= FIFO_DEPTH);
    endproperty

    // ===== Assert all the properties =====
    assert property (reset_behavior)       else $error("Reset behavior assertion failed!");
    assert property (write_ack_check)      else $error("Write acknowledge assertion failed!");
    assert property (overflow_check)       else $error("Overflow detection assertion failed!");
    assert property (underflow_check)      else $error("Underflow detection assertion failed!");
    assert property (empty_flag_check)     else $error("Empty flag assertion failed!");
    assert property (full_flag_check)      else $error("Full flag assertion failed!");
    assert property (almost_full_check)    else $error("Almost full condition assertion failed!");
    assert property (almost_empty_check)   else $error("Almost empty condition assertion failed!");
    assert property (write_ptr_wraparound) else $error("Write pointer wraparound assertion failed!");
    assert property (read_ptr_wraparound)  else $error("Read pointer wraparound assertion failed!");
    assert property (write_ptr_threshold)  else $error("Write pointer threshold assertion failed!");
    assert property (read_ptr_threshold)   else $error("Read pointer threshold assertion failed!");
    assert property (counter_threshold)    else $error("Counter threshold assertion failed!");

    cover property (reset_behavior);
```

```
    cover property (write_ack_check);
    cover property (overflow_check);
    cover property (underflow_check);
    cover property (empty_flag_check);
    cover property (full_flag_check);
    cover property (almost_full_check);
    cover property (almost_empty_check);
    cover property (write_ptr_wraparound);
    cover property (read_ptr_wraparound);
    cover property (write_ptr_threshold);
    cover property (read_ptr_threshold);
    cover property (counter_threshold);

`endif

endmodule
```

2 Bugs report

Here is a summary of all the bugs in the original FIFO implementation and how each was fixed in the corrected version:

Table 1: Bugs report

#	Bug	Original Behavior	Fix in Corrected Code
1	Uninitialized `wr_ack` and `overflow`	On reset, only `wr_ptr` was cleared. `wr_ack` and `overflow` remained unknown until the first write cycle.	Added `wr_ack <= 0;` and `overflow <= 0;` in the reset branch of the write block.
2	`data_out` never reset	unknown data after reset.	In the read block's reset clause, added `data_out <= {FIFO_WIDTH{1'b0}};`.
3	`underflow` not registered	Was a combinational assign (`assign underflow = empty && rd_en`), causing glitches and no clear reset.	Moved underflow into the read always block with its own reset and clear logic "Like overflow".
4	Simultaneous read+write ignored	When both `wr_en` and `rd_en` were high, `count` did not change.	Added explicit cases for `{wr_en,rd_en}==2'b11`: decrement if full, increment if empty.
5	Incomplete overflow clearing	`overflow` stayed asserted if writes retried while full.	Now cleared (`overflow <= 0`) whenever `!(full & wr_en)` in the write block.
6	"Almost-full" threshold off by one	Triggered at `count == FIFO_DEPTH-2` (two slots left).	Changed to `almostfull = (count == FIFO_DEPTH-1)` (one slot left).
7	Count logic incomplete	Only handled two cases (`10` and `01`), missing the four-state nature of {`wr_en,rd_en`}.	Fully enumerated all four conditions (`2'b10, 2'b01, 2'b11 & full, 2'b11 & empty`).

3 Makefile Contain Do File

```
VSIM = vsim
RUN = run
VLOG = qverilog

# Define testbench Directory
TBDIR = ${FIFO_ROOT}/sv_verification

# Target flist
target = src_files
FLIST = ${target}.list

VPATH = $(TEST_DIR) $(TBDIR)
TBFILES = $(TBDIR)/$(FLIST)

# Define 5 seed values
SEEDS = 1111 1511 2515 2236 5215

# Targets
clean:
        rm -rf *.log *.dis *.tbl vcs* simv* *.map transcript *.ucdb *.wlf *.txt \
        work dataset.asdb  library.cfg work

##################### Simulation Runs ####################################
questa: ${TBFILES}
        $(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.FIFO_top -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"

questa+SIM: ${TBFILES}
        $(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.FIFO_top -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"

# Run simulation with a specific seed
seed%: ${TBFILES}
        @echo "Running simulation with seed $*"
        $(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.FIFO_top -cover -sv_seed $* -do "do wave.do; coverage save FIFO_seed$*.ucdb -onexit; run -all"
        vcover report FIFO_seed$*.ucdb -details -annotate -all -output code_coverage_rpt_seed$*.txt -du=FIFO
        vcover report -details -cvg -output functional_coverage_report_seed$*.txt FIFO_seed$*.ucdb

# Run all seeds in sequence
all_seeds: ${TBFILES}
        @echo "Running simulations with all seeds"
        $(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover +cover -covercells -R +nowarn3829
        @for seed in $(SEEDS); do \
                echo ""; \
                echo "Running simulation with seed $$seed"; \
                $(VSIM) -voptargs=+acc work.FIFO_top -cover -sv_seed $$seed -do "do wave.do; coverage save FIFO_seed$$seed.ucdb -onexit;
                vcover report FIFO_seed$$seed.ucdb -details -annotate -all -output code_coverage_rpt_seed$$seed.txt -du=FIFO; \
                vcover report -details -cvg -output functional_coverage_report_seed$$seed.txt FIFO_seed$$seed.ucdb; \
        done
```

```
        @echo "All seed runs completed"

# Merge coverage results from all seeds
merge_coverage:
        @echo "Merging coverage from all seed runs"
        vcover merge merged.ucdb FIFO_seed*.ucdb
        $(VSIM) -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
        vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
        vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
        @echo "Coverage merged to merged.ucdb and reports saved"

# Run all seeds and merge coverage
run_seeds: all_seeds merge_coverage
        @echo "Complete seed-based simulation and coverage analysis finished"

help:
        @echo Make sure the environment variable FIFO_ROOT is set.
        @echo Possible targets:
        @echo "  questa        - Run basic simulation"
        @echo "  questa+SIM    - Run simulation with +SIM defined"
        @echo "  seed<number>  - Run simulation with specific seed (e.g., seed1, seed2)"
        @echo "  all_seeds     - Run simulations with all predefined seeds"
        @echo "  merge_coverage- Merge coverage data from all seed runs"
        @echo "  run_seeds     - Run all seeds and merge coverage"
        @echo "  clean         - Clean up simulation files"
```

4 Functional Coverage Report

4.1 Functional Coverage "seed1" Report

```
Coverage Report by instance with details

================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.75%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   194       191         3    98.45%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100	–	Uncovered
covered/total bins:	191	194	–	
missing/total bins:	3	194	–	
% Hit:	98.45%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	161	1	–	Covered
bin auto[1]	847	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	18	1	–	Covered
bin auto[2048:3071]	15	1	–	Covered
bin auto[3072:4095]	13	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	14	1	–	Covered
bin auto[6144:7167]	13	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	18	1	–	Covered
bin auto[9216:10239]	16	1	–	Covered
bin auto[10240:11263]	14	1	–	Covered
bin auto[11264:12287]	10	1	–	Covered
bin auto[12288:13311]	14	1	–	Covered
bin auto[13312:14335]	19	1	–	Covered
bin auto[14336:15359]	14	1	–	Covered
bin auto[15360:16383]	18	1	–	Covered
bin auto[16384:17407]	21	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered
bin auto[18432:19455]	16	1	–	Covered
bin auto[19456:20479]	11	1	–	Covered
bin auto[20480:21503]	18	1	–	Covered
bin auto[21504:22527]	15	1	–	Covered
bin auto[22528:23551]	15	1	–	Covered
bin auto[23552:24575]	22	1	–	Covered
bin auto[24576:25599]	13	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	19	1	–	Covered
bin auto[27648:28671]	17	1	–	Covered
bin auto[28672:29695]	17	1	–	Covered
bin auto[29696:30719]	17	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered

bin auto[32768:33791]	15	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	20	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	9	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	19	1	–	Covered
bin auto[40960:41983]	10	1	–	Covered
bin auto[41984:43007]	21	1	–	Covered
bin auto[43008:44031]	23	1	–	Covered
bin auto[44032:45055]	15	1	–	Covered
bin auto[45056:46079]	21	1	–	Covered
bin auto[46080:47103]	15	1	–	Covered
bin auto[47104:48127]	12	1	–	Covered
bin auto[48128:49151]	19	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	18	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	13	1	–	Covered
bin auto[53248:54271]	19	1	–	Covered
bin auto[54272:55295]	24	1	–	Covered
bin auto[55296:56319]	17	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	20	1	–	Covered
bin auto[58368:59391]	20	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered
bin auto[62464:63487]	10	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	19	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	675	1	–	Covered
bin auto[1]	333	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	329	1	–	Covered
bin auto[1]	679	1	–	Covered
Coverpoint data_out_cp	95.31%	100	–	Uncovered
covered/total bins:	61	64	–	
missing/total bins:	3	64	–	
% Hit:	95.31%	100	–	
bin auto[0:1023]	516	1	–	Covered
bin auto[1024:2047]	6	1	–	Covered
bin auto[2048:3071]	10	1	–	Covered
bin auto[3072:4095]	4	1	–	Covered
bin auto[4096:5119]	4	1	–	Covered
bin auto[5120:6143]	8	1	–	Covered
bin auto[6144:7167]	0	1	–	ZERO
bin auto[7168:8191]	10	1	–	Covered
bin auto[8192:9215]	17	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	4	1	–	Covered
bin auto[11264:12287]	19	1	–	Covered
bin auto[12288:13311]	3	1	–	Covered
bin auto[13312:14335]	15	1	–	Covered
bin auto[14336:15359]	9	1	–	Covered
bin auto[15360:16383]	8	1	–	Covered
bin auto[16384:17407]	9	1	–	Covered
bin auto[17408:18431]	8	1	–	Covered
bin auto[18432:19455]	14	1	–	Covered
bin auto[19456:20479]	5	1	–	Covered
bin auto[20480:21503]	21	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered
bin auto[22528:23551]	9	1	–	Covered
bin auto[23552:24575]	8	1	–	Covered
bin auto[24576:25599]	0	1	–	ZERO
bin auto[25600:26623]	4	1	–	Covered
bin auto[26624:27647]	9	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	8	1	–	Covered
bin auto[31744:32767]	7	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	2	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	3	1	–	Covered
bin auto[36864:37887]	8	1	–	Covered
bin auto[37888:38911]	8	1	–	Covered
bin auto[38912:39935]	14	1	–	Covered
bin auto[39936:40959]	7	1	–	Covered
bin auto[40960:41983]	1	1	–	Covered
bin auto[41984:43007]	7	1	–	Covered
bin auto[43008:44031]	10	1	–	Covered
bin auto[44032:45055]	4	1	–	Covered

bin auto[45056:46079]	6	1	–	Covered
bin auto[46080:47103]	0	1	–	ZERO
bin auto[47104:48127]	9	1	–	Covered
bin auto[48128:49151]	9	1	–	Covered
bin auto[49152:50175]	6	1	–	Covered
bin auto[50176:51199]	3	1	–	Covered
bin auto[51200:52223]	9	1	–	Covered
bin auto[52224:53247]	23	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	16	1	–	Covered
bin auto[55296:56319]	5	1	–	Covered
bin auto[56320:57343]	17	1	–	Covered
bin auto[57344:58367]	8	1	–	Covered
bin auto[58368:59391]	5	1	–	Covered
bin auto[59392:60415]	7	1	–	Covered
bin auto[60416:61439]	3	1	–	Covered
bin auto[61440:62463]	5	1	–	Covered
bin auto[62464:63487]	1	1	–	Covered
bin auto[63488:64511]	1	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	449	1	–	Covered
bin auto[1]	559	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	976	1	–	Covered
bin auto[1]	32	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	810	1	–	Covered
bin auto[1]	198	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	769	1	–	Covered
bin auto[1]	239	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	820	1	–	Covered
bin auto[1]	188	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	619	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	919	1	–	Covered
bin auto[1]	89	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	188	1	–	Covered
bin <auto[1],auto[1],auto[0]>	38	1	–	Covered
bin <auto[0],auto[1],auto[1]>	371	1	–	Covered
bin <auto[0],auto[1],auto[0]>	82	1	–	Covered
bin <auto[1],auto[0],auto[0]>	107	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	93	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[1],auto[0],auto[0]>	86	1	–	Covered
bin <auto[0],auto[1],auto[0]>	360	1	–	Covered
bin <auto[0],auto[0],auto[0]>	172	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	21		–	Occurred
ignore_bin w_en_r_en_allactv_full	34		–	Occurred
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	

% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	34	1	–	Covered
bin <auto[1],auto[0],auto[1]>	57	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[0],auto[1],auto[0]>	393	1	–	Covered
bin <auto[1],auto[0],auto[0]>	50	1	–	Covered
bin <auto[0],auto[0],auto[0]>	134	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	148		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	44	1	–	Covered
bin <auto[0],auto[1],auto[1]>	71	1	–	Covered
bin <auto[1],auto[0],auto[1]>	23	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	182	1	–	Covered
bin <auto[0],auto[1],auto[0]>	382	1	–	Covered
bin <auto[1],auto[0],auto[0]>	84	1	–	Covered
bin <auto[0],auto[0],auto[0]>	172	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	125	1	–	Covered
bin <auto[0],auto[1],auto[1]>	147	1	–	Covered
bin <auto[1],auto[0],auto[1]>	34	1	–	Covered
bin <auto[0],auto[0],auto[1]>	83	1	–	Covered
bin <auto[1],auto[1],auto[0]>	101	1	–	Covered
bin <auto[0],auto[1],auto[0]>	306	1	–	Covered
bin <auto[1],auto[0],auto[0]>	73	1	–	Covered
bin <auto[0],auto[0],auto[0]>	139	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	7	1	–	Covered
bin <auto[1],auto[1],auto[0]>	219	1	–	Covered
bin <auto[0],auto[1],auto[1]>	25	1	–	Covered
bin <auto[0],auto[1],auto[0]>	428	1	–	Covered
bin <auto[1],auto[0],auto[0]>	107	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	63	1	–	Covered
bin <auto[1],auto[0],auto[1]>	26	1	–	Covered
bin <auto[1],auto[1],auto[0]>	163	1	–	Covered
bin <auto[0],auto[1],auto[0]>	453	1	–	Covered
bin <auto[1],auto[0],auto[0]>	81	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100	–	Uncovered
covered/total bins:	191	194	–	
missing/total bins:	3	194	–	
% Hit:	98.45%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	161	1	–	Covered
bin auto[1]	847	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	18	1	–	Covered
bin auto[2048:3071]	15	1	–	Covered
bin auto[3072:4095]	13	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	14	1	–	Covered
bin auto[6144:7167]	13	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	18	1	–	Covered
bin auto[9216:10239]	16	1	–	Covered

bin auto[10240:11263]	14	1	–	Covered
bin auto[11264:12287]	10	1	–	Covered
bin auto[12288:13311]	14	1	–	Covered
bin auto[13312:14335]	19	1	–	Covered
bin auto[14336:15359]	14	1	–	Covered
bin auto[15360:16383]	18	1	–	Covered
bin auto[16384:17407]	21	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered
bin auto[18432:19455]	16	1	–	Covered
bin auto[19456:20479]	11	1	–	Covered
bin auto[20480:21503]	18	1	–	Covered
bin auto[21504:22527]	15	1	–	Covered
bin auto[22528:23551]	15	1	–	Covered
bin auto[23552:24575]	22	1	–	Covered
bin auto[24576:25599]	13	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	19	1	–	Covered
bin auto[27648:28671]	17	1	–	Covered
bin auto[28672:29695]	17	1	–	Covered
bin auto[29696:30719]	17	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered
bin auto[32768:33791]	15	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	20	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	9	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	19	1	–	Covered
bin auto[40960:41983]	10	1	–	Covered
bin auto[41984:43007]	21	1	–	Covered
bin auto[43008:44031]	23	1	–	Covered
bin auto[44032:45055]	15	1	–	Covered
bin auto[45056:46079]	21	1	–	Covered
bin auto[46080:47103]	15	1	–	Covered
bin auto[47104:48127]	12	1	–	Covered
bin auto[48128:49151]	19	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	18	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	13	1	–	Covered
bin auto[53248:54271]	19	1	–	Covered
bin auto[54272:55295]	24	1	–	Covered
bin auto[55296:56319]	17	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	20	1	–	Covered
bin auto[58368:59391]	20	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered
bin auto[62464:63487]	10	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	19	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	675	1	–	Covered
bin auto[1]	333	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	329	1	–	Covered
bin auto[1]	679	1	–	Covered
Coverpoint data_out_cp	95.31%	100	–	Uncovered
covered/total bins:	61	64	–	
missing/total bins:	3	64	–	
% Hit:	95.31%	100	–	
bin auto[0:1023]	516	1	–	Covered
bin auto[1024:2047]	6	1	–	Covered
bin auto[2048:3071]	10	1	–	Covered
bin auto[3072:4095]	4	1	–	Covered
bin auto[4096:5119]	4	1	–	Covered
bin auto[5120:6143]	8	1	–	Covered
bin auto[6144:7167]	0	1	–	ZERO
bin auto[7168:8191]	10	1	–	Covered
bin auto[8192:9215]	17	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	4	1	–	Covered
bin auto[11264:12287]	19	1	–	Covered
bin auto[12288:13311]	3	1	–	Covered
bin auto[13312:14335]	15	1	–	Covered
bin auto[14336:15359]	9	1	–	Covered
bin auto[15360:16383]	8	1	–	Covered
bin auto[16384:17407]	9	1	–	Covered
bin auto[17408:18431]	8	1	–	Covered
bin auto[18432:19455]	14	1	–	Covered
bin auto[19456:20479]	5	1	–	Covered
bin auto[20480:21503]	21	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered

bin auto[22528:23551]	9	1	–	Covered
bin auto[23552:24575]	8	1	–	Covered
bin auto[24576:25599]	0	1	–	ZERO
bin auto[25600:26623]	4	1	–	Covered
bin auto[26624:27647]	9	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	8	1	–	Covered
bin auto[31744:32767]	7	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	2	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	3	1	–	Covered
bin auto[36864:37887]	8	1	–	Covered
bin auto[37888:38911]	8	1	–	Covered
bin auto[38912:39935]	14	1	–	Covered
bin auto[39936:40959]	7	1	–	Covered
bin auto[40960:41983]	1	1	–	Covered
bin auto[41984:43007]	7	1	–	Covered
bin auto[43008:44031]	10	1	–	Covered
bin auto[44032:45055]	4	1	–	Covered
bin auto[45056:46079]	6	1	–	Covered
bin auto[46080:47103]	0	1	–	ZERO
bin auto[47104:48127]	9	1	–	Covered
bin auto[48128:49151]	9	1	–	Covered
bin auto[49152:50175]	6	1	–	Covered
bin auto[50176:51199]	3	1	–	Covered
bin auto[51200:52223]	9	1	–	Covered
bin auto[52224:53247]	23	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	16	1	–	Covered
bin auto[55296:56319]	5	1	–	Covered
bin auto[56320:57343]	17	1	–	Covered
bin auto[57344:58367]	8	1	–	Covered
bin auto[58368:59391]	5	1	–	Covered
bin auto[59392:60415]	7	1	–	Covered
bin auto[60416:61439]	3	1	–	Covered
bin auto[61440:62463]	5	1	–	Covered
bin auto[62464:63487]	1	1	–	Covered
bin auto[63488:64511]	1	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	449	1	–	Covered
bin auto[1]	559	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	976	1	–	Covered
bin auto[1]	32	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	810	1	–	Covered
bin auto[1]	198	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	769	1	–	Covered
bin auto[1]	239	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	820	1	–	Covered
bin auto[1]	188	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	619	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	919	1	–	Covered
bin auto[1]	89	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	188	1	–	Covered
bin <auto[1],auto[1],auto[0]>	38	1	–	Covered
bin <auto[0],auto[1],auto[1]>	371	1	–	Covered

bin <auto[0],auto[1],auto[0]>	82	1	–	Covered
bin <auto[1],auto[0],auto[0]>	107	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	93	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[1],auto[0],auto[0]>	86	1	–	Covered
bin <auto[0],auto[1],auto[0]>	360	1	–	Covered
bin <auto[0],auto[0],auto[0]>	172	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	21		–	Occurred
ignore_bin w_en_r_en_allactv_full	34		–	Occurred
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	34	1	–	Covered
bin <auto[1],auto[0],auto[1]>	57	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[0],auto[1],auto[0]>	393	1	–	Covered
bin <auto[1],auto[0],auto[0]>	50	1	–	Covered
bin <auto[0],auto[0],auto[0]>	134	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	148		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	44	1	–	Covered
bin <auto[0],auto[1],auto[1]>	71	1	–	Covered
bin <auto[1],auto[0],auto[1]>	23	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	182	1	–	Covered
bin <auto[0],auto[1],auto[0]>	382	1	–	Covered
bin <auto[1],auto[0],auto[0]>	84	1	–	Covered
bin <auto[0],auto[0],auto[0]>	172	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	125	1	–	Covered
bin <auto[0],auto[1],auto[1]>	147	1	–	Covered
bin <auto[1],auto[0],auto[1]>	34	1	–	Covered
bin <auto[0],auto[0],auto[1]>	83	1	–	Covered
bin <auto[1],auto[1],auto[0]>	101	1	–	Covered
bin <auto[0],auto[1],auto[0]>	306	1	–	Covered
bin <auto[1],auto[0],auto[0]>	73	1	–	Covered
bin <auto[0],auto[0],auto[0]>	139	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	7	1	–	Covered
bin <auto[1],auto[1],auto[0]>	219	1	–	Covered
bin <auto[0],auto[1],auto[1]>	25	1	–	Covered
bin <auto[0],auto[1],auto[0]>	428	1	–	Covered
bin <auto[1],auto[0],auto[0]>	107	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	63	1	–	Covered
bin <auto[1],auto[0],auto[1]>	26	1	–	Covered
bin <auto[1],auto[1],auto[0]>	163	1	–	Covered
bin <auto[0],auto[1],auto[0]>	453	1	–	Covered
bin <auto[1],auto[0],auto[0]>	81	1	–	Covered
bin <auto[0],auto[0],auto[0]>	222	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 99.75% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.75%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov...	SVA	✓	Off	847	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	847	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	847	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	2	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	19	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	187	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	23	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	32	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	194	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	58	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	20	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	473	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	161	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 1: SVA "Seed1"

4.2 Functional Coverage "seed2" Report

```
Coverage Report by instance with details

=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.83%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   194       192         2    98.96%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100	–	Uncovered
covered/total bins:	192	194	–	
missing/total bins:	2	194	–	
% Hit:	98.96%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	156	1	–	Covered
bin auto[1]	852	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	22	1	–	Covered
bin auto[1024:2047]	15	1	–	Covered
bin auto[2048:3071]	12	1	–	Covered
bin auto[3072:4095]	16	1	–	Covered
bin auto[4096:5119]	18	1	–	Covered
bin auto[5120:6143]	11	1	–	Covered
bin auto[6144:7167]	20	1	–	Covered
bin auto[7168:8191]	16	1	–	Covered
bin auto[8192:9215]	24	1	–	Covered
bin auto[9216:10239]	19	1	–	Covered
bin auto[10240:11263]	17	1	–	Covered
bin auto[11264:12287]	10	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	13	1	–	Covered
bin auto[14336:15359]	13	1	–	Covered
bin auto[15360:16383]	17	1	–	Covered
bin auto[16384:17407]	15	1	–	Covered
bin auto[17408:18431]	21	1	–	Covered
bin auto[18432:19455]	13	1	–	Covered
bin auto[19456:20479]	19	1	–	Covered
bin auto[20480:21503]	8	1	–	Covered
bin auto[21504:22527]	11	1	–	Covered
bin auto[22528:23551]	11	1	–	Covered
bin auto[23552:24575]	12	1	–	Covered
bin auto[24576:25599]	13	1	–	Covered
bin auto[25600:26623]	8	1	–	Covered
bin auto[26624:27647]	12	1	–	Covered
bin auto[27648:28671]	17	1	–	Covered
bin auto[28672:29695]	10	1	–	Covered
bin auto[29696:30719]	20	1	–	Covered
bin auto[30720:31743]	20	1	–	Covered
bin auto[31744:32767]	20	1	–	Covered
bin auto[32768:33791]	13	1	–	Covered
bin auto[33792:34815]	21	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	18	1	–	Covered
bin auto[36864:37887]	18	1	–	Covered
bin auto[37888:38911]	14	1	–	Covered
bin auto[38912:39935]	17	1	–	Covered
bin auto[39936:40959]	15	1	–	Covered
bin auto[40960:41983]	15	1	–	Covered
bin auto[41984:43007]	14	1	–	Covered
bin auto[43008:44031]	16	1	–	Covered
bin auto[44032:45055]	12	1	–	Covered
bin auto[45056:46079]	22	1	–	Covered

bin auto[46080:47103]	17	1	–	Covered
bin auto[47104:48127]	14	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	15	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	16	1	–	Covered
bin auto[52224:53247]	24	1	–	Covered
bin auto[53248:54271]	17	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered
bin auto[55296:56319]	18	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	19	1	–	Covered
bin auto[58368:59391]	15	1	–	Covered
bin auto[59392:60415]	14	1	–	Covered
bin auto[60416:61439]	17	1	–	Covered
bin auto[61440:62463]	12	1	–	Covered
bin auto[62464:63487]	16	1	–	Covered
bin auto[63488:64511]	24	1	–	Covered
bin auto[64512:65535]	16	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	731	1	–	Covered
bin auto[1]	277	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	291	1	–	Covered
bin auto[1]	717	1	–	Covered
Coverpoint data_out_cp	96.87%	100	–	Uncovered
covered/total bins:	62	64	–	
missing/total bins:	2	64	–	
% Hit:	96.87%	100	–	
bin auto[0:1023]	557	1	–	Covered
bin auto[1024:2047]	2	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	8	1	–	Covered
bin auto[5120:6143]	5	1	–	Covered
bin auto[6144:7167]	32	1	–	Covered
bin auto[7168:8191]	19	1	–	Covered
bin auto[8192:9215]	12	1	–	Covered
bin auto[9216:10239]	2	1	–	Covered
bin auto[10240:11263]	2	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	1	1	–	Covered
bin auto[13312:14335]	11	1	–	Covered
bin auto[14336:15359]	8	1	–	Covered
bin auto[15360:16383]	7	1	–	Covered
bin auto[16384:17407]	2	1	–	Covered
bin auto[17408:18431]	5	1	–	Covered
bin auto[18432:19455]	1	1	–	Covered
bin auto[19456:20479]	8	1	–	Covered
bin auto[20480:21503]	7	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	3	1	–	Covered
bin auto[24576:25599]	3	1	–	Covered
bin auto[25600:26623]	21	1	–	Covered
bin auto[26624:27647]	2	1	–	Covered
bin auto[27648:28671]	1	1	–	Covered
bin auto[28672:29695]	8	1	–	Covered
bin auto[29696:30719]	5	1	–	Covered
bin auto[30720:31743]	6	1	–	Covered
bin auto[31744:32767]	13	1	–	Covered
bin auto[32768:33791]	1	1	–	Covered
bin auto[33792:34815]	17	1	–	Covered
bin auto[34816:35839]	9	1	–	Covered
bin auto[35840:36863]	10	1	–	Covered
bin auto[36864:37887]	2	1	–	Covered
bin auto[37888:38911]	3	1	–	Covered
bin auto[38912:39935]	11	1	–	Covered
bin auto[39936:40959]	2	1	–	Covered
bin auto[40960:41983]	0	1	–	ZERO
bin auto[41984:43007]	4	1	–	Covered
bin auto[43008:44031]	14	1	–	Covered
bin auto[44032:45055]	8	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered
bin auto[46080:47103]	15	1	–	Covered
bin auto[47104:48127]	5	1	–	Covered
bin auto[48128:49151]	11	1	–	Covered
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	6	1	–	Covered
bin auto[51200:52223]	9	1	–	Covered
bin auto[52224:53247]	0	1	–	ZERO
bin auto[53248:54271]	8	1	–	Covered
bin auto[54272:55295]	6	1	–	Covered
bin auto[55296:56319]	10	1	–	Covered
bin auto[56320:57343]	10	1	–	Covered
bin auto[57344:58367]	4	1	–	Covered

bin auto[58368:59391]	5	1	–	Covered
bin auto[59392:60415]	2	1	–	Covered
bin auto[60416:61439]	10	1	–	Covered
bin auto[61440:62463]	2	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	15	1	–	Covered
bin auto[64512:65535]	9	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	447	1	–	Covered
bin auto[1]	561	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	942	1	–	Covered
bin auto[1]	66	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	937	1	–	Covered
bin auto[1]	71	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	784	1	–	Covered
bin auto[1]	224	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	933	1	–	Covered
bin auto[1]	75	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	805	1	–	Covered
bin auto[1]	203	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	949	1	–	Covered
bin auto[1]	59	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	145	1	–	Covered
bin <auto[1],auto[1],auto[0]>	56	1	–	Covered
bin <auto[0],auto[1],auto[1]>	416	1	–	Covered
bin <auto[0],auto[1],auto[0]>	100	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[0],auto[0]>	215	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	62	1	–	Covered
bin <auto[0],auto[0],auto[1]>	9	1	–	Covered
bin <auto[1],auto[1],auto[0]>	201	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[1],auto[0]>	454	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	41	1	–	Covered
bin <auto[1],auto[0],auto[1]>	43	1	–	Covered
bin <auto[1],auto[1],auto[0]>	160	1	–	Covered
bin <auto[0],auto[1],auto[0]>	448	1	–	Covered
bin <auto[1],auto[0],auto[0]>	33	1	–	Covered
bin <auto[0],auto[0],auto[0]>	143	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	140		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	

% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	36	1	–	Covered
bin <auto[0],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[0],auto[1]>	6	1	–	Covered
bin <auto[0],auto[0],auto[1]>	13	1	–	Covered
bin <auto[1],auto[1],auto[0]>	165	1	–	Covered
bin <auto[0],auto[1],auto[0]>	496	1	–	Covered
bin <auto[1],auto[0],auto[0]>	70	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	61	1	–	Covered
bin <auto[0],auto[1],auto[1]>	99	1	–	Covered
bin <auto[1],auto[0],auto[1]>	7	1	–	Covered
bin <auto[0],auto[0],auto[1]>	36	1	–	Covered
bin <auto[1],auto[1],auto[0]>	140	1	–	Covered
bin <auto[0],auto[1],auto[0]>	417	1	–	Covered
bin <auto[1],auto[0],auto[0]>	69	1	–	Covered
bin <auto[0],auto[0],auto[0]>	179	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	27	1	–	Covered
bin <auto[1],auto[1],auto[0]>	174	1	–	Covered
bin <auto[0],auto[1],auto[1]>	39	1	–	Covered
bin <auto[0],auto[1],auto[0]>	477	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[0],auto[0]>	215	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	37	1	–	Covered
bin <auto[1],auto[0],auto[1]>	22	1	–	Covered
bin <auto[1],auto[1],auto[0]>	164	1	–	Covered
bin <auto[0],auto[1],auto[0]>	516	1	–	Covered
bin <auto[1],auto[0],auto[0]>	54	1	–	Covered
bin <auto[0],auto[0],auto[0]>	215	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100	–	Uncovered
covered/total bins:	192	194	–	
missing/total bins:	2	194	–	
% Hit:	98.96%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	156	1	–	Covered
bin auto[1]	852	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	22	1	–	Covered
bin auto[1024:2047]	15	1	–	Covered
bin auto[2048:3071]	12	1	–	Covered
bin auto[3072:4095]	16	1	–	Covered
bin auto[4096:5119]	18	1	–	Covered
bin auto[5120:6143]	11	1	–	Covered
bin auto[6144:7167]	20	1	–	Covered
bin auto[7168:8191]	16	1	–	Covered
bin auto[8192:9215]	24	1	–	Covered
bin auto[9216:10239]	19	1	–	Covered
bin auto[10240:11263]	17	1	–	Covered
bin auto[11264:12287]	10	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	13	1	–	Covered
bin auto[14336:15359]	13	1	–	Covered
bin auto[15360:16383]	17	1	–	Covered
bin auto[16384:17407]	15	1	–	Covered
bin auto[17408:18431]	21	1	–	Covered
bin auto[18432:19455]	13	1	–	Covered
bin auto[19456:20479]	19	1	–	Covered
bin auto[20480:21503]	8	1	–	Covered
bin auto[21504:22527]	11	1	–	Covered
bin auto[22528:23551]	11	1	–	Covered

bin auto[23552:24575]	12	1	–	Covered
bin auto[24576:25599]	13	1	–	Covered
bin auto[25600:26623]	8	1	–	Covered
bin auto[26624:27647]	12	1	–	Covered
bin auto[27648:28671]	17	1	–	Covered
bin auto[28672:29695]	10	1	–	Covered
bin auto[29696:30719]	20	1	–	Covered
bin auto[30720:31743]	20	1	–	Covered
bin auto[31744:32767]	20	1	–	Covered
bin auto[32768:33791]	13	1	–	Covered
bin auto[33792:34815]	21	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	18	1	–	Covered
bin auto[36864:37887]	18	1	–	Covered
bin auto[37888:38911]	14	1	–	Covered
bin auto[38912:39935]	17	1	–	Covered
bin auto[39936:40959]	15	1	–	Covered
bin auto[40960:41983]	15	1	–	Covered
bin auto[41984:43007]	14	1	–	Covered
bin auto[43008:44031]	16	1	–	Covered
bin auto[44032:45055]	12	1	–	Covered
bin auto[45056:46079]	22	1	–	Covered
bin auto[46080:47103]	17	1	–	Covered
bin auto[47104:48127]	14	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	15	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	16	1	–	Covered
bin auto[52224:53247]	24	1	–	Covered
bin auto[53248:54271]	17	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered
bin auto[55296:56319]	18	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	19	1	–	Covered
bin auto[58368:59391]	15	1	–	Covered
bin auto[59392:60415]	14	1	–	Covered
bin auto[60416:61439]	17	1	–	Covered
bin auto[61440:62463]	12	1	–	Covered
bin auto[62464:63487]	16	1	–	Covered
bin auto[63488:64511]	24	1	–	Covered
bin auto[64512:65535]	16	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	731	1	–	Covered
bin auto[1]	277	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	291	1	–	Covered
bin auto[1]	717	1	–	Covered
Coverpoint data_out_cp	96.87%	100	–	Uncovered
covered/total bins:	62	64	–	
missing/total bins:	2	64	–	
% Hit:	96.87%	100	–	
bin auto[0:1023]	557	1	–	Covered
bin auto[1024:2047]	2	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	8	1	–	Covered
bin auto[5120:6143]	5	1	–	Covered
bin auto[6144:7167]	32	1	–	Covered
bin auto[7168:8191]	19	1	–	Covered
bin auto[8192:9215]	12	1	–	Covered
bin auto[9216:10239]	2	1	–	Covered
bin auto[10240:11263]	2	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	1	1	–	Covered
bin auto[13312:14335]	11	1	–	Covered
bin auto[14336:15359]	8	1	–	Covered
bin auto[15360:16383]	7	1	–	Covered
bin auto[16384:17407]	2	1	–	Covered
bin auto[17408:18431]	5	1	–	Covered
bin auto[18432:19455]	1	1	–	Covered
bin auto[19456:20479]	8	1	–	Covered
bin auto[20480:21503]	7	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	3	1	–	Covered
bin auto[24576:25599]	3	1	–	Covered
bin auto[25600:26623]	21	1	–	Covered
bin auto[26624:27647]	2	1	–	Covered
bin auto[27648:28671]	1	1	–	Covered
bin auto[28672:29695]	8	1	–	Covered
bin auto[29696:30719]	5	1	–	Covered
bin auto[30720:31743]	6	1	–	Covered
bin auto[31744:32767]	13	1	–	Covered
bin auto[32768:33791]	1	1	–	Covered
bin auto[33792:34815]	17	1	–	Covered
bin auto[34816:35839]	9	1	–	Covered

bin auto[35840:36863]	10	1	–	Covered
bin auto[36864:37887]	2	1	–	Covered
bin auto[37888:38911]	3	1	–	Covered
bin auto[38912:39935]	11	1	–	Covered
bin auto[39936:40959]	2	1	–	Covered
bin auto[40960:41983]	0	1	–	ZERO
bin auto[41984:43007]	4	1	–	Covered
bin auto[43008:44031]	14	1	–	Covered
bin auto[44032:45055]	8	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered
bin auto[46080:47103]	15	1	–	Covered
bin auto[47104:48127]	5	1	–	Covered
bin auto[48128:49151]	11	1	–	Covered
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	6	1	–	Covered
bin auto[51200:52223]	9	1	–	Covered
bin auto[52224:53247]	0	1	–	ZERO
bin auto[53248:54271]	8	1	–	Covered
bin auto[54272:55295]	6	1	–	Covered
bin auto[55296:56319]	10	1	–	Covered
bin auto[56320:57343]	10	1	–	Covered
bin auto[57344:58367]	4	1	–	Covered
bin auto[58368:59391]	5	1	–	Covered
bin auto[59392:60415]	2	1	–	Covered
bin auto[60416:61439]	10	1	–	Covered
bin auto[61440:62463]	2	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	15	1	–	Covered
bin auto[64512:65535]	9	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	447	1	–	Covered
bin auto[1]	561	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	942	1	–	Covered
bin auto[1]	66	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	937	1	–	Covered
bin auto[1]	71	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	784	1	–	Covered
bin auto[1]	224	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	933	1	–	Covered
bin auto[1]	75	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	805	1	–	Covered
bin auto[1]	203	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	949	1	–	Covered
bin auto[1]	59	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	145	1	–	Covered
bin <auto[1],auto[1],auto[0]>	56	1	–	Covered
bin <auto[0],auto[1],auto[1]>	416	1	–	Covered
bin <auto[0],auto[1],auto[0]>	100	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[0],auto[0]>	215	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	62	1	–	Covered
bin <auto[0],auto[0],auto[1]>	9	1	–	Covered
bin <auto[1],auto[1],auto[0]>	201	1	–	Covered

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov...	SVA	✓	Off	853	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	853	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	853	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	2	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	23	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	159	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	67	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	62	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	191	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	44	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	28	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	472	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	156	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 2: SVA "Seed2"

```
        bin <auto[1],auto[0],auto[0]>                76          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                454         1          -    Covered
        bin <auto[0],auto[0],auto[0]>                206         1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin r_en_actv_wr_full                 0                      -    ZERO
        ignore_bin w_en_r_en_allactv_full            0                      -    ZERO
Cross empty_cross                                    100.00%     100        -    Covered
    covered/total bins:                              6           6          -
    missing/total bins:                              0           6          -
    % Hit:                                           100.00%     100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                41          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                43          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                160         1          -    Covered
        bin <auto[0],auto[1],auto[0]>                448         1          -    Covered
        bin <auto[1],auto[0],auto[0]>                33          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                143         1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin read_nactv_empty                  140                    -    Occurred
Cross almostfull_cross                               100.00%     100        -    Covered
    covered/total bins:                              8           8          -
    missing/total bins:                              0           8          -
    % Hit:                                           100.00%     100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                36          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                20          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                6           1          -    Covered
        bin <auto[0],auto[0],auto[1]>                13          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                165         1          -    Covered
        bin <auto[0],auto[1],auto[0]>                496         1          -    Covered
        bin <auto[1],auto[0],auto[0]>                70          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                202         1          -    Covered
Cross almostempty_cross                              100.00%     100        -    Covered
    covered/total bins:                              8           8          -
    missing/total bins:                              0           8          -
    % Hit:                                           100.00%     100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                61          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                99          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                7           1          -    Covered
        bin <auto[0],auto[0],auto[1]>                36          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                140         1          -    Covered
        bin <auto[0],auto[1],auto[0]>                417         1          -    Covered
        bin <auto[1],auto[0],auto[0]>                69          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                179         1          -    Covered
Cross overflow_cross                                 100.00%     100        -    Covered
    covered/total bins:                              6           6          -
    missing/total bins:                              0           6          -
    % Hit:                                           100.00%     100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                27          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                174         1          -    Covered
        bin <auto[0],auto[1],auto[1]>                39          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                477         1          -    Covered
        bin <auto[1],auto[0],auto[0]>                76          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                215         1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_wr_ack                 0                      -    ZERO
Cross underflow_cross                                100.00%     100        -    Covered
    covered/total bins:                              6           6          -
    missing/total bins:                              0           6          -
    % Hit:                                           100.00%     100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                37          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                22          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                164         1          -    Covered
        bin <auto[0],auto[1],auto[0]>                516         1          -    Covered
        bin <auto[1],auto[0],auto[0]>                54          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                215         1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin r_en_nactv_wr_ack                 0                      -    ZERO

TOTAL COVERGROUP COVERAGE: 99.83%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.83%
```

4.3 Functional Coverage "seed3" Report

Coverage Report by instance with details

```
=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================
```

Covergroup Coverage:

Covergroups	1	na	na	99.83%
Coverpoints/Crosses	19	na	na	na
Covergroup Bins	194	192	2	98.96%

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100	–	Uncovered
covered/total bins:	192	194	–	
missing/total bins:	2	194	–	
% Hit:	98.96%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	143	1	–	Covered
bin auto[1]	865	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	19	1	–	Covered
bin auto[1024:2047]	12	1	–	Covered
bin auto[2048:3071]	14	1	–	Covered
bin auto[3072:4095]	11	1	–	Covered
bin auto[4096:5119]	16	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	9	1	–	Covered
bin auto[7168:8191]	12	1	–	Covered
bin auto[8192:9215]	16	1	–	Covered
bin auto[9216:10239]	11	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	19	1	–	Covered
bin auto[12288:13311]	22	1	–	Covered
bin auto[13312:14335]	17	1	–	Covered
bin auto[14336:15359]	15	1	–	Covered
bin auto[15360:16383]	20	1	–	Covered
bin auto[16384:17407]	19	1	–	Covered
bin auto[17408:18431]	13	1	–	Covered
bin auto[18432:19455]	10	1	–	Covered
bin auto[19456:20479]	20	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	26	1	–	Covered
bin auto[22528:23551]	12	1	–	Covered
bin auto[23552:24575]	11	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	23	1	–	Covered
bin auto[26624:27647]	12	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	15	1	–	Covered
bin auto[29696:30719]	16	1	–	Covered
bin auto[30720:31743]	14	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered
bin auto[32768:33791]	10	1	–	Covered
bin auto[33792:34815]	11	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	15	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	22	1	–	Covered
bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	14	1	–	Covered
bin auto[41984:43007]	22	1	–	Covered
bin auto[43008:44031]	22	1	–	Covered
bin auto[44032:45055]	14	1	–	Covered
bin auto[45056:46079]	19	1	–	Covered
bin auto[46080:47103]	18	1	–	Covered
bin auto[47104:48127]	18	1	–	Covered
bin auto[48128:49151]	12	1	–	Covered
bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	14	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	13	1	–	Covered
bin auto[54272:55295]	12	1	–	Covered
bin auto[55296:56319]	16	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	19	1	–	Covered
bin auto[58368:59391]	14	1	–	Covered
bin auto[59392:60415]	18	1	–	Covered
bin auto[60416:61439]	19	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered

bin auto[62464:63487]	20	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	12	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	716	1	–	Covered
bin auto[1]	292	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	285	1	–	Covered
bin auto[1]	723	1	–	Covered
Coverpoint data_out_cp	96.87%	100	–	Uncovered
covered/total bins:	62	64	–	
missing/total bins:	2	64	–	
% Hit:	96.87%	100	–	
bin auto[0:1023]	502	1	–	Covered
bin auto[1024:2047]	4	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	3	1	–	Covered
bin auto[4096:5119]	3	1	–	Covered
bin auto[5120:6143]	3	1	–	Covered
bin auto[6144:7167]	7	1	–	Covered
bin auto[7168:8191]	6	1	–	Covered
bin auto[8192:9215]	5	1	–	Covered
bin auto[9216:10239]	4	1	–	Covered
bin auto[10240:11263]	11	1	–	Covered
bin auto[11264:12287]	25	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	4	1	–	Covered
bin auto[14336:15359]	4	1	–	Covered
bin auto[15360:16383]	10	1	–	Covered
bin auto[16384:17407]	11	1	–	Covered
bin auto[17408:18431]	10	1	–	Covered
bin auto[18432:19455]	6	1	–	Covered
bin auto[19456:20479]	22	1	–	Covered
bin auto[20480:21503]	1	1	–	Covered
bin auto[21504:22527]	9	1	–	Covered
bin auto[22528:23551]	3	1	–	Covered
bin auto[23552:24575]	0	1	–	ZERO
bin auto[24576:25599]	7	1	–	Covered
bin auto[25600:26623]	7	1	–	Covered
bin auto[26624:27647]	15	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	4	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	13	1	–	Covered
bin auto[31744:32767]	8	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	4	1	–	Covered
bin auto[34816:35839]	3	1	–	Covered
bin auto[35840:36863]	3	1	–	Covered
bin auto[36864:37887]	10	1	–	Covered
bin auto[37888:38911]	7	1	–	Covered
bin auto[38912:39935]	7	1	–	Covered
bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	12	1	–	Covered
bin auto[41984:43007]	16	1	–	Covered
bin auto[43008:44031]	8	1	–	Covered
bin auto[44032:45055]	9	1	–	Covered
bin auto[45056:46079]	6	1	–	Covered
bin auto[46080:47103]	3	1	–	Covered
bin auto[47104:48127]	1	1	–	Covered
bin auto[48128:49151]	2	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	1	1	–	Covered
bin auto[51200:52223]	15	1	–	Covered
bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	6	1	–	Covered
bin auto[54272:55295]	0	1	–	ZERO
bin auto[55296:56319]	6	1	–	Covered
bin auto[56320:57343]	17	1	–	Covered
bin auto[57344:58367]	25	1	–	Covered
bin auto[58368:59391]	7	1	–	Covered
bin auto[59392:60415]	6	1	–	Covered
bin auto[60416:61439]	4	1	–	Covered
bin auto[61440:62463]	20	1	–	Covered
bin auto[62464:63487]	8	1	–	Covered
bin auto[63488:64511]	3	1	–	Covered
bin auto[64512:65535]	10	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	432	1	–	Covered
bin auto[1]	576	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	

% Hit:	100.00%	100	–	
bin auto[0]	957	1	–	Covered
bin auto[1]	51	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	927	1	–	Covered
bin auto[1]	81	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	795	1	–	Covered
bin auto[1]	213	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	955	1	–	Covered
bin auto[1]	53	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	791	1	–	Covered
bin auto[1]	217	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	943	1	–	Covered
bin auto[1]	65	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	172	1	–	Covered
bin <auto[1],auto[1],auto[0]>	42	1	–	Covered
bin <auto[0],auto[1],auto[1]>	404	1	–	Covered
bin <auto[0],auto[1],auto[0]>	105	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[0],auto[0]>	207	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	59	1	–	Covered
bin <auto[0],auto[0],auto[1]>	22	1	–	Covered
bin <auto[1],auto[1],auto[0]>	214	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[1],auto[0]>	450	1	–	Covered
bin <auto[0],auto[0],auto[0]>	185	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	33	1	–	Covered
bin <auto[1],auto[0],auto[1]>	39	1	–	Covered
bin <auto[1],auto[1],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	437	1	–	Covered
bin <auto[1],auto[0],auto[0]>	39	1	–	Covered
bin <auto[0],auto[0],auto[0]>	138	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	141		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[0],auto[1],auto[1]>	17	1	–	Covered
bin <auto[1],auto[0],auto[1]>	8	1	–	Covered
bin <auto[0],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	194	1	–	Covered
bin <auto[0],auto[1],auto[0]>	492	1	–	Covered
bin <auto[1],auto[0],auto[0]>	70	1	–	Covered
bin <auto[0],auto[0],auto[0]>	199	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	79	1	–	Covered

bin <auto[0],auto[1],auto[1]>	91	1	–	Covered
bin <auto[1],auto[0],auto[1]>	11	1	–	Covered
bin <auto[0],auto[0],auto[1]>	36	1	–	Covered
bin <auto[1],auto[1],auto[0]>	135	1	–	Covered
bin <auto[0],auto[1],auto[0]>	418	1	–	Covered
bin <auto[1],auto[0],auto[0]>	67	1	–	Covered
bin <auto[0],auto[0],auto[0]>	171	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	12	1	–	Covered
bin <auto[1],auto[1],auto[0]>	202	1	–	Covered
bin <auto[0],auto[1],auto[1]>	39	1	–	Covered
bin <auto[0],auto[1],auto[0]>	470	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[0],auto[0]>	207	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	45	1	–	Covered
bin <auto[1],auto[0],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	169	1	–	Covered
bin <auto[0],auto[1],auto[0]>	509	1	–	Covered
bin <auto[1],auto[0],auto[0]>	58	1	–	Covered
bin <auto[0],auto[0],auto[0]>	207	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.83%	100	–	Uncovered
covered/total bins:	192	194	–	
missing/total bins:	2	194	–	
% Hit:	98.96%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	143	1	–	Covered
bin auto[1]	865	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	19	1	–	Covered
bin auto[1024:2047]	12	1	–	Covered
bin auto[2048:3071]	14	1	–	Covered
bin auto[3072:4095]	11	1	–	Covered
bin auto[4096:5119]	16	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	9	1	–	Covered
bin auto[7168:8191]	12	1	–	Covered
bin auto[8192:9215]	16	1	–	Covered
bin auto[9216:10239]	11	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	19	1	–	Covered
bin auto[12288:13311]	22	1	–	Covered
bin auto[13312:14335]	17	1	–	Covered
bin auto[14336:15359]	15	1	–	Covered
bin auto[15360:16383]	20	1	–	Covered
bin auto[16384:17407]	19	1	–	Covered
bin auto[17408:18431]	13	1	–	Covered
bin auto[18432:19455]	10	1	–	Covered
bin auto[19456:20479]	20	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	26	1	–	Covered
bin auto[22528:23551]	12	1	–	Covered
bin auto[23552:24575]	11	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	23	1	–	Covered
bin auto[26624:27647]	12	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	15	1	–	Covered
bin auto[29696:30719]	16	1	–	Covered
bin auto[30720:31743]	14	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered
bin auto[32768:33791]	10	1	–	Covered
bin auto[33792:34815]	11	1	–	Covered
bin auto[34816:35839]	14	1	–	Covered
bin auto[35840:36863]	15	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	22	1	–	Covered

bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	14	1	–	Covered
bin auto[41984:43007]	22	1	–	Covered
bin auto[43008:44031]	22	1	–	Covered
bin auto[44032:45055]	14	1	–	Covered
bin auto[45056:46079]	19	1	–	Covered
bin auto[46080:47103]	18	1	–	Covered
bin auto[47104:48127]	18	1	–	Covered
bin auto[48128:49151]	12	1	–	Covered
bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	14	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	13	1	–	Covered
bin auto[54272:55295]	12	1	–	Covered
bin auto[55296:56319]	16	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	19	1	–	Covered
bin auto[58368:59391]	14	1	–	Covered
bin auto[59392:60415]	18	1	–	Covered
bin auto[60416:61439]	19	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered
bin auto[62464:63487]	20	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	12	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	716	1	–	Covered
bin auto[1]	292	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	285	1	–	Covered
bin auto[1]	723	1	–	Covered
Coverpoint data_out_cp	96.87%	100	–	Uncovered
covered/total bins:	62	64	–	
missing/total bins:	2	64	–	
% Hit:	96.87%	100	–	
bin auto[0:1023]	502	1	–	Covered
bin auto[1024:2047]	4	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	3	1	–	Covered
bin auto[4096:5119]	3	1	–	Covered
bin auto[5120:6143]	3	1	–	Covered
bin auto[6144:7167]	7	1	–	Covered
bin auto[7168:8191]	6	1	–	Covered
bin auto[8192:9215]	5	1	–	Covered
bin auto[9216:10239]	4	1	–	Covered
bin auto[10240:11263]	11	1	–	Covered
bin auto[11264:12287]	25	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	4	1	–	Covered
bin auto[14336:15359]	4	1	–	Covered
bin auto[15360:16383]	10	1	–	Covered
bin auto[16384:17407]	11	1	–	Covered
bin auto[17408:18431]	10	1	–	Covered
bin auto[18432:19455]	6	1	–	Covered
bin auto[19456:20479]	22	1	–	Covered
bin auto[20480:21503]	1	1	–	Covered
bin auto[21504:22527]	9	1	–	Covered
bin auto[22528:23551]	3	1	–	Covered
bin auto[23552:24575]	0	1	–	ZERO
bin auto[24576:25599]	7	1	–	Covered
bin auto[25600:26623]	7	1	–	Covered
bin auto[26624:27647]	15	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	4	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	13	1	–	Covered
bin auto[31744:32767]	8	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	4	1	–	Covered
bin auto[34816:35839]	3	1	–	Covered
bin auto[35840:36863]	3	1	–	Covered
bin auto[36864:37887]	10	1	–	Covered
bin auto[37888:38911]	7	1	–	Covered
bin auto[38912:39935]	7	1	–	Covered
bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	12	1	–	Covered
bin auto[41984:43007]	16	1	–	Covered
bin auto[43008:44031]	8	1	–	Covered
bin auto[44032:45055]	9	1	–	Covered
bin auto[45056:46079]	6	1	–	Covered
bin auto[46080:47103]	3	1	–	Covered
bin auto[47104:48127]	1	1	–	Covered
bin auto[48128:49151]	2	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	1	1	–	Covered
bin auto[51200:52223]	15	1	–	Covered

bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	6	1	–	Covered
bin auto[54272:55295]	0	1	–	ZERO
bin auto[55296:56319]	6	1	–	Covered
bin auto[56320:57343]	17	1	–	Covered
bin auto[57344:58367]	25	1	–	Covered
bin auto[58368:59391]	7	1	–	Covered
bin auto[59392:60415]	6	1	–	Covered
bin auto[60416:61439]	4	1	–	Covered
bin auto[61440:62463]	20	1	–	Covered
bin auto[62464:63487]	8	1	–	Covered
bin auto[63488:64511]	3	1	–	Covered
bin auto[64512:65535]	10	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	432	1	–	Covered
bin auto[1]	576	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	957	1	–	Covered
bin auto[1]	51	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	927	1	–	Covered
bin auto[1]	81	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	795	1	–	Covered
bin auto[1]	213	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	955	1	–	Covered
bin auto[1]	53	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	791	1	–	Covered
bin auto[1]	217	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	943	1	–	Covered
bin auto[1]	65	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	172	1	–	Covered
bin <auto[1],auto[1],auto[0]>	42	1	–	Covered
bin <auto[0],auto[1],auto[1]>	404	1	–	Covered
bin <auto[0],auto[1],auto[0]>	105	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[0],auto[0]>	207	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	59	1	–	Covered
bin <auto[0],auto[0],auto[1]>	22	1	–	Covered
bin <auto[1],auto[1],auto[0]>	214	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[1],auto[0]>	450	1	–	Covered
bin <auto[0],auto[0],auto[0]>	185	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	33	1	–	Covered
bin <auto[1],auto[0],auto[1]>	39	1	–	Covered
bin <auto[1],auto[1],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	437	1	–	Covered
bin <auto[1],auto[0],auto[0]>	39	1	–	Covered

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov...	SVA	✓	Off	866	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	866	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	866	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	3	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	24	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	183	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	49	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	72	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	189	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	49	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	28	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	484	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	143	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 3: SVA "Seed3"

```
        bin <auto[0],auto[0],auto[0]>                138          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin read_nactv_empty                  141                     -    Occurred
Cross almostfull_cross                           100.00%        100          -    Covered
    covered/total bins:                                8          8          -
    missing/total bins:                                0          8          -
    % Hit:                                       100.00%        100          -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 20          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                 17          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                  8          1          -    Covered
        bin <auto[0],auto[0],auto[1]>                  8          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                194          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                492          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 70          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                199          1          -    Covered
Cross almostempty_cross                          100.00%        100          -    Covered
    covered/total bins:                                8          8          -
    missing/total bins:                                0          8          -
    % Hit:                                       100.00%        100          -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 79          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                 91          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                 11          1          -    Covered
        bin <auto[0],auto[0],auto[1]>                 36          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                135          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                418          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 67          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                171          1          -    Covered
Cross overflow_cross                             100.00%        100          -    Covered
    covered/total bins:                                6          6          -
    missing/total bins:                                0          6          -
    % Hit:                                       100.00%        100          -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 12          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                202          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                 39          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                470          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 78          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                207          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_wr_ack                   0                     -    ZERO
Cross underflow_cross                            100.00%        100          -    Covered
    covered/total bins:                                6          6          -
    missing/total bins:                                0          6          -
    % Hit:                                       100.00%        100          -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 45          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                 20          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                169          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                509          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 58          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                207          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin r_en_nactv_wr_ack                   0                     -    ZERO

TOTAL COVERGROUP COVERAGE: 99.83%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.83%
```

4.4 Functional Coverage "seed4" Report

```
Coverage Report by instance with details

=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.75%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   194       191         3    98.45%
---------------------------------------------------------------------------------
Covergroup                                  Metric       Goal       Bins     Status
```

TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100	–	Uncovered
covered/total bins:	191	194	–	
missing/total bins:	3	194	–	
% Hit:	98.45%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	159	1	–	Covered
bin auto[1]	849	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	17	1	–	Covered
bin auto[2048:3071]	10	1	–	Covered
bin auto[3072:4095]	18	1	–	Covered
bin auto[4096:5119]	18	1	–	Covered
bin auto[5120:6143]	14	1	–	Covered
bin auto[6144:7167]	16	1	–	Covered
bin auto[7168:8191]	26	1	–	Covered
bin auto[8192:9215]	15	1	–	Covered
bin auto[9216:10239]	15	1	–	Covered
bin auto[10240:11263]	12	1	–	Covered
bin auto[11264:12287]	18	1	–	Covered
bin auto[12288:13311]	15	1	–	Covered
bin auto[13312:14335]	13	1	–	Covered
bin auto[14336:15359]	19	1	–	Covered
bin auto[15360:16383]	16	1	–	Covered
bin auto[16384:17407]	13	1	–	Covered
bin auto[17408:18431]	17	1	–	Covered
bin auto[18432:19455]	17	1	–	Covered
bin auto[19456:20479]	21	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	13	1	–	Covered
bin auto[23552:24575]	18	1	–	Covered
bin auto[24576:25599]	18	1	–	Covered
bin auto[25600:26623]	16	1	–	Covered
bin auto[26624:27647]	21	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	16	1	–	Covered
bin auto[30720:31743]	11	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered
bin auto[32768:33791]	11	1	–	Covered
bin auto[33792:34815]	19	1	–	Covered
bin auto[34816:35839]	12	1	–	Covered
bin auto[35840:36863]	12	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	10	1	–	Covered
bin auto[39936:40959]	13	1	–	Covered
bin auto[40960:41983]	15	1	–	Covered
bin auto[41984:43007]	9	1	–	Covered
bin auto[43008:44031]	18	1	–	Covered
bin auto[44032:45055]	14	1	–	Covered
bin auto[45056:46079]	16	1	–	Covered
bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	15	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	16	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	21	1	–	Covered
bin auto[52224:53247]	11	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered
bin auto[55296:56319]	18	1	–	Covered
bin auto[56320:57343]	23	1	–	Covered
bin auto[57344:58367]	15	1	–	Covered
bin auto[58368:59391]	18	1	–	Covered
bin auto[59392:60415]	19	1	–	Covered
bin auto[60416:61439]	16	1	–	Covered
bin auto[61440:62463]	19	1	–	Covered
bin auto[62464:63487]	20	1	–	Covered
bin auto[63488:64511]	15	1	–	Covered
bin auto[64512:65535]	15	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	709	1	–	Covered
bin auto[1]	299	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	315	1	–	Covered
bin auto[1]	693	1	–	Covered

Coverpoint data_out_cp	95.31%	100	–	Uncovered
covered/total bins:	61	64	–	
missing/total bins:	3	64	–	
% Hit:	95.31%	100	–	
bin auto[0:1023]	541	1	–	Covered
bin auto[1024:2047]	5	1	–	Covered
bin auto[2048:3071]	5	1	–	Covered
bin auto[3072:4095]	6	1	–	Covered
bin auto[4096:5119]	9	1	–	Covered
bin auto[5120:6143]	8	1	–	Covered
bin auto[6144:7167]	4	1	–	Covered
bin auto[7168:8191]	17	1	–	Covered
bin auto[8192:9215]	18	1	–	Covered
bin auto[9216:10239]	9	1	–	Covered
bin auto[10240:11263]	5	1	–	Covered
bin auto[11264:12287]	3	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	14	1	–	Covered
bin auto[14336:15359]	5	1	–	Covered
bin auto[15360:16383]	9	1	–	Covered
bin auto[16384:17407]	8	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered
bin auto[18432:19455]	0	1	–	ZERO
bin auto[19456:20479]	3	1	–	Covered
bin auto[20480:21503]	8	1	–	Covered
bin auto[21504:22527]	0	1	–	ZERO
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	11	1	–	Covered
bin auto[24576:25599]	9	1	–	Covered
bin auto[25600:26623]	4	1	–	Covered
bin auto[26624:27647]	9	1	–	Covered
bin auto[27648:28671]	9	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	3	1	–	Covered
bin auto[30720:31743]	5	1	–	Covered
bin auto[31744:32767]	9	1	–	Covered
bin auto[32768:33791]	6	1	–	Covered
bin auto[33792:34815]	10	1	–	Covered
bin auto[34816:35839]	2	1	–	Covered
bin auto[35840:36863]	4	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	6	1	–	Covered
bin auto[38912:39935]	3	1	–	Covered
bin auto[39936:40959]	6	1	–	Covered
bin auto[40960:41983]	8	1	–	Covered
bin auto[41984:43007]	1	1	–	Covered
bin auto[43008:44031]	29	1	–	Covered
bin auto[44032:45055]	7	1	–	Covered
bin auto[45056:46079]	0	1	–	ZERO
bin auto[46080:47103]	6	1	–	Covered
bin auto[47104:48127]	15	1	–	Covered
bin auto[48128:49151]	5	1	–	Covered
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	4	1	–	Covered
bin auto[51200:52223]	12	1	–	Covered
bin auto[52224:53247]	12	1	–	Covered
bin auto[53248:54271]	7	1	–	Covered
bin auto[54272:55295]	2	1	–	Covered
bin auto[55296:56319]	5	1	–	Covered
bin auto[56320:57343]	18	1	–	Covered
bin auto[57344:58367]	6	1	–	Covered
bin auto[58368:59391]	8	1	–	Covered
bin auto[59392:60415]	2	1	–	Covered
bin auto[60416:61439]	1	1	–	Covered
bin auto[61440:62463]	11	1	–	Covered
bin auto[62464:63487]	7	1	–	Covered
bin auto[63488:64511]	9	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	443	1	–	Covered
bin auto[1]	565	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	977	1	–	Covered
bin auto[1]	31	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	972	1	–	Covered
bin auto[1]	36	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	772	1	–	Covered
bin auto[1]	236	1	–	Covered

Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	958	1	–	Covered
bin auto[1]	50	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	790	1	–	Covered
bin auto[1]	218	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	939	1	–	Covered
bin auto[1]	69	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	155	1	–	Covered
bin <auto[1],auto[1],auto[0]>	43	1	–	Covered
bin <auto[0],auto[1],auto[1]>	410	1	–	Covered
bin <auto[0],auto[1],auto[0]>	85	1	–	Covered
bin <auto[1],auto[0],auto[0]>	101	1	–	Covered
bin <auto[0],auto[0],auto[0]>	214	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	32	1	–	Covered
bin <auto[0],auto[0],auto[1]>	4	1	–	Covered
bin <auto[1],auto[1],auto[0]>	198	1	–	Covered
bin <auto[1],auto[0],auto[0]>	101	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	210	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	34	1	–	Covered
bin <auto[1],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	164	1	–	Covered
bin <auto[0],auto[1],auto[0]>	421	1	–	Covered
bin <auto[1],auto[0],auto[0]>	51	1	–	Covered
bin <auto[0],auto[0],auto[0]>	136	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	17	1	–	Covered
bin <auto[0],auto[1],auto[1]>	19	1	–	Covered
bin <auto[1],auto[0],auto[1]>	5	1	–	Covered
bin <auto[0],auto[0],auto[1]>	9	1	–	Covered
bin <auto[1],auto[1],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	476	1	–	Covered
bin <auto[1],auto[0],auto[0]>	96	1	–	Covered
bin <auto[0],auto[0],auto[0]>	205	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	71	1	–	Covered
bin <auto[0],auto[1],auto[1]>	97	1	–	Covered
bin <auto[1],auto[0],auto[1]>	12	1	–	Covered
bin <auto[0],auto[0],auto[1]>	38	1	–	Covered
bin <auto[1],auto[1],auto[0]>	127	1	–	Covered
bin <auto[0],auto[1],auto[0]>	398	1	–	Covered
bin <auto[1],auto[0],auto[0]>	89	1	–	Covered
bin <auto[0],auto[0],auto[0]>	176	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	14	1	–	Covered
bin <auto[1],auto[1],auto[0]>	184	1	–	Covered
bin <auto[0],auto[1],auto[1]>	17	1	–	Covered

bin <auto[0],auto[1],auto[0]>	478	1	–	Covered
bin <auto[1],auto[0],auto[0]>	101	1	–	Covered
bin <auto[0],auto[0],auto[0]>	214	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	45	1	–	Covered
bin <auto[1],auto[0],auto[1]>	24	1	–	Covered
bin <auto[1],auto[1],auto[0]>	153	1	–	Covered
bin <auto[0],auto[1],auto[0]>	495	1	–	Covered
bin <auto[1],auto[0],auto[0]>	77	1	–	Covered
bin <auto[0],auto[0],auto[0]>	214	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.75%	100	–	Uncovered
covered/total bins:	191	194	–	
missing/total bins:	3	194	–	
% Hit:	98.45%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	159	1	–	Covered
bin auto[1]	849	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	17	1	–	Covered
bin auto[2048:3071]	10	1	–	Covered
bin auto[3072:4095]	18	1	–	Covered
bin auto[4096:5119]	18	1	–	Covered
bin auto[5120:6143]	14	1	–	Covered
bin auto[6144:7167]	16	1	–	Covered
bin auto[7168:8191]	26	1	–	Covered
bin auto[8192:9215]	15	1	–	Covered
bin auto[9216:10239]	15	1	–	Covered
bin auto[10240:11263]	12	1	–	Covered
bin auto[11264:12287]	18	1	–	Covered
bin auto[12288:13311]	15	1	–	Covered
bin auto[13312:14335]	13	1	–	Covered
bin auto[14336:15359]	19	1	–	Covered
bin auto[15360:16383]	16	1	–	Covered
bin auto[16384:17407]	13	1	–	Covered
bin auto[17408:18431]	17	1	–	Covered
bin auto[18432:19455]	17	1	–	Covered
bin auto[19456:20479]	21	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	13	1	–	Covered
bin auto[23552:24575]	18	1	–	Covered
bin auto[24576:25599]	18	1	–	Covered
bin auto[25600:26623]	16	1	–	Covered
bin auto[26624:27647]	21	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	16	1	–	Covered
bin auto[30720:31743]	11	1	–	Covered
bin auto[31744:32767]	18	1	–	Covered
bin auto[32768:33791]	11	1	–	Covered
bin auto[33792:34815]	19	1	–	Covered
bin auto[34816:35839]	12	1	–	Covered
bin auto[35840:36863]	12	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	10	1	–	Covered
bin auto[39936:40959]	13	1	–	Covered
bin auto[40960:41983]	15	1	–	Covered
bin auto[41984:43007]	9	1	–	Covered
bin auto[43008:44031]	18	1	–	Covered
bin auto[44032:45055]	14	1	–	Covered
bin auto[45056:46079]	16	1	–	Covered
bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	15	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	16	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	21	1	–	Covered
bin auto[52224:53247]	11	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered

bin auto[55296:56319]	18	1	–	Covered
bin auto[56320:57343]	23	1	–	Covered
bin auto[57344:58367]	15	1	–	Covered
bin auto[58368:59391]	18	1	–	Covered
bin auto[59392:60415]	19	1	–	Covered
bin auto[60416:61439]	16	1	–	Covered
bin auto[61440:62463]	19	1	–	Covered
bin auto[62464:63487]	20	1	–	Covered
bin auto[63488:64511]	15	1	–	Covered
bin auto[64512:65535]	15	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	709	1	–	Covered
bin auto[1]	299	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	315	1	–	Covered
bin auto[1]	693	1	–	Covered
Coverpoint data_out_cp	95.31%	100	–	Uncovered
covered/total bins:	61	64	–	
missing/total bins:	3	64	–	
% Hit:	95.31%	100	–	
bin auto[0:1023]	541	1	–	Covered
bin auto[1024:2047]	5	1	–	Covered
bin auto[2048:3071]	5	1	–	Covered
bin auto[3072:4095]	6	1	–	Covered
bin auto[4096:5119]	9	1	–	Covered
bin auto[5120:6143]	8	1	–	Covered
bin auto[6144:7167]	4	1	–	Covered
bin auto[7168:8191]	17	1	–	Covered
bin auto[8192:9215]	18	1	–	Covered
bin auto[9216:10239]	9	1	–	Covered
bin auto[10240:11263]	5	1	–	Covered
bin auto[11264:12287]	3	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	14	1	–	Covered
bin auto[14336:15359]	5	1	–	Covered
bin auto[15360:16383]	9	1	–	Covered
bin auto[16384:17407]	8	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered
bin auto[18432:19455]	0	1	–	ZERO
bin auto[19456:20479]	3	1	–	Covered
bin auto[20480:21503]	8	1	–	Covered
bin auto[21504:22527]	0	1	–	ZERO
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	11	1	–	Covered
bin auto[24576:25599]	9	1	–	Covered
bin auto[25600:26623]	4	1	–	Covered
bin auto[26624:27647]	9	1	–	Covered
bin auto[27648:28671]	9	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	3	1	–	Covered
bin auto[30720:31743]	5	1	–	Covered
bin auto[31744:32767]	9	1	–	Covered
bin auto[32768:33791]	6	1	–	Covered
bin auto[33792:34815]	10	1	–	Covered
bin auto[34816:35839]	2	1	–	Covered
bin auto[35840:36863]	4	1	–	Covered
bin auto[36864:37887]	12	1	–	Covered
bin auto[37888:38911]	6	1	–	Covered
bin auto[38912:39935]	3	1	–	Covered
bin auto[39936:40959]	6	1	–	Covered
bin auto[40960:41983]	8	1	–	Covered
bin auto[41984:43007]	1	1	–	Covered
bin auto[43008:44031]	29	1	–	Covered
bin auto[44032:45055]	7	1	–	Covered
bin auto[45056:46079]	0	1	–	ZERO
bin auto[46080:47103]	6	1	–	Covered
bin auto[47104:48127]	15	1	–	Covered
bin auto[48128:49151]	5	1	–	Covered
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	4	1	–	Covered
bin auto[51200:52223]	12	1	–	Covered
bin auto[52224:53247]	12	1	–	Covered
bin auto[53248:54271]	7	1	–	Covered
bin auto[54272:55295]	2	1	–	Covered
bin auto[55296:56319]	5	1	–	Covered
bin auto[56320:57343]	18	1	–	Covered
bin auto[57344:58367]	6	1	–	Covered
bin auto[58368:59391]	8	1	–	Covered
bin auto[59392:60415]	2	1	–	Covered
bin auto[60416:61439]	1	1	–	Covered
bin auto[61440:62463]	11	1	–	Covered
bin auto[62464:63487]	7	1	–	Covered
bin auto[63488:64511]	9	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	

missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	443	1	–	Covered
bin auto[1]	565	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	977	1	–	Covered
bin auto[1]	31	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	972	1	–	Covered
bin auto[1]	36	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	772	1	–	Covered
bin auto[1]	236	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	958	1	–	Covered
bin auto[1]	50	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	790	1	–	Covered
bin auto[1]	218	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	939	1	–	Covered
bin auto[1]	69	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	155	1	–	Covered
bin <auto[1],auto[1],auto[0]>	43	1	–	Covered
bin <auto[0],auto[1],auto[1]>	410	1	–	Covered
bin <auto[0],auto[1],auto[0]>	85	1	–	Covered
bin <auto[1],auto[0],auto[0]>	101	1	–	Covered
bin <auto[0],auto[0],auto[0]>	214	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	32	1	–	Covered
bin <auto[0],auto[0],auto[1]>	4	1	–	Covered
bin <auto[1],auto[1],auto[0]>	198	1	–	Covered
bin <auto[1],auto[0],auto[0]>	101	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	210	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	34	1	–	Covered
bin <auto[1],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	164	1	–	Covered
bin <auto[0],auto[1],auto[0]>	421	1	–	Covered
bin <auto[1],auto[0],auto[0]>	51	1	–	Covered
bin <auto[0],auto[0],auto[0]>	136	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	17	1	–	Covered
bin <auto[0],auto[1],auto[1]>	19	1	–	Covered
bin <auto[1],auto[0],auto[1]>	5	1	–	Covered
bin <auto[0],auto[0],auto[1]>	9	1	–	Covered
bin <auto[1],auto[1],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	476	1	–	Covered
bin <auto[1],auto[0],auto[0]>	96	1	–	Covered

```
        bin <auto[0],auto[0],auto[0]>                205          1          -    Covered
Cross almostempty_cross                              100.00%      100        -    Covered
    covered/total bins:                                8          8          -
    missing/total bins:                                0          8          -
    % Hit:                                         100.00%      100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 71          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                 97          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                 12          1          -    Covered
        bin <auto[0],auto[0],auto[1]>                 38          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                127          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                398          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 89          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                176          1          -    Covered
Cross overflow_cross                                 100.00%      100        -    Covered
    covered/total bins:                                6          6          -
    missing/total bins:                                0          6          -
    % Hit:                                         100.00%      100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 14          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                184          1          -    Covered
        bin <auto[0],auto[1],auto[1]>                 17          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                478          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                101          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                214          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_wr_ack                   0                     -    ZERO
Cross underflow_cross                                100.00%      100        -    Covered
    covered/total bins:                                6          6          -
    missing/total bins:                                0          6          -
    % Hit:                                         100.00%      100        -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 45          1          -    Covered
        bin <auto[1],auto[0],auto[1]>                 24          1          -    Covered
        bin <auto[1],auto[1],auto[0]>                153          1          -    Covered
        bin <auto[0],auto[1],auto[0]>                495          1          -    Covered
        bin <auto[1],auto[0],auto[0]>                 77          1          -    Covered
        bin <auto[0],auto[0],auto[0]>                214          1          -    Covered
    Illegal and Ignore Bins:
        ignore_bin r_en_nactv_wr_ack                   0                     -    ZERO

TOTAL COVERGROUP COVERAGE: 99.75%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.75%
```

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov...	SVA	✓	Off	850	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	850	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	850	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	1	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	21	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	181	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	43	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	29	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	197	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	55	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	9	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	484	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	159	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 4: SVA "Seed4"

4.5 Functional Coverage "seed5" Report

```
Coverage Report by instance with details

=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                      1        na        na    99.91%
        Coverpoints/Crosses         19        na        na        na
            Covergroup Bins        194       193         1    99.48%
--------------------------------------------------------------------------------
Covergroup                                          Metric         Goal       Bins    Status
--------------------------------------------------------------------------------
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg       99.91%          100          -    Uncovered
    covered/total bins:                               193          194          -
    missing/total bins:                                 1          194          -
    % Hit:                                         99.48%          100          -
    Coverpoint rst_n_cp                           100.00%          100          -    Covered
        covered/total bins:                             2            2          -
        missing/total bins:                             0            2          -
        % Hit:                                    100.00%          100          -
        bin auto[0]                                   162            1          -    Covered
        bin auto[1]                                   846            1          -    Covered
    Coverpoint data_in_cp                         100.00%          100          -    Covered
        covered/total bins:                            64           64          -
        missing/total bins:                             0           64          -
        % Hit:                                    100.00%          100          -
```

bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	12	1	–	Covered
bin auto[2048:3071]	21	1	–	Covered
bin auto[3072:4095]	14	1	–	Covered
bin auto[4096:5119]	19	1	–	Covered
bin auto[5120:6143]	17	1	–	Covered
bin auto[6144:7167]	12	1	–	Covered
bin auto[7168:8191]	16	1	–	Covered
bin auto[8192:9215]	9	1	–	Covered
bin auto[9216:10239]	10	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	21	1	–	Covered
bin auto[12288:13311]	16	1	–	Covered
bin auto[13312:14335]	9	1	–	Covered
bin auto[14336:15359]	16	1	–	Covered
bin auto[15360:16383]	14	1	–	Covered
bin auto[16384:17407]	21	1	–	Covered
bin auto[17408:18431]	18	1	–	Covered
bin auto[18432:19455]	18	1	–	Covered
bin auto[19456:20479]	19	1	–	Covered
bin auto[20480:21503]	16	1	–	Covered
bin auto[21504:22527]	14	1	–	Covered
bin auto[22528:23551]	17	1	–	Covered
bin auto[23552:24575]	17	1	–	Covered
bin auto[24576:25599]	16	1	–	Covered
bin auto[25600:26623]	25	1	–	Covered
bin auto[26624:27647]	14	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	18	1	–	Covered
bin auto[29696:30719]	10	1	–	Covered
bin auto[30720:31743]	18	1	–	Covered
bin auto[31744:32767]	10	1	–	Covered
bin auto[32768:33791]	19	1	–	Covered
bin auto[33792:34815]	17	1	–	Covered
bin auto[34816:35839]	21	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	20	1	–	Covered
bin auto[37888:38911]	17	1	–	Covered
bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	16	1	–	Covered
bin auto[41984:43007]	21	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	10	1	–	Covered
bin auto[45056:46079]	11	1	–	Covered
bin auto[46080:47103]	9	1	–	Covered
bin auto[47104:48127]	12	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	21	1	–	Covered
bin auto[50176:51199]	16	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	15	1	–	Covered
bin auto[54272:55295]	13	1	–	Covered
bin auto[55296:56319]	13	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	14	1	–	Covered
bin auto[58368:59391]	13	1	–	Covered
bin auto[59392:60415]	14	1	–	Covered
bin auto[60416:61439]	19	1	–	Covered
bin auto[61440:62463]	19	1	–	Covered
bin auto[62464:63487]	12	1	–	Covered
bin auto[63488:64511]	17	1	–	Covered
bin auto[64512:65535]	16	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	713	1	–	Covered
bin auto[1]	295	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	297	1	–	Covered
bin auto[1]	711	1	–	Covered
Coverpoint data_out_cp	98.43%	100	–	Uncovered
covered/total bins:	63	64	–	
missing/total bins:	1	64	–	
% Hit:	98.43%	100	–	
bin auto[0:1023]	506	1	–	Covered
bin auto[1024:2047]	3	1	–	Covered
bin auto[2048:3071]	18	1	–	Covered
bin auto[3072:4095]	1	1	–	Covered
bin auto[4096:5119]	10	1	–	Covered
bin auto[5120:6143]	9	1	–	Covered
bin auto[6144:7167]	13	1	–	Covered
bin auto[7168:8191]	8	1	–	Covered
bin auto[8192:9215]	2	1	–	Covered
bin auto[9216:10239]	1	1	–	Covered
bin auto[10240:11263]	7	1	–	Covered
bin auto[11264:12287]	8	1	–	Covered

bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	2	1	–	Covered
bin auto[14336:15359]	12	1	–	Covered
bin auto[15360:16383]	5	1	–	Covered
bin auto[16384:17407]	30	1	–	Covered
bin auto[17408:18431]	5	1	–	Covered
bin auto[18432:19455]	7	1	–	Covered
bin auto[19456:20479]	10	1	–	Covered
bin auto[20480:21503]	13	1	–	Covered
bin auto[21504:22527]	2	1	–	Covered
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	9	1	–	Covered
bin auto[24576:25599]	7	1	–	Covered
bin auto[25600:26623]	5	1	–	Covered
bin auto[26624:27647]	4	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	15	1	–	Covered
bin auto[29696:30719]	2	1	–	Covered
bin auto[30720:31743]	0	1	–	ZERO
bin auto[31744:32767]	3	1	–	Covered
bin auto[32768:33791]	5	1	–	Covered
bin auto[33792:34815]	13	1	–	Covered
bin auto[34816:35839]	22	1	–	Covered
bin auto[35840:36863]	2	1	–	Covered
bin auto[36864:37887]	3	1	–	Covered
bin auto[37888:38911]	14	1	–	Covered
bin auto[38912:39935]	6	1	–	Covered
bin auto[39936:40959]	6	1	–	Covered
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	26	1	–	Covered
bin auto[43008:44031]	4	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	3	1	–	Covered
bin auto[47104:48127]	4	1	–	Covered
bin auto[48128:49151]	8	1	–	Covered
bin auto[49152:50175]	23	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	3	1	–	Covered
bin auto[53248:54271]	3	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered
bin auto[55296:56319]	2	1	–	Covered
bin auto[56320:57343]	7	1	–	Covered
bin auto[57344:58367]	3	1	–	Covered
bin auto[58368:59391]	4	1	–	Covered
bin auto[59392:60415]	1	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	2	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	433	1	–	Covered
bin auto[1]	575	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	959	1	–	Covered
bin auto[1]	49	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	949	1	–	Covered
bin auto[1]	59	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	780	1	–	Covered
bin auto[1]	228	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	953	1	–	Covered
bin auto[1]	55	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	777	1	–	Covered
bin auto[1]	231	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	

bin auto[0]	950	1	–	Covered
bin auto[1]	58	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	168	1	–	Covered
bin <auto[1],auto[1],auto[0]>	32	1	–	Covered
bin <auto[0],auto[1],auto[1]>	407	1	–	Covered
bin <auto[0],auto[1],auto[0]>	104	1	–	Covered
bin <auto[1],auto[0],auto[0]>	95	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	48	1	–	Covered
bin <auto[0],auto[0],auto[1]>	11	1	–	Covered
bin <auto[1],auto[1],auto[0]>	200	1	–	Covered
bin <auto[1],auto[0],auto[0]>	95	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	191	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	23	1	–	Covered
bin <auto[1],auto[0],auto[1]>	53	1	–	Covered
bin <auto[1],auto[1],auto[0]>	177	1	–	Covered
bin <auto[0],auto[1],auto[0]>	435	1	–	Covered
bin <auto[1],auto[0],auto[0]>	42	1	–	Covered
bin <auto[0],auto[0],auto[0]>	126	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	24	1	–	Covered
bin <auto[0],auto[1],auto[1]>	22	1	–	Covered
bin <auto[1],auto[0],auto[1]>	1	1	–	Covered
bin <auto[0],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	176	1	–	Covered
bin <auto[0],auto[1],auto[0]>	489	1	–	Covered
bin <auto[1],auto[0],auto[0]>	94	1	–	Covered
bin <auto[0],auto[0],auto[0]>	194	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	82	1	–	Covered
bin <auto[0],auto[1],auto[1]>	103	1	–	Covered
bin <auto[1],auto[0],auto[1]>	6	1	–	Covered
bin <auto[0],auto[0],auto[1]>	40	1	–	Covered
bin <auto[1],auto[1],auto[0]>	118	1	–	Covered
bin <auto[0],auto[1],auto[0]>	408	1	–	Covered
bin <auto[1],auto[0],auto[0]>	89	1	–	Covered
bin <auto[0],auto[0],auto[0]>	162	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	15	1	–	Covered
bin <auto[1],auto[1],auto[0]>	185	1	–	Covered
bin <auto[0],auto[1],auto[1]>	34	1	–	Covered
bin <auto[0],auto[1],auto[0]>	477	1	–	Covered
bin <auto[1],auto[0],auto[0]>	95	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	41	1	–	Covered
bin <auto[1],auto[0],auto[1]>	17	1	–	Covered
bin <auto[1],auto[1],auto[0]>	159	1	–	Covered
bin <auto[0],auto[1],auto[0]>	511	1	–	Covered
bin <auto[1],auto[0],auto[0]>	78	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered

Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.91%	100	–	Uncovered
covered/total bins:	193	194	–	
missing/total bins:	1	194	–	
% Hit:	99.48%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	162	1	–	Covered
bin auto[1]	846	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	18	1	–	Covered
bin auto[1024:2047]	12	1	–	Covered
bin auto[2048:3071]	21	1	–	Covered
bin auto[3072:4095]	14	1	–	Covered
bin auto[4096:5119]	19	1	–	Covered
bin auto[5120:6143]	17	1	–	Covered
bin auto[6144:7167]	12	1	–	Covered
bin auto[7168:8191]	16	1	–	Covered
bin auto[8192:9215]	9	1	–	Covered
bin auto[9216:10239]	10	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	21	1	–	Covered
bin auto[12288:13311]	16	1	–	Covered
bin auto[13312:14335]	9	1	–	Covered
bin auto[14336:15359]	16	1	–	Covered
bin auto[15360:16383]	14	1	–	Covered
bin auto[16384:17407]	21	1	–	Covered
bin auto[17408:18431]	18	1	–	Covered
bin auto[18432:19455]	18	1	–	Covered
bin auto[19456:20479]	19	1	–	Covered
bin auto[20480:21503]	16	1	–	Covered
bin auto[21504:22527]	14	1	–	Covered
bin auto[22528:23551]	17	1	–	Covered
bin auto[23552:24575]	17	1	–	Covered
bin auto[24576:25599]	16	1	–	Covered
bin auto[25600:26623]	25	1	–	Covered
bin auto[26624:27647]	14	1	–	Covered
bin auto[27648:28671]	15	1	–	Covered
bin auto[28672:29695]	18	1	–	Covered
bin auto[29696:30719]	10	1	–	Covered
bin auto[30720:31743]	18	1	–	Covered
bin auto[31744:32767]	10	1	–	Covered
bin auto[32768:33791]	19	1	–	Covered
bin auto[33792:34815]	17	1	–	Covered
bin auto[34816:35839]	21	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	20	1	–	Covered
bin auto[37888:38911]	17	1	–	Covered
bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	18	1	–	Covered
bin auto[40960:41983]	16	1	–	Covered
bin auto[41984:43007]	21	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	10	1	–	Covered
bin auto[45056:46079]	11	1	–	Covered
bin auto[46080:47103]	9	1	–	Covered
bin auto[47104:48127]	12	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	21	1	–	Covered
bin auto[50176:51199]	16	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	21	1	–	Covered
bin auto[53248:54271]	15	1	–	Covered
bin auto[54272:55295]	13	1	–	Covered
bin auto[55296:56319]	13	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	14	1	–	Covered
bin auto[58368:59391]	13	1	–	Covered
bin auto[59392:60415]	14	1	–	Covered
bin auto[60416:61439]	19	1	–	Covered
bin auto[61440:62463]	19	1	–	Covered
bin auto[62464:63487]	12	1	–	Covered
bin auto[63488:64511]	17	1	–	Covered
bin auto[64512:65535]	16	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	713	1	–	Covered
bin auto[1]	295	1	–	Covered

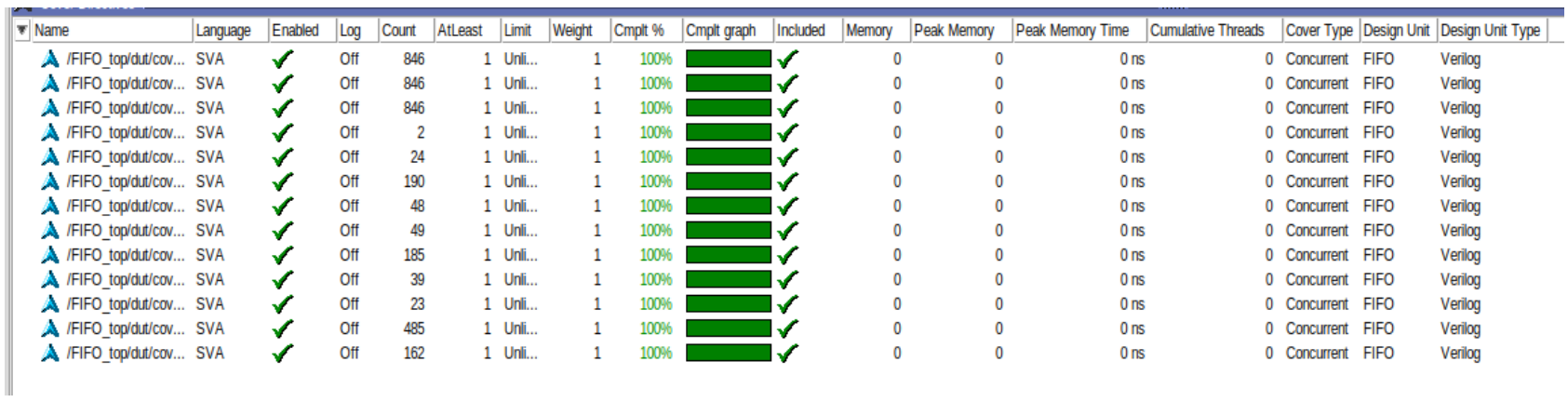
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	297	1	–	Covered
bin auto[1]	711	1	–	Covered
Coverpoint data_out_cp	98.43%	100	–	Uncovered
covered/total bins:	63	64	–	
missing/total bins:	1	64	–	
% Hit:	98.43%	100	–	
bin auto[0:1023]	506	1	–	Covered
bin auto[1024:2047]	3	1	–	Covered
bin auto[2048:3071]	18	1	–	Covered
bin auto[3072:4095]	1	1	–	Covered
bin auto[4096:5119]	10	1	–	Covered
bin auto[5120:6143]	9	1	–	Covered
bin auto[6144:7167]	13	1	–	Covered
bin auto[7168:8191]	8	1	–	Covered
bin auto[8192:9215]	2	1	–	Covered
bin auto[9216:10239]	1	1	–	Covered
bin auto[10240:11263]	7	1	–	Covered
bin auto[11264:12287]	8	1	–	Covered
bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	2	1	–	Covered
bin auto[14336:15359]	12	1	–	Covered
bin auto[15360:16383]	5	1	–	Covered
bin auto[16384:17407]	30	1	–	Covered
bin auto[17408:18431]	5	1	–	Covered
bin auto[18432:19455]	7	1	–	Covered
bin auto[19456:20479]	10	1	–	Covered
bin auto[20480:21503]	13	1	–	Covered
bin auto[21504:22527]	2	1	–	Covered
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	9	1	–	Covered
bin auto[24576:25599]	7	1	–	Covered
bin auto[25600:26623]	5	1	–	Covered
bin auto[26624:27647]	4	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	15	1	–	Covered
bin auto[29696:30719]	2	1	–	Covered
bin auto[30720:31743]	0	1	–	ZERO
bin auto[31744:32767]	3	1	–	Covered
bin auto[32768:33791]	5	1	–	Covered
bin auto[33792:34815]	13	1	–	Covered
bin auto[34816:35839]	22	1	–	Covered
bin auto[35840:36863]	2	1	–	Covered
bin auto[36864:37887]	3	1	–	Covered
bin auto[37888:38911]	14	1	–	Covered
bin auto[38912:39935]	6	1	–	Covered
bin auto[39936:40959]	6	1	–	Covered
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	26	1	–	Covered
bin auto[43008:44031]	4	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	3	1	–	Covered
bin auto[47104:48127]	4	1	–	Covered
bin auto[48128:49151]	8	1	–	Covered
bin auto[49152:50175]	23	1	–	Covered
bin auto[50176:51199]	13	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	3	1	–	Covered
bin auto[53248:54271]	3	1	–	Covered
bin auto[54272:55295]	18	1	–	Covered
bin auto[55296:56319]	2	1	–	Covered
bin auto[56320:57343]	7	1	–	Covered
bin auto[57344:58367]	3	1	–	Covered
bin auto[58368:59391]	4	1	–	Covered
bin auto[59392:60415]	1	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	2	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	12	1	–	Covered
bin auto[64512:65535]	8	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	433	1	–	Covered
bin auto[1]	575	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	959	1	–	Covered
bin auto[1]	49	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	949	1	–	Covered
bin auto[1]	59	1	–	Covered

Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	780	1	–	Covered
bin auto[1]	228	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	953	1	–	Covered
bin auto[1]	55	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	777	1	–	Covered
bin auto[1]	231	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	950	1	–	Covered
bin auto[1]	58	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	168	1	–	Covered
bin <auto[1],auto[1],auto[0]>	32	1	–	Covered
bin <auto[0],auto[1],auto[1]>	407	1	–	Covered
bin <auto[0],auto[1],auto[0]>	104	1	–	Covered
bin <auto[1],auto[0],auto[0]>	95	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	48	1	–	Covered
bin <auto[0],auto[0],auto[1]>	11	1	–	Covered
bin <auto[1],auto[1],auto[0]>	200	1	–	Covered
bin <auto[1],auto[0],auto[0]>	95	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	191	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	23	1	–	Covered
bin <auto[1],auto[0],auto[1]>	53	1	–	Covered
bin <auto[1],auto[1],auto[0]>	177	1	–	Covered
bin <auto[0],auto[1],auto[0]>	435	1	–	Covered
bin <auto[1],auto[0],auto[0]>	42	1	–	Covered
bin <auto[0],auto[0],auto[0]>	126	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	152		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	24	1	–	Covered
bin <auto[0],auto[1],auto[1]>	22	1	–	Covered
bin <auto[1],auto[0],auto[1]>	1	1	–	Covered
bin <auto[0],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	176	1	–	Covered
bin <auto[0],auto[1],auto[0]>	489	1	–	Covered
bin <auto[1],auto[0],auto[0]>	94	1	–	Covered
bin <auto[0],auto[0],auto[0]>	194	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	82	1	–	Covered
bin <auto[0],auto[1],auto[1]>	103	1	–	Covered
bin <auto[1],auto[0],auto[1]>	6	1	–	Covered
bin <auto[0],auto[0],auto[1]>	40	1	–	Covered
bin <auto[1],auto[1],auto[0]>	118	1	–	Covered
bin <auto[0],auto[1],auto[0]>	408	1	–	Covered
bin <auto[1],auto[0],auto[0]>	89	1	–	Covered
bin <auto[0],auto[0],auto[0]>	162	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	

```
        missing/total bins:                          0          6          -
        % Hit:                                 100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>           15          1          -    Covered
            bin <auto[1],auto[1],auto[0]>          185          1          -    Covered
            bin <auto[0],auto[1],auto[1]>           34          1          -    Covered
            bin <auto[0],auto[1],auto[0]>          477          1          -    Covered
            bin <auto[1],auto[0],auto[0]>           95          1          -    Covered
            bin <auto[0],auto[0],auto[0]>          202          1          -    Covered
        Illegal and Ignore Bins:
            ignore_bin w_en_nactv_wr_ack             0                     -    ZERO
    Cross underflow_cross                      100.00%        100          -    Covered
        covered/total bins:                          6          6          -
        missing/total bins:                          0          6          -
        % Hit:                                 100.00%        100          -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>           41          1          -    Covered
            bin <auto[1],auto[0],auto[1]>           17          1          -    Covered
            bin <auto[1],auto[1],auto[0]>          159          1          -    Covered
            bin <auto[0],auto[1],auto[0]>          511          1          -    Covered
            bin <auto[1],auto[0],auto[0]>           78          1          -    Covered
            bin <auto[0],auto[0],auto[0]>          202          1          -    Covered
        Illegal and Ignore Bins:
            ignore_bin r_en_nactv_wr_ack             0                     -    ZERO

TOTAL COVERGROUP COVERAGE: 99.91%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.91%
```



Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/FIFO_top/dut/cov...	SVA	✓	Off	846	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	846	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	846	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	2	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	24	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	190	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	48	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	49	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	185	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	39	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	23	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	485	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog
/FIFO_top/dut/cov...	SVA	✓	Off	162	1	Unli...	1	100%	✓		0	0	0 ns	0	Concurrent	FIFO	Verilog

Figure 5: SVA "Seed5"

5 Code Coverage Report

5.1 Code Coverage "seed1" Report

```
Coverage Report by DU with details

================================================================================
=== Design Unit: work.FIFO
================================================================================

Assertion Coverage:
    Assertions                       13          13           0     100.00%
--------------------------------------------------------------------------------
Name                                 File(Line)                    Failure      Pass
                                                                   Count        Count
--------------------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                                   0            1
work.FIFO::assert__read_ptr_threshold
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                                   0            1
work.FIFO::assert__write_ptr_threshold
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                                   0            1
work.FIFO::assert__read_ptr_wraparound
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                                   0            1
work.FIFO::assert__write_ptr_wraparound
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                                   0            1
work.FIFO::assert__almost_empty_check
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                                   0            1
work.FIFO::assert__almost_full_check
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                                   0            1
work.FIFO::assert__full_flag_check
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                                   0            1
work.FIFO::assert__empty_flag_check
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                                   0            1
work.FIFO::assert__underflow_check
                                     /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                                   0            1
```

```
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                          0          1
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                          0          1
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                          0          1
Branch Coverage:
    Enabled Coverage                Bins      Hits    Misses  Coverage
    ----------------                ----      ----    ------  --------
    Branches                          25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO
NOTE: The modification timestamp for source file '/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv' has been altered since com

    Line         Item                           Count     Source
    ----         ----                           -----     ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                          1135     Count coming in to IF
    13              1                            289         if (!fifo_intf.rst_n) begin
    18              1                            559         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                            287         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                           287     Count coming in to IF
    25              1                             26                 if (fifo_intf.full & fifo_intf.wr_en)
    27              1                            261                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                          1135     Count coming in to IF
    33              1                            289         if (!fifo_intf.rst_n) begin
    38              1                            213         else if (fifo_intf.rd_en && count != 0) begin
    42              1                            633         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                           633     Count coming in to IF
    43              1                             65                 if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                            568                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                          1045     Count coming in to IF
    51              1                            279         if (!fifo_intf.rst_n) begin
    54              1                            766         else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                           766     Count coming in to IF
    55              1                            371                 if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                             66                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                              4                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                             45                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                 280     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                           856     Count coming in to IF
    66              1                            255     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                            601     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                           856     Count coming in to IF
    67              1                            386     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                            470     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                           856     Count coming in to IF
    68              1                            261     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                            595     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                           856     Count coming in to IF
    69              1                            389     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                            467     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                Bins    Covered    Misses  Coverage
    ----------------                ----    -------    ------  --------
    Conditions                        28         26         2    92.85%
```

```
=================================Condition Details=================================

Condition Coverage for Design Unit work.FIFO —
NOTE: The modification timestamp for source file '/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv' has been altered since com

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     ------------  -------  ----------------------  --------------
  fifo_intf.wr_en         Y
      (count < 8)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:          1  fifo_intf.wr_en_0     -
  Row    2:          1  fifo_intf.wr_en_1     (count < 8)
  Row    3:          1  (count < 8)_0         fifo_intf.wr_en
  Row    4:          1  (count < 8)_1         fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
     ------------  -------  ----------------------  --------------
   fifo_intf.full         N  '_0' not hit            Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:     ***0***  fifo_intf.full_0      fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1      fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0     fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1     fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     ------------  -------  ----------------------  --------------
  fifo_intf.rd_en         Y
     (count != 0)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0     -
  Row    2:          1  fifo_intf.rd_en_1     (count != 0)
  Row    3:          1  (count != 0)_0         fifo_intf.rd_en
  Row    4:          1  (count != 0)_1         fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
     ------------  -------  ----------------------  --------------
  fifo_intf.empty         N  '_0' not hit            Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:     ***0***  fifo_intf.empty_0     fifo_intf.rd_en
  Row    2:          1  fifo_intf.empty_1     fifo_intf.rd_en
  Row    3:          1  fifo_intf.rd_en_0     fifo_intf.empty
  Row    4:          1  fifo_intf.rd_en_1     fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     ------------  -------  ----------------------  --------------
  fifo_intf.rd_en         Y
  fifo_intf.wr_en         Y
   fifo_intf.full         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0     (~fifo_intf.full && fifo_intf.wr_en)
  Row    2:          1  fifo_intf.rd_en_1     -
  Row    3:          1  fifo_intf.wr_en_0     ~fifo_intf.rd_en
  Row    4:          1  fifo_intf.wr_en_1     (~fifo_intf.full && ~fifo_intf.rd_en)
  Row    5:          1  fifo_intf.full_0      (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:          1  fifo_intf.full_1      (~fifo_intf.rd_en && fifo_intf.wr_en)

----------------Focused Condition View----------------
Line       57 Item    1  ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
```

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 66 Item 1 ((count == 8) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 8)_0	fifo_intf.rst_n
Row 2:	1	(count == 8)_1	-
Row 3:	1	fifo_intf.rst_n_0	~(count == 8)
Row 4:	1	fifo_intf.rst_n_1	~(count == 8)

----------Focused Condition View----------
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	-
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 ((count == (8 - 1)) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint

(count == (8 - 1))	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == (8 - 1))_0	fifo_intf.rst_n
Row 2:	1	(count == (8 - 1))_1	-
Row 3:	1	fifo_intf.rst_n_0	~(count == (8 - 1))
Row 4:	1	fifo_intf.rst_n_1	~(count == (8 - 1))

----------Focused Condition View----------
Line 69 Item 1 ((count == 1) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 1)_0	fifo_intf.rst_n
Row 2:	1	(count == 1)_1	-
Row 3:	1	fifo_intf.rst_n_0	~(count == 1)
Row 4:	1	fifo_intf.rst_n_1	~(count == 1)

Directive Coverage:
Directives 13 13 0 100.00%

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	847	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	847	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	847	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	2	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	19	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	187	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	23	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	32	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	194	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	58	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	20	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	473	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	161	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO —
NOTE: The modification timestamp for source file '/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv' has been altered since com

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1135	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	289	wr_ptr <= 0;
15	1	289	fifo_intf.wr_ack <= 0;
16	1	289	fifo_intf.overflow <= 0;

```
17                                          end
18                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19              1                    559       mem[wr_ptr] <= fifo_intf.data_in;
20              1                    559       fifo_intf.wr_ack <= 1;
21              1                    559       wr_ptr <= wr_ptr + 1;
22                                          end
23                                          else begin
24              1                    287       fifo_intf.wr_ack <= 0;
25                                             if (fifo_intf.full & fifo_intf.wr_en)
26              1                     26          fifo_intf.overflow <= 1;
27                                             else
28              1                    261          fifo_intf.overflow <= 0;
29                                          end
30                                        end
31
32              1                   1135    always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                          if (!fifo_intf.rst_n) begin
34              1                    289       rd_ptr <= 0;
35              1                    289       fifo_intf.underflow <= 0;
36              1                    289       fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                          end
38                                          else if (fifo_intf.rd_en && count != 0) begin
39              1                    213       fifo_intf.data_out <= mem[rd_ptr];
40              1                    213       rd_ptr <= rd_ptr + 1;
41                                          end
42                                          else begin
43                                             if (fifo_intf.empty & fifo_intf.rd_en)
44              1                     65          fifo_intf.underflow <= 1;
45                                             else
46              1                    568          fifo_intf.underflow <= 0;
47                                          end
48                                        end
49
50              1                   1045    always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                          if (!fifo_intf.rst_n) begin
52              1                    279       count <= 0;
53                                          end
54                                          else begin
55                                             if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                    371          count <= count + 1;
57                                             else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                     66          count <= count - 1;
59                                             else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                      4          count <= count - 1;
61                                             else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                     45          count <= count + 1;
63                                          end
64                                        end
65
66              1                    857    assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                    857    assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                    857    assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                    857    assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

Total Node Count	=	10
Toggled Node Count	=	10
Untoggled Node Count	=	0
Toggle Coverage	=	100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	847	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	847	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	847	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	2	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	19	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)		

```
                                                                         187 Covered
work.FIFO::cover__almost_full_check       FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
                                                                         23 Covered
work.FIFO::cover__full_flag_check         FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                         32 Covered
work.FIFO::cover__empty_flag_check        FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                                         194 Covered
work.FIFO::cover__underflow_check         FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                                         58 Covered
work.FIFO::cover__overflow_check          FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
                                                                         20 Covered
work.FIFO::cover__write_ack_check         FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                                         473 Covered
work.FIFO::cover__reset_behavior          FIFO   Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                         161 Covered

TOTAL DIRECTIVE COVERAGE: 100.00%   COVERS: 13

ASSERTION RESULTS:
--------------------------------------------------------------------
Name                    File(Line)                      Failure    Pass
                                                        Count      Count
--------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                              0          1
work.FIFO::assert__read_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                              0          1
work.FIFO::assert__write_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                              0          1
work.FIFO::assert__read_ptr_wraparound
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                              0          1
work.FIFO::assert__write_ptr_wraparound
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                              0          1
work.FIFO::assert__almost_empty_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                              0          1
work.FIFO::assert__almost_full_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                              0          1
work.FIFO::assert__full_flag_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                              0          1
work.FIFO::assert__empty_flag_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                              0          1
work.FIFO::assert__underflow_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                              0          1
work.FIFO::assert__overflow_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                              0          1
work.FIFO::assert__write_ack_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                              0          1
work.FIFO::assert__reset_behavior
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                              0          1

Total Coverage By Design Unit (filtered view): 98.80%
```

5.2 Code Coverage "seed2" Report

```
Coverage Report by DU with details

=================================================================================
=== Design Unit: work.FIFO
=================================================================================

Assertion Coverage:
    Assertions                      13         13          0    100.00%
--------------------------------------------------------------------
Name                    File(Line)                      Failure    Pass
                                                        Count      Count
--------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                              0          1
work.FIFO::assert__read_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                              0          1
work.FIFO::assert__write_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                              0          1
work.FIFO::assert__read_ptr_wraparound
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                              0          1
work.FIFO::assert__write_ptr_wraparound
```

```
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                        0          1
work.FIFO::assert__almost_empty_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                        0          1
work.FIFO::assert__almost_full_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                        0          1
work.FIFO::assert__full_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                        0          1
work.FIFO::assert__empty_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                        0          1
work.FIFO::assert__underflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                        0          1
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                        0          1
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                        0          1
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                        0          1
Branch Coverage:
    Enabled Coverage                Bins      Hits    Misses  Coverage
    ----------------                ----      ----    ------  --------
    Branches                          25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line          Item                          Count      Source
    ----          ----                          -----      ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                         1140      Count coming in to IF
    13              1                           288         if (!fifo_intf.rst_n) begin
    18              1                           562         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                           290         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                          290      Count coming in to IF
    25              1                            47                 if (fifo_intf.full & fifo_intf.wr_en)
    27              1                           243                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                         1140      Count coming in to IF
    33              1                           288         if (!fifo_intf.rst_n) begin
    38              1                           170         else if (fifo_intf.rd_en && count != 0) begin
    42              1                           682         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                          682      Count coming in to IF
    43              1                            53                 if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                           629                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                         1057      Count coming in to IF
    51              1                           277         if (!fifo_intf.rst_n) begin
    54              1                           780         else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                          780      Count coming in to IF
    55              1                           416                 if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                            41                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                            15                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                            32                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                276      All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                          627      Count coming in to IF
    66              1                            30      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                           597      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                          891      Count coming in to IF
    67              1                           395      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                           496      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
```

```
    68                                    627     Count coming in to IF
    68              1                      41     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                     586     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                    627     Count coming in to IF
    69              1                     138     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                     489     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
  fifo_intf.wr_en         Y
     (count < 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.wr_en_0       -
  Row    2:          1  fifo_intf.wr_en_1       (count < 8)
  Row    3:          1  (count < 8)_0           fifo_intf.wr_en
  Row    4:          1  (count < 8)_1           fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
   fifo_intf.full         N  '_0' not hit            Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0       fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1       fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
  fifo_intf.rd_en         Y
    (count != 0)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
  Row    3:          1  (count != 0)_0           fifo_intf.rd_en
  Row    4:          1  (count != 0)_1           fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
  fifo_intf.empty         N  '_0' not hit            Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.empty_0       fifo_intf.rd_en
  Row    2:          1  fifo_intf.empty_1       fifo_intf.rd_en
  Row    3:          1  fifo_intf.rd_en_0       fifo_intf.empty
  Row    4:          1  fifo_intf.rd_en_1       fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
     -----------  --------  ----------------------  --------------
```

fifo_intf.rd_en	Y
fifo_intf.wr_en	Y
fifo_intf.full	Y

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	–
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

——————Focused Condition View——————
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

——————Focused Condition View——————
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	–
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == (8 - 1))_0	–
Row 2:	1	(count == (8 - 1))_1	–

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 1)_0	–
Row 2:	1	(count == 1)_1	–

Directive Coverage:

Directives	13	13	0	100.00%

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	853	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	853	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	853	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	2	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	23	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	159	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	67	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	62	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	191	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	44	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	28	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	472	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	156	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			

```
12              1                    1140     always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13                                               if (!fifo_intf.rst_n) begin
14              1                     288                wr_ptr <= 0;
15              1                     288                fifo_intf.wr_ack <= 0;
16              1                     288                fifo_intf.overflow <= 0;
17                                               end
18                                               else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19              1                     562                mem[wr_ptr] <= fifo_intf.data_in;
20              1                     562                fifo_intf.wr_ack <= 1;
21              1                     562                wr_ptr <= wr_ptr + 1;
22                                               end
23                                               else begin
24              1                     290                fifo_intf.wr_ack <= 0;
25                                                       if (fifo_intf.full & fifo_intf.wr_en)
26              1                      47                       fifo_intf.overflow <= 1;
27                                                       else
28              1                     243                       fifo_intf.overflow <= 0;
29                                               end
30                                           end
31
32              1                    1140     always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                               if (!fifo_intf.rst_n) begin
34              1                     288                rd_ptr <= 0;
35              1                     288                fifo_intf.underflow <= 0;
36              1                     288                fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                               end
38                                               else if (fifo_intf.rd_en && count != 0) begin
39              1                     170                fifo_intf.data_out <= mem[rd_ptr];
40              1                     170                rd_ptr <= rd_ptr + 1;
41                                               end
42                                               else begin
43                                                       if (fifo_intf.empty & fifo_intf.rd_en)
44              1                      53                       fifo_intf.underflow <= 1;
45                                                       else
46              1                     629                       fifo_intf.underflow <= 0;
47                                               end
48                                           end
49
50              1                    1057     always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                               if (!fifo_intf.rst_n) begin
52              1                     277                count <= 0;
53                                               end
54                                               else begin
55                                                       if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                     416                       count <= count + 1;
57                                                       else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                      41                       count <= count - 1;
59                                                       else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                      15                       count <= count - 1;
61                                                       else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                      32                       count <= count + 1;
63                                               end
64                                           end
65
66              1                     628     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                     892     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                     628     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                     628     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

Total Node Count	=	10
Toggled Node Count	=	10
Untoggled Node Count	=	0
Toggle Coverage	=	100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	853	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	853	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	853	Covered

```
work.FIFO::cover__read_ptr_wraparound     FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
                                                                                                  2 Covered
work.FIFO::cover__write_ptr_wraparound    FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
                                                                                                 23 Covered
work.FIFO::cover__almost_empty_check      FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
                                                                                                159 Covered
work.FIFO::cover__almost_full_check       FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
                                                                                                 67 Covered
work.FIFO::cover__full_flag_check         FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                                                 62 Covered
work.FIFO::cover__empty_flag_check        FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                                                                191 Covered
work.FIFO::cover__underflow_check         FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                                                                 44 Covered
work.FIFO::cover__overflow_check          FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
                                                                                                 28 Covered
work.FIFO::cover__write_ack_check         FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                                                                472 Covered
work.FIFO::cover__reset_behavior          FIFO    Verilog  SVA  /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                                                156 Covered
```

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1
work.FIFO::assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	1
work.FIFO::assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)	0	1
work.FIFO::assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)	0	1
work.FIFO::assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)	0	1
work.FIFO::assert__almost_empty_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)	0	1
work.FIFO::assert__almost_full_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)	0	1
work.FIFO::assert__full_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)	0	1
work.FIFO::assert__empty_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)	0	1
work.FIFO::assert__underflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)	0	1
work.FIFO::assert__overflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)	0	1
work.FIFO::assert__write_ack_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)	0	1
work.FIFO::assert__reset_behavior	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)	0	1

Total Coverage By Design Unit (filtered view): 98.66%

5.3 Code Coverage "seed3" Report

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.FIFO
================================================================================

Assertion Coverage:
    Assertions                      13          13           0    100.00%
```

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1
work.FIFO::assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	1
work.FIFO::assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)		

```
                                                    0          1
work.FIFO::assert__read_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                    0          1
work.FIFO::assert__write_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                    0          1
work.FIFO::assert__almost_empty_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                    0          1
work.FIFO::assert__almost_full_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                    0          1
work.FIFO::assert__full_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                    0          1
work.FIFO::assert__empty_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                    0          1
work.FIFO::assert__underflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                    0          1
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                    0          1
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                    0          1
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                    0          1

Branch Coverage:
    Enabled Coverage                 Bins      Hits    Misses  Coverage
    ----------------                 ----      ----    ------  --------
    Branches                           25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                          Count     Source
    ----         ----                          -----     ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                         1132     Count coming in to IF
    13              1                           267        if (!fifo_intf.rst_n) begin
    18              1                           577        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                           288        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                          288     Count coming in to IF
    25              1                            42                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                           246                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                         1132     Count coming in to IF
    33              1                           267        if (!fifo_intf.rst_n) begin
    38              1                           192        else if (fifo_intf.rd_en && count != 0) begin
    42              1                           673        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                          673     Count coming in to IF
    43              1                            56                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                           617                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                         1068     Count coming in to IF
    51              1                           261        if (!fifo_intf.rst_n) begin
    54              1                           807        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                          807     Count coming in to IF
    55              1                           405                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                            52                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                             9                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                            41                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                 300     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                          626     Count coming in to IF
    66              1                            26     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                           600     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                          874     Count coming in to IF
```

```
    67              1                      380      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                      494      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                     626      Count coming in to IF
    68              1                       34      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                      592      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                     626      Count coming in to IF
    69              1                      143      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                      483      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  ------------
  fifo_intf.wr_en         Y
      (count < 8)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.wr_en_0       -
  Row    2:          1  fifo_intf.wr_en_1       (count < 8)
  Row    3:          1  (count < 8)_0           fifo_intf.wr_en
  Row    4:          1  (count < 8)_1           fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  ------------
   fifo_intf.full         N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0       fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1       fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  ------------
  fifo_intf.rd_en         Y
     (count != 0)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
  Row    3:          1  (count != 0)_0          fifo_intf.rd_en
  Row    4:          1  (count != 0)_1          fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  ------------
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.empty_0       fifo_intf.rd_en
  Row    2:          1  fifo_intf.empty_1       fifo_intf.rd_en
  Row    3:          1  fifo_intf.rd_en_0       fifo_intf.empty
  Row    4:          1  fifo_intf.rd_en_1       fifo_intf.empty

----------------Focused Condition View----------------
```

Line 55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	–
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

——————Focused Condition View——————
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

——————Focused Condition View——————
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

——————Focused Condition View——————
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	–
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == (8 - 1))_0	–
Row 2:	1	(count == (8 - 1))_1	–

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 1)_0	–
Row 2:	1	(count == 1)_1	–

Directive Coverage:
Directives 13 13 0 100.00%

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	866	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	866	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	866	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	3	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	24	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	183	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	49	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	72	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	189	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	49	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	28	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	484	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	143	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			

```
7                                       reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];  // 1-D Array
8
9                                       reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10                                      reg [max_fifo_addr:0] count;
11
12              1                 1132  always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13                                          if (!fifo_intf.rst_n) begin
14              1                  267              wr_ptr <= 0;
15              1                  267              fifo_intf.wr_ack <= 0;
16              1                  267              fifo_intf.overflow <= 0;
17                                          end
18                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19              1                  577              mem[wr_ptr] <= fifo_intf.data_in;
20              1                  577              fifo_intf.wr_ack <= 1;
21              1                  577              wr_ptr <= wr_ptr + 1;
22                                          end
23                                          else begin
24              1                  288              fifo_intf.wr_ack <= 0;
25                                               if (fifo_intf.full & fifo_intf.wr_en)
26              1                   42                       fifo_intf.overflow <= 1;
27                                               else
28              1                  246                       fifo_intf.overflow <= 0;
29                                          end
30                                      end
31
32              1                 1132  always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                          if (!fifo_intf.rst_n) begin
34              1                  267              rd_ptr <= 0;
35              1                  267              fifo_intf.underflow <= 0;
36              1                  267              fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                          end
38                                          else if (fifo_intf.rd_en && count != 0) begin
39              1                  192              fifo_intf.data_out <= mem[rd_ptr];
40              1                  192              rd_ptr <= rd_ptr + 1;
41                                          end
42                                          else begin
43                                               if (fifo_intf.empty & fifo_intf.rd_en)
44              1                   56                       fifo_intf.underflow <= 1;
45                                               else
46              1                  617                       fifo_intf.underflow <= 0;
47                                          end
48                                      end
49
50              1                 1068  always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                          if (!fifo_intf.rst_n) begin
52              1                  261              count <= 0;
53                                          end
54                                          else begin
55                                               if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                  405                       count <= count + 1;
57                                               else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                   52                       count <= count - 1;
59                                               else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                    9                       count <= count - 1;
61                                               else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                   41                       count <= count + 1;
63                                          end
64                                      end
65
66              1                  627  assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                  875  assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                  627  assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                  627  assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

Total Node Count	=	10
Toggled Node Count	=	10
Untoggled Node Count	=	0
Toggle Coverage	=	100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)		

					866 Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	
					866 Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	
					866 Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	
					3 Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	
					24 Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	
					183 Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	
					49 Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	
					72 Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	
					189 Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	
					49 Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	
					28 Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	
					484 Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	
					143 Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1
work.FIFO::assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	1
work.FIFO::assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)	0	1
work.FIFO::assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)	0	1
work.FIFO::assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)	0	1
work.FIFO::assert__almost_empty_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)	0	1
work.FIFO::assert__almost_full_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)	0	1
work.FIFO::assert__full_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)	0	1
work.FIFO::assert__empty_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)	0	1
work.FIFO::assert__underflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)	0	1
work.FIFO::assert__overflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)	0	1
work.FIFO::assert__write_ack_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)	0	1
work.FIFO::assert__reset_behavior	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)	0	1

Total Coverage By Design Unit (filtered view): 98.66%

5.4 Code Coverage "seed4" Report

Coverage Report by DU with details

==== Design Unit: work.FIFO

Assertion Coverage:

Assertions	13	13	0	100.00%

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1

```
work.FIFO::assert__read_ptr_threshold
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                        0          1
work.FIFO::assert__write_ptr_threshold
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                        0          1
work.FIFO::assert__read_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                        0          1
work.FIFO::assert__write_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                        0          1
work.FIFO::assert__almost_empty_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                        0          1
work.FIFO::assert__almost_full_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                        0          1
work.FIFO::assert__full_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                        0          1
work.FIFO::assert__empty_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                        0          1
work.FIFO::assert__underflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                        0          1
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                        0          1
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                        0          1
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                        0          1
Branch Coverage:
    Enabled Coverage                 Bins      Hits     Misses  Coverage
    ----------------                 ----      ----     ------  --------
    Branches                           25        25          0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                           Count      Source
    ----         ----                           -----      ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                          1135      Count coming in to IF
    13              1                            286         if (!fifo_intf.rst_n) begin
    18              1                            566         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                            283         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                          283      Count coming in to IF
    25              1                            20                 if (fifo_intf.full & fifo_intf.wr_en)
    27              1                            263                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                          1135      Count coming in to IF
    33              1                            286         if (!fifo_intf.rst_n) begin
    38              1                            193         else if (fifo_intf.rd_en && count != 0) begin
    42              1                            656         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                          656      Count coming in to IF
    43              1                            61                 if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                            595                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                         1071      Count coming in to IF
    51              1                            277         if (!fifo_intf.rst_n) begin
    54              1                            794         else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                          794      Count coming in to IF
    55              1                            410                 if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                             71                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                              9                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                             43                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                261      All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                          653      Count coming in to IF
    66              1                             21      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
```

```
    66              2                        632     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                       907     Count coming in to IF
    67              1                        394     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                        513     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                       653     Count coming in to IF
    68              1                         33     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                        620     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                       653     Count coming in to IF
    69              1                        152     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                        501     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins    Covered     Misses  Coverage
    ----------------              ----    -------     ------  --------
    Conditions                      25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----------
  fifo_intf.wr_en        Y
     (count < 8)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
  ---------  ---------  --------------------  --------------------------
  Row    1:          1  fifo_intf.wr_en_0     -
  Row    2:          1  fifo_intf.wr_en_1     (count < 8)
  Row    3:          1  (count < 8)_0         fifo_intf.wr_en
  Row    4:          1  (count < 8)_1         fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----------
   fifo_intf.full         N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
  ---------  ---------  --------------------  --------------------------
  Row    1:     ***0***  fifo_intf.full_0      fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1      fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0     fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1     fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----------
  fifo_intf.rd_en        Y
    (count != 0)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
  ---------  ---------  --------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0     -
  Row    2:          1  fifo_intf.rd_en_1     (count != 0)
  Row    3:          1  (count != 0)_0         fifo_intf.rd_en
  Row    4:          1  (count != 0)_1         fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----------
  fifo_intf.empty        N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en        Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
  ---------  ---------  --------------------  --------------------------
  Row    1:     ***0***  fifo_intf.empty_0     fifo_intf.rd_en
```

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 2:	1	fifo_intf.empty_1	fifo_intf.rd_en
Row 3:	1	fifo_intf.rd_en_0	fifo_intf.empty
Row 4:	1	fifo_intf.rd_en_1	fifo_intf.empty

----------Focused Condition View----------
Line 55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	–
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

```
----------------Focused Condition View-------------------
Line       67 Item    1  ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  -------------
     (count == 0)         Y
  fifo_intf.rst_n         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  ----------------------  --------------------------
  Row    1:          1  (count == 0)_0         fifo_intf.rst_n
  Row    2:          1  (count == 0)_1         -
  Row    3:          1  fifo_intf.rst_n_0      ~(count == 0)
  Row    4:          1  fifo_intf.rst_n_1      ~(count == 0)

----------------Focused Condition View-------------------
Line       68 Item    1  (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

         Input Term   Covered  Reason for no coverage   Hint
        -----------  --------  ----------------------  -------------
  (count == (8 - 1))         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  ----------------------  --------------------------
  Row    1:          1  (count == (8 - 1))_0   -
  Row    2:          1  (count == (8 - 1))_1   -

----------------Focused Condition View-------------------
Line       69 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  -------------
  (count == 1)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  ----------------------  --------------------------
  Row    1:          1  (count == 1)_0         -
  Row    2:          1  (count == 1)_1         -


Directive Coverage:
    Directives                  13         13          0    100.00%

DIRECTIVE COVERAGE:

Name                                  Design Unit  Design UnitType  Lang  File(Line)                                                                  Hits  Status
work.FIFO::cover__counter_threshold   FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)              850  Covered
work.FIFO::cover__read_ptr_threshold  FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)              850  Covered
work.FIFO::cover__write_ptr_threshold FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)              850  Covered
work.FIFO::cover__read_ptr_wraparound FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)                1  Covered
work.FIFO::cover__write_ptr_wraparound FIFO        Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)               21  Covered
work.FIFO::cover__almost_empty_check  FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)              181  Covered
work.FIFO::cover__almost_full_check   FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)               43  Covered
work.FIFO::cover__full_flag_check     FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)               29  Covered
work.FIFO::cover__empty_flag_check    FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)              197  Covered
work.FIFO::cover__underflow_check     FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)               55  Covered
work.FIFO::cover__overflow_check      FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)                9  Covered
work.FIFO::cover__write_ack_check     FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)              484  Covered
work.FIFO::cover__reset_behavior      FIFO         Verilog          SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)              159  Covered

Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      28        28         0   100.00%

================================Statement Details================================

Statement Coverage for Design Unit work.FIFO —

    Line         Item                           Count     Source
    ----         ----                           -----     ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
    1                                                     module FIFO(FIFO_IF.DUT fifo_intf);
```

```
2                                                 parameter FIFO_WIDTH = 16;
3                                                 parameter FIFO_DEPTH = 8;
4
5                                                 localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6
7                                                 reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];  // 1-D Array
8
9                                                 reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10                                                reg [max_fifo_addr:0] count;
11
12              1                          1135   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13                                                   if (!fifo_intf.rst_n) begin
14              1                           286           wr_ptr <= 0;
15              1                           286           fifo_intf.wr_ack <= 0;
16              1                           286           fifo_intf.overflow <= 0;
17                                                   end
18                                                   else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19              1                           566           mem[wr_ptr] <= fifo_intf.data_in;
20              1                           566           fifo_intf.wr_ack <= 1;
21              1                           566           wr_ptr <= wr_ptr + 1;
22                                                   end
23                                                   else begin
24              1                           283           fifo_intf.wr_ack <= 0;
25                                                    if (fifo_intf.full & fifo_intf.wr_en)
26              1                            20             fifo_intf.overflow <= 1;
27                                                    else
28              1                           263             fifo_intf.overflow <= 0;
29                                                   end
30                                                end
31
32              1                          1135   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                                   if (!fifo_intf.rst_n) begin
34              1                           286           rd_ptr <= 0;
35              1                           286           fifo_intf.underflow <= 0;
36              1                           286           fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                                   end
38                                                   else if (fifo_intf.rd_en && count != 0) begin
39              1                           193           fifo_intf.data_out <= mem[rd_ptr];
40              1                           193           rd_ptr <= rd_ptr + 1;
41                                                   end
42                                                   else begin
43                                                    if (fifo_intf.empty & fifo_intf.rd_en)
44              1                            61             fifo_intf.underflow <= 1;
45                                                    else
46              1                           595             fifo_intf.underflow <= 0;
47                                                   end
48                                                end
49
50              1                          1071   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                                   if (!fifo_intf.rst_n) begin
52              1                           277           count <= 0;
53                                                   end
54                                                   else begin
55                                                    if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                           410             count <= count + 1;
57                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                            71             count <= count - 1;
59                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                             9             count <= count - 1;
61                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                            43             count <= count + 1;
63                                                   end
64                                                end
65
66              1                           654   assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                           908   assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                           654   assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                           654   assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

Total Node Count	=	10
Toggled Node Count	=	10
Untoggled Node Count	=	0
Toggle Coverage	=	100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	850	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	850	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	850	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	1	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	21	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	181	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	43	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	29	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	197	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	55	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	9	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	484	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	159	Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1
work.FIFO::assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	1
work.FIFO::assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)	0	1
work.FIFO::assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)	0	1
work.FIFO::assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)	0	1
work.FIFO::assert__almost_empty_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)	0	1
work.FIFO::assert__almost_full_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)	0	1
work.FIFO::assert__full_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)	0	1
work.FIFO::assert__empty_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)	0	1
work.FIFO::assert__underflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)	0	1
work.FIFO::assert__overflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)	0	1
work.FIFO::assert__write_ack_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)	0	1
work.FIFO::assert__reset_behavior	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)	0	1

Total Coverage By Design Unit (filtered view): 98.66%

5.5 Code Coverage "seed5" Report

Coverage Report by DU with details

==== Design Unit: work.FIFO

Assertion Coverage:				
Assertions	13	13	0	100.00%

Name	File(Line)	Failure	Pass

```
                                                    Count         Count
--------------------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                        0             1
work.FIFO::assert__read_ptr_threshold
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                        0             1
work.FIFO::assert__write_ptr_threshold
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                        0             1
work.FIFO::assert__read_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                        0             1
work.FIFO::assert__write_ptr_wraparound
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                        0             1
work.FIFO::assert__almost_empty_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                        0             1
work.FIFO::assert__almost_full_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                        0             1
work.FIFO::assert__full_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                        0             1
work.FIFO::assert__empty_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                        0             1
work.FIFO::assert__underflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                        0             1
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                        0             1
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                        0             1
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                        0             1
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                     1139     Count coming in to IF
    13              1                       294        if (!fifo_intf.rst_n) begin
    18              1                       575        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                       270        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                      270     Count coming in to IF
    25              1                        37                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                       233                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                     1139     Count coming in to IF
    33              1                       294        if (!fifo_intf.rst_n) begin
    38              1                       203        else if (fifo_intf.rd_en && count != 0) begin
    42              1                       642        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                      642     Count coming in to IF
    43              1                        49                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                       593                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                     1065     Count coming in to IF
    51              1                       281        if (!fifo_intf.rst_n) begin
    54              1                       784        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                      784     Count coming in to IF
    55              1                       407                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                        61                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                         9                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                        35                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                             272     All False Count
```

```
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                    632     Count coming in to IF
    66              1                      20     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                     612     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                    893     Count coming in to IF
    67              1                     400     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                     493     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                    632     Count coming in to IF
    68              1                      32     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                     600     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                    632     Count coming in to IF
    69              1                     144     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                     488     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
    -------------  --------  ----------------------  ------------
  fifo_intf.wr_en         Y
      (count < 8)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.wr_en_0       -
  Row    2:          1  fifo_intf.wr_en_1       (count < 8)
  Row    3:          1  (count < 8)_0           fifo_intf.wr_en
  Row    4:          1  (count < 8)_1           fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
    -------------  --------  ----------------------  ------------
   fifo_intf.full         N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0       fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1       fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
    -------------  --------  ----------------------  ------------
  fifo_intf.rd_en         Y
     (count != 0)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
  Row    3:          1  (count != 0)_0           fifo_intf.rd_en
  Row    4:          1  (count != 0)_1           fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
    -------------  --------  ----------------------  ------------
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
```

```
  fifo_intf.rd_en          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:     ***0***  fifo_intf.empty_0       fifo_intf.rd_en
  Row    2:           1  fifo_intf.empty_1       fifo_intf.rd_en
  Row    3:           1  fifo_intf.rd_en_0       fifo_intf.empty
  Row    4:           1  fifo_intf.rd_en_1       fifo_intf.empty

-----------------Focused Condition View-----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
 ---------------  ---------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
   fifo_intf.full          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       (~fifo_intf.full && fifo_intf.wr_en)
  Row    2:           1  fifo_intf.rd_en_1       -
  Row    3:           1  fifo_intf.wr_en_0       ~fifo_intf.rd_en
  Row    4:           1  fifo_intf.wr_en_1       (~fifo_intf.full && ~fifo_intf.rd_en)
  Row    5:           1  fifo_intf.full_0        (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:           1  fifo_intf.full_1        (~fifo_intf.rd_en && fifo_intf.wr_en)

-----------------Focused Condition View-----------------
Line       57 Item    1  ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
 ---------------  ---------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
  fifo_intf.empty          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       -
  Row    2:           1  fifo_intf.rd_en_1       (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row    3:           1  fifo_intf.wr_en_0       (~fifo_intf.empty && fifo_intf.rd_en)
  Row    4:           1  fifo_intf.wr_en_1       fifo_intf.rd_en
  Row    5:           1  fifo_intf.empty_0       (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row    6:           1  fifo_intf.empty_1       (fifo_intf.rd_en && ~fifo_intf.wr_en)

-----------------Focused Condition View-----------------
Line       59 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
 ---------------  ---------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
   fifo_intf.full          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       -
  Row    2:           1  fifo_intf.rd_en_1       (fifo_intf.full && fifo_intf.wr_en)
  Row    3:           1  fifo_intf.wr_en_0       fifo_intf.rd_en
  Row    4:           1  fifo_intf.wr_en_1       (fifo_intf.full && fifo_intf.rd_en)
  Row    5:           1  fifo_intf.full_0        (fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:           1  fifo_intf.full_1        (fifo_intf.rd_en && fifo_intf.wr_en)

-----------------Focused Condition View-----------------
Line       61 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
 ---------------  ---------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
  fifo_intf.empty          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       -
  Row    2:           1  fifo_intf.rd_en_1       (fifo_intf.empty && fifo_intf.wr_en)
  Row    3:           1  fifo_intf.wr_en_0       fifo_intf.rd_en
  Row    4:           1  fifo_intf.wr_en_1       (fifo_intf.empty && fifo_intf.rd_en)
  Row    5:           1  fifo_intf.empty_0       (fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:           1  fifo_intf.empty_1       (fifo_intf.rd_en && fifo_intf.wr_en)

-----------------Focused Condition View-----------------
Line       66 Item    1  (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
 --------------  ---------  ----------------------  --------------
  (count == 8)          Y
```

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

Focused Condition View

Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	–
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

Focused Condition View

Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == (8 - 1))_0	–
Row 2:	1	(count == (8 - 1))_1	–

Focused Condition View

Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 1)_0	–
Row 2:	1	(count == 1)_1	–

Directive Coverage:

Directives	13	13	0	100.00%

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	846	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	846	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	846	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	2	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	24	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	190	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	48	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	49	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	185	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	39	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	23	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	485	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	162	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1139	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	294	wr_ptr <= 0;
15	1	294	fifo_intf.wr_ack <= 0;
16	1	294	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	575	mem[wr_ptr] <= fifo_intf.data_in;
20	1	575	fifo_intf.wr_ack <= 1;
21	1	575	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	270	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	37	fifo_intf.overflow <= 1;
27			else
28	1	233	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	1139	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	294	rd_ptr <= 0;
35	1	294	fifo_intf.underflow <= 0;
36	1	294	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	203	fifo_intf.data_out <= mem[rd_ptr];
40	1	203	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	49	fifo_intf.underflow <= 1;
45			else
46	1	593	fifo_intf.underflow <= 0;
47			end
48			end
49			
50	1	1065	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51			if (!fifo_intf.rst_n) begin
52	1	281	count <= 0;
53			end
54			else begin
55			if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56	1	407	count <= count + 1;
57			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58	1	61	count <= count - 1;
59			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60	1	9	count <= count - 1;
61			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62	1	35	count <= count + 1;
63			end
64			end
65			
66	1	633	assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67	1	894	assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68	1	633	assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69	1	633	assign fifo_intf.almostempty = (count == 1)? 1 : 0;

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

Total Node Count	10
Toggled Node Count	10
Untoggled Node Count	0

Toggle Coverage = 100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	846	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	846	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	846	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	2	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	24	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	190	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	48	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	49	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	185	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	39	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	23	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	485	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	162	Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
work.FIFO::assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	1
work.FIFO::assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	1
work.FIFO::assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)	0	1
work.FIFO::assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)	0	1
work.FIFO::assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)	0	1
work.FIFO::assert__almost_empty_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)	0	1
work.FIFO::assert__almost_full_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)	0	1
work.FIFO::assert__full_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)	0	1
work.FIFO::assert__empty_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)	0	1
work.FIFO::assert__underflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)	0	1
work.FIFO::assert__overflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)	0	1
work.FIFO::assert__write_ack_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)	0	1
work.FIFO::assert__reset_behavior	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)	0	1

Total Coverage By Design Unit (filtered view): 98.66%

6 Waveform

6.1 Waveform & Transcript "seed1" Report

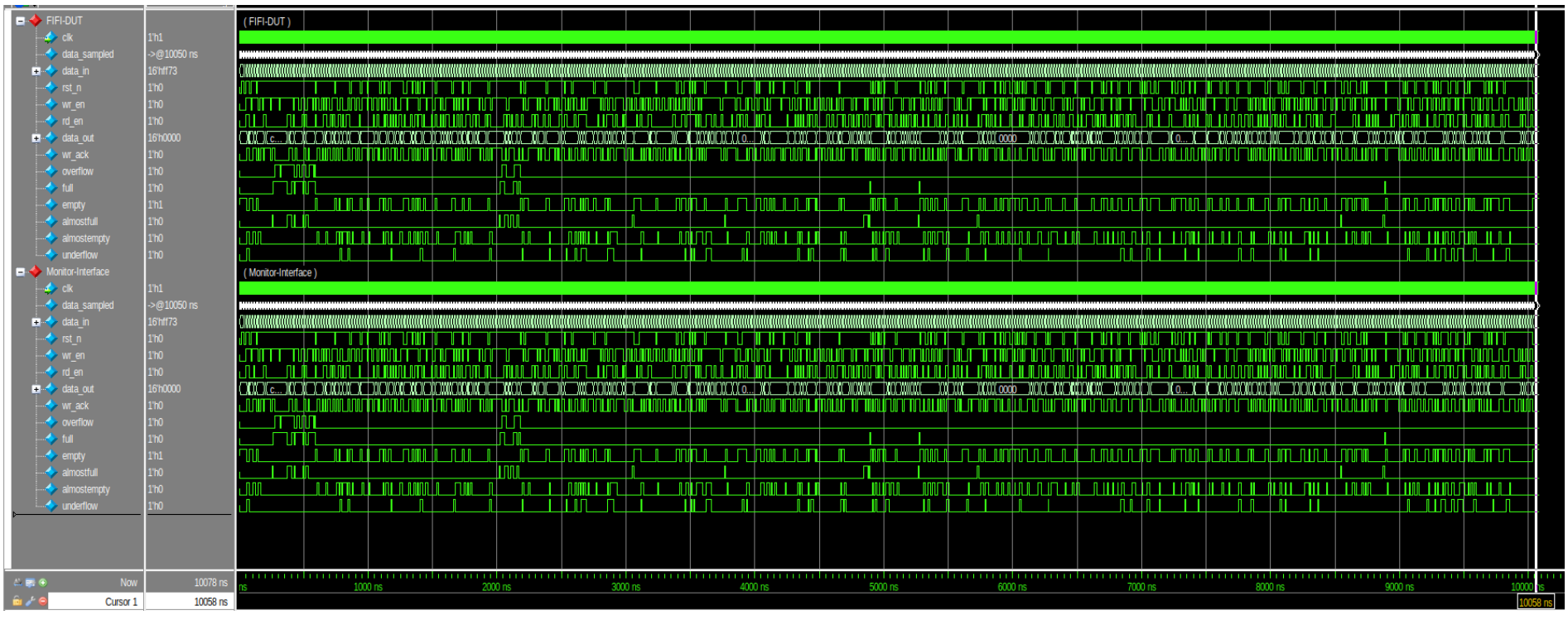


Figure 6: simulation waveform "seed1"

```
# Loading sv_std.std
# Loading work.Shared_pkg(fast)
# Loading work.Shared_pkg_sv_unit(fast)
# Loading work.FIFO_top(fast)
# Loading work.FIFO_IF(fast__1)
# Loading work.FIFO(fast)
# Loading work.FIFO_transaction_pkg(fast)
# Loading work.FIFO_tb(fast)
# Loading work.FIFO_scoreboard_pkg(fast)
# Loading work.FIFO_coverage_pkg(fast)
# Loading work.FIFO_monitor(fast)
# run -all
# Test Summary:
#   Total Correct: 1008
#   Total Errors: 0
#   Coverage: 99.75%
# ** Note: $stop    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
#    Time: 10078 ns  Iteration: 0  Instance: /FIFO_top/mon
# Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
# Stopped at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
#  quit -f
# End time: 14:44:51 on May 01,2025, Elapsed time: 0:00:04
# Errors: 0, Warnings: 0

Running simulation with seed 1111
Reading pref.tcl
```

Figure 7: Transcript : all test cases passed "seed1"

6.2 Waveform & Transcript "seed2" Report

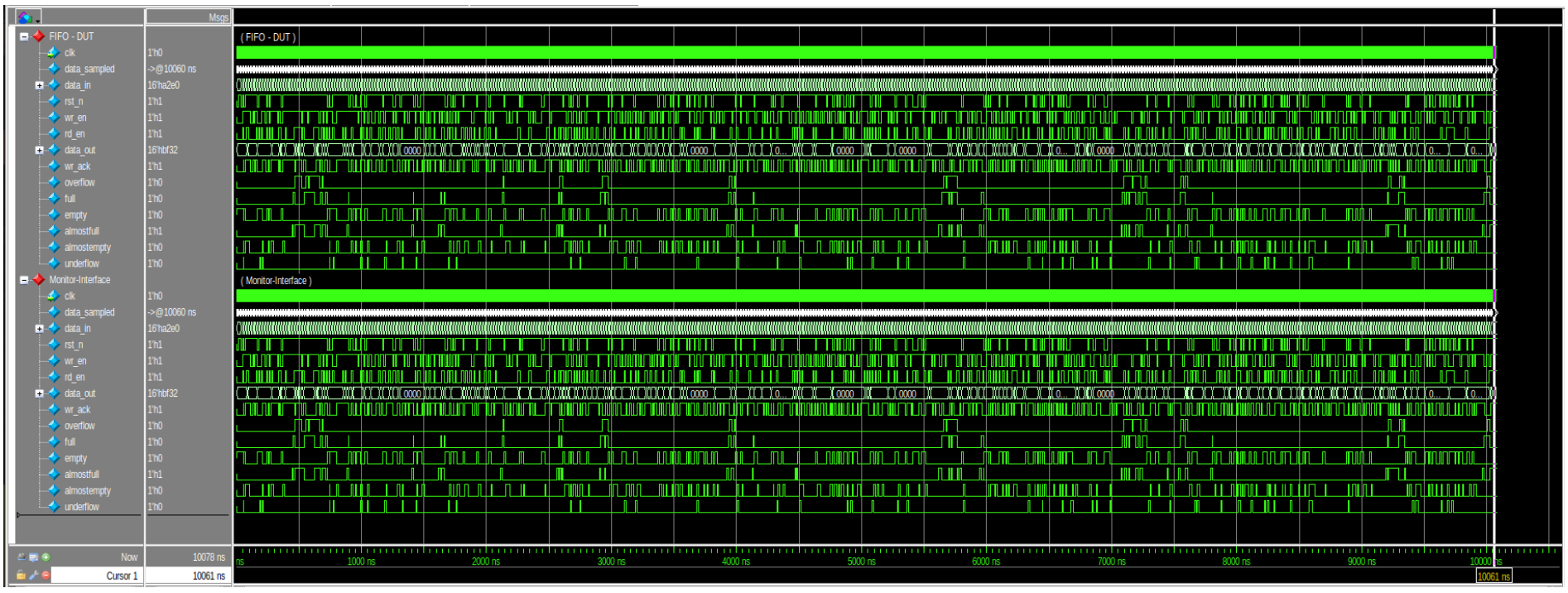


Figure 8: simulation waveform "seed2"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIFO_seed1111.ucdb
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 1511
Reading pref.tcl
```

```
# Test Summary:
#   Total Correct: 1008
#   Total Errors: 0
#   Coverage: 99.84%
# ** Note: $stop    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
#    Time: 10078 ns  Iteration: 0  Instance: /FIFO_top/mon
# Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
```

Figure 9: Transcript : all test cases passed "seed2"

6.3 Waveform & Transcript "seed3" Report

Figure 10: simulation waveform "seed3"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:48:24 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIFO_seed1111.ucdb
End time: 14:48:24 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIFO_seed1511.ucdb
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2515
Reading pref.tcl
# Test Summary:
#   Total Correct: 1008
#   Total Errors: 0
#   Coverage: 99.84%
# ** Note: $stop    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
#    Time: 10078 ns  Iteration: 0  Instance: /FIFO_top/mon
# Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
```

Figure 11: Transcript : all test cases passed ”seed3”

6.4 Waveform & Transcript ”seed4” Report

Figure 12: simulation waveform ”seed4”

```
Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:55:10 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIFO_seed1511.ucdb
End time: 14:55:10 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIFO_seed2515.ucdb
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2236
Reading pref.tcl
```

```
Test Summary:
  Total Correct: 1008
  Total Errors: 0
  Coverage: 99.75%
** Note: $stop    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
   Time: 10078 ns  Iteration: 0  Instance: /FIFO_top/mon
Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
```

Figure 13: Transcript : all test cases passed "seed4"

6.5 Waveform & Transcript "seed5" Report

Figure 14: simulation waveform "seed5"

```
Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 14:58:44 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIFO_seed2515.ucdb
End time: 14:58:44 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2236
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:01:48 on May 01,2025
vcover report FIFO_seed2236.ucdb -details -annotate -all -output code_coverage_rpt_seed2236.txt -du=FIFO
End time: 15:01:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:01:48 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2236.txt FIFO_seed2236.ucdb
End time: 15:01:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 5215
Reading pref.tcl
```

```
Test Summary:
  Total Correct: 1008
  Total Errors: 0
  Coverage: 99.92%
** Note: $stop    : /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv(66)
   Time: 10078 ns  Iteration: 0  Instance: /FIFO_top/mon
Break in Module FIFO_monitor at /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv line 66
```

Figure 15: Transcript : all test cases passed "seed5"

7 Merged Coverage

```
Merging coverage from all seed runs
vcover merge merged.ucdb FIFO_seed*.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:15 on May 01,2025
vcover merge merged.ucdb FIFO_seed1111.ucdb FIFO_seed1511.ucdb FIFO_seed2236.ucdb FIFO_seed2515.ucdb FIFO_seed5215.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Merging file FIFO_seed1111.ucdb
Merging file FIFO_seed1511.ucdb
Merging file FIFO_seed2236.ucdb
Merging file FIFO_seed2515.ucdb
Merging file FIFO_seed5215.ucdb
Writing merged result to merged.ucdb

End time: 15:09:15 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
Reading pref.tcl

# 2021.2_1

# coverage open merged.ucdb
# coverage read -dataset merged merged.ucdb
# merged.ucdb opened as coverage dataset "merged"
#  coverage report -output merged_coverage_report.txt -srcfile=* -detail
#  quit -f
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:17 on May 01,2025
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
End time: 15:09:17 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 15:09:17 on May 01,2025
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
End time: 15:09:17 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Coverage merged to merged.ucdb and reports saved
```

Figure 16: Merge seed

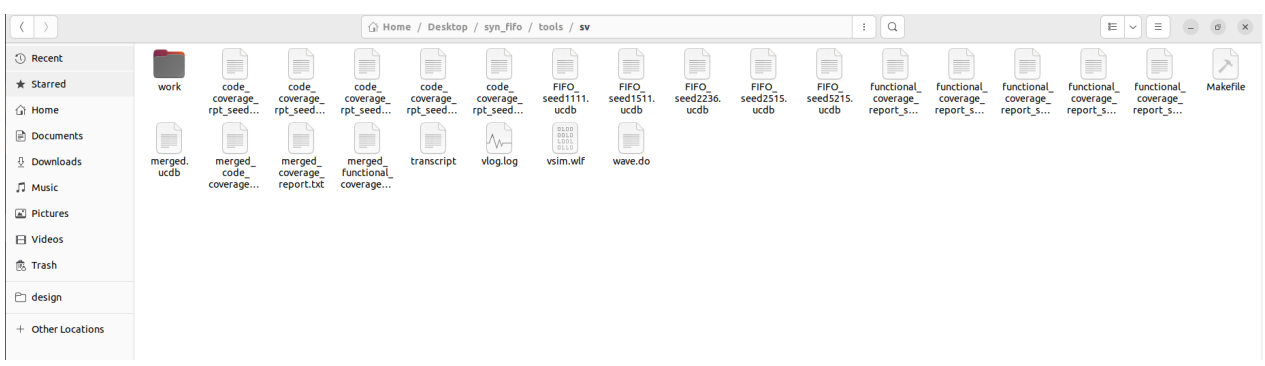


Figure 17: generated files *.ucdb

7.1 Functional Coverage "Merged" Report

Coverage Report by instance with details

```
=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   194       194         0   100.00%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	–	Covered
covered/total bins:	194	194	–	
missing/total bins:	0	194	–	
% Hit:	100.00%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	781	1	–	Covered
bin auto[1]	4259	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	95	1	–	Covered
bin auto[1024:2047]	74	1	–	Covered
bin auto[2048:3071]	72	1	–	Covered
bin auto[3072:4095]	72	1	–	Covered
bin auto[4096:5119]	84	1	–	Covered
bin auto[5120:6143]	71	1	–	Covered
bin auto[6144:7167]	70	1	–	Covered
bin auto[7168:8191]	88	1	–	Covered
bin auto[8192:9215]	82	1	–	Covered
bin auto[9216:10239]	71	1	–	Covered
bin auto[10240:11263]	75	1	–	Covered
bin auto[11264:12287]	78	1	–	Covered
bin auto[12288:13311]	76	1	–	Covered
bin auto[13312:14335]	71	1	–	Covered
bin auto[14336:15359]	77	1	–	Covered
bin auto[15360:16383]	85	1	–	Covered
bin auto[16384:17407]	89	1	–	Covered
bin auto[17408:18431]	84	1	–	Covered
bin auto[18432:19455]	74	1	–	Covered
bin auto[19456:20479]	90	1	–	Covered
bin auto[20480:21503]	76	1	–	Covered
bin auto[21504:22527]	79	1	–	Covered
bin auto[22528:23551]	68	1	–	Covered
bin auto[23552:24575]	80	1	–	Covered
bin auto[24576:25599]	75	1	–	Covered
bin auto[25600:26623]	82	1	–	Covered
bin auto[26624:27647]	78	1	–	Covered
bin auto[27648:28671]	79	1	–	Covered
bin auto[28672:29695]	79	1	–	Covered
bin auto[29696:30719]	79	1	–	Covered
bin auto[30720:31743]	72	1	–	Covered
bin auto[31744:32767]	84	1	–	Covered
bin auto[32768:33791]	68	1	–	Covered
bin auto[33792:34815]	80	1	–	Covered
bin auto[34816:35839]	81	1	–	Covered
bin auto[35840:36863]	67	1	–	Covered
bin auto[36864:37887]	71	1	–	Covered
bin auto[37888:38911]	69	1	–	Covered
bin auto[38912:39935]	87	1	–	Covered
bin auto[39936:40959]	83	1	–	Covered
bin auto[40960:41983]	70	1	–	Covered
bin auto[41984:43007]	87	1	–	Covered
bin auto[43008:44031]	92	1	–	Covered
bin auto[44032:45055]	65	1	–	Covered
bin auto[45056:46079]	89	1	–	Covered
bin auto[46080:47103]	72	1	–	Covered
bin auto[47104:48127]	71	1	–	Covered
bin auto[48128:49151]	82	1	–	Covered
bin auto[49152:50175]	73	1	–	Covered
bin auto[50176:51199]	74	1	–	Covered
bin auto[51200:52223]	90	1	–	Covered
bin auto[52224:53247]	90	1	–	Covered
bin auto[53248:54271]	74	1	–	Covered
bin auto[54272:55295]	85	1	–	Covered
bin auto[55296:56319]	82	1	–	Covered
bin auto[56320:57343]	83	1	–	Covered
bin auto[57344:58367]	87	1	–	Covered
bin auto[58368:59391]	80	1	–	Covered
bin auto[59392:60415]	81	1	–	Covered
bin auto[60416:61439]	82	1	–	Covered
bin auto[61440:62463]	80	1	–	Covered

bin auto[62464:63487]	78	1	–	Covered
bin auto[63488:64511]	80	1	–	Covered
bin auto[64512:65535]	78	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3544	1	–	Covered
bin auto[1]	1496	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1517	1	–	Covered
bin auto[1]	3523	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	2622	1	–	Covered
bin auto[1024:2047]	20	1	–	Covered
bin auto[2048:3071]	47	1	–	Covered
bin auto[3072:4095]	29	1	–	Covered
bin auto[4096:5119]	34	1	–	Covered
bin auto[5120:6143]	33	1	–	Covered
bin auto[6144:7167]	56	1	–	Covered
bin auto[7168:8191]	60	1	–	Covered
bin auto[8192:9215]	54	1	–	Covered
bin auto[9216:10239]	28	1	–	Covered
bin auto[10240:11263]	29	1	–	Covered
bin auto[11264:12287]	66	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	46	1	–	Covered
bin auto[14336:15359]	38	1	–	Covered
bin auto[15360:16383]	39	1	–	Covered
bin auto[16384:17407]	60	1	–	Covered
bin auto[17408:18431]	43	1	–	Covered
bin auto[18432:19455]	28	1	–	Covered
bin auto[19456:20479]	48	1	–	Covered
bin auto[20480:21503]	50	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	23	1	–	Covered
bin auto[23552:24575]	31	1	–	Covered
bin auto[24576:25599]	26	1	–	Covered
bin auto[25600:26623]	41	1	–	Covered
bin auto[26624:27647]	39	1	–	Covered
bin auto[27648:28671]	33	1	–	Covered
bin auto[28672:29695]	45	1	–	Covered
bin auto[29696:30719]	26	1	–	Covered
bin auto[30720:31743]	32	1	–	Covered
bin auto[31744:32767]	40	1	–	Covered
bin auto[32768:33791]	28	1	–	Covered
bin auto[33792:34815]	46	1	–	Covered
bin auto[34816:35839]	50	1	–	Covered
bin auto[35840:36863]	22	1	–	Covered
bin auto[36864:37887]	35	1	–	Covered
bin auto[37888:38911]	38	1	–	Covered
bin auto[38912:39935]	41	1	–	Covered
bin auto[39936:40959]	39	1	–	Covered
bin auto[40960:41983]	26	1	–	Covered
bin auto[41984:43007]	54	1	–	Covered
bin auto[43008:44031]	65	1	–	Covered
bin auto[44032:45055]	41	1	–	Covered
bin auto[45056:46079]	23	1	–	Covered
bin auto[46080:47103]	27	1	–	Covered
bin auto[47104:48127]	34	1	–	Covered
bin auto[48128:49151]	35	1	–	Covered
bin auto[49152:50175]	40	1	–	Covered
bin auto[50176:51199]	27	1	–	Covered
bin auto[51200:52223]	58	1	–	Covered
bin auto[52224:53247]	59	1	–	Covered
bin auto[53248:54271]	34	1	–	Covered
bin auto[54272:55295]	42	1	–	Covered
bin auto[55296:56319]	28	1	–	Covered
bin auto[56320:57343]	69	1	–	Covered
bin auto[57344:58367]	46	1	–	Covered
bin auto[58368:59391]	29	1	–	Covered
bin auto[59392:60415]	18	1	–	Covered
bin auto[60416:61439]	29	1	–	Covered
bin auto[61440:62463]	40	1	–	Covered
bin auto[62464:63487]	22	1	–	Covered
bin auto[63488:64511]	40	1	–	Covered
bin auto[64512:65535]	43	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2204	1	–	Covered
bin auto[1]	2836	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	

% Hit:	100.00%	100	–	
bin auto[0]	4811	1	–	Covered
bin auto[1]	229	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4756	1	–	Covered
bin auto[1]	284	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3900	1	–	Covered
bin auto[1]	1140	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4780	1	–	Covered
bin auto[1]	260	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3943	1	–	Covered
bin auto[1]	1097	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4700	1	–	Covered
bin auto[1]	340	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	828	1	–	Covered
bin <auto[1],auto[1],auto[0]>	211	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2008	1	–	Covered
bin <auto[0],auto[1],auto[0]>	476	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	234	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1039	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2250	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1010	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	165	1	–	Covered
bin <auto[1],auto[0],auto[1]>	242	1	–	Covered
bin <auto[1],auto[1],auto[0]>	874	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2134	1	–	Covered
bin <auto[1],auto[0],auto[0]>	215	1	–	Covered
bin <auto[0],auto[0],auto[0]>	677	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	733		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	107	1	–	Covered
bin <auto[0],auto[1],auto[1]>	89	1	–	Covered
bin <auto[1],auto[0],auto[1]>	22	1	–	Covered
bin <auto[0],auto[0],auto[1]>	42	1	–	Covered
bin <auto[1],auto[1],auto[0]>	932	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2395	1	–	Covered
bin <auto[1],auto[0],auto[0]>	435	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1018	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	384	1	–	Covered

bin <auto[0],auto[1],auto[1]>	477	1	–	Covered
bin <auto[1],auto[0],auto[1]>	49	1	–	Covered
bin <auto[0],auto[0],auto[1]>	187	1	–	Covered
bin <auto[1],auto[1],auto[0]>	655	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2007	1	–	Covered
bin <auto[1],auto[0],auto[0]>	408	1	–	Covered
bin <auto[0],auto[0],auto[0]>	873	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	75	1	–	Covered
bin <auto[1],auto[1],auto[0]>	964	1	–	Covered
bin <auto[0],auto[1],auto[1]>	154	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2330	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	231	1	–	Covered
bin <auto[1],auto[0],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	808	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2484	1	–	Covered
bin <auto[1],auto[0],auto[0]>	348	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	–	Covered
covered/total bins:	194	194	–	
missing/total bins:	0	194	–	
% Hit:	100.00%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	781	1	–	Covered
bin auto[1]	4259	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	95	1	–	Covered
bin auto[1024:2047]	74	1	–	Covered
bin auto[2048:3071]	72	1	–	Covered
bin auto[3072:4095]	72	1	–	Covered
bin auto[4096:5119]	84	1	–	Covered
bin auto[5120:6143]	71	1	–	Covered
bin auto[6144:7167]	70	1	–	Covered
bin auto[7168:8191]	88	1	–	Covered
bin auto[8192:9215]	82	1	–	Covered
bin auto[9216:10239]	71	1	–	Covered
bin auto[10240:11263]	75	1	–	Covered
bin auto[11264:12287]	78	1	–	Covered
bin auto[12288:13311]	76	1	–	Covered
bin auto[13312:14335]	71	1	–	Covered
bin auto[14336:15359]	77	1	–	Covered
bin auto[15360:16383]	85	1	–	Covered
bin auto[16384:17407]	89	1	–	Covered
bin auto[17408:18431]	84	1	–	Covered
bin auto[18432:19455]	74	1	–	Covered
bin auto[19456:20479]	90	1	–	Covered
bin auto[20480:21503]	76	1	–	Covered
bin auto[21504:22527]	79	1	–	Covered
bin auto[22528:23551]	68	1	–	Covered
bin auto[23552:24575]	80	1	–	Covered
bin auto[24576:25599]	75	1	–	Covered
bin auto[25600:26623]	82	1	–	Covered
bin auto[26624:27647]	78	1	–	Covered
bin auto[27648:28671]	79	1	–	Covered
bin auto[28672:29695]	79	1	–	Covered
bin auto[29696:30719]	79	1	–	Covered
bin auto[30720:31743]	72	1	–	Covered
bin auto[31744:32767]	84	1	–	Covered
bin auto[32768:33791]	68	1	–	Covered
bin auto[33792:34815]	80	1	–	Covered
bin auto[34816:35839]	81	1	–	Covered
bin auto[35840:36863]	67	1	–	Covered
bin auto[36864:37887]	71	1	–	Covered
bin auto[37888:38911]	69	1	–	Covered
bin auto[38912:39935]	87	1	–	Covered

bin auto[39936:40959]	83	1	–	Covered
bin auto[40960:41983]	70	1	–	Covered
bin auto[41984:43007]	87	1	–	Covered
bin auto[43008:44031]	92	1	–	Covered
bin auto[44032:45055]	65	1	–	Covered
bin auto[45056:46079]	89	1	–	Covered
bin auto[46080:47103]	72	1	–	Covered
bin auto[47104:48127]	71	1	–	Covered
bin auto[48128:49151]	82	1	–	Covered
bin auto[49152:50175]	73	1	–	Covered
bin auto[50176:51199]	74	1	–	Covered
bin auto[51200:52223]	90	1	–	Covered
bin auto[52224:53247]	90	1	–	Covered
bin auto[53248:54271]	74	1	–	Covered
bin auto[54272:55295]	85	1	–	Covered
bin auto[55296:56319]	82	1	–	Covered
bin auto[56320:57343]	83	1	–	Covered
bin auto[57344:58367]	87	1	–	Covered
bin auto[58368:59391]	80	1	–	Covered
bin auto[59392:60415]	81	1	–	Covered
bin auto[60416:61439]	82	1	–	Covered
bin auto[61440:62463]	80	1	–	Covered
bin auto[62464:63487]	78	1	–	Covered
bin auto[63488:64511]	80	1	–	Covered
bin auto[64512:65535]	78	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3544	1	–	Covered
bin auto[1]	1496	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1517	1	–	Covered
bin auto[1]	3523	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	2622	1	–	Covered
bin auto[1024:2047]	20	1	–	Covered
bin auto[2048:3071]	47	1	–	Covered
bin auto[3072:4095]	29	1	–	Covered
bin auto[4096:5119]	34	1	–	Covered
bin auto[5120:6143]	33	1	–	Covered
bin auto[6144:7167]	56	1	–	Covered
bin auto[7168:8191]	60	1	–	Covered
bin auto[8192:9215]	54	1	–	Covered
bin auto[9216:10239]	28	1	–	Covered
bin auto[10240:11263]	29	1	–	Covered
bin auto[11264:12287]	66	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	46	1	–	Covered
bin auto[14336:15359]	38	1	–	Covered
bin auto[15360:16383]	39	1	–	Covered
bin auto[16384:17407]	60	1	–	Covered
bin auto[17408:18431]	43	1	–	Covered
bin auto[18432:19455]	28	1	–	Covered
bin auto[19456:20479]	48	1	–	Covered
bin auto[20480:21503]	50	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	23	1	–	Covered
bin auto[23552:24575]	31	1	–	Covered
bin auto[24576:25599]	26	1	–	Covered
bin auto[25600:26623]	41	1	–	Covered
bin auto[26624:27647]	39	1	–	Covered
bin auto[27648:28671]	33	1	–	Covered
bin auto[28672:29695]	45	1	–	Covered
bin auto[29696:30719]	26	1	–	Covered
bin auto[30720:31743]	32	1	–	Covered
bin auto[31744:32767]	40	1	–	Covered
bin auto[32768:33791]	28	1	–	Covered
bin auto[33792:34815]	46	1	–	Covered
bin auto[34816:35839]	50	1	–	Covered
bin auto[35840:36863]	22	1	–	Covered
bin auto[36864:37887]	35	1	–	Covered
bin auto[37888:38911]	38	1	–	Covered
bin auto[38912:39935]	41	1	–	Covered
bin auto[39936:40959]	39	1	–	Covered
bin auto[40960:41983]	26	1	–	Covered
bin auto[41984:43007]	54	1	–	Covered
bin auto[43008:44031]	65	1	–	Covered
bin auto[44032:45055]	41	1	–	Covered
bin auto[45056:46079]	23	1	–	Covered
bin auto[46080:47103]	27	1	–	Covered
bin auto[47104:48127]	34	1	–	Covered
bin auto[48128:49151]	35	1	–	Covered
bin auto[49152:50175]	40	1	–	Covered
bin auto[50176:51199]	27	1	–	Covered
bin auto[51200:52223]	58	1	–	Covered

bin auto[52224:53247]	59	1	–	Covered
bin auto[53248:54271]	34	1	–	Covered
bin auto[54272:55295]	42	1	–	Covered
bin auto[55296:56319]	28	1	–	Covered
bin auto[56320:57343]	69	1	–	Covered
bin auto[57344:58367]	46	1	–	Covered
bin auto[58368:59391]	29	1	–	Covered
bin auto[59392:60415]	18	1	–	Covered
bin auto[60416:61439]	29	1	–	Covered
bin auto[61440:62463]	40	1	–	Covered
bin auto[62464:63487]	22	1	–	Covered
bin auto[63488:64511]	40	1	–	Covered
bin auto[64512:65535]	43	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2204	1	–	Covered
bin auto[1]	2836	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4811	1	–	Covered
bin auto[1]	229	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4756	1	–	Covered
bin auto[1]	284	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3900	1	–	Covered
bin auto[1]	1140	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4780	1	–	Covered
bin auto[1]	260	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3943	1	–	Covered
bin auto[1]	1097	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4700	1	–	Covered
bin auto[1]	340	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	828	1	–	Covered
bin <auto[1],auto[1],auto[0]>	211	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2008	1	–	Covered
bin <auto[0],auto[1],auto[0]>	476	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	234	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1039	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2250	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1010	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	165	1	–	Covered
bin <auto[1],auto[0],auto[1]>	242	1	–	Covered
bin <auto[1],auto[1],auto[0]>	874	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2134	1	–	Covered
bin <auto[1],auto[0],auto[0]>	215	1	–	Covered

bin <auto[0],auto[0],auto[0]>	677	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	733		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	107	1	–	Covered
bin <auto[0],auto[1],auto[1]>	89	1	–	Covered
bin <auto[1],auto[0],auto[1]>	22	1	–	Covered
bin <auto[0],auto[0],auto[1]>	42	1	–	Covered
bin <auto[1],auto[1],auto[0]>	932	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2395	1	–	Covered
bin <auto[1],auto[0],auto[0]>	435	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1018	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	384	1	–	Covered
bin <auto[0],auto[1],auto[1]>	477	1	–	Covered
bin <auto[1],auto[0],auto[1]>	49	1	–	Covered
bin <auto[0],auto[0],auto[1]>	187	1	–	Covered
bin <auto[1],auto[1],auto[0]>	655	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2007	1	–	Covered
bin <auto[1],auto[0],auto[0]>	408	1	–	Covered
bin <auto[0],auto[0],auto[0]>	873	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	75	1	–	Covered
bin <auto[1],auto[1],auto[0]>	964	1	–	Covered
bin <auto[0],auto[1],auto[1]>	154	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2330	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	231	1	–	Covered
bin <auto[1],auto[0],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	808	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2484	1	–	Covered
bin <auto[1],auto[0],auto[0]>	348	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%

7.2 Code Coverage "Merged" Report

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.FIFO
================================================================================

Assertion Coverage:
    Assertions                      13          13           0    100.00%
--------------------------------------------------------------------------------
Name                      File(Line)                    Failure      Pass
                                                        Count        Count
--------------------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                            0            5
work.FIFO::assert__read_ptr_threshold
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                            0            5
work.FIFO::assert__write_ptr_threshold
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                            0            5
work.FIFO::assert__read_ptr_wraparound
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                            0            5
work.FIFO::assert__write_ptr_wraparound
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                            0            5
work.FIFO::assert__almost_empty_check
                          /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                            0            5
```

```
work.FIFO::assert__almost_full_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                        0          5
work.FIFO::assert__full_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                        0          5
work.FIFO::assert__empty_flag_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                        0          5
work.FIFO::assert__underflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                        0          5
work.FIFO::assert__overflow_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                        0          5
work.FIFO::assert__write_ack_check
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                        0          5
work.FIFO::assert__reset_behavior
                    /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                        0          5
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                            Count     Source
    ----         ----                            -----     ------
  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                   5681     Count coming in to IF
    13              1                    1424        if (!fifo_intf.rst_n) begin
    18              1                    2839        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                    1418        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                   1418     Count coming in to IF
    25              1                     172              if (fifo_intf.full & fifo_intf.wr_en)
    27              1                    1246              else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                   5681     Count coming in to IF
    33              1                    1424        if (!fifo_intf.rst_n) begin
    38              1                     971        else if (fifo_intf.rd_en && count != 0) begin
    42              1                    3286        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                   3286     Count coming in to IF
    43              1                     284              if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                    3002              else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                   5306     Count coming in to IF
    51              1                    1375        if (!fifo_intf.rst_n) begin
    54              1                    3931        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                   3931     Count coming in to IF
    55              1                    2009              if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                     291              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                      46              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                     196              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                         1389     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                   3141     Count coming in to IF
    66              1                     108     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                    3033     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                   4421     Count coming in to IF
    67              1                    1955     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                    2466     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                   3141     Count coming in to IF
    68              1                     157     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                    2984     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    69                                  3141     Count coming in to IF
    69              1                    722     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                   2419     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                     Bins    Covered     Misses  Coverage
    ----------------                     ----    -------     ------  --------
    Conditions                             25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.wr_en         Y
     (count < 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          5  fifo_intf.wr_en_0      -
  Row    2:          5  fifo_intf.wr_en_1      (count < 8)
  Row    3:          5  (count < 8)_0          fifo_intf.wr_en
  Row    4:          5  (count < 8)_1          fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
   fifo_intf.full         N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.full_0      fifo_intf.wr_en
  Row    2:          5  fifo_intf.full_1      fifo_intf.wr_en
  Row    3:          5  fifo_intf.wr_en_0     fifo_intf.full
  Row    4:          5  fifo_intf.wr_en_1     fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.rd_en         Y
     (count != 0)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          5  fifo_intf.rd_en_0      -
  Row    2:          5  fifo_intf.rd_en_1      (count != 0)
  Row    3:          5  (count != 0)_0          fifo_intf.rd_en
  Row    4:          5  (count != 0)_1          fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.empty_0     fifo_intf.rd_en
  Row    2:          5  fifo_intf.empty_1     fifo_intf.rd_en
  Row    3:          5  fifo_intf.rd_en_0     fifo_intf.empty
  Row    4:          5  fifo_intf.rd_en_1     fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.rd_en         Y
  fifo_intf.wr_en         Y
   fifo_intf.full         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
```

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	5	fifo_intf.rd_en_1	–
Row 3:	5	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	5	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	5	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	5	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	5	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

Focused Condition View

Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	5	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	5	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 66 Item 1 (count == 8)

Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == 8)_0	–
Row 2:	5	(count == 8)_1	–

Focused Condition View

Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == 0)_0	fifo_intf.rst_n
Row 2:	5	(count == 0)_1	–
Row 3:	5	fifo_intf.rst_n_0	~(count == 0)

Row 4:	5	fifo_intf.rst_n_1	~(count == 0)

Focused Condition View

Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	5	(count == (8 - 1))_0	-
Row 2:	5	(count == (8 - 1))_1	-

Focused Condition View

Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	5	(count == 1)_0	-
Row 2:	5	(count == 1)_1	-

Directive Coverage:

Directives	13	13	0	100.00%

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	4262	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	4262	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	4262	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	10	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	111	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)	900	Covered
work.FIFO::cover__almost_full_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)	230	Covered
work.FIFO::cover__full_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)	244	Covered
work.FIFO::cover__empty_flag_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)	956	Covered
work.FIFO::cover__underflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)	245	Covered
work.FIFO::cover__overflow_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)	108	Covered
work.FIFO::cover__write_ack_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)	2398	Covered
work.FIFO::cover__reset_behavior	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)	781	Covered

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	5681	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	1424	wr_ptr <= 0;
15	1	1424	fifo_intf.wr_ack <= 0;
16	1	1424	fifo_intf.overflow <= 0;

```
17                                          end
18                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19              1                 2839          mem[wr_ptr] <= fifo_intf.data_in;
20              1                 2839          fifo_intf.wr_ack <= 1;
21              1                 2839          wr_ptr <= wr_ptr + 1;
22                                          end
23                                          else begin
24              1                 1418          fifo_intf.wr_ack <= 0;
25                                              if (fifo_intf.full & fifo_intf.wr_en)
26              1                  172                  fifo_intf.overflow <= 1;
27                                              else
28              1                 1246                  fifo_intf.overflow <= 0;
29                                          end
30                                      end
31
32              1                 5681      always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                          if (!fifo_intf.rst_n) begin
34              1                 1424          rd_ptr <= 0;
35              1                 1424          fifo_intf.underflow <= 0;
36              1                 1424          fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                          end
38                                          else if (fifo_intf.rd_en && count != 0) begin
39              1                  971          fifo_intf.data_out <= mem[rd_ptr];
40              1                  971          rd_ptr <= rd_ptr + 1;
41                                          end
42                                          else begin
43                                              if (fifo_intf.empty & fifo_intf.rd_en)
44              1                  284                  fifo_intf.underflow <= 1;
45                                              else
46              1                 3002                  fifo_intf.underflow <= 0;
47                                          end
48                                      end
49
50              1                 5306      always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                          if (!fifo_intf.rst_n) begin
52              1                 1375              count <= 0;
53                                          end
54                                          else begin
55                                              if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                 2009                  count <= count + 1;
57                                              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                  291                  count <= count - 1;
59                                              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                   46                  count <= count - 1;
61                                              else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                  196                  count <= count + 1;
63                                          end
64                                      end
65
66              1                 3146      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                 4426      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                 3146      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                 3146      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	5	5	100.00
rd_ptr[0-2]	5	5	100.00
wr_ptr[0-2]	5	5	100.00

Total Node Count	=	10
Toggled Node Count	=	10
Untoggled Node Count	=	0
Toggle Coverage	=	100.00% (20 of 20 bins)

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
work.FIFO::cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	4262	Covered
work.FIFO::cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	4262	Covered
work.FIFO::cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	4262	Covered
work.FIFO::cover__read_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)	10	Covered
work.FIFO::cover__write_ptr_wraparound	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)	111	Covered
work.FIFO::cover__almost_empty_check	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)		

```
                                                                                          900  Covered
work.FIFO::cover__almost_full_check     FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
                                                                                          230  Covered
work.FIFO::cover__full_flag_check       FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
                                                                                          244  Covered
work.FIFO::cover__empty_flag_check      FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
                                                                                          956  Covered
work.FIFO::cover__underflow_check       FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
                                                                                          245  Covered
work.FIFO::cover__overflow_check        FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
                                                                                          108  Covered
work.FIFO::cover__write_ack_check       FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
                                                                                         2398  Covered
work.FIFO::cover__reset_behavior        FIFO   Verilog  SVA   /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
                                                                                          781  Covered

TOTAL DIRECTIVE COVERAGE: 100.00%   COVERS: 13

ASSERTION RESULTS:
--------------------------------------------------------------------
Name                    File(Line)                    Failure     Pass
                                                      Count       Count
--------------------------------------------------------------------
work.FIFO::assert__counter_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)
                                                            0          5
work.FIFO::assert__read_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)
                                                            0          5
work.FIFO::assert__write_ptr_threshold
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)
                                                            0          5
work.FIFO::assert__read_ptr_wraparound
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)
                                                            0          5
work.FIFO::assert__write_ptr_wraparound
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)
                                                            0          5
work.FIFO::assert__almost_empty_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)
                                                            0          5
work.FIFO::assert__almost_full_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)
                                                            0          5
work.FIFO::assert__full_flag_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)
                                                            0          5
work.FIFO::assert__empty_flag_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)
                                                            0          5
work.FIFO::assert__underflow_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)
                                                            0          5
work.FIFO::assert__overflow_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)
                                                            0          5
work.FIFO::assert__write_ack_check
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)
                                                            0          5
work.FIFO::assert__reset_behavior
                        /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)
                                                            0          5

Total Coverage By Design Unit (filtered view): 98.66%
```

7.3 Coverage "Merged" Report

```
Coverage Report by file with details

=================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_IF.sv
=================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       1         1         0   100.00%

================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_IF.sv --

    29              1                    10045
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         86        86         0   100.00%

================================Toggle Details================================

Toggle Coverage for File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_IF.sv --

       Line                                  Node      1H->0L      0L->1H  "Coverage"
```

```
Total Node Count     =          43
Toggled Node Count   =          43
Untoggled Node Count =           0

Toggle Coverage      =     100.00% (86 of 86 bins)

================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_coverage_pkg.sv
================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       4         4         0   100.00%

=================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_coverage_pkg.sv --

    61                   1                        5
    62                   1                        5
    67                   1                     5040
    69                   1                     5040

================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         2         0   100.00%

=================================Branch Details===================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv --

------------------------------------IF Branch-------------------------------------
    60                                       5040     Count coming in to IF
    60                   1                      5
                                             5035     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      27        27         0   100.00%

=================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_monitor.sv --

    18                   1                        5
    19                   1                        5
    20                   1                        5
    23                   1                        5
    25                   1                     5040
    28                   1                     5040
    32                   1                     5040
    33                   1                     5040
    34                   1                     5040
    35                   1                     5040
    37                   1                     5040
    38                   1                     5040
    39                   1                     5040
    40                   1                     5040
    41                   1                     5040
    42                   1                     5040
    43                   1                     5040
    44                   1                     5040
    49                   1                     5040
    52                   1                     5040
    54                   1                     5040
    55                   1                     5040
    62                   1                        5
    63                   1                        5
    64                   1                        5
    65                   1                        5
    66                   1                        5

================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        33        16        17    48.48%

=================================Branch Details===================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv --
```

```
------------------------------------IF Branch------------------------------------
    31                                    5040      Count coming in to IF
    31              1                      781
    44              1                     4259
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                    4259      Count coming in to IF
    51              1                     2836
    55              1                     1423
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    57                                    1423      Count coming in to IF
    57              1                      172
    60              1                     1251
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                    4259      Count coming in to IF
    66              1                      969
    69              1                     3290
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    70                                    3290      Count coming in to IF
    70              1                      284
    73              1                     3006
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    79                                    4259      Count coming in to IF
    79              1                     2008
    82              1                      291
    85              1                      196
    88              1                       46
                                          1718      All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    108                                   5040      Count coming in to IF
    108             1                     5040
    117             1                   ***0***
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    120                                 ***0***     Count coming in to IF
    120             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    121                                 ***0***     Count coming in to IF
    121             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    122                                 ***0***     Count coming in to IF
    122             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    123                                 ***0***     Count coming in to IF
    123             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    124                                 ***0***     Count coming in to IF
    124             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    125                                 ***0***     Count coming in to IF
    125             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    126                                 ***0***     Count coming in to IF
    126             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    127                                 ***0***     Count coming in to IF
    127             1                   ***0***
                                        ***0***     All False Count
```

Branch totals: 0 hits of 2 branches = 0.00%

Condition Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Conditions	36	18	18	50.00%

==========Condition Details==========

Condition Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv —

----------Focused Condition View----------
Line 51 Item 1 (F_txn.wr_en && (this.count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

----------Focused Condition View----------
Line 57 Item 1 (F_txn.wr_en && (this.count == 8))
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
F_txn.wr_en	Y		
(this.count == 8)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	5	F_txn.wr_en_0	-
Row 2:	5	F_txn.wr_en_1	(this.count == 8)
Row 3:	***0***	(this.count == 8)_0	F_txn.wr_en
Row 4:	5	(this.count == 8)_1	F_txn.wr_en

----------Focused Condition View----------
Line 66 Item 1 (F_txn.rd_en && (this.count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

----------Focused Condition View----------
Line 70 Item 1 (F_txn.rd_en && (this.count == 0))
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
F_txn.rd_en	Y		
(this.count == 0)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	5	F_txn.rd_en_0	-
Row 2:	5	F_txn.rd_en_1	(this.count == 0)
Row 3:	***0***	(this.count == 0)_0	F_txn.rd_en
Row 4:	5	(this.count == 0)_1	F_txn.rd_en

----------Focused Condition View----------
Line 79 Item 1 (~F_txn.rd_en && F_txn.wr_en && ~this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line 82 Item 1 (F_txn.rd_en && ~F_txn.wr_en && ~this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line 85 Item 1 (F_txn.wr_en && F_txn.rd_en && this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line 88 Item 1 (F_txn.wr_en && F_txn.rd_en && this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line 108 Item 1 ((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this.wr_ack_ref) && (F_txn.overflow == this.over
Condition totals: 0 of 8 input terms covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.data_out == this.data_out_ref)	N	'_0' not hit	Hit '_0'
(F_txn.wr_ack == this.wr_ack_ref)	N	'_0' not hit	Hit '_0'
(F_txn.overflow == this.overflow_ref)	N	'_0' not hit	Hit '_0'
(F_txn.underflow == this.underflow_ref)	N	'_0' not hit	Hit '_0'
(F_txn.full == this.full_ref)	N	'_0' not hit	Hit '_0'
(F_txn.empty == this.empty_ref)	N	'_0' not hit	Hit '_0'
(F_txn.almostfull == this.almostfull_ref)	N	'_0' not hit	Hit '_0'
(F_txn.almostempty == this.almostempty_ref)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.data_out == this.data_out_ref)_0	-
Row 2:	5	(F_txn.data_out == this.data_out_ref)_1	((F_txn.wr_ack == this.wr_ack_ref) && ((F_txn.overflow == this.
Row 3:	***0***	(F_txn.wr_ack == this.wr_ack_ref)_0	(F_txn.data_out == this.data_out_ref)
Row 4:	5	(F_txn.wr_ack == this.wr_ack_ref)_1	((F_txn.data_out == this.data_out_ref) && ((F_txn.overflow == t
Row 5:	***0***	(F_txn.overflow == this.overflow_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 6:	5	(F_txn.overflow == this.overflow_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 7:	***0***	(F_txn.underflow == this.underflow_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this

Row 8:	5	(F_txn.underflow == this.underflow_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 9:	***0***	(F_txn.full == this.full_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 10:	5	(F_txn.full == this.full_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 11:	***0***	(F_txn.empty == this.empty_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 12:	5	(F_txn.empty == this.empty_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 13:	***0***	(F_txn.almostfull == this.almostfull_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 14:	5	(F_txn.almostfull == this.almostfull_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 15:	***0***	(F_txn.almostempty == this.almostempty_ref)_0	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this
Row 16:	5	(F_txn.almostempty == this.almostempty_ref)_1	((F_txn.data_out == this.data_out_ref) && (F_txn.wr_ack == this

----------Focused Condition View----------
Line 120 Item 1 (F_txn.data_out !== this.data_out_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.data_out !== this.data_out_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.data_out !== this.data_out_ref)_0	-
Row 2:	***0***	(F_txn.data_out !== this.data_out_ref)_1	-

----------Focused Condition View----------
Line 121 Item 1 (F_txn.wr_ack !== this.wr_ack_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.wr_ack !== this.wr_ack_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.wr_ack !== this.wr_ack_ref)_0	-
Row 2:	***0***	(F_txn.wr_ack !== this.wr_ack_ref)_1	-

----------Focused Condition View----------
Line 122 Item 1 (F_txn.overflow !== this.overflow_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.overflow !== this.overflow_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.overflow !== this.overflow_ref)_0	-
Row 2:	***0***	(F_txn.overflow !== this.overflow_ref)_1	-

----------Focused Condition View----------
Line 123 Item 1 (F_txn.underflow !== this.underflow_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.underflow !== this.underflow_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.underflow !== this.underflow_ref)_0	-
Row 2:	***0***	(F_txn.underflow !== this.underflow_ref)_1	-

----------Focused Condition View----------
Line 124 Item 1 (F_txn.full !== this.full_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.full !== this.full_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.full !== this.full_ref)_0	-
Row 2:	***0***	(F_txn.full !== this.full_ref)_1	-

----------Focused Condition View----------
Line 125 Item 1 (F_txn.empty !== this.empty_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.empty !== this.empty_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.empty !== this.empty_ref)_0	-
Row 2:	***0***	(F_txn.empty !== this.empty_ref)_1	-

----------Focused Condition View----------
Line 126 Item 1 (F_txn.almostfull !== this.almostfull_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.almostfull !== this.almostfull_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.almostfull !== this.almostfull_ref)_0	-
Row 2:	***0***	(F_txn.almostfull !== this.almostfull_ref)_1	-

----------Focused Condition View----------
Line 127 Item 1 (F_txn.almostempty !== this.almostempty_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(F_txn.almostempty !== this.almostempty_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(F_txn.almostempty !== this.almostempty_ref)_0	-
Row 2:	***0***	(F_txn.almostempty !== this.almostempty_ref)_1	-

Expression Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Expressions	4	4	0	100.00%

==========Expression Details==========

Expression Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv --

----------Focused Expression View----------
Line 95 Item 1 (this.count == 0)
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 96 Item 1 (this.count == 8)
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 97 Item 1 (this.count == (8 - 1))
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 98 Item 1 (this.count == 1)
Expression totals: 1 of 1 input term covered = 100.00%

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	43	33	10	76.74%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_scoreboard_pkg.sv --

28	1	5040
32	1	781
33	1	781
34	1	781
35	1	781
36	1	781
37	1	781
38	1	781
39	1	781
40	1	781
41	1	781
42	1	781
43	1	781
52	1	2836
53	1	2836
54	1	2836
56	1	1423
59	1	172
61	1	1251
67	1	969
68	1	969
72	1	284
74	1	3006
80	1	2008
83	1	291
87	1	196
90	1	46
95	1	5040
96	1	5040
97	1	5040
98	1	5040
104	1	5040
116	1	5040
118	1	***0***

119	1	***0***
120	1	***0***
121	1	***0***
122	1	***0***
123	1	***0***
124	1	***0***
125	1	***0***
126	1	***0***
127	1	***0***

==
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv
==

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	2	1	1	50.00%

==========Branch Details==========

Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv —

----------IF Branch----------

41		5000	Count coming in to IF
41	1	***0***	
		5000	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	30	27	3	90.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_tb.sv —

11	1	5
14	1	5
15	1	5
18	1	5
19	1	5
20	1	5
21	1	5
24	1	5
27	1	10
27	2	10
30	1	5
32	1	10
32	2	10
35	1	5
36	1	5
39	1	5
39	2	5000
42	1	***0***
43	1	***0***
47	1	5000
50	1	5000
51	1	5000
52	1	5000
53	1	5000
56	1	5000
61	1	25
61	2	25
62	1	5
65	1	***0***
65	2	5

==
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_top.sv
==

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	4	4	0	100.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_top.sv —

8	1	5
9	1	5
9	2	10080
9	3	10075

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	2	2	0	100.00%

==========Toggle Details==========

```
Toggle Coverage for File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_top.sv --

      Line                                  Node      1H->0L      0L->1H  "Coverage"
--------------------------------------------------------------------------------

Total Node Count     =          1
Toggled Node Count   =          1
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (2 of 2 bins)

================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_transaction_pkg.sv
================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       2         2         0   100.00%

=================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_transaction_pkg.sv --

    44                1                                20
    45                1                                20

================================================================================
=== File: /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

=================================Branch Details=================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv --

------------------------------------IF Branch------------------------------------
    13                                         5681     Count coming in to IF
    13                1                        1424
    18                1                        2839
    23                1                        1418
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                         1418     Count coming in to IF
    25                1                         172
    27                1                        1246
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                         5681     Count coming in to IF
    33                1                        1424
    38                1                         971
    42                1                        3286
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                         3286     Count coming in to IF
    43                1                         284
    45                1                        3002
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                         5306     Count coming in to IF
    51                1                        1375
    54                1                        3931
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                         3931     Count coming in to IF
    55                1                        2009
    57                1                         291
    59                1                          46
    61                1                         196
                                               1389     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                         3141     Count coming in to IF
    66                1                         108
    66                2                        3033
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                         4421     Count coming in to IF
    67                1                        1955
    67                2                        2466
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
```

```
    68                                    3141      Count coming in to IF
    68                1                    157
    68                2                   2984
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                    3141      Count coming in to IF
    69                1                    722
    69                2                   2419
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                    Bins    Covered     Misses  Coverage
    ----------------                    ----    -------     ------  --------
    Conditions                            25         23          2    92.00%

================================Condition Details================================

Condition Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv --

----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.full          N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:    ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          5  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          5  fifo_intf.wr_en_0       fifo_intf.full
  Row    4:          5  fifo_intf.wr_en_1       fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:    ***0***  fifo_intf.empty_0       fifo_intf.rd_en
  Row    2:          5  fifo_intf.empty_1       fifo_intf.rd_en
  Row    3:          5  fifo_intf.rd_en_0       fifo_intf.empty
  Row    4:          5  fifo_intf.rd_en_1       fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       57 Item    1  ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       59 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       61 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       66 Item    1  (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View----------------
Line       67 Item    1  ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View----------------
Line       68 Item    1  (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

----------------Focused Condition View----------------
Line       69 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
```

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv —

12	1	5681
14	1	1424
15	1	1424
16	1	1424
19	1	2839
20	1	2839
21	1	2839
24	1	1418
26	1	172
28	1	1246
32	1	5681
34	1	1424
35	1	1424
36	1	1424
39	1	971
40	1	971
44	1	284
46	1	3002
50	1	5306
52	1	1375
56	1	2009
58	1	291
60	1	46
62	1	196
66	1	3146
67	1	4426
68	1	3146
69	1	3146

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for File /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv —

Line	Node	1H–>0L	0L–>1H	"Coverage"

Total Node Count = 10
Toggled Node Count = 10
Untoggled Node Count = 0

Toggle Coverage = 100.00% (20 of 20 bins)

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	–	Covered
covered/total bins:	194	194	–	
missing/total bins:	0	194	–	
% Hit:	100.00%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	781	1	–	Covered
bin auto[1]	4259	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	95	1	–	Covered
bin auto[1024:2047]	74	1	–	Covered
bin auto[2048:3071]	72	1	–	Covered
bin auto[3072:4095]	72	1	–	Covered
bin auto[4096:5119]	84	1	–	Covered
bin auto[5120:6143]	71	1	–	Covered
bin auto[6144:7167]	70	1	–	Covered
bin auto[7168:8191]	88	1	–	Covered
bin auto[8192:9215]	82	1	–	Covered
bin auto[9216:10239]	71	1	–	Covered
bin auto[10240:11263]	75	1	–	Covered
bin auto[11264:12287]	78	1	–	Covered
bin auto[12288:13311]	76	1	–	Covered
bin auto[13312:14335]	71	1	–	Covered
bin auto[14336:15359]	77	1	–	Covered
bin auto[15360:16383]	85	1	–	Covered

bin auto[16384:17407]	89	1	–	Covered
bin auto[17408:18431]	84	1	–	Covered
bin auto[18432:19455]	74	1	–	Covered
bin auto[19456:20479]	90	1	–	Covered
bin auto[20480:21503]	76	1	–	Covered
bin auto[21504:22527]	79	1	–	Covered
bin auto[22528:23551]	68	1	–	Covered
bin auto[23552:24575]	80	1	–	Covered
bin auto[24576:25599]	75	1	–	Covered
bin auto[25600:26623]	82	1	–	Covered
bin auto[26624:27647]	78	1	–	Covered
bin auto[27648:28671]	79	1	–	Covered
bin auto[28672:29695]	79	1	–	Covered
bin auto[29696:30719]	79	1	–	Covered
bin auto[30720:31743]	72	1	–	Covered
bin auto[31744:32767]	84	1	–	Covered
bin auto[32768:33791]	68	1	–	Covered
bin auto[33792:34815]	80	1	–	Covered
bin auto[34816:35839]	81	1	–	Covered
bin auto[35840:36863]	67	1	–	Covered
bin auto[36864:37887]	71	1	–	Covered
bin auto[37888:38911]	69	1	–	Covered
bin auto[38912:39935]	87	1	–	Covered
bin auto[39936:40959]	83	1	–	Covered
bin auto[40960:41983]	70	1	–	Covered
bin auto[41984:43007]	87	1	–	Covered
bin auto[43008:44031]	92	1	–	Covered
bin auto[44032:45055]	65	1	–	Covered
bin auto[45056:46079]	89	1	–	Covered
bin auto[46080:47103]	72	1	–	Covered
bin auto[47104:48127]	71	1	–	Covered
bin auto[48128:49151]	82	1	–	Covered
bin auto[49152:50175]	73	1	–	Covered
bin auto[50176:51199]	74	1	–	Covered
bin auto[51200:52223]	90	1	–	Covered
bin auto[52224:53247]	90	1	–	Covered
bin auto[53248:54271]	74	1	–	Covered
bin auto[54272:55295]	85	1	–	Covered
bin auto[55296:56319]	82	1	–	Covered
bin auto[56320:57343]	83	1	–	Covered
bin auto[57344:58367]	87	1	–	Covered
bin auto[58368:59391]	80	1	–	Covered
bin auto[59392:60415]	81	1	–	Covered
bin auto[60416:61439]	82	1	–	Covered
bin auto[61440:62463]	80	1	–	Covered
bin auto[62464:63487]	78	1	–	Covered
bin auto[63488:64511]	80	1	–	Covered
bin auto[64512:65535]	78	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3544	1	–	Covered
bin auto[1]	1496	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1517	1	–	Covered
bin auto[1]	3523	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	2622	1	–	Covered
bin auto[1024:2047]	20	1	–	Covered
bin auto[2048:3071]	47	1	–	Covered
bin auto[3072:4095]	29	1	–	Covered
bin auto[4096:5119]	34	1	–	Covered
bin auto[5120:6143]	33	1	–	Covered
bin auto[6144:7167]	56	1	–	Covered
bin auto[7168:8191]	60	1	–	Covered
bin auto[8192:9215]	54	1	–	Covered
bin auto[9216:10239]	28	1	–	Covered
bin auto[10240:11263]	29	1	–	Covered
bin auto[11264:12287]	66	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	46	1	–	Covered
bin auto[14336:15359]	38	1	–	Covered
bin auto[15360:16383]	39	1	–	Covered
bin auto[16384:17407]	60	1	–	Covered
bin auto[17408:18431]	43	1	–	Covered
bin auto[18432:19455]	28	1	–	Covered
bin auto[19456:20479]	48	1	–	Covered
bin auto[20480:21503]	50	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	23	1	–	Covered
bin auto[23552:24575]	31	1	–	Covered
bin auto[24576:25599]	26	1	–	Covered
bin auto[25600:26623]	41	1	–	Covered
bin auto[26624:27647]	39	1	–	Covered
bin auto[27648:28671]	33	1	–	Covered

bin auto[28672:29695]	45	1	–	Covered
bin auto[29696:30719]	26	1	–	Covered
bin auto[30720:31743]	32	1	–	Covered
bin auto[31744:32767]	40	1	–	Covered
bin auto[32768:33791]	28	1	–	Covered
bin auto[33792:34815]	46	1	–	Covered
bin auto[34816:35839]	50	1	–	Covered
bin auto[35840:36863]	22	1	–	Covered
bin auto[36864:37887]	35	1	–	Covered
bin auto[37888:38911]	38	1	–	Covered
bin auto[38912:39935]	41	1	–	Covered
bin auto[39936:40959]	39	1	–	Covered
bin auto[40960:41983]	26	1	–	Covered
bin auto[41984:43007]	54	1	–	Covered
bin auto[43008:44031]	65	1	–	Covered
bin auto[44032:45055]	41	1	–	Covered
bin auto[45056:46079]	23	1	–	Covered
bin auto[46080:47103]	27	1	–	Covered
bin auto[47104:48127]	34	1	–	Covered
bin auto[48128:49151]	35	1	–	Covered
bin auto[49152:50175]	40	1	–	Covered
bin auto[50176:51199]	27	1	–	Covered
bin auto[51200:52223]	58	1	–	Covered
bin auto[52224:53247]	59	1	–	Covered
bin auto[53248:54271]	34	1	–	Covered
bin auto[54272:55295]	42	1	–	Covered
bin auto[55296:56319]	28	1	–	Covered
bin auto[56320:57343]	69	1	–	Covered
bin auto[57344:58367]	46	1	–	Covered
bin auto[58368:59391]	29	1	–	Covered
bin auto[59392:60415]	18	1	–	Covered
bin auto[60416:61439]	29	1	–	Covered
bin auto[61440:62463]	40	1	–	Covered
bin auto[62464:63487]	22	1	–	Covered
bin auto[63488:64511]	40	1	–	Covered
bin auto[64512:65535]	43	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2204	1	–	Covered
bin auto[1]	2836	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4811	1	–	Covered
bin auto[1]	229	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4756	1	–	Covered
bin auto[1]	284	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3900	1	–	Covered
bin auto[1]	1140	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4780	1	–	Covered
bin auto[1]	260	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3943	1	–	Covered
bin auto[1]	1097	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4700	1	–	Covered
bin auto[1]	340	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	828	1	–	Covered
bin <auto[1],auto[1],auto[0]>	211	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2008	1	–	Covered
bin <auto[0],auto[1],auto[0]>	476	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered

covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	234	1	–	Covered
bin <auto[0],auto[0],auto[1]>	50	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1039	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2250	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1010	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	165	1	–	Covered
bin <auto[1],auto[0],auto[1]>	242	1	–	Covered
bin <auto[1],auto[1],auto[0]>	874	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2134	1	–	Covered
bin <auto[1],auto[0],auto[0]>	215	1	–	Covered
bin <auto[0],auto[0],auto[0]>	677	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	733		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	107	1	–	Covered
bin <auto[0],auto[1],auto[1]>	89	1	–	Covered
bin <auto[1],auto[0],auto[1]>	22	1	–	Covered
bin <auto[0],auto[0],auto[1]>	42	1	–	Covered
bin <auto[1],auto[1],auto[0]>	932	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2395	1	–	Covered
bin <auto[1],auto[0],auto[0]>	435	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1018	1	–	Covered
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	8	8	–	
missing/total bins:	0	8	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	384	1	–	Covered
bin <auto[0],auto[1],auto[1]>	477	1	–	Covered
bin <auto[1],auto[0],auto[1]>	49	1	–	Covered
bin <auto[0],auto[0],auto[1]>	187	1	–	Covered
bin <auto[1],auto[1],auto[0]>	655	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2007	1	–	Covered
bin <auto[1],auto[0],auto[0]>	408	1	–	Covered
bin <auto[0],auto[0],auto[0]>	873	1	–	Covered
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	75	1	–	Covered
bin <auto[1],auto[1],auto[0]>	964	1	–	Covered
bin <auto[0],auto[1],auto[1]>	154	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2330	1	–	Covered
bin <auto[1],auto[0],auto[0]>	457	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	231	1	–	Covered
bin <auto[1],auto[0],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	808	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2484	1	–	Covered
bin <auto[1],auto[0],auto[0]>	348	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1060	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
/FIFO_top/dut/cover__counter_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(169)	4262	Covered
/FIFO_top/dut/cover__read_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(168)	4262	Covered
/FIFO_top/dut/cover__write_ptr_threshold	FIFO	Verilog	SVA	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(167)	4262	Covered

/FIFO_top/dut/cover__read_ptr_wraparound FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(166)
10 Covered
/FIFO_top/dut/cover__write_ptr_wraparound
FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(165)
111 Covered
/FIFO_top/dut/cover__almost_empty_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(164)
900 Covered
/FIFO_top/dut/cover__almost_full_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(163)
230 Covered
/FIFO_top/dut/cover__full_flag_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(162)
244 Covered
/FIFO_top/dut/cover__empty_flag_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(161)
956 Covered
/FIFO_top/dut/cover__underflow_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(160)
245 Covered
/FIFO_top/dut/cover__overflow_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(159)
108 Covered
/FIFO_top/dut/cover__write_ack_check FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(158)
2398 Covered
/FIFO_top/dut/cover__reset_behavior FIFO Verilog SVA /home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(157)
781 Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 13

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
/FIFO_top/dut/assert__counter_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(155)	0	5
/FIFO_top/dut/assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(154)	0	5
/FIFO_top/dut/assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(153)	0	5
/FIFO_top/dut/assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(152)	0	5
/FIFO_top/dut/assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(151)	0	5
/FIFO_top/dut/assert__almost_empty_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(150)	0	5
/FIFO_top/dut/assert__almost_full_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(149)	0	5
/FIFO_top/dut/assert__full_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(148)	0	5
/FIFO_top/dut/assert__empty_flag_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(147)	0	5
/FIFO_top/dut/assert__underflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(146)	0	5
/FIFO_top/dut/assert__overflow_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(145)	0	5
/FIFO_top/dut/assert__write_ack_check	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(144)	0	5
/FIFO_top/dut/assert__reset_behavior	/home/tare/Desktop/syn_fifo/sv_verification/FIFO_v1.0.0.sv(143)	0	5

Total Coverage By File (code coverage only, filtered view): 85.76%