SV Project

Digital Design Verification

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	ndronous FIFO Stard padage* - 'up Middle* - IPD-3d pk - IFD-3d pk

1 Synchronous FIFO

1.1 Shared package

```
package Shared_pkg;
// ===== Global parameter for Signal Declaration =====

parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;

// ===== Signals For Test Control ======

// ==== #No of Randomization ======

parameter TEST_COUNT = 1000;
// ===== Counter For Failed and Successed Test Transactions ======

int unsigned error_count = 0;
int unsigned correct_count = 0;
// ===== When eq 1 Trim Test =====

bit test_finished = 0;
endpackage
```

1.2 Top Module

1.3 FIFO_IF

```
import Shared_pkg::*;
import FIFO_test_pkg::*;
import uvm_pkg::*;
4 'include "uvm_macros.svh"
6 module top();
     bit clk;
     initial begin
       forever
          #1 clk = ~clk;
11
12
     FIFO_IF fifo_intf (clk);
14
16
     FIFO #(
      .FIFO_WIDTH(FIFO_WIDTH),
17
       .FIFO_DEPTH(FIFO_DEPTH)
18
     ) dut (
19
      .fifo_intf(fifo_intf)
20
22
     initial begin
23
        uvm_config_db#(virtual FIF0_IF)::set(null, "uvm_test_top", "FIF0_VIF", fifo_intf);
24
        run_test("FIFO_test");
25
26
30 // Assertions using conditional compilation
32 'ifdef SIM
       // ===== Reset behavior assertion =====
34
       property reset_behavior;
35
          @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=> (dut.count == 0 && dut.rd_ptr == 0 && dut.wr_ptr == 0
                       && !fifo_intf.wr_ack && !fifo_intf.overflow && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
       endproperty
       // ===== Whenever the FIFO is full, wr_ack is always = 0 =====
       property n_wr_ack_with_FIF0_Full;
                  @(posedge clk) disable iff (!fifo_intf.rst_n) (fifo_intf.full |=> !fifo_intf.wr_ack)
       endproperty
       // ===== Write acknowledge assertion =====
       property write_ack_check;
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
       endproperty
       // ===== Overflow detection assertion =====
       property overflow_check;
51
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
52
       endproperty
54
       // ===== Underflow detection assertion =====
       property underflow_check;
56
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
57
58
       endproperty
59
       // ===== Empty flag assertion =====
60
61
       property empty_flag_check;
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.count == 0) |-> fifo_intf.empty;
62
63
       endproperty
64
       // ===== Full flag assertion =====
65
66
       property full_flag_check;
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.count == FIFO_DEPTH) |-> fifo_intf.full;
67
       endproperty
68
69
       // ===== Almost full condition assertion =====
70
       property almost_full_check;
71
          @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
72
       endproperty
```

```
// ===== Almost empty condition assertion =====
        property almost_empty_check;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.count == 1) |-> fifo_intf.almostempty;
        endproperty
79
        // ===== Pointer wraparound assertion for write_ptr =====
80
        property write_ptr_wraparound;
81
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && dut.wr_ptr == FIFO_DEPTH-1) |=>
                (dut.wr_ptr == 0);
        endproperty
83
84
        // ===== Pointer wraparound assertion for read_ptr =====
        property read_ptr_wraparound;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && dut.rd_ptr == FIFO_DEPTH-1) |=>
87
                (dut.rd_ptr == 0);
        {\tt endproperty}
88
        // ===== Pointer threshold assertion for write_ptr =====
        property write_ptr_threshold;
91
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.wr_ptr < FIFO_DEPTH);</pre>
92
        endproperty
94
        // ===== Pointer threshold assertion for read_ptr =====
95
        property read_ptr_threshold;
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.rd_ptr < FIFO_DEPTH);</pre>
97
98
        endproperty
99
        // ===== Counter threshold assertion =====
100
        property counter_threshold;
101
            @(posedge fifo_intf.clk) disable iff (!fifo_intf.rst_n) (dut.count <= FIFO_DEPTH);</pre>
102
        endproperty
103
104
        // ===== Assert all the properties =====
105
                                                else $error("Reset_behavior_assertion_failed!");
        assert property (reset_behavior)
106
        assert property (write_ack_check)
                                                else $error("Write acknowledge assertion failed!");
107
                                                else $error("Overflow detection assertion failed!");
        assert property (overflow_check)
108
        assert property (underflow_check)
                                                else $error("Underflow_detection_assertion_failed!");
109
110
        assert property (empty_flag_check)
                                                else $error("Empty_flag_assertion_failed!");
        assert property (full_flag_check)
                                                else $error("Full_\_flag_\_assertion_\_failed!");
        assert property (almost_full_check)
                                                else $error("Almostufulluconditionuassertionufailed!");
112
        assert property (almost_empty_check)
                                                else $error("Almost⊥empty⊥condition⊥assertion⊥failed!");
113
        assert property (write_ptr_wraparound) else $error("Write_pointer_wraparound_assertion_failed!");
114
        assert property (read_ptr_wraparound)
                                                else $error("Read_pointer_wraparound_assertion_failed!");
115
        assert property (write_ptr_threshold)
                                                else $error("Write_pointer_threshold_assertion_failed!");
116
        assert property (read_ptr_threshold)
                                                else $error("Read_pointer_threshold_assertion_failed!");
117
        assert property (counter_threshold)
                                                else $error("Counter threshold assertion failed!");
118
        assert property (n_wr_ack_with_FIFO_Full) else $error("Dasserted_Write_Ack_With_FIFO_Full_assertion_failed!");
119
120
        cover property (reset_behavior);
121
        cover property (write_ack_check);
122
        cover property (overflow_check);
123
124
        cover property (underflow_check);
125
        cover property (empty_flag_check);
        cover property (full_flag_check);
126
        cover property (almost_full_check);
127
        cover property (almost_empty_check);
128
        cover property (write_ptr_wraparound);
129
130
        cover property (read_ptr_wraparound);
131
        cover property (write_ptr_threshold);
        cover property (read_ptr_threshold);
132
        cover property (counter_threshold);
133
        cover property (n_wr_ack_with_FIF0_Full);
134
135
136
    'endif
137
138 endmodule
    1.4 FIFO_config_obj_pkg
 package FIFO_config_obj_pkg;
      import uvm_pkg::*;
      'include "uvm_macros.svh"
      class FIFO_config_obj extends uvm_object;
        'uvm_object_utils(FIFO_config_obj)
        virtual FIF0_IF FIF0_config_vif;
 10
        function new (string name = "FIFO_config_obj");
11
          super.new(name);
12
        endfunction
13
14
      endclass
15
16
    endpackage
    1.5 	ext{ FIFO_test_pkg}
 package FIFO_test_pkg;
 3 import FIFO_env_pkg::*;
   import FIFO_config_obj_pkg::*;
    import FIFO_sequence_pkg::*;
    import uvm_pkg::*;
    'include "uvm_macros.svh"
```

```
class FIFO_test extends uvm_test;
          'uvm_component_utils(FIFO_test)
11
           FIFO_env env;
           FIFO_config_obj FIFO_config_obj_test;
13
           FIF0_Sequence seq;
14
           function new (string name = "FIFO_test", uvm_component parent = null);
               super.new(name,parent);
           endfunction
19
           function void build_phase(uvm_phase phase);
20
21
               super.build_phase(phase);
22
               env = FIFO_env::type_id::create("env",this);
               FIFO_config_obj_test = FIFO_config_obj::type_id::create("FIFO_config_obj_test",this);
               seq = FIFO_Sequence::type_id::create("seq");
               if (!uvm_config_db#(virtual FIF0_IF)::get(this, "", "FIF0_VIF", FIF0_config_obj_test.FIF0_config_vif))
26
                            \verb"uvm_fatal("NOVIF", "Virtual_interface_FIFO_test_vif_was_not_found_in_the_configuration_database");
               uvm_config_db#(FIF0_config_obj)::set(this,"*","CFG",FIF0_config_obj_test);
           endfunction
31
           task run_phase(uvm_phase phase);
32
               super.run_phase(phase);
               phase.raise_objection(this);
34
                'uvm_info("run_phase","Inside_the_FIFO_test.",UVM_MEDIUM);
           seq.start(env.agt.sqr);
           phase.drop_objection(this);
37
38
           endtask : run_phase
       endclass : FIFO_test
42 endpackage
   1.6 FIFO_sequence_pkg
package FIFO_sequence_pkg;
3 import uvm_pkg::*;
   'include "uvm_macros.svh"
   import FIFO_sequence_item_pkg::*;
   class FIFO_Sequence extends uvm_sequence #(FIFO_seq_item);
       'uvm_object_utils(FIFO_Sequence)
       FIFO_seq_item item;
       function new(string name = "FIFO_Sequence");
11
           super.new(name);
12
       endfunction
13
14
       virtual task body();
       item = FIFO_seq_item::type_id::create("item");
            // ===== force reset ====
17
           item.force_rst_item;
           repeat(5) begin
19
               start_item(item);
           if (!item.randomize())
                   'uvm_error("RAND_FAIL", "FailedutouforceureseturandomizeuFIFOusequenceuitem");
22
           finish_item(item);
23
24
       end
25
           // ===== simultaneous Read And Write =====
26
27
       item.ctrl_seq_item(30,70);
       repeat (1000) begin
28
           start_item(item);
29
           if (!item.randomize())
                    'uvm_error("RAND_FAIL", "FailedutousimultaneousuReaduAnduWriteurandomizeuFIFOusequenceuitem");
31
           finish_item(item);
33
       end
34
35
       // ===== Read only =====
       item.ctrl_seq_item(0,100);
       repeat (100) begin
37
           start_item(item);
           if (!item.randomize())
                    'uvm_error("RAND_FAIL", "FailedutouReaduonlyurandomizeuFIFOusequenceuitem");
           finish_item(item);
42
43
       // ===== Write only =====
       item.ctrl_seq_item(100,0);
45
       repeat (100) begin
46
           start_item(item);
47
           if (!item.randomize())
48
                    'uvm_error("RAND_FAIL", "FailedutouWriteuonlyurandomizeuFIFOusequenceuitem");
49
50
           finish_item(item);
       end
51
52
53
       endtask
54
   endclass
57 endpackage
```

1.7 FIFO_env_pkg

package FIF0_env_pkg;

```
3 import uvm_pkg::*;
  'include "uvm_macros.svh"
5 import FIFO_coverage_pkg::*;
6 import FIFO_scoreboard_pkg::*;
   import FIF0_agent_pkg::*;
       class FIFO_env extends uvm_env;
           'uvm_component_utils(FIFO_env)
           FIFO_agent agt;
12
           FIFO_scoreboard sb;
13
           FIFO_coverage cov;
           function new (string name = "FIFO_env", uvm_component parent = null);
           super.new(name,parent);
           endfunction
19
           function void build_phase(uvm_phase phase);
               super.build_phase(phase);
               agt = FIFO_agent::type_id::create("agt",this);
               sb = FIFO_scoreboard::type_id::create("sb",this);
               cov = FIF0_coverage::type_id::create("cov",this);
           endfunction: build_phase
               function void connect_phase(uvm_phase phase);
               agt.agt_ap.connect(sb.sb_export);
               agt.agt_ap.connect(cov.cov_export);
           endfunction: connect_phase
30
31
       endclass : FIFO_env
32
34 endpackage
        FIFO_coverage_pkg
package FIFO_coverage_pkg;
3 import uvm_pkg::*;
   'include "uvm_macros.svh"
   import FIFO_sequence_item_pkg::*;
   class FIFO_coverage extends uvm_component;
       'uvm_component_utils(FIFO_coverage)
       uvm_analysis_export #(FIFO_seq_item) cov_export;
       uvm_tlm_analysis_fifo #(FIFO_seq_item) cov_fifo;
       FIFO_seq_item seq_item_cov;
12
       // ===== Cover Group =====
       covergroup fifo_cg;
15
           // ===== Cover I/O Ports =====
           rst_n_cp: coverpoint seq_item_cov.rst_n;
           data_in_cp: coverpoint seq_item_cov.data_in;
           r_en_cp: coverpoint seq_item_cov.rd_en;
           w_en_cp: coverpoint seq_item_cov.wr_en;
           data_out_cp: coverpoint seq_item_cov.data_out;
21
                           coverpoint seq_item_cov.wr_ack;
           wr_ack_cp:
           overflow_cp: coverpoint seq_item_cov.overflow;
           full_cp: coverpoint seq_item_cov.full;
                           coverpoint seq_item_cov.empty;
           empty_cp:
           almostfull_cp: coverpoint seq_item_cov.almostfull;
27
           almostempty_cp: coverpoint seq_item_cov.almostempty;
           underflow_cp: coverpoint seq_item_cov.underflow;
           // ===== "7" Cross Coverage =====
           wr_ack_cross: cross r_en_cp ,w_en_cp ,wr_ack_cp{
32
                                                    = binsof(w_en_cp) intersect {1'b0} && binsof(wr_ack_cp) intersect {1'b1};
               ignore_bins w_en_nactv_wr_ack
33
                              cross r_en_cp ,w_en_cp ,full_cp{
               // full not asserted when both read and write enabled
               ignore_bins w_en_r_en_allactv_full = binsof(w_en_cp) intersect {1'b1} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
                   intersect {1'b1};
               // full not asserted when read enabled
               ignore_bins r_en_actv_wr_full
                                                  = binsof(w_en_cp) intersect {1'b0} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
                  intersect {1'b1};
           }
                            cross r_en_cp ,w_en_cp ,empty_cp{
           empty_cross:
42
               ignore_bins read_nactv_empty
                                                = binsof(r_en_cp) intersect {1'b0} && binsof(empty_cp) intersect {1'b1};
43
44
45
           almostfull\_cross: cross r\_en\_cp , w\_en\_cp , almostfull\_cp\{
                   // who almostfull with read
47
               ignore_bins w_en_nactv_almostfull
                                                  = binsof(r_en_cp) intersect {1'b0} && binsof(almostfull_cp) intersect {1'b1};
48
49
50
           almostempty_cross: cross r_en_cp ,w_en_cp ,almostempty_cp{
51
               // who almostempty with write
               ignore\_bins \ w\_en\_nactv\_almostempty \ = \ binsof(w\_en\_cp) \ intersect \ \{1'b0\} \ \&\& \ binsof(almostempty\_cp) \ intersect \ \{1'b1\};
53
54
55
           \verb| overflow_cross: | cross r_en_cp , w_en_cp , overflow_cp{|}
56
               ignore_bins w_en_nactv_wr_ack
                                                  = binsof(w_en_cp) intersect {1'b0} && binsof(overflow_cp) intersect {1'b1};
57
58
59
           underflow_cross: cross r_en_cp ,w_en_cp ,underflow_cp{
60
                                                = binsof(r_en_cp) intersect {1'b0} && binsof(underflow_cp) intersect {1'b1};
               ignore_bins r_en_nactv_wr_ack
61
62
```

```
endgroup
      function new(string name="FIF0_coverage" , uvm_component parent = null);
          super.new(name,parent);
          fifo_cg = new();
69
      endfunction
      function void build_phase (uvm_phase phase);
          super.build_phase(phase);
73
          cov_export = new("cov_export",this);
74
          cov_fifo = new("cov_fifo",this);
      endfunction: build_phase
      function void connect_phase (uvm_phase phase);
          super.connect_phase(phase);
          cov_export.connect(cov_fifo.analysis_export);
80
      endfunction: connect_phase
      task run_phase (uvm_phase phase);
          super.run_phase(phase);
          forever begin
85
             cov_fifo.get(seq_item_cov);
             fifo_cg.sample();
      endtask: run_phase
91 endclass
92 endpackage
       FIFO_sequence_item_pkg
  package FIFO_sequence_item_pkg ;
3 import Shared_pkg::*;
  import uvm_pkg::*;
   'include "uvm_macros.svh"
   class FIFO_seq_item extends uvm_sequence_item;
      'uvm_object_utils(FIFO_seq_item)
      // -----
      // Transaction Distribution "Set to Default Values"
      int RD_EN_ON_DIST;
13
      int WR_EN_ON_DIST;
      bit force_rst = 1;
      // Class Constructor
      // ========
          function new(string name = "FIFO_seq_item");
          super.new(name);
      \verb"endfunction"
24
      // ==== input signals ====
      rand bit rst_n;
      rand bit [FIF0_WIDTH-1:0] data_in;
      rand bit wr_en;
      rand bit rd_en;
      // ==== output signals ====
      bit [FIFO_WIDTH-1:0] data_out;
      bit wr_ack, overflow;
      bit full, empty, almostfull, almostempty, underflow;
35
36
      // Dassert Reset "Asyn - Active Low" most of the times
          constraint rst_c {
             if (!force_rst) {
                rst_n dist {0:/10 , 1:/90};
41
             if (force_rst) {
                rst_n dist {0:=100, 1:=0};
             }
47
           constraint data_in_c {
48
                 data_in dist {0:/15 , {FIFO_WIDTH{1'b1}}:/15 , [1:{FIFO_WIDTH{1'b1}}-1] :/ 70};
49
50
      // -----
52
      // Only, Enable Write Enable Signal During "WR_EN_ON_DIST"
53
      // -----
54
      constraint wr_en_c { wr_en dist {1 := WR_EN_ON_DIST, 0 := 100-WR_EN_ON_DIST};}
55
56
57
      // -----
      // Only, Enable Read Enable Signal During "RD_EN_ON_DIST"
58
      // -----
59
      constraint rd_en_c { rd_en dist {1 := RD_EN_ON_DIST, 0 := 100-RD_EN_ON_DIST};}
60
61
      function void ctrl_seq_item (int rd_dist = 30 ,int wr_dist = 70);
62
63
          RD_EN_ON_DIST = rd_dist;
          WR_EN_ON_DIST = wr_dist;
64
          force_rst = 0;
65
      endfunction
66
```

```
function void force_rst_item;
           force_rst = 1;
       endfunction
72 endclass
74 endpackage
   1.10 FIFO_sequencer_pkg
package FIFO_sequencer_pkg;
3 import uvm_pkg::*;
   'include "uvm_macros.svh"
   import FIFO_sequence_item_pkg::*;
   class FIFO_sequencer extends uvm_sequencer #(FIFO_seq_item);
       'uvm_component_utils(FIFO_sequencer)
       function new(string name = "FIFO_sequencer" ,uvm_component parent = null);
11
           super.new(name ,parent);
       endfunction
14 endclass
15
16 endpackage
   1.11 FIFO_agent_pkg
package FIFO_agent_pkg;
import uvm_pkg::*;
import FIFO_sequencer_pkg::*;
5 import FIFO_driver_pkg::*;
6 import FIFO_monitor_pkg::*;
7 import FIFO_config_obj_pkg::*;
   import FIFO_sequence_item_pkg::*;
   'include "uvm_macros.svh"
   class FIFO_agent extends uvm_agent;
11
12
           'uvm_component_utils(FIFO_agent)
       FIFO_sequencer sqr;
14
       FIFO_driver drv;
15
       FIFO_monitor mon;
       FIFO_config_obj FIFO_cfg;
           uvm_analysis_port #(FIFO_seq_item) agt_ap;
19
       function new(string name = "FIF0_agent",uvm_component parent = null);
20
           super.new(name,parent);
21
22
       endfunction
23
24
       function void build_phase(uvm_phase phase);
           super.build_phase(phase);
           if(!uvm_config_db #(FIFO_config_obj)::get(this,"","CFG",FIFO_cfg))
26
                'uvm_fatal("build_phase","unableutougetuconfigurationuobject");
           sqr=FIF0_sequencer::type_id::create("sqr",this);
           drv=FIFO_driver::type_id::create("drv",this);
           mon=FIFO_monitor::type_id::create("mon",this);
31
           agt_ap = new("agt_ap", this);
       endfunction
32
33
34
       function void connect_phase(uvm_phase phase);
               super.connect_phase(phase);
35
           drv.FIFO_driver_vif=FIFO_cfg.FIFO_config_vif;
           mon.FIF0_vif=FIF0_cfg.FIF0_config_vif;
37
           drv.seq_item_port.connect(sqr.seq_item_export);
38
               mon.mon_ap.connect(agt_ap);
       endfunction
42 endclass
44 endpackage
   1.12 FIFO_driver_pkg
   package FIFO_driver_pkg;
   import uvm_pkg::*;
   import FIFO_config_obj_pkg::*;
   import FIFO_sequence_item_pkg::*;
   'include "uvm_macros.svh"
       class FIFO_driver extends uvm_driver #(FIFO_seq_item);
         'uvm_component_utils(FIFO_driver)
10
         virtual FIF0_IF FIF0_driver_vif;
11
         FIFO_config_obj FIFO_cfg_obj_drv;
12
         FIFO_seq_item stim_seq_item;
13
14
         function new(string name = "FIFO_driver", uvm_component parent = null);
15
           super.new(name, parent);
16
         endfunction
17
18
         function void build_phase(uvm_phase phase);
19
           super.build_phase(phase);
20
           if (!uvm_config_db#(FIFO_config_obj)::get(this, "", "CFG", FIFO_cfg_obj_drv)) begin
21
```

```
"uvm_fatal("build_phase", "Driveru-Unableutougetuconfigurationuobject")
           end
         endfunction
         function void connect_phase(uvm_phase phase);
           FIFO_driver_vif = FIFO_cfg_obj_drv.FIFO_config_vif;
27
         endfunction
28
           task run_phase(uvm_phase phase);
               super.run_phase(phase);
32
               forever begin
33
34
                   stim_seq_item = FIFO_seq_item::type_id::create("stim_seq_item");
                   seq_item_port.get_next_item(stim_seq_item);
                   // ==== Input =====
                   FIFO_driver_vif.data_in = stim_seq_item.data_in;
                   FIFO_driver_vif.wr_en = stim_seq_item.wr_en;
39
                   FIFO_driver_vif.rd_en
                                            = stim_seq_item.rd_en;
                                           = stim_seq_item.rst_n;
                   FIFO_driver_vif.rst_n
41
                   // Wait for the next negative clock edge
                   @(negedge FIFO_driver_vif.clk);
44
45
                   seq_item_port.item_done();
               end
47
           endtask
50
       endclass
51
   endpackage
   1.13 FIFO_monitor_pkg
package FIFO_monitor_pkg;
   import uvm_pkg::*;
   'include "uvm_macros.svh"
   import FIFO_sequence_item_pkg::*;
   class FIFO_monitor extends uvm_monitor ;
          'uvm_component_utils(FIFO_monitor)
       virtual FIFO_IF FIFO_vif;
       FIFO_seq_item rsp_seq_item;
11
       uvm_analysis_port #(FIFO_seq_item) mon_ap;
13
       function new(string name = "FIFO_monitor", uvm_component parent = null);
14
           super.new(name ,parent);
15
       endfunction
16
17
       function void build_phase (uvm_phase phase);
           super.build_phase(phase);
19
           mon_ap = new("mon_ap",this);
20
21
       endfunction
22
       task run_phase (uvm_phase phase);
23
           super.run_phase(phase);
           forever begin
25
               rsp_seq_item = FIFO_seq_item::type_id::create("rsp_seq_item");
26
                   // ==== Wait for posedge clock to sample data ====
                   @(posedge FIFO_vif.clk);
                   // ==== smale delay for stable output ====
                           #1;
31
                   // ==== Wait for sampling event from testbench ====
32
                   FIFO_vif.trigger_sample();
34
               // ==== Input =====
               rsp_seq_item.data_in = FIFO_vif.data_in;
               rsp_seq_item.wr_en = FIF0_vif.wr_en;
37
                                    = FIFO_vif.rd_en;
               rsp_seq_item.rd_en
               rsp_seq_item.rst_n = FIFO_vif.rst_n;
               // ==== Output =====
               rsp_seq_item.data_out
                                        = FIF0_vif.data_out ;
                                        = FIFO_vif.full;
               rsp_seq_item.full
43
               rsp_seq_item.empty
                                        = FIFO_vif.empty
               rsp_seq_item.almostfull = FIF0_vif.almostfull;
               rsp_seq_item.almostempty = FIFO_vif.almostempty;
               rsp_seq_item.overflow = FIFO_vif.overflow ;
               rsp_seq_item.underflow = FIF0_vif.underflow;
48
               rsp_seq_item.wr_ack
                                        = FIFO_vif.wr_ack ;
49
50
               mon_ap.write(rsp_seq_item);
51
52
           end
53
       endtask
54
55
   endclass
```

1.14 FIFO_scoreboard_pkg

1.15 FIFO

57 endpackage

```
module FIFO(FIFO_IF.DUT fifo_intf);
   parameter FIFO_WIDTH = 16;
  parameter FIFO_DEPTH = 8;
5 localparam max_fifo_addr = $clog2(FIFO_DEPTH);
   reg [FIF0_WIDTH-1:0] mem [FIF0_DEPTH-1:0]; // 1-D Array
   reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
12
13
       if (!fifo_intf.rst_n) begin
           wr_ptr <= 0;
14
           fifo_intf.wr_ack <= 0;
15
           fifo_intf.overflow <= 0;</pre>
17
       else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin</pre>
18
           mem[wr_ptr] <= fifo_intf.data_in;</pre>
           fifo_intf.wr_ack <= 1;</pre>
20
           wr_ptr <= wr_ptr + 1;
21
       end
       else begin
23
           fifo_intf.wr_ack <= 0;
24
           if (fifo_intf.full & fifo_intf.wr_en)
               fifo_intf.overflow <= 1;</pre>
26
                fifo_intf.overflow <= 0;
29
       end
30 end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
32
       if (!fifo_intf.rst_n) begin
           rd_ptr <= 0;
           fifo_intf.underflow <= 0;</pre>
35
           fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};</pre>
36
37
       else if (fifo_intf.rd_en && count != 0) begin
38
           fifo_intf.data_out <= mem[rd_ptr];</pre>
40
           rd_ptr <= rd_ptr + 1;
41
       else begin
           if (fifo_intf.empty & fifo_intf.rd_en)
43
                fifo_intf.underflow <= 1;</pre>
44
           else
               fifo_intf.underflow <= 0;
46
       end
47
   end
   always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
       if (!fifo_intf.rst_n) begin
           count <= 0;
52
53
54
       else begin
           if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
                count <= count + 1;</pre>
           else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
               count <= count - 1;</pre>
           else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.full)
               count <= count - 1;
           else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.empty)
61
                count <= count + 1;</pre>
63
64 end
assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;
71 endmodule
```

2 Makefile Contain Do File

```
VSIM = vsim
VLOG = qverilog
# Define UVM Directory
UVMDIR = ${FIFO_ROOT}/uvm_verification
# Target flist
target = src_files
FLIST = \{target\}.list
VPATH = \$(UVMDIR)
TBFILES = (UVMDIR)/(FLIST)
# Define 5 seed values
SEEDS = 1111 \ 1511 \ 2515 \ 2236 \ 5215
# Targets
clean:
       rm -rf *.log *.dis *.tbl vcs* simv* *.map transcript *.ucdb *.wlf *.txt \
       work dataset.asdb library.cfg work
questa: ${TBFILES}
```

```
$(VLOG) -1 vlog.log -sv -mfcu -f ${TBFILES} +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"
questa+SIM: ${TBFILES}
        $(VLOG) -1 vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"
# Run simulation with a specific seed
seed%: ${TBFILES}
        @echo "Running simulation with seed $*"
        $(VLOG) -1 vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
        $(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -sv_seed $* -do "do wave.do; coverage save FIFO_seed$*.ucdb -
        vcover report FIFO_seed$*.ucdb -details -annotate -all -output code_coverage_rpt_seed$*.txt -du=FIFO
        vcover report -details -cvg -output functional_coverage_report_seed$*.txt FIFO_seed$*.ucdb
# Run all seeds in sequence
all_seeds: ${TBFILES}
        @echo "Running simulations with all seeds"
        VOG -1 \ vlog.log -sv -mfcu -f \ TBFILES + define + SIM + cover - covercells -R + now arn 3829
        @for seed in $(SEEDS); do \
                echo ""; \
                echo "Running simulation with seed $$seed"; \
                $(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -sv_seed $$seed -do "do wave.do; coverage save FIFO_s
                vcover report FIFO_seed$$seed.ucdb -details -annotate -all -output code_coverage_rpt_seed$$seed.txt -du=FIFO; \
                vcover report -details -cvg -output functional_coverage_report_seed$$seed.txt FIFO_seed$$seed.ucdb; \
        done
        @echo "All seed runs completed"
# Merge coverage results from all seeds
merge_coverage:
        @echo "Merging coverage from all seed runs"
        vcover merge merged.ucdb FIFO_seed*.ucdb
        $(VSIM) -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
        vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
        vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
        @echo "Coverage merged to merged.ucdb and reports saved"
# Run all seeds and merge coverage
run_seeds: all_seeds merge_coverage
        @echo "Complete seed-based simulation and coverage analysis finished"
help:
        @echo Make sure the environment variable FIFO_ROOT is set.
        @echo Possible targets:
        @echo "
                 questa
                               - Run basic simulation"
        @echo "
                 questa+SIM - Run simulation with +SIM defined"
        @echo "
                 seed < number > - Run simulation with specific seed (e.g., seed1, seed2)"
        @echo "
                             - Run simulations with all predefined seeds"
        @echo "
                 merge_coverage - Merge coverage data from all seed runs"
        @echo "
                              - Run all seeds and merge coverage"
                 run\_seeds
        @echo "
                 clean
                               - Clean up simulation files"
```

3 Functional Coverage Report

3.1 Functional Coverage "seed1" Report

Coverage Report by instance with details

Covergroup Bins

185

190

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100		Uncovered
covered/total bins:	185	190	_	
missing/total bins:	5	190	_	
% Hit:	97.36%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	137	1	_	Covered
bin auto[1]	1068	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0\!:\!1023\right]$	190	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[1024 \colon\! 2047 \right]$	9	1	_	Covered
bin auto $[2048:3071]$	9	1	_	Covered
bin auto $[3072:4095]$	12	1	_	Covered
bin auto [4096:5119]	13	1	_	Covered
bin auto [5120:6143]	12	1	_	Covered

97.36%

bin auto $[6144:7167]$	10	1	_	Covered
bin auto [7168:8191]	11	1	_	Covered
bin auto [8192:9215]	12	1	_	Covered
bin auto [9216:10239]	12	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
bin auto $[11264:12287]$	11	1	_	Covered
bin auto [12288:13311]	15	1	_	Covered
bin auto [13312:14335]	12	1	_	Covered
bin auto [14336:15359]	17	1	_	Covered
bin auto [15360:16383]	9	1	_	Covered
bin auto $[16384:17407]$	13	1	_	Covered
bin auto [17408:18431]	14	1	_	Covered
bin auto [18432:19455]	20	1	_	Covered
bin auto [19456:20479]	21	1		Covered
			_	
$\operatorname{bin} \ \operatorname{auto} \left[20480 \colon\! 21503 \right]$	7	1	_	Covered
bin auto $[21504:22527]$	18	1	_	Covered
bin auto $[22528:23551]$	18	1	_	Covered
bin auto [23552:24575]	13	1	_	Covered
bin auto $[24576:25599]$	10	1	_	Covered
bin auto $[25600:26623]$	17	1	_	Covered
bin auto $[26624:27647]$	17	1	_	Covered
bin auto [27648:28671]	12	1	_	Covered
bin auto [28672:29695]	19	1	_	Covered
bin auto $[29696:30719]$	11	1	_	Covered
bin auto $[30720:31743]$	9	1	_	Covered
bin auto [31744:32767]	12	1	_	$\operatorname{Covered}$
bin auto [32768:33791]	11	1	_	Covered
bin auto [33792:34815]	14	1	_	Covered
bin auto $[34816:35839]$	13	1	_	Covered
bin auto $[35840:36863]$	13	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	13	1	_	Covered
bin auto [37888:38911]	12	1	_	Covered
bin auto [38912:39935]	9	1		Covered
			_	
$\operatorname{bin} \ \operatorname{auto} \left[39936 \!:\! 40959 \right]$	9	1	_	Covered
bin auto $[40960:41983]$	19	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	9	1	_	Covered
bin auto [43008:44031]	13	1	_	Covered
· · · · · · · · · · · · · · · · · · ·		1		
bin auto $[44032:45055]$	13	1	_	Covered
bin auto $[45056:46079]$	7	1	_	Covered
bin auto [46080:47103]	13	1	_	$\operatorname{Covered}$
bin auto [47104:48127]	11	1	_	Covered
bin auto [48128:49151]	15	1	_	Covered
bin auto [49152:50175]	10	1	_	Covered
bin auto $[50176:51199]$	11	1	_	Covered
${ m bin \ auto} [51200 {:} 52223]$	14	1	_	$\operatorname{Covered}$
bin auto [52224:53247]	12	1	_	Covered
bin auto [53248:54271]	10	1		Covered
		_	_	
bin auto $[54272:55295]$	20	1	_	Covered
bin auto [55296:56319]	11	1	_	$\operatorname{Covered}$
bin auto $[56320:57343]$	10	1	_	Covered
bin auto [57344:58367]	16	1	_	Covered
bin auto [58368:59391]	15	1		Covered
			_	
$\operatorname{bin} \ \operatorname{auto} \left[59392 \!:\! 60415 \right]$	17	1	_	Covered
bin auto $[60416:61439]$	18	1	_	$\operatorname{Covered}$
bin auto $[61440:62463]$	18	1	_	$\operatorname{Covered}$
bin auto [62464:63487]	13	1	_	Covered
bin auto [63488:64511]	14	1		Covered
			_	
bin auto $[64512:65535]$	201	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	C 1
bin auto [0]	777	1	_	Covered
bin auto [1]	428	1	_	Covered
$\operatorname{Coverpoint} \ \operatorname{w_en_cp}$	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing / total bins:	0	2	_	
% Hit:	100.00%	100		
				Commad
bin auto[0]	396	1	_	Covered
bin auto[1]	809	1	_	Covered
Coverpoint data_out_cp	92.18%	100	_	$\operatorname{Uncovered}$
covered/total bins:	59	64	_	
missing/total bins:	5	64	_	
% Hit:	92.18%	100	-	
			_	~ ,
bin auto [0:1023]	687	1	_	Covered
bin auto [1024:2047]	1	1	_	Covered
bin auto [2048:3071]	5	1	_	Covered
bin auto [3072:4095]	4	1		Covered
			_	
bin auto [4096:5119]	15	1	_	Covered
bin auto $[5120:6143]$	9	1	_	Covered
bin auto [6144:7167]	2	1	_	Covered
bin auto [7168:8191]	4	1	_	Covered
bin auto[7103.3191] bin auto[8192:9215]		1		Covered
	3		_	
bin auto [9216:10239]	3	1	_	Covered
bin auto $[10240:11263]$	30	1	_	Covered
bin auto [11264:12287]	9	1	_	Covered
bin auto [12288:13311]	7	1	_	Covered
· · · · · · · · · · · · · · · · · · ·				
bin auto [13312:14335]	8	1	_	Covered
		4		
bin auto $[14336:15359]$	6	1	_	Covered
bin auto [14336:15359] bin auto [15360:16383]	6 0	1 1	_	Covered ZERO
bin auto [15360:16383]	0	1		ZERO
bin auto [15360:16383] bin auto [16384:17407]	0	1 1	_ _	ZERO ZERO
bin auto [15360:16383]	0	1	_	ZERO

bin auto [18432:19455]	7	1	_	Covered
bin auto [19456:20479]	14	1	_	Covered
bin auto [20480:21503]	3	1	_	Covered
bin auto [21504:22527]	5	1	_	Covered
$\mathrm{bin} \ \mathrm{auto} \left[22528{:}23551 \right]$	1	1	_	Covered
bin auto $[23552:24575]$	0	1	_	ZERO
bin auto $[24576:25599]$	11	1	_	$\operatorname{Covered}$
bin auto [25600:26623]	13	1	_	Covered
bin auto $[26624:27647]$	8	1	_	Covered
bin auto $[27648:28671]$	11	1	_	Covered
bin auto $[28672:29695]$	19	1	_	$\operatorname{Covered}$
bin auto $[29696:30719]$	8	1	_	Covered
bin auto $[30720:31743]$	3	1	_	Covered
bin auto $[31744:32767]$	3	1	_	Covered
bin auto [32768:33791]	4	1	_	Covered
bin auto [33792:34815]	8	1	_	Covered
bin auto [34816:35839]	4	1	_	Covered
bin auto [35840:36863]	6	1	_	Covered
bin auto [36864:37887]	2	1	_	Covered
bin auto [37888:38911]	1	1	_	Covered
bin auto [38912:39935]	4	1	_	Covered
bin auto [39936:40959]	9	1	_	Covered
bin auto [40960:41983]	10	1	_	Covered
bin auto [41984:43007]	$\frac{1}{2}$	1	_	Covered
bin auto [43008:44031]	11	1	_	Covered
bin auto $[44032:45055]$	3	1	_	Covered
bin auto [45056:46079]	$\frac{3}{2}$	1	_	Covered
bin auto [46080:47103]	7	1	_	Covered
bin auto [47104:48127]	0	1	_	ZERO
bin auto [48128:49151]	1	1	_	Covered
bin auto $[49152:50175]$	10	1	_	Covered
bin auto $[49132:30173]$ bin auto $[50176:51199]$	7	1	_	Covered
	13	1	_	Covered
bin auto [51200:52223]			_	Covered
bin auto [52224:53247]	1	1	_	
bin auto [53248:54271]	3	1	_	Covered
bin auto [54272:55295]	12	1	_	Covered
bin auto [55296:56319]	14	1	_	Covered
bin auto [56320:57343]	1	1	_	Covered
bin auto [57344:58367]	3	1	_	Covered
bin auto [58368:59391]	6	1	_	Covered
bin auto [59392:60415]	24	1	_	Covered
bin auto [60416:61439]	8	1	_	Covered
bin auto $[61440:62463]$	16	1	_	Covered
bin auto $[62464:63487]$	5	1	_	Covered
bin auto $[63488:64511]$	0	1	_	ZERO
bin auto $[64512:65535]$	108	1	_	$\operatorname{Covered}$
Coverpoint wr_ack_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	575	1	_	Covered
bin auto[1]	630	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	1109	1	_	Covered
bin auto[1]	96	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	1091	1	_	Covered
bin auto[1]	114	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	919	1	_	Covered
bin auto[1]	286	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1128	1	_	$\operatorname{Covered}$
bin auto[1]	77	1	_	$\operatorname{Covered}$
${\tt Coverpoint\ almost empty_cp}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
${\rm bin \ auto} [0]$	973	1	_	Covered
bin auto[1]	232	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
${\rm bin \ auto} [0]$	1050	1	_	Covered
bin auto[1]	155	1	_	Covered
Cross wr_ack_cross	400 000	100	_	Covered
acreared /total bing.	100.00%	100		
covered/total bins:	100.00%	6	_	
missing/total bins:	6 0	6 6	_	
	6	6	_ _ _	

Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]=""></auto[1],>	191	1	_	Covered
bin < auto[1], $auto[1]$, $auto[0] >$	47	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	439 132	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	190	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	206	1	_	Covered
Illegal and Ignore Bins:	0			ZERO
ignore_bin w_en_nactv_wr_ack Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6 \\ 100$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	104	1	_	Covered
$egin{aligned} ext{bin } < & ext{auto} \left[0 ight], & ext{auto} \left[1 ight] > \ ext{bin } < & ext{auto} \left[1 ight], & ext{auto} \left[0 ight] > \end{aligned}$	$10 \\ 238$	1 1	_ _	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	190	1	_	Covered
$\operatorname{bin} < \operatorname{auto}\left[0\right], \operatorname{auto}\left[1\right], \operatorname{auto}\left[0\right] >$	467	1	_	Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	196	1	_	Covered
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: $bin < auto[1], auto[1], auto[1] >$	32	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	141	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	206	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$509 \\ 49$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	155	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty Cross almostfull_cross	$\frac{113}{100.00\%}$	100	_	Occurred Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
$\mathrm{bin} \ <\! \mathrm{auto} [1] \ , \\ \mathrm{auto} [1] \ , \\ \mathrm{auto} [1] >$	32	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\begin{array}{c} 4 \\ 206 \end{array}$	1 1	_	Covered Covered
bin $<$ auto [1], auto [1], auto [0] $>$	542	1	_	Covered
bin < auto[1], auto[0], auto[0] >	186	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [0], \operatorname{auto} [0] > \\ \operatorname{Illegal} \ \operatorname{and} \ \operatorname{Ignore} \ \operatorname{Bins}:$	194	1	_	Covered
ignore_bin w_en_nactv_almostfull	41		_	Occurred
Cross almostempty_cross covered/total bins:	100.00%	$\frac{100}{6}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: $bin < auto[1], auto[1], auto[1] >$	86	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	152	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	$\begin{array}{c} 88 \\ 483 \end{array}$	1 1	_	Covered Covered
$egin{aligned} ext{bin } < & ext{auto} \left[0 ight], & ext{auto} \left[0 ight] > \ ext{bin } < & ext{auto} \left[1 ight], & ext{auto} \left[0 ight], & ext{auto} \left[0 ight] > \end{aligned}$	171	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	167	1	_	Covered
Illegal and Ignore Bins:	E0			Occurred
ignore_bin w_en_nactv_almostempty Cross overflow_cross	$58 \\ 100.00\%$	100	_	Occurred Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6\\100$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	20	1	_	Covered
bin $<$ auto [1], auto [1], auto [0] $>$ bin $<$ auto [0], auto [1], auto [1]	$\begin{array}{c} 218 \\ 76 \end{array}$	1 1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\frac{76}{495}$	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	190	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	206	1	_	Covered
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0\\100.00\%$	$6 \\ 100$	_	
Auto, Default and User Defined Bins:		4		С :
$egin{aligned} & ext{bin } < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] > \ & ext{bin } < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] > \end{aligned}$	$\frac{49}{106}$	1 1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto}\left[1\right], \operatorname{auto}\left[1\right], \operatorname{auto}\left[0\right] >$	189	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	571	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$84 \\ 206$	1 1	_	Covered Covered
Illegal and Ignore Bins:		-		
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
COVERGROUP COVERAGE:				

Covergroup

 ${\rm Metric}$

 Goal

 ${\bf Status}$

 Bins

TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100	_	Uncovered
covered/total bins:	185	190	_	
missing/total bins:	5	190	_	
% Hit:	97.36%	100	_	C 1
Coverpoint rst_n_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	137	1	_	Covered
bin auto [1]	1068	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	190	1	_	Covered
bin auto [1024:2047]	9	1	_	Covered
bin auto [2048:3071]	$9\\12$	1 1	_	Covered Covered
bin auto [3072:4095] bin auto [4096:5119]	13	1	_	Covered
bin auto [5120:6143]	12	1		Covered
bin auto [6144:7167]	10	1	_	Covered
bin auto [7168:8191]	11	1	_	Covered
bin auto [8192:9215]	12	1	_	Covered
bin auto [9216:10239]	12	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
bin auto $[11264:12287]$	11	1	_	Covered
bin auto [12288:13311]	15	1	_	Covered
bin auto [13312:14335]	12	1	_	Covered
bin auto [14336:15359]	17	1	_	Covered
bin auto [15360:16383]	9	1	_	Covered
bin auto [16384:17407]	13	1	_	Covered
bin auto [17408:18431]	$14\\20$	1 1	_	Covered Covered
$egin{array}{ll} ext{bin auto} & [18432:19455] \ ext{bin auto} & [19456:20479] \end{array}$	$\frac{20}{21}$	1	_	Covered
bin auto [19430:20479] bin auto [20480:21503]	7	1		Covered
bin auto $[21504:22527]$	18	1		Covered
bin auto [22528:23551]	18	1	_	Covered
bin auto [23552:24575]	13	1	_	Covered
bin auto [24576:25599]	10	1	_	Covered
bin auto [25600:26623]	17	1	_	Covered
bin auto [26624:27647]	17	1	_	Covered
bin auto [27648:28671]	12	1	_	Covered
bin auto [28672:29695]	19	1	_	Covered
bin auto $[29696:30719]$	11	1	_	Covered
bin auto [30720:31743]	9	1	_	Covered
$bin \ \ auto \left[31744{:}32767\right]$	12	1	_	Covered
bin auto [32768:33791]	11	1	_	Covered
bin auto [33792:34815]	14	1	_	Covered
bin auto [34816:35839] bin auto [35840:36863]	$\begin{array}{c} 13 \\ 13 \end{array}$	1 1	_	Covered Covered
bin auto [36864:37887]	13	1	_	Covered
bin auto [37888:38911]	$\frac{13}{12}$	1	_	Covered
bin auto [38912:39935]	9	1	_	Covered
bin auto [39936:40959]	9	1	_	Covered
bin auto [40960:41983]	19	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	9	1	_	Covered
bin auto [43008:44031]	13	1	_	Covered
bin auto $[44032:45055]$	13	1	_	Covered
bin auto $[45056:46079]$	7	1	_	Covered
bin auto [46080:47103]	13	1	_	Covered
bin auto [47104:48127]	11	1	_	Covered
bin auto [48128:49151]	15	1	_	Covered
bin auto [49152:50175]	$\begin{array}{c} 10 \\ 11 \end{array}$	1	_	Covered Covered
bin auto [50176:51199] bin auto [51200:52223]	$\frac{11}{14}$	1 1	_	Covered Covered
bin auto $[51200:52223]$	$\frac{14}{12}$	1	_	Covered
bin auto [52224:55247]	10	1	_	Covered
bin auto [5248.54271] bin auto [54272:55295]	$\frac{10}{20}$	1	_	Covered
bin auto [55296:56319]	11	1	_	Covered
bin auto [56320:57343]	10	1	_	Covered
bin auto [57344:58367]	16	1	_	Covered
bin auto [58368:59391]	15	1	_	Covered
bin auto [59392:60415]	17	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[60416 \!:\! 61439 \right]$	18	1	_	Covered
bin auto [61440:62463]	18	1	_	Covered
bin auto [62464:63487]	13	1	_	Covered
bin auto [63488:64511]	14	1	_	Covered
bin auto [64512:65535]	201	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$\begin{matrix}2\\100\end{matrix}$	_	
% Hit: bin auto $[0]$	100.00% 777	100	_	Covered
bin auto[0]	$\frac{777}{428}$	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	55,5164
missing/total bins:	0	$\overset{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	396	1	_	Covered
bin auto [1]	809	1	_	Covered

Coverpoint data_out_cp	92.18%	100		Uncovered
covered/total bins:	59.1870 59	64	_	Uncovered
missing/total bins: % Hit:	$5\\92.18\%$	$64 \\ 100$	_	
bin auto [0:1023]	$\frac{92.18\%}{687}$	100	_	Covered
bin auto [1024:2047]	1	1	_	Covered
bin auto [2048:3071] bin auto [3072:4095]	$rac{5}{4}$	1 1	_	Covered Covered
bin auto [4096:5119]	15	1	_	Covered
bin auto [5120:6143] bin auto [6144:7167]	$\frac{9}{2}$	1 1	_	Covered Covered
bin auto [7168:8191]	$\frac{2}{4}$	1	_	Covered
bin auto [8192:9215]	3	1	_	Covered
bin auto [9216:10239] bin auto [10240:11263]	$\frac{3}{30}$	1 1	_	Covered Covered
bin auto [11264:12287]	9	1	_	Covered
bin auto [12288:13311]	7	1	_	Covered
bin auto [13312:14335] bin auto [14336:15359]	8	1 1	_	Covered Covered
bin auto [15360:16383]	0	1	_	ZERO
bin auto [16384:17407] bin auto [17408:18431]	$0 \\ 1$	1 1	_	ZERO Covered
bin auto [17403.13431]	7	1	_	Covered
bin auto [19456:20479]	14	1	_	Covered
$egin{array}{ll} ext{bin auto} \left[20480; 21503 ight] \ ext{bin auto} \left[21504; 22527 ight] \end{array}$	3 5	1 1	_	Covered Covered
bin auto [21504.22521]	1	1	_	Covered
bin auto [23552:24575]	0	1	_	ZERO
$egin{array}{ll} ext{bin auto} \left[24576 \hbox{:} 25599 ight] \ ext{bin auto} \left[25600 \hbox{:} 26623 ight] \end{array}$	$\begin{array}{c} 11 \\ 13 \end{array}$	1 1	_	Covered Covered
bin auto $[26624:27647]$	8	1	_	Covered
bin auto [27648:28671]	11	1	_	Covered
bin auto [28672:29695]	19	1	_	Covered Covered
bin auto [29696:30719] bin auto [30720:31743]	8 3	1 1	_	Covered
bin auto [31744:32767]	3	1	_	Covered
bin auto [32768:33791]	4	1	_	Covered
bin auto [33792:34815] bin auto [34816:35839]	$\frac{8}{4}$	1 1	_	Covered Covered
bin auto [35840:36863]	6	1	_	Covered
bin auto [36864:37887]	2	1	_	Covered
bin auto [37888:38911] bin auto [38912:39935]	$1 \\ 4$	1 1	_	Covered Covered
bin auto [39936:40959]	9	1	_	Covered
bin auto [40960:41983]	10	1	_	Covered
bin auto [41984:43007]	$\begin{array}{c} 2 \\ 11 \end{array}$	1	_	Covered Covered
bin auto $[43008:44031]$ bin auto $[44032:45055]$	$\frac{11}{3}$	1 1	_	Covered
bin auto [45056:46079]	2	1	_	Covered
bin auto [46080:47103]	7	1	_	Covered
bin auto [47104:48127] bin auto [48128:49151]	$0 \\ 1$	1 1	_	ZERO Covered
bin auto [49152:50175]	10	1	_	Covered
bin auto [50176:51199]	7	1	_	Covered
bin auto [51200:52223] bin auto [52224:53247]	$\frac{13}{1}$	1 1	_	Covered Covered
bin auto [53248:54271]	3	1	_	Covered
bin auto [54272:55295]	12	1	_	Covered
bin auto [55296:56319] bin auto [56320:57343]	14 1	1 1	_	Covered Covered
bin auto [57344:58367]	3	1	_	Covered
bin auto [58368:59391]	6	1	_	Covered
bin auto [59392:60415] bin auto [60416:61439]	$\frac{24}{8}$	1 1	_	Covered Covered
bin auto $[61440:62463]$	16	1	_	Covered
bin auto [62464:63487]	5	1	_	Covered
bin auto $[63488:64511]$ bin auto $[64512:65535]$	$0 \\ 108$	1 1	_	ZERO Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$\begin{matrix}2\\100\end{matrix}$	_	
bin auto [0]	575	1	_	Covered
bin auto[1]	630	1	_	Covered
Coverpoint overflow_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	1109	1	_	Covered
bin auto [1] Coverpoint full_cp	$96 \\ 100.00\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
covered/total bins:	2	2	_	
missing/total bins:	100.00%	2	_	
% Hit: bin auto [0]	$100.00\% \ 1091$	$100\\1$	_	Covered
bin auto[1]	114	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	$\frac{2}{0}$	$\frac{2}{2}$	_ _	
% Hit:	100.00%	100	_	
bin auto [0]	919	1	_	Covered
bin auto[1]	286	1	_	Covered

Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins: missing/total bins:	$\frac{2}{0}$	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	1128	1	_	Covered
bin auto[1] Coverpoint almostempty_cp	$77\\100.00\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0\\100.00\%$	$\begin{array}{c} 2 \\ 100 \end{array}$	_	
bin auto $[0]$	973	1	_	Covered
bin auto [1]	232	1	_	Covered
Coverpoint underflow_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0	2	_	
% Hit:	$100.00\% \ 1050$	100	_	Covered
$egin{array}{ll} ext{bin auto} \left[0 ight] \ ext{bin auto} \left[1 ight] \end{array}$	1050 155	1 1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	6 0	$\frac{6}{6}$	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	101	1		C 1
$egin{aligned} ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$191 \\ 47$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	439	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	132	1	_	Covered
$egin{aligned} ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight]> \ \end{aligned} \\ ext{bin } &< ext{auto} \left[0 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight]> \end{aligned}$	$190 \\ 206$	1 1	_	Covered Covered
Illegal and Ignore Bins:	200	1		Covered
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO
Cross full_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: bin $<$ auto $[0]$, auto $[1]$, auto $[1]$	104	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	10	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	238	1	_	Covered
$egin{aligned} ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ ext{bin } & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$190\\467$	1 1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	196	1	_	Covered
Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full	0			ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6 0	6 6	_	
missing/total bins: % Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	$\frac{32}{141}$	1 1	_	Covered Covered
$egin{aligned} ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight]> \ \end{aligned} \\ ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight]> \end{aligned}$	$\frac{141}{206}$	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	509	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	49	1		Covered
			_	
$\mathrm{bin} \ < \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	155	1	_	Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty</auto[0],>	155 113	_		Occurred
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	$155\\113\\100.00\%$	100		
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty</auto[0],>	155 113	_	_ _ _ _ _	Occurred
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	$155 \\ 113 \\ 100.00\% \\ 6$	100		Occurred
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$	100 6 6 100	- - - - -	Occurred Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0	100 6 6	- - - - - -	Occurred
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""> bin <auto[1], auto[0]=""> bin <auto[1], auto[0]=""></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206	100 6 6 100 1 1 1	- - - - - -	Occurred Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542	100 6 6 100 1 1 1 1	- - - - - - -	Occurred Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""> bin <auto[1], auto[0]=""> bin <auto[1], auto[0]=""></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206	100 6 6 100 1 1 1		Occurred Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins:</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194	100 6 6 100 1 1 1 1	_	Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41	100 6 6 100 1 1 1 1 1	_	Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins:</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194	100 6 6 100 1 1 1 1	_	Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 6 6	_	Covered Covered Covered Covered Covered Covered Covered Covered
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bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_	Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152 88	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_	Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> covered/total bins: covered/total</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	113 100.00% 6 0 100.00% 32 4 206 542 186 194 41 100.00% 6 0 100.00% 86 152 88 483 171	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_	Covered
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bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152 88 483 171 167	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 100.00% 6 0 100.00% 32 4 206 542 186 194 41 100.00% 6 0 100.00% 86 152 88 483 171 167 58 100.00% 6	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
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bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152 88 483 171 167 58 $100.00%$ 6 0 $100.00%$	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152 88 483 171 167 58 $100.00%$ 6 0 $100.00%$	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],>	155 113 $100.00%$ 6 0 $100.00%$ 32 4 206 542 186 194 41 $100.00%$ 6 0 $100.00%$ 86 152 88 483 171 167 58 $100.00%$ 6 0 $100.00%$	100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

bin <auto [0]="" [0],="" [1],="" auto=""></auto>	495	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	190	1	_	Covered
bin < auto[0], auto[0], auto[0] >	206	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	49	1	_	Covered
bin < auto[1], auto[0], auto[1] >	106	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	189	1	_	Covered
bin < auto[0], auto[1], auto[0] >	571	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	84	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [0], \operatorname{auto} [0] >$	206	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 99.58% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.58%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover_n_wr_a	SVA	1	Off	86	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_counte	SVA	1	Off	1068	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	1	Off	1068	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	1	Off	1068	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	1	Off	6	1	Unli	1	100%		V	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	√	Off	34	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	1	Off	203	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	1	Off	69	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_full_fla	SVA	√	Off	99	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_empty	SVA	√	Off	255	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_underfl	SVA	1	Off	122	1	Unli	1	100%		1	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_overflo	SVA	1	Off	62	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_a	SVA	1	Off	553	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_reset	SVA	1	Off	137	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 1: SVA "Seed1"

3.2 Functional Coverage "seed2" Report

Coverage Report by instance with details

== Instance: /FIFO_coverage_pkg == Design Unit: work.FIFO_coverage_pkg

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.50%	100		Uncovered
covered/total bins:	184	190	_	
missing/total bins:	6	190	_	
% Hit:	96.84%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	130	1	_	Covered
bin auto [1]	1075	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0:1023\right]$	195	1	_	Covered
bin auto $[1024:2047]$	15	1	_	Covered
bin auto [2048:3071]	17	1	_	Covered
bin auto [3072:4095]	15	1	_	Covered
bin auto [4096:5119]	12	1	_	Covered
bin auto [5120:6143]	13	1	_	Covered
bin auto [6144:7167]	8	1	_	Covered
bin auto [7168:8191]	18	1	_	Covered
bin auto [8192:9215]	15	1	_	Covered
bin auto [9216:10239]	13	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
bin auto [11264:12287]	16	1	_	Covered
bin auto [12288:13311]	13	1	_	Covered
bin auto [13312:14335]	17	1	_	Covered
bin auto [14336:15359]	11	1	_	Covered
bin auto [15360:16383]	11	1	_	Covered
bin auto [16384:17407]	14	1	_	Covered
bin auto [17408:18431]	15	1	_	Covered

1.1	4.0			G 1
bin auto [18432:19455]	12	1	_	Covered
bin auto [19456:20479]	12	1	_	Covered
bin auto [20480:21503]	11	1	_	Covered
bin auto [21504:22527]	13	1	_	Covered
bin auto [22528:23551]	16	1	_	Covered
bin auto [23552:24575]	17	1	_	Covered
bin auto [24576:25599]	15	1	_	Covered
bin auto [25600:26623]	11	1	_	Covered
	7			Covered
bin auto [26624:27647]		1	_	
bin auto [27648:28671]	11	1	_	Covered
bin auto [28672:29695]	16	1	_	Covered
bin auto $[29696:30719]$	12	1	_	Covered
bin auto [30720:31743]	15	1	_	Covered
bin auto [31744:32767]	14	1	_	Covered
bin auto [32768:33791]	19	1	_	Covered
bin auto [33792:34815]	11	1	_	Covered
bin auto [34816:35839]	15	1	_	Covered
bin auto [35840:36863]	12	1		Covered
			_	
bin auto [36864:37887]	14	1	_	Covered
bin auto [37888:38911]	13	1	_	Covered
bin auto [38912:39935]	16	1	_	Covered
bin auto $[39936:40959]$	10	1	_	Covered
bin auto [40960:41983]	17	1	_	Covered
bin auto $[41984:43007]$	15	1	_	Covered
bin auto [43008:44031]	18	1	_	Covered
bin auto $[44032:45055]$	10	1	_	Covered
bin auto [45056:46079]	8	1	_	Covered
	8			
bin auto [46080:47103]		1	_	Covered
bin auto [47104:48127]	10	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto $[49152:50175]$	12	1	_	Covered
bin auto [50176:51199]	17	1	_	Covered
bin auto [51200:52223]	20	1	_	Covered
bin auto [52224:53247]	13	1	_	Covered
bin auto [53248:54271]	$\frac{12}{12}$	1	_	Covered
bin auto [54272:55295]	15	1		Covered
			_	
bin auto [55296:56319]	15	1	_	Covered
bin auto [56320:57343]	13	1	_	Covered
bin auto $[57344:58367]$	9	1	_	$\operatorname{Covered}$
bin auto [58368:59391]	8	1	_	$\operatorname{Covered}$
bin auto $[59392:60415]$	10	1	_	Covered
bin auto $[60416:61439]$	11	1	_	Covered
bin auto [61440:62463]	14	1	_	Covered
bin auto [62464:63487]	17	1	_	Covered
bin auto [63488:64511]	16	1	_	Covered
bin auto[00400.04011]				
bin auto [64512:65535]	174	1		Cowarad
bin auto [64512:65535]	174	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered Covered
Coverpoint r_en_cp covered/total bins:	100.00%	$100 \\ 2$		
Coverpoint r_en_cp covered/total bins: missing/total bins:	$100.00\% \ 2 \ 0$	$100 \\ 2 \\ 2$	_	
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit:	$100.00\% \ 2 \ 0 \ 100.00\%$	$100 \\ 2$	_	Covered
Coverpoint r_en_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 816	$100 \\ 2 \\ 2$	_	
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit:	$100.00\% \ 2 \ 0 \ 100.00\%$	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \end{array} $	_	Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0]	100.00% 2 0 $100.00%$ 816	$ \begin{array}{r} 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $	_ _ _ _	Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp	100.00% 2 0 $100.00%$ 816 389	100 2 2 100 1 1 100	_ _ _ _	Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins:	100.00% 2 0 $100.00%$ 816 389 $100.00%$	100 2 2 100 1 1 100 2	_ _ _ _	Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0	100 2 2 100 1 1 100 2	_ _ _ _	Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit:	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100	_ _ _ _	Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401	100 2 2 100 1 1 100 2 2 100		Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804	100 2 2 100 1 1 100 2 2 100 1	- - - - - - - - -	Covered Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$	100 2 2 100 1 1 100 2 2 100 1 1 100		Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] coverpoint data_out_cp covered/total bins:	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58	100 2 2 100 1 1 100 2 2 100 1 1 100 64	- - - - - - - - -	Covered Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64	- - - - - - - - -	Covered Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit:	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100	 	Covered Covered Covered Covered Uncovered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1	- - - - - - - - -	Covered Covered Covered Covered Uncovered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1	 	Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1		Covered Covered Covered Covered Uncovered Covered Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1		Covered Covered Covered Covered Uncovered Covered Covered Covered Covered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1		Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1		Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[0:24:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint ren_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[3072:4095] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[0240:11263]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint w_en_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[10240:11263] bin auto[11264:12287] bin auto[11268:13311]	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Uncovered Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 100.00% 816 389 100.00% 2 0 100.00% 401 804 90.62% 58 6 90.62% 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 2 7 10	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7 5	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7 5 2	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 $100.00%$ 816 389 $100.00%$ 2 0 $100.00%$ 401 804 $90.62%$ 58 6 $90.62%$ 666 3 6 12 6 11 0 6 10 6 3 12 7 5 3 5 1 4 13 2 27 10 1 7 5 2 0	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 100.00% 816 389 100.00% 2 0 100.00% 401 804 90.62% 58 6 90.62% 666 3 6 12 6 11 0 6 3 12 7 5 3 5 1 4 13 2 2 7 10 1 7 5 2 0 9 3	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Coverpoint r_en_cp	100.00% 2 0 100.00% 816 389 100.00% 2 0 100.00% 401 804 90.62% 58 6 90.62% 666 11 0 6 10 6 10 6 3 12 7 5 3 5 1 4 13 2 2 7 10 1 7 5 2 0 9	100 2 2 100 1 1 100 2 2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

bin auto [30720:31743]	1	1	_	Covered
bin auto [31744:32767]	14	1	_	Covered
bin auto $[32768:33791]$	8	1	_	Covered
bin auto [33792:34815]	6	1	_	Covered
bin auto [34816:35839]	11	1	_	Covered
bin auto [35840:36863]	11	1	_	Covered
bin auto [36864:37887]	15	1	_	Covered
bin auto [37888:38911]	11	1	_	Covered
bin auto [38912:39935]	14	1	_	Covered
bin auto 39936:40959	0	1	_	ZERO
bin auto [40960:41983]	5	1	_	Covered
bin auto [41984:43007]	7	1	_	Covered
bin auto [43008:44031]	1	1	_	Covered
bin auto $[44032:45055]$	3	1	_	Covered
bin auto [45056:46079]	9	1	_	Covered
bin auto [46080:47103]	11	1	_	Covered
bin auto [47104:48127]	2	1	_	Covered
bin auto [48128:49151]	$\frac{2}{7}$	1		Covered
bin auto [49152:50175]	0	1		ZERO
bin auto [49132.30173] bin auto [50176:51199]	10	1		Covered
bin auto $[51200:52223]$	20	1	_	Covered
			_	
bin auto [52224:53247]	8	1	_	Covered
bin auto [53248:54271]	4	1	_	Covered
bin auto [54272:55295]	8	1	_	Covered
bin auto [55296:56319]	16	1	_	Covered
bin auto [56320:57343]	14	1	_	Covered
bin auto [57344:58367]	4	1	_	Covered
bin auto [58368:59391]	6	1	_	Covered
bin auto [59392:60415]	25	1	_	Covered
bin auto $[60416:61439]$	0	1	_	ZERO
bin auto $[61440:62463]$	0	1	_	ZERO
bin auto $[62464:63487]$	12	1	_	$\operatorname{Covered}$
bin auto $[63488:64511]$	5	1	_	$\operatorname{Covered}$
bin auto $[64512 : 65535]$	78	1	_	$\operatorname{Covered}$
Coverpoint wr_ack_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	593	1	_	Covered
bin auto[1]	612	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1067	1	_	Covered
bin auto[1]	138	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100		
bin auto $[0]$	100.00% 1045	1		Covered
	160		_	Covered
bin auto[1]	100.00%	1	_	Covered
Coverpoint empty_cp		100	_	Covered
covered/total bins:	2	$rac{2}{2}$	_	
missing/total bins:	100.0007	_	_	
% Hit:	100.00%	100	_	C 1
bin auto [0]	932	1	_	Covered
bin auto[1]	273	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	G 1
bin auto [0]	1105	1	_	Covered
bin auto[1]	100	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1023	1	_	Covered
bin auto[1]	182	1	_	Covered
$\operatorname{Coverpoint}$ $\operatorname{underflow_cp}$	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
${\rm bin \ \ auto} [0]$	1068	1	_	$\operatorname{Covered}$
bin auto[1]	137	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	161	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	45	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	451	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	147	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	183	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	218	1	_	Covered
Illegal and Ignore Bins:		•		
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	51001
missing/total bins:	0	6	_	
∪ 1	, and the second	=		

YPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg covered/total bins:	99.50% 184	100 190		Uncovered
overgroup	Metric	Goal	Bins	Status
VERGROUP COVERAGE:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	218	1	_	Covered
bin $<$ auto [1], auto [0], auto [0] $>$	85 218	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	598	1	_	Covered
$egin{aligned} ext{bin } < & ext{auto} [1] \ , & ext{auto} [0] \ , & ext{auto} [1] \ , & ext{auto} [0] \ > \end{aligned}$	$\frac{98}{167}$	1 1	_	Covered Covered
bin $<$ auto[1], auto[1], auto[1]>	$\frac{39}{98}$	1 1	_	Covered Covered
Auto, Default and User Defined Bins:				<i>-</i>
missing/total bins: % Hit:	100.00%	100	_	
covered/total bins:	6 0	6 6	_	
Cross underflow_cross	100.00%	100	_	Covered
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Illegal and Ignore Bins:	210	1	_	Oovered
$egin{aligned} ext{bin } < & ext{auto} \left[1 ight], & ext{auto} \left[0 ight] > \ ext{bin } < & ext{auto} \left[0 ight], & ext{auto} \left[0 ight] > \end{aligned}$	$183 \\ 218$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	490	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right] >$	108	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	176	1	_	Covered
bin $<$ auto [1], auto [1], auto [1]>	30	1	_	Covered
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
missing/total bins:	0	6	_	
covered/total bins:	6	6	_	
Cross overflow_cross	100.00%	100	_	Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty	47		_	Occurred
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	184	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	170	1	_	Covered
bin $<$ auto[0], auto[1], auto[0]>	523	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	75	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] \ > \end{aligned}$	$60\\146$	1 1	_	Covered Covered
Auto, Default and User Defined Bins:	2-			
% Hit:	100.00%	100	_	
missing/total bins:	0	6	_	
Cross almostempty_cross covered/total bins:	100.00%	$100 \\ 6$	_	Covered
ignore_bin w_en_nactv_almostfull	52	100	_	Occurred
Illegal and Ignore Bins:				
bin $<$ auto[0], auto[0], auto[0]>	201	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	565 175	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\frac{166}{563}$	1 1	_	$egin{array}{c} ext{Covered} \end{array}$
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	8	1	_	Covered
bin < auto[1], auto[1], auto[1] >	40	1	_	Covered
Auto, Default and User Defined Bins:	100.0070	100		
missing/total bins: % Hit:	100.00%	$6 \\ 100$	_	
covered/total bins:	6 0	6	_	
Cross almostfull_cross	100.00%	100	_	Covered
ignore_bin read_nactv_empty	119		_	Occurred
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > \\ \operatorname{Illegal} \ \operatorname{and} \ \operatorname{Ignore} \ \operatorname{Bins}:$	156	1	_	Covered
bin $<$ auto [1], auto [0], auto [0] $>$	49	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	541	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[0] >$	186	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	134	1	_	Covered Covered
Auto, Default and User Defined Bins: bin $<$ auto[1], auto[1], auto[1]>	20	1	_	Covered
% Hit:	100.00%	100	_	
missing/total bins:	0	6	_	
covered/total bins:	6	6	_	50,010u
rgnore_bin w_en_r_en_allactv_full Cross empty_cross	100.00%	100	_	ZERO Covered
ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full	0		_	ZERO ZERO
Illegal and Ignore Bins:	_			TTED C
$\operatorname{bin} \ \operatorname{$	198	1	_	Covered
bin $<$ auto [1], auto [0], auto [0] $>$ bin $<$ auto [0], auto [1], auto [0] $>$	458	1	_	Covered Covered
$egin{aligned} & ext{bin } < ext{auto} [1] \ , ext{auto} [0] > \ & ext{bin } < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [0] > \end{aligned}$	$\frac{206}{183}$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	20	1	_	Covered
$\begin{array}{ll} \text{bin } < \text{auto} \begin{bmatrix} 0 \end{bmatrix}, \text{auto} \begin{bmatrix} 1 \end{bmatrix}, \text{auto} \begin{bmatrix} 1 \end{bmatrix} > \\ \\ \end{array}$	140	1	_	Covered
Auto, Default and User Defined Bins:		-00		
% Hit:	100.00%	100	_	

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Covergroup	Metric	Goal	$_{ m Bins}$	Status
${\rm TYPE\ /FIFO_coverage_pkg/FIFO_coverage/fifo_cg}$	99.50%	100	_	$\operatorname{Uncovered}$
covered/total bins:	184	190	_	
missing/total bins:	6	190	_	
% Hit:	96.84%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	130	1	_	$\operatorname{Covered}$
bin auto[1]	1075	1	_	Covered

Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	$0 \\ 100.00\%$	$64 \\ 100$	_	
% Hit: bin auto[0:1023]	100.00% 195	100	_	Covered
bin auto $[0.1023]$ bin auto $[1024:2047]$	15	1	_	Covered
bin auto [2048:3071]	17	1	_	Covered
bin auto [3072:4095]	15	1	_	Covered
bin auto [4096:5119]	12	1	_	Covered
bin auto [5120:6143]	13	1	_	Covered
bin auto [6144:7167]	8	1	_	Covered
bin auto [7168:8191]	18	1	_	Covered
bin auto [8192:9215]	15	1	_	Covered
bin auto [9216:10239]	13	1	_	Covered
bin auto [10240:11263]	16	1	_	Covered
bin auto [11264:12287]	$\frac{16}{13}$	1 1	_	Covered Covered
bin auto [12288:13311] bin auto [13312:14335]	13 17	1	_	Covered
bin auto $[14336:15359]$	11	1	_	Covered
bin auto [15360:16383]	11	1	_	Covered
bin auto [16384:17407]	14	1	_	Covered
bin auto [17408:18431]	15	1	_	Covered
bin auto [18432:19455]	12	1	_	Covered
bin auto $[19456:20479]$	12	1	_	Covered
bin auto $[20480:21503]$	11	1	_	Covered
bin auto $[21504:22527]$	13	1	_	Covered
bin auto [22528:23551]	16	1	_	Covered
bin auto [23552:24575]	17	1	_	Covered
bin auto $[24576:25599]$	15	1	_	Covered
bin auto [25600:26623]	$\frac{11}{7}$	1 1	_	Covered
$\begin{array}{ll} \text{bin } \text{ auto} \left[26624 \hbox{:} 27647 \right] \\ \text{bin } \text{ auto} \left[27648 \hbox{:} 28671 \right] \end{array}$	7 11	1	_	Covered Covered
bin auto $[28672:29695]$	16	1	_	Covered
bin auto [29696:30719]	12	1	_	Covered
bin auto [30720:31743]	15	1	_	Covered
bin auto [31744:32767]	14	1	_	Covered
bin auto [32768:33791]	19	1	_	Covered
bin auto [33792:34815]	11	1	_	Covered
bin auto $[34816:35839]$	15	1	_	Covered
bin auto [35840:36863]	12	1	_	Covered
bin auto [36864:37887]	14	1	_	Covered
bin auto [37888:38911]	13	1	_	Covered
bin auto [38912:39935] bin auto [39936:40959]	$\frac{16}{10}$	1 1	_	Covered Covered
bin auto [40960:41983]	17	1		Covered
bin auto [41984:43007]	15	1	_	Covered
bin auto [43008:44031]	18	1	_	Covered
bin auto [44032:45055]	10	1	_	Covered
bin auto $[45056:46079]$	8	1	_	Covered
bin auto $[46080:47103]$	8	1	_	Covered
bin auto [47104:48127]	10	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto [49152:50175]	12	1	_	Covered
bin auto [50176:51199] bin auto [51200:52223]	$\begin{array}{c} 17 \\ 20 \end{array}$	1 1	_	Covered Covered
bin auto $[51200.32223]$	13	1	_	Covered
bin auto [53248:54271]	12	1	_	Covered
bin auto [54272:55295]	15	1	_	Covered
bin auto [55296:56319]	15	1	_	Covered
bin auto [56320:57343]	13	1	_	Covered
bin auto $[57344:58367]$	9	1	_	Covered
$bin auto \left[58368;59391\right]$	8	1	_	Covered
bin auto [59392:60415]	10	1	_	Covered
bin auto [60416:61439]	11	1	_	Covered
bin auto $[61440:62463]$ bin auto $[62464:63487]$	$\frac{14}{17}$	1 1	_	Covered Covered
bin auto [63488:64511]	16	1	_	Covered
bin auto [64512:65535]	174	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	816	1	_	Covered
bin auto[1]	389	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$\frac{2}{100}$	_	
bin auto $[0]$	401	100	_	Covered
bin auto $[1]$	804	1	_	Covered
Coverpoint data_out_cp	90.62%	100	_	Uncovered
covered/total bins:	58	64	_	-
missing/total bins:	6	64	_	
% Hit:	90.62%	100	_	
bin auto [0:1023]	666	1	_	Covered
bin auto [1024:2047]	3	1	_	Covered
bin auto [2048:3071]	6	1	_	Covered
bin auto [3072:4095]	12	1	_	Covered Covered
bin auto [4096:5119] bin auto [5120:6143]	6 11	1 1	_	Covered Covered
bin auto $[6144:7167]$	0	1	_	ZERO
bin auto [7168:8191]	6	1	_	Covered
	-			-

bin auto [8192:9215]	10	1	_	Covered
bin auto $[9216:10239]$	6	1	_	Covered
bin auto [10240:11263]	3	1	_	Covered
bin auto [11264:12287]	12	1	_	Covered
bin auto [12288:13311]	7	1	_	Covered
bin auto [13312:14335]	5	1	_	Covered
bin auto [14336:15359]	3	1	_	Covered
bin auto [15360:16383]	5	1	_	Covered
bin auto [16384:17407]	1	1		Covered
			_	
bin auto [17408:18431]	4	1	_	Covered
bin auto $[18432:19455]$	13	1	_	Covered
bin auto $[19456:20479]$	2	1	_	Covered
bin auto [20480:21503]	27	1	_	Covered
bin auto [21504:22527]	10	1	_	Covered
bin auto [22528:23551]	1	1	_	Covered
bin auto [23552:24575]	7	1	_	Covered
bin auto [24576:25599]	5	1	_	Covered
bin auto $[25600:26623]$	2	1	_	Covered
bin auto [26624:27647]	0	1	_	ZERO
bin auto $[27648:28671]$	9	1	_	Covered
bin auto [28672:29695]	3	1	_	Covered
bin auto [29696:30719]	14	1	_	Covered
bin auto [30720:31743]	1	1	_	Covered
bin auto [31744:32767]	14	1	_	Covered
bin auto [32768:33791]	8	1	_	Covered
bin auto [33792:34815]	6	1	_	Covered
bin auto $[34816:35839]$	11	1	_	$\operatorname{Covered}$
bin auto $[35840:36863]$	11	1	_	Covered
bin auto [36864:37887]	15	1	_	Covered
bin auto [37888:38911]	11	1	_	Covered
bin auto [38912:39935]	14	1	_	Covered
bin auto [39936:40959]	0	1	_	ZERO
bin auto [40960:41983]	5	1	_	Covered
bin auto [41984:43007]	7	1	_	Covered
bin auto $[43008:44031]$	1	1	_	$\operatorname{Covered}$
bin auto[44032:45055]	3	1	_	Covered
bin auto $[45056:46079]$	9	1	_	Covered
bin auto [46080:47103]	11	1	_	Covered
bin auto [47104:48127]	$\frac{1}{2}$	1	_	Covered
bin auto [48128:49151]	7	1		Covered
	0	1		ZERO
bin auto [49152:50175]			_	
bin auto [50176:51199]	10	1	_	Covered
bin auto $[51200:52223]$	20	1	_	$\operatorname{Covered}$
bin auto[52224:53247]	8	1	_	Covered
bin auto [53248:54271]	4	1	_	Covered
bin auto [54272:55295]	8	1	_	Covered
bin auto [55296:56319]	16	1	_	Covered
bin auto [56320:57343]	14	1		Covered
			_	
bin auto [57344:58367]	4	1	_	Covered
$\mathrm{bin} \ \mathrm{auto} \left[58368{:}59391\right]$	6	1	_	Covered
bin auto $[59392:60415]$	25	1	_	Covered
bin auto $[60416:61439]$	0	1	_	ZERO
bin auto [61440:62463]	0	1	_	ZERO
bin auto [62464:63487]	12	1	_	Covered
bin auto [63488:64511]	5	1	_	Covered
bin auto $[64512:65535]$	78	1	_	Covered
	100.00%	100		Covered
Coverpoint wr_ack_cp			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin } \text{ auto} \left[0 \right]$	593	1	_	$\operatorname{Covered}$
bin auto[1]	612	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
bin auto $[0]$	100.00% 1067	100	_	Covered
			_	
bin auto[1]	138	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	1045	1	_	Covered
bin auto[1]	160	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2		Covered
	-	$\frac{2}{2}$	_	
missing/total bins:	100.00%	-	_	
% Hit:	100.00%	100	_	C -
bin auto [0]	932	1	_	Covered
bin auto[1]	273	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	100.00% 1105	100		Covered
			_	
bin auto[1]	100	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1023	1	_	Covered
bin auto[1]	182	1	_	Covered
	102	_		55,516d

Coverpoint underflow_cp	100.00%	100	_	Covered	
covered/total bins: missing/total bins:	$\frac{2}{0}$	$\frac{2}{2}$	_ _		
% Hit:	100.00%	100	_		
$egin{array}{ll} egin{array}{ll} egi$	$1068 \\ 137$	1 1	_ _	Covered Covered	
Cross wr_ack_cross	100.00%	100	_	Covered	
covered/total bins: missing/total bins:	6 0	6 6	_		
% Hit:	100.00%	100	_		
Auto, Default and User Defined Bins: bin < auto[1], auto[1], auto[1] >	161	1	_	Covered	
$\mathrm{bin} \ < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	45	1	_	Covered	
$egin{aligned} & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$451\\147$	1 1	_	Covered Covered	
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	183	1	_	Covered	
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > $ $\operatorname{Illegal} \ \operatorname{and} \ \operatorname{Ignore} \ \operatorname{Bins}:$	218	1	_	Covered	
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO Covered	
Cross full_cross covered/total bins:	100.00%	$100 \\ 6$	_	Covered	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6\\100$	_		
Auto, Default and User Defined Bins:	100.00%	100	_		
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \end{aligned}$	$\begin{array}{c} 140 \\ 20 \end{array}$	1 1	_	Covered Covered	
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	206	1	_	Covered	
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$183 \\ 458$	1 1	_	Covered Covered	
$\operatorname{bin} \ < \operatorname{auto} \left[0 ight], \operatorname{auto} \left[0 ight], \operatorname{auto} \left[0 ight] >$	198	1	_	Covered	
Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full	0		_	ZERO	
ignore_bin w_en_r_en_allactv_full	0		_	ZERO	
Cross empty_cross covered/total bins:	100.00%	$100 \\ 6$	_	Covered	
missing/total bins:	0	6	_		
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_		
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right] >$	20	1	_	Covered	
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$134\\186$	1 1	_	Covered Covered	
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	541	1	_	Covered	
$egin{aligned} ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight]> \ \end{aligned} \\ ext{bin } &< ext{auto} \left[0 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight]> \end{aligned}$	$49 \\ 156$	1 1	_	Covered Covered	
Illegal and Ignore Bins:		1			
ignore_bin read_nactv_empty Cross almostfull_cross	$119\\100.00\%$	100	_	Occurred Covered	
covered/total bins:	6	6	_		
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6\\100$	_		
Auto, Default and User Defined Bins:	4.0	1		C 1	
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] \ > \end{aligned} \ egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] \ > \end{aligned}$	$\frac{40}{8}$	$1 \\ 1$	_	Covered Covered	
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\!>$	166	1	_	Covered	
$egin{aligned} ext{bin } & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\frac{563}{175}$	1 1	_	Covered Covered	
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	201	1	_	Covered	
ignore_bin_w_en_nactv_almostfull	52		_	Occurred	
Cross almostempty_cross covered/total bins:	100.00%	$100 \\ 6$	_	Covered	
missing/total bins:	0	6	_		
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_		
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	60	1	_	Covered	
$egin{aligned} ext{bin } &< ext{auto} [1] \ , ext{auto} [0] > \ ext{bin } &< ext{auto} [0] \ , ext{auto} [1] \ , ext{auto} [1] > \end{aligned}$	$\frac{146}{75}$	1 1	_	Covered Covered	
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	523	1	_	Covered	
$egin{aligned} ext{bin} & < ext{auto} [1], ext{auto} [0], ext{auto} [0] > \ ext{bin} & < ext{auto} [0], ext{auto} [0], ext{auto} [0] > \end{aligned}$	$170 \\ 184$	1 1	_	Covered Covered	
Illegal and Ignore Bins:					
ignore_bin w_en_nactv_almostempty Cross overflow_cross	$47 \\ 100.00\%$	100	_	Occurred Covered	
covered/total bins:	6	6	_		
missing/total bins: % Hit:	$0\\100.00\%$	$6 \\ 100$	_		
Auto, Default and User Defined Bins:	20	1		Covered	
$egin{aligned} ext{bin } &< ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] \ > \end{aligned} \ \ egin{aligned} ext{bin } &< ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] \ > \end{aligned}$	$\frac{30}{176}$	1 1	_	Covered	
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	108	1	_	Covered Covered	
$egin{aligned} ext{bin } &< ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin } &< ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$490 \\ 183$	1	_	Covered	
bin $<$ auto $\begin{bmatrix} 0 \end{bmatrix}$, auto $\begin{bmatrix} 0 \end{bmatrix}$, auto $\begin{bmatrix} 0 \end{bmatrix}$ $>$ Illegal and Ignore Bins:	218	1	_	Covered	
ignore_bin w_en_nactv_wr_ack	0		_	ZERO	
Cross underflow_cross covered/total bins:	100.00%	$100 \\ 6$	_	Covered	
missing/total bins:	0	6	_		
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_		
bin <auto[1], ,="" auto[1]=""></auto[1],>					
	39	1	_	Covered	
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	39 98	1 1	_ _	Covered Covered	

```
bin <auto[1], auto[1], auto[0] > bin <auto[0], auto[1], auto[0] > bin <auto[1], auto[0], auto[0] > bin <auto[0], auto[0], auto[0] >
                                                                                                                1
                                                                                                                                              Covered
                                                                                         167
                                                                                         598
                                                                                                                                              Covered
                                                                                                                1
                                                                                                                                              Covered
                                                                                          85
                                                                                                                1
                                                                                         218
                                                                                                                1
                                                                                                                                              Covered
Illegal and Ignore Bins:
      ignore\_bin \quad r\_en\_nactv\_wr\_ack
                                                                                            0
                                                                                                                                             ZERO
```

TOTAL COVERGROUP COVERAGE: 99.50% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.50%

▼ Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover_n_wr_a	SVA	1	Off	130	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_counte	SVA	1	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	V	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	√	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	V	Off	5	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	√	Off	31	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	✓	Off	166	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	√	Off	91	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/coverfull_fla	SVA	√	Off	143	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_empty	SVA	√	Off	239	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_underfl	SVA	✓	Off	115	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_overflo	SVA	✓	Off	80	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_a	SVA	✓	Off	551	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_reset	SVA	√	Off	130	1	Unli	1	100%		I ✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 2: SVA "Seed2"

3.3 Functional Coverage "seed3" Report

Coverage Report by instance with details

== Instance: /FIFO_coverage_pk					
=== Design Unit: work.FIFO_cove	erage_pkg				
Covergroup Coverage:					
$\operatorname{Covergroups}$	1	na	na	99.42%	
$\operatorname{Coverpoints}/\operatorname{Crosses}$	19	na	na	na	
Covergroup Bins	190	183	7	96.31%	

Covergroup Bins 190 183	7 96	.31%		
Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.42%	100		Uncovered
covered/total bins:	183	190	_	
missing/total bins:	7	190	_	
% Hit:	96.31%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	123	1	_	$\operatorname{Covered}$
bin auto[1]	1082	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	00,0104
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	205	1	_	Covered
bin auto $[1024:2047]$	9	1	_	Covered
bin auto $[2048:3071]$	14	1	_	Covered
bin auto [3072:4095]	15	1	_	Covered
bin auto [4096:5119]	15	1	_	Covered
bin auto [5120:6143]	$\frac{16}{16}$	1		Covered
bin auto $[6144:7167]$	17	1	_	Covered
bin auto [7168:8191]	14	1	_	Covered
· ·		1	_	Covered
bin auto [8192:9215]	9	1	_	
bin auto [9216:10239]	12	1	_	Covered
bin auto [10240:11263]	4	1	_	Covered
bin auto [11264:12287]	8	1	_	Covered
bin auto [12288:13311]	13	1	_	Covered
bin auto [13312:14335]	$\frac{14}{7}$	1	_	Covered
bin auto [14336:15359]	7	1	_	Covered
bin auto [15360:16383]	8	1	_	Covered
bin auto [16384:17407]	15	1	_	Covered
bin auto [17408:18431]	12	1	_	Covered
bin auto [18432:19455]	11	1	_	Covered
bin auto [19456:20479]	11	1	_	Covered
bin auto [20480:21503]	17	1	_	Covered
bin auto [21504:22527]	9	1	_	Covered
bin auto [22528:23551]	18	1	_	Covered
bin auto $[23552:24575]$	14	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[24576 \colon\! 25599 \right]$	15	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[25600 \colon\! 26623 \right]$	10	1	_	Covered
bin auto $[26624:27647]$	14	1	_	$\operatorname{Covered}$
bin auto $[27648:28671]$	14	1	_	$\operatorname{Covered}$
bin auto $[28672:29695]$	9	1	_	Covered
bin auto [29696:30719]	11	1	_	Covered
bin auto [30720:31743]	14	1	_	Covered
bin auto [31744:32767]	14	1	_	$\operatorname{Covered}$
bin auto [32768:33791]	13	1	_	Covered

bin auto [33792:34815]				
	10	1	_	Covered
bin auto [34816:35839]	10	1	_	Covered
bin auto [35840:36863]	11	1	_	Covered
bin auto [36864:37887]	7	1	_	Covered
bin auto [37888:38911]	22	1	_	Covered
bin auto $[38912:39935]$	12	1	_	$\operatorname{Covered}$
bin auto $[39936:40959]$	16	1	_	$\operatorname{Covered}$
bin auto $[40960:41983]$	7	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	12	1	_	Covered
bin auto [43008:44031]	11	1	_	Covered
bin auto [44032:45055]	13	1	_	Covered
bin auto $[45056:46079]$	20	1	_	$\operatorname{Covered}$
bin auto [46080:47103]	14	1	_	Covered
bin auto [47104:48127]	13	1	_	Covered
bin auto [48128:49151]	14			Covered
		1	_	
bin auto [49152:50175]	14	1	_	Covered
bin auto [50176:51199]	12	1	_	Covered
${\rm bin \ \ auto} [51200 \colon\! 52223]$	15	1	_	Covered
bin auto $[52224:53247]$	11	1	_	$\operatorname{Covered}$
bin auto $[53248:54271]$	12	1	_	$\operatorname{Covered}$
${ m bin \ auto} [54272 \!:\! 55295]$	15	1	_	Covered
bin auto [55296:56319]	17	1	_	Covered
bin auto [56320:57343]	13	1	_	$\operatorname{Covered}$
bin auto $[57344:58367]$	5	1	_	Covered
bin auto [58368:59391]	$1\overline{2}$	1	_	Covered
bin auto [59392:60415]	17	1	_	Covered
bin auto [60416:61439]	16	1		Covered
			_	
bin auto $[61440:62463]$	14	1	_	Covered
bin auto $[62464:63487]$	19	1	_	Covered
bin auto $[63488:64511]$	8	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	212	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
	787	1		Covered
bin auto [0]		_	_	
bin auto [1]	418	1	_	Covered
$Coverpoint w_en_cp$	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	411	1	_	Covered
bin auto[1]	794	1	_	Covered
Coverpoint data_out_cp	89.06%	100	_	Uncovered
covered/total bins:	57	64	_	
missing/total bins:	7	64	_	
% Hit:	89.06%	100	_	
bin auto [0:1023]	656	1	_	Covered
bin auto $[1024:2047]$	10	1	_	Covered
		1		
bin auto [2048:3071]	2	1	_	Covered
bin auto [2048:3071] bin auto [3072:4095]	2 18	1 1	_ _	Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$	$\begin{array}{c} 2\\18\\13\end{array}$	1 1 1	_	Covered Covered Covered
bin $auto[2048:3071]$ bin $auto[3072:4095]$ bin $auto[4096:5119]$ bin $auto[5120:6143]$	$egin{array}{c} 2 \\ 18 \\ 13 \\ 15 \end{array}$	1 1 1 1	_ _	Covered Covered Covered Covered
bin auto $\begin{bmatrix} 2048:3071 \end{bmatrix}$ bin auto $\begin{bmatrix} 3072:4095 \end{bmatrix}$ bin auto $\begin{bmatrix} 4096:5119 \end{bmatrix}$ bin auto $\begin{bmatrix} 5120:6143 \end{bmatrix}$ bin auto $\begin{bmatrix} 6144:7167 \end{bmatrix}$	2 18 13 15 5	1 1 1 1 1	_ _ _	Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$	$egin{array}{c} 2 \\ 18 \\ 13 \\ 15 \end{array}$	1 1 1 1 1	_ _ _ _	Covered Covered Covered Covered Covered Covered
bin auto $\begin{bmatrix} 2048:3071 \end{bmatrix}$ bin auto $\begin{bmatrix} 3072:4095 \end{bmatrix}$ bin auto $\begin{bmatrix} 4096:5119 \end{bmatrix}$ bin auto $\begin{bmatrix} 5120:6143 \end{bmatrix}$ bin auto $\begin{bmatrix} 6144:7167 \end{bmatrix}$	2 18 13 15 5	1 1 1 1 1 1	_ _ _ _	Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$	2 18 13 15 5 7	1 1 1 1 1 1 1	- - - -	Covered Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$	2 18 13 15 5 7 10	1 1 1 1 1 1 1 1	- - - - -	Covered Covered Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$	2 18 13 15 5 7 10 6	1 1 1 1 1 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$	2 18 13 15 5 7 10 6 0	1 1 1 1 1 1 1 1	- - - - - - - -	Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$	2 18 13 15 5 7 10 6 0 1	1 1 1 1 1 1 1 1 1	- - - - - - - -	Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$	2 18 13 15 5 7 10 6 0 1 2 4	1 1 1 1 1 1 1 1 1 1	- - - - - - - - -	Covered ZERO Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$	2 18 13 15 5 7 10 6 0 1 2 4	1 1 1 1 1 1 1 1 1 1	- - - - - - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[14336:15359]$ bin auto $[14336:15359]$ bin auto $[15360:16383]$	2 18 13 15 5 7 10 6 0 1 2 4 0	1 1 1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered Covered Covered Covered Covered Covered Covered Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$ bin auto $[15360:16383]$ bin auto $[16384:17407]$	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8	1 1 1 1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$ bin auto $[15360:16383]$ bin auto $[16384:17407]$ bin auto $[17408:18431]$	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9	1 1 1 1 1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$ bin auto $[16384:17407]$ bin auto $[17408:18431]$ bin auto $[18432:19455]$	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$ bin auto $[15360:16383]$ bin auto $[16384:17407]$ bin auto $[17408:18431]$ bin auto $[18432:19455]$ bin auto $[19456:20479]$	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2 8	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	 	Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered
bin auto $[2048:3071]$ bin auto $[3072:4095]$ bin auto $[4096:5119]$ bin auto $[5120:6143]$ bin auto $[6144:7167]$ bin auto $[7168:8191]$ bin auto $[8192:9215]$ bin auto $[9216:10239]$ bin auto $[10240:11263]$ bin auto $[11264:12287]$ bin auto $[12288:13311]$ bin auto $[13312:14335]$ bin auto $[14336:15359]$ bin auto $[16384:17407]$ bin auto $[17408:18431]$ bin auto $[18432:19455]$	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered
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bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [1336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [24576:25599] bin auto [25600:26623] bin auto [26624:27647] bin auto [27648:28671] bin auto [29696:30719] bin auto [30720:31743] bin auto [31744:32767] bin auto [32768:33791] bin auto [32768:33791] bin auto [35840:36863] bin auto [36864:37887] bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [49960:41983]	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2 8 3 0 2 8 15 0 5 6 12 2 9 1 5 12 0 5 3 12 4 13 8 2	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
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bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263] bin auto [1264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [24576:25599] bin auto [25600:26623] bin auto [26624:27647] bin auto [28672:29695] bin auto [29696:30719] bin auto [30720:31743] bin auto [31744:32767] bin auto [32768:33791] bin auto [34816:35839] bin auto [35840:36863] bin auto [36864:37887] bin auto [37888:38911] bin auto [37888:38911] bin auto [38912:39935] bin auto [39936:40959] bin auto [40960:41983] bin auto [449308:44031] bin auto [440308:44031] bin auto [440308:44031] bin auto [440308:44031] bin auto [44032:45055]	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2 8 3 0 2 8 15 0 5 6 12 2 9 1 5 12 0 5 3 12 4 13 8 2 3 11	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [8192:9215] bin auto [8192:9215] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [15360:16383] bin auto [16384:17407] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503] bin auto [21504:22527] bin auto [22528:23551] bin auto [24576:25599] bin auto [24576:25599] bin auto [26624:27647] bin auto [27648:28671] bin auto [27648:28671] bin auto [27648:28671] bin auto [30720:31743] bin auto [31744:32767] bin auto [33792:34815] bin auto [34816:35839] bin auto [35840:36863] bin auto [36864:37887] bin auto [36864:37887] bin auto [38912:39935] bin auto [38912:39935] bin auto [419884:43007] bin auto [419884:43007] bin auto [419884:43007] bin auto [449080:44983] bin auto [449080:44031]	2 18 13 15 5 7 10 6 0 1 2 4 0 13 8 9 2 8 3 0 2 8 15 0 5 6 12 2 9 1 5 12 0 5 3 12 4 13 8 2 3			Covered Covered Covered Covered Covered Covered Covered Covered ZERO Covered

bin auto [46080:47103]	13	1	_	Covered
bin auto [47104:48127]	9	1	_	Covered
bin auto [48128:49151]	8	1	_	Covered
bin auto $[49152:50175]$	9	1	_	Covered
bin auto [50176:51199]	1	1	_	Covered
bin auto [51200:52223]	8	1	_	Covered
bin auto [52224:53247]	0	1	_	ZERO
	-		_	
bin auto [53248:54271]	11	1	_	Covered
bin auto $[54272:55295]$	17	1	_	Covered
bin auto $[55296:56319]$	6	1	_	Covered
bin auto [56320:57343]	4	1	_	Covered
bin auto [57344:58367]	0	1	_	ZERO
bin auto [58368:59391]	11	1	_	Covered
	12			Covered
bin auto [59392:60415]		1	_	
bin auto $[60416:61439]$	4	1	_	Covered
bin auto $[61440:62463]$	12	1	_	Covered
bin auto [62464:63487]	10	1	_	Covered
bin auto [63488:64511]	3	1	_	Covered
$bin auto \begin{bmatrix} 64512:65535 \end{bmatrix}$	128	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$		Covered
, ,			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0 \right]$	581	1	_	Covered
bin auto[1]	624	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	00.0100
,	0	$\frac{2}{2}$		
missing/total bins:			_	
% Hit:	100.00%	100	_	
bin auto [0]	1110	1	_	Covered
bin auto[1]	95	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	$\overline{2}$	_	
missing/total bins:	0	$\frac{2}{2}$		
	_		_	
% Hit:	100.00%	100	_	
bin auto [0]	1084	1	_	Covered
bin auto[1]	121	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100		
			_	<i>C</i> 1
bin auto [0]	925	1	_	Covered
$\mathrm{bin} \ \mathrm{auto} \left[1 \right]$	280	1	_	$\operatorname{Covered}$
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	C 1
bin auto [0]	1110	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} [1]$	95	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	C 1
bin auto[0]	1025	1	_	Covered
bin auto[1]	180	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1060	1		Covered
	145	1		Covered
bin auto[1]		_	_	
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $<$ auto [1], auto [1], auto [1]>	181	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	44	1		Covered
			_	
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	443	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[1]\;,\mathrm{auto}[0]\!>$	126	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[0]\;,\mathrm{auto}[0]>$	193	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] >$	218	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100		Covered
				Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	106	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [1] \rangle$	15	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	225	1	_	Covered
			_	
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	193	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	463	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	203	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full				ZERO
	0			
Cross empty cross	0	100	_	
Cross empty_cross	$0 \\ 100.00\%$	100	_	Covered
covered/total bins:	$0 \\ 100.00\% \\ 6$	6	_ _ _	
<pre>covered/total bins: missing/total bins:</pre>	$0 \\ 100.00\% \\ 6 \\ 0$	6 6	_ _ _ _	
covered/total bins:	$0 \\ 100.00\% \\ 6$	6	- - - -	

Auto, Default and User Defined Bins:	2.0			G 1
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	29	1	_	Covered
bin < auto[1], auto[0], auto[1] >	134	1	_	Covered
bin < auto[1], auto[1], auto[0] >	196	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right] >$	512	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	59	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [0], \operatorname{auto} [0] >$	158	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	117		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right] >$	33	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right] >$	10	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	192	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[1]$, $\operatorname{auto}[0] >$	535	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0] >$	183	1	_	Covered
bin < auto [0], auto [0], auto [0] >	200	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	52		_	Occurred
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	67	1	_	Covered
bin < auto[1], auto[1], auto[0] >	158	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	80	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	489	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	185	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	193	1	_	Covered
Illegal and Ignore Bins:	100	1		Covered
ignore_bin_w_en_nactv_almostempty	33		_	Occurred
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin $<$ auto [1], auto [1] $>$	20	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	205	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	75	1		Covered
	$\frac{75}{494}$	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	193		_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$		1	_	
$\begin{array}{c} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Hillowed and Lemma Pines.} \end{array}$	218	1	_	Covered
Illegal and Ignore Bins:	0			ZEDO
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO
Cross underflow_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				~ ,
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right] >$	42	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight]>$	103	1	_	$\operatorname{Covered}$
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight]>$	183	1	_	Covered
${\color{blue} \text{bin }} < {\color{blue} \text{auto}} \left[0 \right], {\color{blue} \text{auto}} \left[1 \right], {\color{blue} \text{auto}} \left[0 \right] >$	569	1	_	$\widetilde{\text{Covered}}$
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[0 ight]>$	90	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	218	1	_	$\operatorname{Covered}$
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

COVERGROUP COVERAGE:

Covergroup	${ m Metric}$	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.42%	100		Uncovered
covered/total bins:	183	190	_	
missing/total bins:	7	190	_	
% Hit:	96.31%	100	_	
$Coverpoint rst_n_cp$	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	123	1	_	$\operatorname{Covered}$
bin auto[1]	1082	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	205	1	_	$\operatorname{Covered}$
bin auto $[1024:2047]$	9	1	_	$\operatorname{Covered}$
bin auto [2048:3071]	14	1	_	$\operatorname{Covered}$
bin auto $[3072:4095]$	15	1	_	$\operatorname{Covered}$
bin auto [4096:5119]	15	1	_	$\operatorname{Covered}$
bin auto [5120:6143]	16	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	17	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	14	1	_	$\operatorname{Covered}$
bin auto [8192:9215]	9	1	_	$\operatorname{Covered}$
bin auto [9216:10239]	12	1	_	Covered
bin auto [10240:11263]	4	1	_	Covered

bin auto [11264:12287]	8	1	_	Covered
bin auto [12288:13311]	13	1	_	Covered
bin auto [13312:14335]	14	1	_	Covered
bin auto $[14336:15359]$	7	1	_	Covered
bin auto [15360:16383]	8	1	_	Covered
bin auto [16384:17407]	15	1	_	Covered
bin auto $[17408:18431]$	12	1	_	Covered
bin auto [18432:19455]	11	1	_	Covered
bin auto [19456:20479]	11	1	_	Covered
	17	1		
bin auto $[20480:21503]$			_	Covered
bin auto $[21504:22527]$	9	1	_	$\operatorname{Covered}$
bin auto [22528:23551]	18	1	_	Covered
	14	1		
bin auto [23552:24575]			_	Covered
bin auto $[24576:25599]$	15	1	_	Covered
bin auto [25600:26623]	10	1	_	Covered
bin auto [26624:27647]	14	1	_	Covered
bin auto $[27648:28671]$	14	1	_	Covered
bin auto [28672:29695]	9	1	_	Covered
bin auto [29696:30719]	11	1	_	Covered
bin auto $[30720:31743]$	14	1	_	$\operatorname{Covered}$
bin auto $[31744:32767]$	14	1	_	$\operatorname{Covered}$
bin auto [32768:33791]	13	1	_	Covered
	10			Covered
bin auto [33792:34815]		1	_	
bin auto $[34816:35839]$	10	1	_	Covered
bin auto [35840:36863]	11	1	_	Covered
bin auto [36864:37887]	7	1	_	Covered
bin auto $[37888:38911]$	22	1	_	$\operatorname{Covered}$
bin auto [38912:39935]	12	1	_	$\operatorname{Covered}$
bin auto [39936:40959]	16	1	_	Covered
bin auto $[40960:41983]$	7	1	_	$\operatorname{Covered}$
bin auto $[41984:43007]$	12	1	_	Covered
bin auto [43008:44031]	11	1	_	Covered
${\rm bin \ \ auto} [44032\!:\!45055]$	13	1	_	$\operatorname{Covered}$
bin auto $[45056:46079]$	20	1	_	$\operatorname{Covered}$
bin auto [46080:47103]	14	1	_	Covered
		_		
bin auto $[47104:48127]$	13	1	_	$\operatorname{Covered}$
bin auto $[48128:49151]$	14	1	_	$\operatorname{Covered}$
bin auto [49152:50175]	14	1	_	Covered
	12	_		
bin auto $[50176:51199]$		1	_	Covered
bin auto[51200:52223]	15	1	_	Covered
bin auto $[52224:53247]$	11	1	_	Covered
bin auto $[53248:54271]$	12	1		Covered
			_	
bin auto $[54272:55295]$	15	1	_	$\operatorname{Covered}$
bin auto $[55296:56319]$	17	1	_	Covered
bin auto [56320:57343]	13	1	_	Covered
			_	
bin auto $[57344:58367]$	5	1	_	Covered
bin auto [58368:59391]	12	1	_	$\operatorname{Covered}$
bin auto [59392:60415]	17	1	_	Covered
		-		
bin auto $[60416:61439]$	16	1	_	$\operatorname{Covered}$
bin auto $[61440:62463]$	14	1	_	$\operatorname{Covered}$
bin auto [62464:63487]	19	1	_	Covered
bin auto $[63488:64511]$	8	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	212	1	_	$\operatorname{Covered}$
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{1}{2}$		00.0104
,			_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	787	1	_	Covered
bin auto [1]	418	1	_	$\operatorname{Covered}$
$\operatorname{Coverpoint} w_{-\operatorname{en_cp}}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
	0			
missing/total bins:		2	_	
% Hit:	100.00%	100	_	
bin auto [0]	411	1	_	Covered
bin auto[1]	794	1	_	Covered
Coverpoint data_out_cp	89.06%	100	_	${\it Uncovered}$
covered/total bins:	57	64	_	
missing/total bins:	7	64	_	
% Hit:	89.06%	100		
			_	· ·
$\operatorname{bin} \ \operatorname{auto} \left[0\!:\!1023 \right]$	656	1	_	$\operatorname{Covered}$
bin auto [1024:2047]	10	1	_	Covered
bin auto [2048:3071]	$\overset{\circ}{2}$	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[3072 \!:\! 4095 \right]$	18	1	_	Covered
bin auto $[4096:5119]$	13	1	_	Covered
bin auto [5120:6143]	15	1	_	Covered
bin auto [6144:7167]	5	1	_	Covered
bin auto $[7168:8191]$	7	1	_	Covered
bin auto [8192:9215]	10	1	_	Covered
bin auto [9216:10239]	6	1	_	Covered
bin auto $[10240:11263]$	0	1	_	ZERO
bin auto [11264:12287]	1	1	_	Covered
bin auto [12288:13311]	$\stackrel{ ext{-}}{2}$	1	_	Covered
· · ·				
bin auto [13312:14335]	4	1	_	Covered
bin auto [14336:15359]	0	1	_	ZERO
bin auto [15360:16383]	13	1	_	Covered
bin auto [16384:17407]	8	1	_	Covered
bin auto [17408:18431]	9	1	_	Covered
bin auto [18432:19455]	2	1	_	Covered
bin auto [19456:20479]	8	1	_	Covered
bin auto $[20480:21503]$	3	1	_	Covered
bin auto [21504:22527]	0	1	_	ZERO
bin auto [22528:23551]	$\overset{\circ}{2}$	1	_	Covered
DIII - auto [22020:2001]	Δ	1	_	Covered

1. [00270 0.4771]				
bin auto [23552:24575]	8	1	_	Covered
bin auto [24576:25599]	15	1		Covered
bin auto [25600:26623]	0	1		ZERO
bin auto [26624:27647]	5 6	1	_	Covered Covered
bin auto [27648:28671]	6	1	_	
bin auto [28672:29695]	$\frac{12}{2}$	1	_	Covered
bin auto [29696:30719]	2	1	_	Covered
bin auto [30720:31743]	9	1	_	Covered
bin auto [31744:32767]	1	1	_	Covered
bin auto [32768:33791]	5	1	_	Covered
bin auto [33792:34815]	12	1	_	Covered
bin auto $[34816:35839]$	0	1	_	ZERO
bin auto $[35840:36863]$	5	1	_	Covered
bin auto $[36864:37887]$	3	1	_	$\operatorname{Covered}$
bin auto [37888:38911]	12	1	_	Covered
bin auto [38912:39935]	4	1	_	$\operatorname{Covered}$
bin auto $[39936:40959]$	13	1	_	Covered
bin auto [40960:41983]	8	1	_	Covered
bin auto [41984:43007]	2	1	_	Covered
bin auto [43008:44031]	3	1	_	Covered
bin auto [44032:45055]	11	1	_	Covered
bin auto $[45056:46079]$	9	1	_	Covered
bin auto [46080:47103]	13	1	_	Covered
bin auto [47104:48127]	9	1	_	Covered
bin auto [48128:49151]	8	1	_	Covered
bin auto [49152:50175]	9	1	_	Covered
bin auto [50176:51199]	1	1	_	Covered
bin auto $[50176:31199]$	8	1		Covered
			_	ZERO
bin auto [52224:53247]	0	1	_	
bin auto [53248:54271]	11	1	_	Covered
bin auto [54272:55295]	17	1	_	Covered
bin auto [55296:56319]	6	1	_	Covered
bin auto [56320:57343]	4	1	_	Covered
bin auto [57344:58367]	0	1	_	ZERO
bin auto $[58368:59391]$	11	1	_	Covered
bin auto $[59392:60415]$	12	1	_	$\operatorname{Covered}$
bin auto $[60416:61439]$	4	1	_	Covered
bin auto $[61440:62463]$	12	1	_	Covered
bin auto $[62464:63487]$	10	1	_	Covered
bin auto [63488:64511]	3	1	_	Covered
bin auto $[64512:65535]$	128	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	581	1	_	Covered
bin auto[1]	624	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	9	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$		
		_	_	
% Hit:	100.00%	100	_	C 1
bin auto[0]	1110	1	_	Covered
bin auto[1]	95	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	<i>a</i> 1
bin auto [0]	1084	1	_	Covered
bin auto [1]	121	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	925	1	_	Covered
bin auto[1]	280	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	-
$\operatorname{bin} \operatorname{auto} [0]$	1110	1	_	Covered
bin auto[1]	95	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1025	1	_	Covered
bin auto[1]	180	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1060	1	_	Covered
bin auto[1]	145	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin $<$ auto [1], auto [1], auto [1]>	181	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	44	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	$44 \\ 443$	1	-	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{443}{126}$	1	-	Covered
om <auto[0], auto[0]="" auto[1],=""></auto[0],>	120	1	_	ooverea

$\begin{array}{c} \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{Illegal and Ignore Bins:} \end{array}$	193 218	1 1	_ _	Covered Covered
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: bin $<$ auto $[0]$, auto $[1]$, auto $[1]$	106	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	15	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] > \ \end{aligned} \\ ext{bin} & < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [0] > \end{aligned}$	$\begin{array}{c} 225 \\ 193 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	463	1	_	Covered
bin < auto [0], auto [0], auto [0] >	203	1	_	Covered
Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: $bin < auto[1], auto[1], auto[1] >$	29	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	134	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right]\! >$	196	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$512 \\ 59$	1 1	_	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
bin $\langle auto[0], auto[0], auto[0] \rangle$	158	1	_	Covered
Illegal and Ignore Bins:	117			0 1
ignore_bin read_nactv_empty Cross almostfull_cross	$117\\100.00\%$	100	_	Occurred Covered
covered/total bins:	6	6	_	00,0104
missing/total bins:	$0 \\ 100.00\%$	6	_	
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] >$	33	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$10\\192$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	535	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[0]$, $\operatorname{auto}[0] >$	183	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	200	1	_	Covered
ignore_bin_w_en_nactv_almostfull	52		_	Occurred
Cross almostempty_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	6 0	6 6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	67	1		Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ \end{aligned} \ egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	158	1 1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right] >$	80	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$489 \\ 185$	1 1	_	$egin{array}{c} ext{Covered} \ ext{Covered} \end{array}$
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	193	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty Cross overflow_cross	$\frac{33}{100.00\%}$	100	_	Occurred Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	20	1	_	Covered
bin <auto [0]="" [1],="" auto=""></auto>	205	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[1 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$75 \\ 494$	1 1	_	$egin{array}{c} { m Covered} \\ { m Covered} \end{array}$
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	193	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	218	1	_	Covered
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	6 0	6 6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				C :
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [1] > \end{aligned}$	$42 \\ 103$	1 1	_	Covered Covered
$\mathrm{bin} \ < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	183	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	569	1	_	Covered
$egin{aligned} ext{bin } & < ext{auto} [1] \ , ext{auto} [0] \ , ext{auto} [0] > \ \end{aligned} \\ ext{bin } & < ext{auto} [0] \ , ext{auto} [0] \ , ext{auto} [0] > \end{aligned}$	$90 \\ 218$	1 1	_	Covered Covered
Illegal and Ignore Bins:		•		
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 99.42% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.42%

3.4 Functional Coverage "seed4" Report

Coverage Report by instance with details

▼ Name La	anguage	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover_n_wr_a S	VA	1	Off	96	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_counte S\	VA	✓	Off	1082	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p S\	VA	✓	Off	1082	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p S\	VA	✓	Off	1082	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p S\	VA	✓	Off	3	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p S\	VA	✓	Off	34	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost S\	VA	✓	Off	170	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost S\	VA	✓	Off	84	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
// /top/cover_full_fla S\	VA	✓	Off	109	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_empty S\	VA	✓	Off	249	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_underfl S\	VA	✓	Off	119	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_overflo S\	VA	✓	Off	63	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_a S\	VA	✓	Off	571	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_reset S\	VA	√	Off	123	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog

Figure 3: SVA "Seed3"

=== Instance: /FIFO_coverage_pkg	
== Design Unit: work.FIFO_coverage_pkg	

Covergroup Coverage:				
$\operatorname{Covergroups}$	1	na	na	99.58%
$\operatorname{Coverpoints}/\operatorname{Crosses}$	19	na	na	na

Covergroup Bins 190 185	5 97	.36%		
Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100		Uncovered
covered/total bins:	185	190	_	
missing/total bins:	5	190	_	
% Hit:	97.36%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	$100.00\% \ 130$	100	_	Commad
$egin{array}{ll} ext{bin auto} \left[0 ight] \ ext{bin auto} \left[1 ight] \end{array}$	1075	1 1	_	Covered Covered
Coverpoint data_in_cp	107.00%	100	_	Covered
covered/total bins:	64	64	_	Covered
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	186	1	_	Covered
bin auto $[1024:2047]$	14	1	_	Covered
bin auto [2048:3071]	15	1	_	Covered
bin auto [3072:4095]	12	1	_	$\operatorname{Covered}$
bin auto [4096:5119]	17	1	_	$\operatorname{Covered}$
bin auto $[5120:6143]$	20	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	16	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	14	1	_	$\operatorname{Covered}$
bin auto [8192:9215]	17	1	_	Covered
bin auto [9216:10239]	11	1	_	Covered
bin auto [10240:11263]	15	1	_	Covered
bin auto [11264:12287]	13	1	_	Covered
bin auto $[12288:13311]$ bin auto $[13312:14335]$	$\frac{14}{8}$	1 1	_	Covered Covered
bin auto $[13312:14335]$ bin auto $[14336:15359]$	19	1	_	Covered
bin auto [15360:16383]	$\frac{19}{14}$	1	_	Covered
bin auto [16384:17407]	10	1	_	Covered
bin auto [17408:18431]	10	1	_	Covered
bin auto [18432:19455]	17	1	_	Covered
bin auto [19456:20479]	7	1	_	Covered
bin auto [20480:21503]	8	1	_	Covered
bin auto $[21504:22527]$	9	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[22528 {:} 23551 \right]$	12	1	_	$\operatorname{Covered}$
$\begin{array}{ll} \text{bin} & \text{auto} \left[23552 \colon\! 24575\right] \end{array}$	10	1	_	$\operatorname{Covered}$
bin auto [24576:25599]	11	1	_	Covered
bin auto [25600:26623]	18	1	_	Covered
bin auto [26624:27647]	12	1	_	Covered
bin auto [27648:28671]	$\frac{14}{16}$	1 1	_	Covered Covered
bin auto [28672:29695] bin auto [29696:30719]	$\frac{16}{19}$	1	_	Covered
bin auto [30720:31743]	7	1		Covered
bin auto [31744:32767]	12	1	_	Covered
bin auto [32768:33791]	$\frac{12}{25}$	1	_	Covered
bin auto [33792:34815]	14	1	_	Covered
bin auto [34816:35839]	15	1	_	Covered
bin auto [35840:36863]	19	1	_	Covered
bin auto [36864:37887]	21	1	_	Covered
bin auto [37888:38911]	10	1	_	Covered
bin auto [38912:39935]	16	1	_	Covered
bin auto [39936:40959]	11	1	_	Covered
bin auto [40960:41983]	14	1	_	Covered
bin auto [41984:43007]	12	1	_	Covered
bin auto [43008:44031]	12	1	_	Covered
bin auto [44032:45055]	18	1	_	Covered
bin auto [45056:46079]	12	1	_	Covered
bin auto [46080:47103] bin auto [47104:48127]	10	1 1	_	Covered Covered
bin auto [47104:48127] bin auto [48128:49151]	$9\\17$	1	_	Covered Covered
DIII auto [40140149191]	1 (1	_	Covered

bin auto [49152:50175]	14	1	_	Covered
bin auto [50176:51199]	11	1	_	Covered
bin auto [51200:52223]	10	1	_	Covered
bin auto [52224:53247]	16	1	_	Covered
bin auto [53248:54271]	8	1	_	Covered
bin auto [54272:55295]	$2\overline{2}$	1	_	Covered
bin auto [55296:56319]	12	1	_	Covered
bin auto [56320:57343]	15	1	_	Covered
bin auto [57344:58367]	15	1	_	Covered
bin auto [58368:59391]	17	1		Covered
bin auto [59392:60415]	16	1	_	Covered
			_	
bin auto [60416:61439]	12	1	_	Covered
bin auto [61440:62463]	14	1	_	Covered
bin auto [62464:63487]	14	1	_	Covered
bin auto [63488:64511]	11	1	_	Covered
bin auto [64512:65535]	166	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	795	1	_	Covered
bin auto[1]	410	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\overline{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	395	1	_	Covered
bin auto[1]	810	1		Covered
Coverpoint data_out_cp	92.18%	100		Uncovered
			_	Uncovered
covered/total bins:	59	64	_	
missing/total bins:	5	64	_	
% Hit:	92.18%	100	_	
bin auto [0:1023]	640	1	_	Covered
bin auto $[1024:2047]$	20	1	_	Covered
bin auto $[2048:3071]$	0	1	_	ZERO
bin auto [3072:4095]	5	1	_	Covered
bin auto [4096:5119]	5	1	_	Covered
bin auto [5120:6143]	7	1	_	Covered
bin auto [6144:7167]	18	1	_	Covered
bin auto [7168:8191]	13	1	_	Covered
bin auto [8192:9215]	14	1	_	Covered
bin auto [9216:10239]	4	1	_	Covered
	10	1		Covered
bin auto [10240:11263]			_	
bin auto [11264:12287]	15	1	_	Covered
bin auto [12288:13311]	17	1	_	Covered
bin auto [13312:14335]	12	1	_	Covered
bin auto [14336:15359]	11	1	_	Covered
${ m bin \ auto} [15360{:}16383]$	3	1	_	$\operatorname{Covered}$
bin auto $[16384:17407]$	1	1	_	$\operatorname{Covered}$
bin auto $[17408:18431]$	4	1	_	Covered
bin auto $[18432:19455]$	21	1	_	Covered
bin auto $[19456:20479]$	0	1	_	ZERO
bin auto [20480:21503]	3	1	_	Covered
bin auto [21504:22527]	1	1	_	Covered
bin auto [22528:23551]	5	1	_	Covered
bin auto $[23552:24575]$	$\overline{4}$	1	_	Covered
bin auto [24576:25599]	$\stackrel{\circ}{4}$	1	_	Covered
bin auto [25600:26623]	6	1	_	Covered
bin auto $[26624:27647]$	5	1	_	Covered
bin auto [27648:28671]	13	1	_	Covered
bin auto [28672:29695]	1	1	_	Covered
bin auto [29696:30719]	1	1	_	Covered
	9	1		Covered
bin auto [30720:31743]			_	
bin auto [31744:32767]	5	1	_	Covered
bin auto [32768:33791]	22	1	_	Covered
bin auto [33792:34815]	$\frac{12}{7}$	1	_	Covered
bin auto [34816:35839]	7	1	_	Covered
bin auto $[35840:36863]$	14	1	_	Covered
bin auto [36864:37887]	6	1	_	Covered
bin auto [37888:38911]	3	1	_	Covered
bin auto $[38912:39935]$	19	1	_	Covered
bin auto $[39936:40959]$	5	1	_	Covered
bin auto [40960:41983]	5	1	_	Covered
bin auto [41984:43007]	11	1	_	Covered
bin auto [43008:44031]	13	1	_	Covered
bin auto [44032:45055]	9	1	_	Covered
bin auto [45056:46079]	$\overline{2}$	1	_	Covered
bin auto [46080:47103]	$1\overline{4}$	1	_	Covered
bin auto [47104:48127]	0	1	_	ZERO
bin auto [48128:49151]	16	1	_	Covered
bin auto [49152:50175]	7	1		Covered
			_	Covered
bin auto [50176:51199]	4	1		
bin auto [51200:52223]	$\frac{16}{7}$	1	_	Covered
bin auto [52224:53247]	7	1	_	Covered
bin auto [53248:54271]	0	1		ZERO
bin auto [54272:55295]	9	1	_	Covered
$bin \ \ auto \left[55296{:}56319\right]$	3	1	_	Covered
bin auto [56320:57343]	0	1	_	ZERO
bin auto [57344:58367]	9	1	_	Covered
bin auto [58368:59391]	11	1	_	Covered
bin auto [59392:60415]	11	1		Covered
bin auto [60416:61439]	7	1	_	Covered
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bin auto $[61440:62463]$	6	1	_	Covered
bin auto [62464:63487]	3	1	_	Covered
bin auto [63488:64511]	9	1	_	Covered
bin auto [64512:65535]	68	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	582	1	_	Covered
bin auto[1]	623	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	C 1
bin auto[0]	1099	1	_	Covered Covered
bin auto[1]	106	1	_	
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	0 1
bin auto[0]	1071	1	_	Covered
bin auto[1]	134	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	934	1	_	Covered
bin auto [1]	271	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1114	1	_	Covered
bin auto[1]	91	1	_	Covered
$\operatorname{Coverpoint}$ $\operatorname{almostempty_cp}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1002	1	_	Covered
bin auto [1]	203	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	1070	1	_	Covered
bin auto[1]	135	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6		Covered
·	0	6	_	
missing/total bins: % Hit:	100.00%	100	_	
	100.00%	100	_	
Auto, Default and User Defined Bins:	100	1		Commad
bin <auto [1]="" [1],="" auto=""></auto>	188	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	43	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	435	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	144	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	179	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	216	1	_	Covered
Illegal and Ignore Bins:	0			ZEDO
ignore_bin w_en_nactv_wr_ack	0	100	_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
	440	4		· ·
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	118	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	16	1	_ _	Covered
$\begin{array}{ll} \text{bin } <& \text{auto } \llbracket 0 \rrbracket \text{ , auto } \llbracket 0 \rrbracket \text{ , auto } \llbracket 1 \rrbracket >\\ \text{bin } <& \text{auto } \llbracket 1 \rrbracket \text{ , auto } \llbracket 1 \rrbracket \text{ , auto } \llbracket 0 \rrbracket > \end{array}$	$\begin{array}{c} 16 \\ 231 \end{array}$	1 1	_ _ _	Covered Covered
$\begin{array}{l} \text{bin } <& \text{auto } \left[0\right], \text{ auto } \left[1\right] >\\ \text{bin } <& \text{auto } \left[1\right], \text{ auto } \left[1\right], \text{ auto } \left[0\right] >\\ \text{bin } <& \text{auto } \left[1\right], \text{ auto } \left[0\right], \text{ auto } \left[0\right] > \end{array}$	$16 \\ 231 \\ 179$	1 1 1	- - -	Covered Covered Covered
$\begin{array}{l} \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[1\right], \text{auto} \left[0\right], \text{auto} \left[0\right] > \\ \text{bin } < \text{auto} \left[0\right], \text{auto} \left[1\right], \text{auto} \left[0\right] > \end{array}$	16 231 179 461	1 1 1		Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$16 \\ 231 \\ 179$	1 1 1	_	Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200	1 1 1	_ _	Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$ \begin{array}{r} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ 0 \end{array} $	1 1 1	_ _	Covered Covered Covered Covered Covered
<pre>bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></pre>	16 231 179 461 200 0 0	1 1 1 1	_ _	Covered Covered Covered Covered ZERO
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$ \begin{array}{r} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ 0 \end{array} $	1 1 1	_ _	Covered Covered Covered Covered Covered
<pre>bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></pre>	16 231 179 461 200 0 0 $100.00%$ 6	1 1 1 1 1 100 6	_ _	Covered Covered Covered Covered ZERO
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0	1 1 1 1 1 1 100 6 6	_ _	Covered Covered Covered Covered ZERO
<pre>bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></pre>	16 231 179 461 200 0 0 $100.00%$ 6	1 1 1 1 1 100 6	_ _	Covered Covered Covered Covered ZERO
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 100 6 6	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 100 6 6	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125	1 1 1 1 1 1 100 6 6 100	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ \\ \end{array}$	1 1 1 1 1 1 100 6 6 100	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125	1 1 1 1 1 1 1 100 6 6 100	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ \\ \end{array}$	1 1 1 1 1 1 1 100 6 6 100	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> </auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ 513 \\ \\ \end{array}$	1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> </auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54	1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> </auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54	1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ 513 \\ 54 \\ 161 \\ \\ \end{array}$	1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross</auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54 161 121	1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54 161 121 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ 513 \\ 54 \\ 161 \\ \\ \\ 121 \\ 100.00\% \\ \\ 6 \\ 0 \\ \\ \end{array}$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit:</auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54 161 121 $100.00%$ 6	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	16 231 179 461 200 0 0 $100.00%$ 6 0 $100.00%$ 25 125 206 513 54 161 121 $100.00%$ 6 0 $100.00%$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered
bin <auto[0], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full Cross empty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: missing/total bins: % Hit:</auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],>	$egin{array}{c} 16 \\ 231 \\ 179 \\ 461 \\ 200 \\ \\ \\ 0 \\ 100.00\% \\ \\ 6 \\ 0 \\ 100.00\% \\ \\ 25 \\ 125 \\ 206 \\ 513 \\ 54 \\ 161 \\ \\ \\ 121 \\ 100.00\% \\ \\ 6 \\ 0 \\ \\ \end{array}$	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_ _	Covered Covered Covered Covered ZERO ZERO Covered

$\operatorname{bin} < \operatorname{auto} [1], \operatorname{auto} [0], \operatorname{auto} [1] >$	8	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [1], \operatorname{auto} [1], \operatorname{auto} [0] >$	195	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right] >$	546	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[0\right]\!>$	171	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	202	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	47		_	Occurred
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	73	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	158	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	79	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	500	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	167	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	177	1	_	Covered
Illegal and Ignore Bins:	111	1		covered
ignore_bin_w_en_nactv_almostempty	51		_	Occurred
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6		Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
	100.0070	100	_	
Auto, Default and User Defined Bins:	10	1		Covered
bin <auto [1]="" [1],="" auto=""></auto>	18	1	_	
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	213	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	88	1	_	Covered
bin < auto[0], auto[1], auto[0] >	491	1	_	Covered
bin < auto[1], auto[0], auto[0] >	179	1	_	Covered
$ \text{bin } < \text{auto} \left[0 \right], \text{auto} \left[0 \right], \text{auto} \left[0 \right] >$	216	1	_	$\operatorname{Covered}$
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} < \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight] >$	36	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [1]$, $\operatorname{auto} [0]$, $\operatorname{auto} [1] >$	99	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	195	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [1], \operatorname{auto} [0] >$	579	1	_	Covered
bin < auto[1], auto[0], auto[0] >	80	1	_	Covered
bin < auto[0], auto[0], auto[0] >	216	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
•				

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100		Uncovered
covered/total bins:	185	190	_	
missing/total bins:	5	190	_	
% Hit:	97.36%	100	_	
$Coverpoint rst_n_cp$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	130	1	_	$\operatorname{Covered}$
bin auto [1]	1075	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0\!:\!1023 \right]$	186	1	_	$\operatorname{Covered}$
bin auto [1024:2047]	14	1	_	$\operatorname{Covered}$
bin auto [2048:3071]	15	1	_	$\operatorname{Covered}$
bin auto $[3072:4095]$	12	1	_	$\operatorname{Covered}$
bin auto $[4096:5119]$	17	1	_	$\operatorname{Covered}$
bin auto [5120:6143]	20	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	16	1	_	$\operatorname{Covered}$
bin auto $[7168:8191]$	14	1	_	$\operatorname{Covered}$
bin auto $[8192:9215]$	17	1	_	$\operatorname{Covered}$
bin auto $[9216:10239]$	11	1	_	$\operatorname{Covered}$
bin auto $[10240:11263]$	15	1	_	$\operatorname{Covered}$
bin auto $[11264:12287]$	13	1	_	$\operatorname{Covered}$
bin auto $[12288:13311]$	14	1	_	$\operatorname{Covered}$
bin auto $[13312:14335]$	8	1	_	$\operatorname{Covered}$
bin auto $[14336:15359]$	19	1	_	$\operatorname{Covered}$
bin auto $[15360:16383]$	14	1	_	$\operatorname{Covered}$
bin auto [16384:17407]	10	1	_	Covered
bin auto [17408:18431]	10	1	_	$\operatorname{Covered}$
bin auto [18432:19455]	17	1	_	Covered
bin auto $[19456:20479]$	7	1	_	$\operatorname{Covered}$
bin auto $[20480:21503]$	8	1	_	Covered
bin auto $[21504:22527]$	9	1	_	Covered
bin auto $[22528:23551]$	12	1	_	Covered
bin auto $[23552:24575]$	10	1	_	Covered
bin auto $[24576:25599]$	11	1	_	Covered
bin auto $[25600:26623]$	18	1	_	$\operatorname{Covered}$

bin auto [26624:27647]	12	1	_	Covered
bin auto [27648:28671]	14	1	_	Covered
bin auto [28672:29695]	16	1	_	Covered
bin auto [29696:30719]	19	1	_	Covered
bin auto [30720:31743]	7	1	_	Covered
bin auto $[31744:32767]$	12	1	_	Covered
bin auto [32768:33791]	25	1	_	Covered
bin auto [33792:34815]	14	1	_	Covered
bin auto [34816:35839]	15	1	_	Covered
bin auto [35840:36863]	19	1	_	Covered
bin auto [36864:37887]	21	1		Covered
			_	
bin auto [37888:38911]	10	1	_	Covered
bin auto [38912:39935]	16	1	_	Covered
bin auto [39936:40959]	11	1	_	Covered
bin auto [40960:41983]	14	1	_	Covered
bin auto [41984:43007]	12	1	_	Covered
bin auto [43008:44031]	12	1		Covered
			_	
$\mathrm{bin} \ \mathrm{auto} \left[44032; 45055 \right]$	18	1	_	Covered
bin auto $[45056:46079]$	12	1	_	$\operatorname{Covered}$
bin auto $[46080:47103]$	10	1	_	Covered
bin auto [47104:48127]	9	1	_	Covered
bin auto [48128:49151]	17	1	_	Covered
bin auto [49152:50175]	14	1	_	Covered
	11			
bin auto [50176:51199]		1	_	Covered
$\mathrm{bin} \ \mathrm{auto} \left[51200 ; 52223 \right]$	10	1	_	Covered
bin auto $[52224:53247]$	16	1	_	$\operatorname{Covered}$
bin auto [53248:54271]	8	1	_	$\operatorname{Covered}$
bin auto [54272:55295]	22	1	_	Covered
bin auto [55296:56319]	$\overline{12}$	1	_	Covered
bin auto [56320:57343]	15	1	_	Covered
bin auto $[57344:58367]$	15	1	_	Covered
bin auto [58368:59391]	17	1	_	$\operatorname{Covered}$
bin auto $[59392:60415]$	16	1	_	Covered
bin auto [60416:61439]	12	1	_	Covered
bin auto $[61440:62463]$	14	1	_	Covered
bin auto $[62464:63487]$	14	1	_	Covered
bin auto $[63488:64511]$	11	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	166	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%			
		100	_	0 1
$\operatorname{bin} \operatorname{auto} [0]$	795	1	_	Covered
bin auto[1]	410	1	_	$\operatorname{Covered}$
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:		2	_	
covered/total bins:	2	2		
missing/total bins:	$\frac{2}{0}$	2		
missing/total bins: % Hit:	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \end{array}$	$\begin{matrix}2\\100\end{matrix}$		
missing/total bins: % Hit: bin auto[0]	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \\ 395 \end{array}$	2		Covered
missing/total bins: % Hit:	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \end{array}$	$\begin{matrix}2\\100\end{matrix}$	_ _	
missing/total bins: % Hit: bin auto[0] bin auto[1]	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \\ 395 \end{array}$	$\begin{matrix}2\\100\\1\end{matrix}$	_ _ _	Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp	$\begin{array}{c} 2 \\ 0 \\ 100.00\% \\ 395 \\ 810 \\ 92.18\% \end{array}$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \end{array}$	_ _ _ _	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins:	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \end{array} $	_ _ _ _	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins:	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \end{array} $	_ _ _ _	Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit:</pre>	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\% \end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \end{array} $	 	Covered Covered Uncovered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640 \end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \end{array} $	_ _ _ _	Covered Covered Uncovered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\% \end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \end{array} $	 	Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640 \end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \end{array} $	 	Covered Covered Uncovered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ \end{array}$	$ \begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \end{array} $	- - - - - - -	Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640\\20\\0\\5\end{array}$	$ \begin{array}{c} 2\\100\\ 1\\ 1\\ 100\\ 64\\ 64\\ 100\\ 1\\ 1\\ 1 \end{array} $	 	Covered Uncovered Covered Covered ZERO
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640\\20\\0\\5\\5\end{array}$	$ \begin{array}{c} 2\\ 100\\ 1\\ 1\\ 100\\ 64\\ 64\\ 100\\ 1\\ 1\\ 1\\ 1\\ 1 \end{array} $	 	Covered Covered Covered Covered ZERO Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7 \end{array} $	2 100 1 1 100 64 64 100 1 1 1 1		Covered Covered Covered Covered ZERO Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640\\20\\0\\5\\7\\18\end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1		Covered Covered Covered Covered ZERO Covered Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640\\20\\0\\5\\7\\18\\13\end{array}$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\$		Covered Covered Covered ZERO Covered Covered Covered Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215]	$\begin{array}{c} 2\\0\\100.00\%\\395\\810\\92.18\%\\59\\5\\92.18\%\\640\\20\\0\\5\\5\\7\\18\\13\\14\\\end{array}$	$\begin{array}{c} 2 \\ 100 \\ 1 \\ 1 \\ 100 \\ 64 \\ 64 \\ 100 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\$		Covered Covered Covered ZERO Covered Covered Covered Covered Covered Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[5120:6143] bin auto[7168:8191] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4 \end{array} $	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1		Covered Covered Covered ZERO Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[9216:10239] bin auto[10240:11263]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ \end{array} $	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
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missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [14336:15359] bin auto [14384:17407] bin auto [17408:18431] bin auto [19456:20479] bin auto [20480:21503] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [22500:26623] bin auto [22600:26623] bin auto [22600:26623] bin auto [22648:28671] bin auto [27648:28671]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 6\\ 5\\ 13\\ 1\\ 1\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered ZERO Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [6144:7167] bin auto [8192:9215] bin auto [10240:11263] bin auto [10240:11263] bin auto [10240:11263] bin auto [12288:13311] bin auto [14336:15359] bin auto [14336:15359] bin auto [14343:19455] bin auto [18432:19455] bin auto [19456:20479] bin auto [22528:23551] bin auto [22528:23551] bin auto [22528:23551] bin auto [24576:25599] bin auto [26624:27647] bin auto [26624:27647] bin auto [27648:28671] bin auto [27648:28671] bin auto [27648:28671] bin auto [28672:29695] bin auto [29696:30719]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 6\\ 5\\ 13\\ 1\\ 1\\ 1\end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered ZERO Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 14\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 9\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [8192:9215] bin auto [8192:9215] bin auto [9216:10239] bin auto [12248:13311] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [2052227] bin auto [20528:23551] bin auto [20528:23551] bin auto [24576:25599] bin auto [24576:25599] bin auto [26624:27647] bin auto [26624:27647] bin auto [27648:28671] bin auto [28672:29695] bin auto [29696:30719] bin auto [29696:30719] bin auto [30720:31743] bin auto [30720:31743] bin auto [30720:31743] bin auto [31744:32767]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 5\\ 5\\ 13\\ 1\\ 1\\ 9\\ 5\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered ZERO Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[5120:6143] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[10240:11263] bin auto[12248:13311] bin auto[13312:14335] bin auto[14336:15359] bin auto[14336:15359] bin auto[14348:17407] bin auto[19456:20479] bin auto[20480:21503] bin auto[21504:22527] bin auto[22528:23551] bin auto[24576:25599] bin auto[24576:25599] bin auto[24600:26623] bin auto[26624:27647] bin auto[27648:28671] bin auto[27648:28671] bin auto[28672:29695] bin auto[29696:30719] bin auto[30720:317443] bin auto[30720:317445] bin auto[30720:317443] bin auto[30720:317445]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 14\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 6\\ 5\\ 13\\ 1\\ 1\\ 9\\ 5\\ 22\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Uncovered Covered ZERO Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [8192:9215] bin auto [8192:9215] bin auto [9216:10239] bin auto [12248:13311] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [19456:20479] bin auto [20480:21503] bin auto [20480:21503] bin auto [2052227] bin auto [20528:23551] bin auto [20528:23551] bin auto [24576:25599] bin auto [24576:25599] bin auto [26624:27647] bin auto [26624:27647] bin auto [27648:28671] bin auto [28672:29695] bin auto [29696:30719] bin auto [29696:30719] bin auto [30720:31743] bin auto [30720:31743] bin auto [30720:31743] bin auto [31744:32767]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 5\\ 5\\ 13\\ 1\\ 1\\ 9\\ 5\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered ZERO Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[5120:6143] bin auto[5120:6143] bin auto[6144:7167] bin auto[7168:8191] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[10240:11263] bin auto[12248:13311] bin auto[13312:14335] bin auto[14336:15359] bin auto[14336:15359] bin auto[14348:17407] bin auto[19456:20479] bin auto[20480:21503] bin auto[21504:22527] bin auto[22528:23551] bin auto[24576:25599] bin auto[24576:25599] bin auto[24600:26623] bin auto[26624:27647] bin auto[27648:28671] bin auto[27648:28671] bin auto[28672:29695] bin auto[29696:30719] bin auto[30720:317443] bin auto[30720:317445] bin auto[30720:317443] bin auto[30720:317445]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 14\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 1\\ 5\\ 4\\ 4\\ 6\\ 6\\ 5\\ 13\\ 1\\ 1\\ 9\\ 5\\ 22\\ \end{array}$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Uncovered Covered ZERO Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0:1023] bin auto[1024:2047] bin auto[2048:3071] bin auto[3072:4095] bin auto[4096:5119] bin auto[6144:7167] bin auto[6144:7167] bin auto[7168:8191] bin auto[8192:9215] bin auto[9216:10239] bin auto[10240:11263] bin auto[12248:13311] bin auto[12288:13311] bin auto[13312:14335] bin auto[14336:15359] bin auto[17408:18431] bin auto[17408:18431] bin auto[17408:18431] bin auto[2450:2257] bin auto[2252:23551] bin auto[20480:21503] bin auto[25600:26623] bin auto[25600:26623] bin auto[26624:27647] bin auto[27648:28671] bin auto[27648:28671] bin auto[29696:30719] bin auto[30720:31743] bin auto[31744:32767] bin auto[31792:34815] bin auto[33792:34815] bin auto[34816:35839]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 5\\ 4\\ 4\\ 21\\ 0\\ 3\\ 1\\ 5\\ 4\\ 4\\ 21\\ 0\\ 3\\ 1\\ 5\\ 4\\ 7\\ 12\\ 11\\ 0\\ 3\\ 1\\ 1\\ 1\\ 9\\ 5\\ 22\\ 12\\ 7\\ 7\\ 12\\ 12\\ 11\\ 11\\ 21\\ 11\\ 21\\ 11\\ 21\\ 11\\ 21\\ 2$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [1264:12287] bin auto [1288:13311] bin auto [1264:12287] bin auto [1288:13311] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [29480:21503] bin auto [29528:23551] bin auto [23552:24575] bin auto [23552:24575] bin auto [26624:27647] bin auto [26624:27647] bin auto [27648:28671] bin auto [28672:29695] bin auto [29696:30719] bin auto [30720:31743] bin auto [31744:32767] bin auto [31748:3787] bin auto [34816:35839] bin auto [35840:36863]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 7\\ 14$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [6144:7167] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [10240:11263] bin auto [1264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [1436:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [18432:19455] bin auto [20480:21503] bin auto [30720:31743] bin auto [30864:37887]	$\begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 4\\ 21\\ 0\\ 0\\ 3\\ 1\\ 1\\ 4\\ 6\\ 6\\ 5\\ 13\\ 1\\ 4\\ 6\\ 6\\ 6\\ 5\\ 13\\ 1\\ 4\\ 6\\ 6\\ 6\\ 6\\ 5\\ 13\\ 1\\ 4\\ 6\\ 6\\ 6\\ 6\\ 5\\ 13\\ 1\\ 4\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 5\\ 13\\ 1\\ 4\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 7\\ 14\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 7\\ 14\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\ 6\\$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered
missing/total bins: % Hit: bin auto [0] bin auto [1] Coverpoint data_out_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto [0:1023] bin auto [1024:2047] bin auto [2048:3071] bin auto [3072:4095] bin auto [4096:5119] bin auto [5120:6143] bin auto [7168:8191] bin auto [8192:9215] bin auto [9216:10239] bin auto [1264:12287] bin auto [1288:13311] bin auto [1264:12287] bin auto [1288:13311] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [29480:21503] bin auto [29528:23551] bin auto [23552:24575] bin auto [23552:24575] bin auto [26624:27647] bin auto [26624:27647] bin auto [27648:28671] bin auto [28672:29695] bin auto [29696:30719] bin auto [30720:31743] bin auto [31744:32767] bin auto [31748:3787] bin auto [34816:35839] bin auto [35840:36863]	$ \begin{array}{c} 2\\ 0\\ 100.00\%\\ 395\\ 810\\ 92.18\%\\ 59\\ 5\\ 92.18\%\\ 640\\ 20\\ 0\\ 5\\ 7\\ 18\\ 13\\ 14\\ 4\\ 10\\ 15\\ 17\\ 12\\ 11\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 3\\ 1\\ 4\\ 21\\ 0\\ 7\\ 14$	2 100 1 1 100 64 64 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Uncovered Covered

bin auto [38912:39935]	19	1	_	Covered
bin auto $[39936:40959]$	5	1	_	Covered
bin auto $[40960:41983]$	5	1	_	Covered
bin auto [41984:43007]	11	1	_	Covered
bin auto [43008:44031]	13	1	_	Covered
bin auto $[44032:45055]$	9	1	_	Covered
bin auto $[45056:46079]$	2	1	_	Covered
bin auto [46080:47103]	14	1	_	Covered
bin auto [47104:48127]	0	1	_	ZERO
bin auto [48128:49151]	16	1	_	Covered
bin auto [49152:50175]	7	1	_	Covered
bin auto [50176:51199]	4	1	_	Covered
bin auto [51200:52223]	16	1	_	Covered
bin auto [52224:53247]	7	1	_	Covered
bin auto [53248:54271]	0	1	_	ZERO
bin auto [54272:55295]	9	1	_	Covered
bin auto [55296:56319]	3	1	_	Covered
bin auto [56320:57343]	0	1	_	ZERO
bin auto [57344:58367]	9	1	_	Covered
bin auto [57344.58307]	11	1		Covered
bin auto [58308.59391] bin auto [59392:60415]	11	1	_	Covered
			_	Covered
bin auto [60416:61439]	7	1	_	
bin auto [61440:62463]	6	1	_	Covered
bin auto [62464:63487]	3	1	_	Covered
bin auto [63488:64511]	9	1	_	Covered
bin auto [64512:65535]	68	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	582	1	_	Covered
bin auto [1]	623	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	1099	1	_	Covered
bin auto[1]	106	1	_	Covered
Coverpoint full_cp	100.00%	100		Covered
covered/total bins:	2	2		Covered
missing/total bins:	0	$\frac{2}{2}$		
% Hit:	100.00%	100		
			_	Correnad
bin auto [0]	1071	1	_	Covered
bin auto[1]	134	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{2}$	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
$ \text{bin auto} \left[0 \right]$	934	1	_	$\operatorname{Covered}$
bin auto [1]	271	1	_	$\operatorname{Covered}$
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1114	1	_	Covered
bin auto[1]	91	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100^{-}	_	
bin auto[0]	1002	1	_	Covered
bin auto[1]	203	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{1}{2}$	_	covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	$100.00\% \\ 1070$	100	_	Covered
bin auto[0]	135	1		Covered
Cross wr_ack_cross	100.00%	100	_	Covered
		6	_	Covered
covered/total bins:	6	-	_	
missing/total bins:	100.00%	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100	4		0
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	188	1	_	Covered
bin <auto [0]="" [1],="" auto=""></auto>	43	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [1] \rangle$	435	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	144	1	_	Covered
bin < auto[1], auto[0], auto[0] >	179	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [0], \operatorname{auto} [0] >$	216	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin <auto [0],="" [1]="" [1],="" auto=""></auto>	118	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	16	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	$2\overline{3}\overline{1}$	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0] \rangle$	179	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	461	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	200	1	_	Covered
[-],	_~~	_		

Illegel and Impace Direct				
Illegal and Ignore Bins: ignore_bin r_en_actv_wr_full	0			ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} <\! \mathrm{auto} [1] , \mathrm{auto} [1] , \mathrm{auto} [1] >$	25	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right] >$	125	1	_	Covered
bin < auto[1], auto[1], auto[0] >	206	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	513	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$54\\161$	1 1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] > $ Illegal and Ignore Bins:	101	1	_	Covered
ignore_bin_read_nactv_empty	121		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	36	1	_	Covered
$\operatorname{bin} < \operatorname{auto}\left[1\right], \operatorname{auto}\left[0\right], \operatorname{auto}\left[1\right] >$	8	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[1]\;,\mathrm{auto}[1]\;,\mathrm{auto}[0]\!>$	195	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[1]\;,\mathrm{auto}[0]\!>$	546	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right], \operatorname{auto} \left[0 \right] >$	171	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] >$	202	1	_	Covered
Illegal and Ignore Bins:	4.77			0 1
ignore_bin w_en_nactv_almostfull	47	100	_	Occurred
Cross almostempty_cross covered/total bins:	100.00%	100	_	Covered
missing/total bins:	0	6 6		
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	73	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] >$	158	1	_	Covered
bin < auto[0], auto[1], auto[1] >	79	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	500	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	167	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}[0]\;,\mathrm{auto}[0]\;,\mathrm{auto}[0]>$	177	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	51	100	_	Occurred
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0\\100.00\%$	$\frac{6}{100}$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin $<$ auto [1], auto [1] $>$	18	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	213	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	88	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	491	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	179	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	216	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	6	6	_	
missing/total bins:	100.007	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: $bin < auto[1], auto[1] >$	36	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	99	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	195	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	579	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	80	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	216	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

TOTAL COVERGROUP COVERAGE: 99.58% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.58%

▼ Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Typ
/top/cover_n_wr_a	SVA	1	Off	105	1	Unli	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_counte	SVA	✓	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	1	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	1	Off	1075	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_read_p	SVA	✓	Off	6	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_p	SVA	1	Off	38	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	✓	Off	182	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_almost	SVA	1	Off	81	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_full_fla	SVA	1	Off	120	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_empty	SVA	✓	Off	237	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_underfl	SVA	1	Off	112	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_overflo	SVA	✓	Off	67	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_write_a	SVA	1	Off	562	1	Unli	1	100%		/	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover_reset	SVA	√	Off	130	1	Unli	1	100%		√	0	0	0 ns	0	Concurrent	top	Verilog

Figure 4: SVA "Seed4"

3.5 Functional Coverage "seed5" Report

= Instance: /FIFO_coverage_pkg

= Design Unit: work.FIFO_coverage_pkg

Covergroup Coverage:

 Covergroups
 1
 na
 na
 99.25%

 Coverpoints/Crosses
 19
 na
 na
 na

 Covergroup Bins
 190
 181
 9
 95.26%

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.25%	100		Uncovered
<pre>covered/total bins: missing/total bins:</pre>	181 9	$\frac{190}{190}$	_	
% Hit:	95.26%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit: bin auto[0]	$100.00\% \ 124$	$100 \\ 1$	_	Covered
bin auto[1]	1081	1		Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	Covered
bin auto $[0:1023]$ bin auto $[1024:2047]$	$\frac{200}{10}$	1 1	_	Covered Covered
bin auto [2048:3071]	7	1	_	Covered
bin auto [3072:4095]	10	1	_	Covered
bin auto [4096:5119]	16	1	_	Covered
bin auto [5120:6143]	16	1	_	Covered
bin auto [6144:7167]	9	1	_	Covered
bin auto [7168:8191] bin auto [8192:9215]	18 13	1	_	Covered Covered
bin auto $[9216:10239]$	14	1	_	Covered
bin auto [10240:11263]	9	1	_	Covered
bin auto[11264:12287]	11	1	_	Covered
bin auto [12288:13311]	9	1	_	$\operatorname{Covered}$
bin auto [13312:14335]	11	1	_	Covered
bin auto $[14336:15359]$	12	1	_	Covered
bin auto [15360:16383] bin auto [16384:17407]	$\begin{array}{c} 11 \\ 14 \end{array}$	1	_	Covered Covered
bin auto [17408:18431]	7	1	_	Covered
bin auto [18432:19455]	19	1	_	Covered
bin auto [19456:20479]	17	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[20480 \colon\! 21503 \right]$	11	1	_	$\operatorname{Covered}$
bin auto [21504:22527]	16	1	_	Covered
bin auto [22528:23551]	$\frac{8}{14}$	1	_	Covered Covered
$egin{array}{lll} & ext{bin} & ext{auto} \left[23552 {:} 24575 ight] \ & ext{bin} & ext{auto} \left[24576 {:} 25599 ight] \end{array}$	15	1 1	_	Covered
bin auto [25600:26623]	10	1	_	Covered
bin auto [26624:27647]	19	1	_	Covered
bin auto [27648:28671]	27	1	_	Covered
bin auto [28672:29695]	14	1	_	Covered
bin auto [29696:30719]	13	1	_	Covered
bin auto [30720:31743] bin auto [31744:32767]	$16\\12$	1 1	_	Covered Covered
bin auto [31744.32707] bin auto [32768:33791]	9	1		Covered
bin auto [33792:34815]	$1\overline{2}$	1	_	Covered
bin auto [34816:35839]	19	1	_	Covered
bin auto $[35840:36863]$	13	1	_	$\operatorname{Covered}$
bin auto [36864:37887]	20	1	_	Covered
bin auto [37888:38911] bin auto [38912:39935]	13	1 1	_	Covered Covered
bin auto [39936:40959]	9	1	_	Covered
bin auto [40960:41983]	16	1	_	Covered
bin auto [41984:43007]	12	1	_	Covered
bin auto [43008:44031]	16	1	_	Covered
bin auto [44032:45055]	15	1	_	Covered
bin auto [45056:46079]	15	1	_	Covered
bin auto [46080:47103] bin auto [47104:48127]	18 19	1 1	_	Covered Covered
bin auto $[47104:48127]$	19	1	_	Covered
bin auto [49152:50175]	$\frac{10}{12}$	1	_	Covered
bin auto [50176:51199]	14	1	_	Covered
bin auto [51200:52223]	10	1	_	Covered
bin auto [52224:53247]	18	1	_	Covered
bin auto [53248:54271] bin auto [54272:55295]	9	1	_	Covered
bin auto $[54272:55295]$ bin auto $[55296:56319]$	11 15	1 1		Covered Covered
bin auto [56320:57343]	9	1	_	Covered
bin auto [57344:58367]	9	1	_	Covered
bin auto [58368:59391]	17	1	_	Covered
bin auto [59392:60415]	16	1	_	Covered
bin auto [60416:61439]	10	1	_	Covered
bin auto [61440:62463]	15	1	_	Covered
bin auto [62464:63487] bin auto [63488:64511]	$\begin{array}{c} 13 \\ 6 \end{array}$	1	_	Covered Covered
DIII - AULO 10 3 4 5 5 1 0 4 3 1 1 1	О	1	_	Coverea

bin auto $[64512:65535]$	188	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	816	1	_	Covered
bin auto[1]	389	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$\begin{array}{c} 2 \\ 100 \end{array}$	_	
% HIT: bin auto[0]	100.00% 414		_	Covered
bin auto[0]	791	1 1	_	Covered
Coverpoint data_out_cp	85.93%	100	_	Uncovered
covered/total bins:	55	64		Oncovered
missing/total bins:	9	64		
% Hit:	85.93%	100	_	
bin auto [0:1023]	685	1	_	Covered
bin auto $[1024:2047]$	$\frac{3}{2}$	1	_	Covered
bin auto [2048:3071]	0	1	_	ZERO
bin auto [3072:4095]	5	1	_	Covered
bin auto $[4096:5119]$	14	1	_	Covered
bin auto [5120:6143]	15	1	_	Covered
bin auto [6144:7167]	23	1	_	Covered
bin auto [7168:8191]	20	1	_	Covered
bin auto [8192:9215]	6	1	_	$\operatorname{Covered}$
bin auto [9216:10239]	8	1	_	Covered
bin auto [10240:11263]	1	1	_	Covered
bin auto $[11264:12287]$	7	1	_	$\operatorname{Covered}$
bin auto [12288:13311]	0	1	_	ZERO
bin auto $[13312:14335]$	5	1	_	$\operatorname{Covered}$
bin auto $[14336:15359]$	5	1	_	$\operatorname{Covered}$
bin auto $[15360:16383]$	0	1	_	ZERO
bin auto $[16384:17407]$	7	1	_	$\operatorname{Covered}$
bin auto $[17408:18431]$	1	1	_	Covered
bin auto $[18432:19455]$	8	1	_	Covered
bin auto $[19456:20479]$	1	1	_	Covered
bin auto $[20480:21503]$	3	1	_	$\operatorname{Covered}$
$bin auto \left[21504{:}22527\right]$	12	1	_	Covered
bin auto $[22528:23551]$	0	1	_	ZERO
bin auto [23552:24575]	$\frac{2}{2}$	1	_	Covered
bin auto $[24576:25599]$	2	1	_	Covered
bin auto [25600:26623]	17	1	_	Covered
bin auto [26624:27647]	17	1	_	Covered
bin auto [27648:28671]	13	1	_	Covered
bin auto [28672:29695]	9	1	_	Covered
bin auto [29696:30719]	<u>6</u>	1	_	Covered
bin auto [30720:31743]	7	1	_	Covered
bin auto [31744:32767]	$\frac{2}{7}$	1	_	Covered
bin auto [32768:33791]	7	1	_	Covered
bin auto [33792:34815]	0	1	_	ZERO
bin auto [34816:35839]	19	1	_	Covered
bin auto [35840:36863]	1	1	_	Covered
bin auto [36864:37887]	0	1	_	ZERO
bin auto [37888:38911]	5	1	_	Covered
bin auto [38912:39935]	9	1	_	Covered
$egin{array}{ll} { m bin } & { m auto} \left[39936; 40959 ight] \ { m bin } & { m auto} \left[40960; 41983 ight] \end{array}$	3 3	1	_	Covered Covered
bin auto [41984:43007]	3 11	1	_	Covered
bin auto [43008:44031]	17	1	_	Covered
bin auto [44032:45055]	3	1	_	Covered
bin auto [45056:46079]	4	1	_	Covered
bin auto [46080:47103]	$\frac{4}{2}$	1	_	Covered
bin auto [47104:48127]	0	1	_	ZERO
bin auto [48128:49151]	0	1	_	ZERO
bin auto [49152:50175]	$\overset{\circ}{2}$	1	_	Covered
bin auto [50176:51199]	3	1	_	Covered
bin auto [51200:52223]	$\frac{3}{4}$	1	_	Covered
bin auto [52224:53247]	6	1	_	Covered
bin auto [53248:54271]	0	1	_	ZERO
bin auto [54272:55295]	1	1	_	Covered
bin auto [55296:56319]	$\overline{21}$	1	_	Covered
bin auto [56320:57343]	22	1	_	Covered
bin auto [57344:58367]	1	1	_	Covered
bin auto [58368:59391]	10	1	_	Covered
bin auto [59392:60415]	10	1	_	Covered
bin auto [60416:61439]	12	1	_	$\operatorname{Covered}$
bin auto $[61440:62463]$	18	1	_	Covered
bin auto [62464:63487]	2	1	_	Covered
bin auto [63488:64511]	4	1	_	Covered
bin auto [64512:65535]	102	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	612	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[1 \right]$	593	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
${\rm bin \ \ auto} [0]$	1072	1	_	Covered

				~ ,
bin auto[1]	133	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	G 1
bin auto [0]	1047	1	_	Covered
bin auto[1]	158	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	C1
bin auto [0]	922	1	_	Covered
bin auto[1]	$283 \\ 100.00\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
Coverpoint almostfull_cp	$\frac{100.00\%}{2}$		_	Covered
<pre>covered/total bins: missing/total bins:</pre>	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	100.00% 1113	1	_	Covered
bin auto [0]	92	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100		
bin auto $[0]$	100.00% 1021	1	_	Covered
bin auto[0]	184	1		Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	1058	1	_	Covered
bin auto[1]	147	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	200.00,0	200		
$\mathrm{bin} \ <\! \mathrm{auto} \ [1] \ , \ \mathrm{auto} \ [1] \ , \ \mathrm{auto} \ [1] >$	171	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	37	1	_	Covered
bin < auto[0], auto[1], auto[1] >	422	1	_	Covered
bin < auto[0], auto[1], auto[0] >	161	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	181	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [0], \text{auto} [0] \rangle$	233	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[0]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	145	1	_	Covered
bin < auto[0], auto[0], auto[1] >	13	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	208	1	_	Covered
$\mathrm{bin} < \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right] >$	181	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	438	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] , \mathrm{auto} \left[0 \right] >$	220	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross $\operatorname{empty_cross}$	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight], \mathrm{auto} \left[1 ight] >$	20	1	_	$\operatorname{Covered}$
bin < auto[1], auto[0], auto[1] >	133	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	188	1	_	Covered
bin $\langle \text{auto} [0], \text{auto} [1], \text{auto} [0] \rangle$	526	1	_	Covered
bin < auto[1], auto[0], auto[0] >	48	1	_	Covered
	160	1	_	Covered
Illegal and Ignore Bins:	100			0 1
ignore_bin read_nactv_empty	130	100	_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	100.0097	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	20	1		Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[1] > \\ \operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[1] > $	$\frac{30}{7}$	1	_	Covered Covered
	7	1	_	
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] > \\ \operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[1], \operatorname{auto}[0] > $	$\begin{array}{c} 178 \\ 551 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$\begin{array}{c} 551 \\ 174 \end{array}$	1		Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	$\begin{array}{c} 174 \\ 210 \end{array}$	1	_	Covered Covered
Illegal and Ignore Bins:	210	1	_	Covered
ignore_bin_w_en_nactv_almostfull	55			Occurred
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
missing/total bins: % Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin $<$ auto[1], auto[1] $>$	C 4	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	nΔ			
	64 144		_	
	144	1	_ _	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$			_	

$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	504	1	_	Covered
bin $\langle \text{auto} [1], \text{auto} [0], \text{auto} [0] \rangle$	174	1	_	Covered
bin < auto[0], auto[0], auto[0] >	199	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	41		_	Occurred
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	21	1	_	Covered
bin < auto[1], auto[1], auto[0] >	187	1	_	Covered
bin < auto[0], auto[1], auto[1] >	112	1	_	Covered
bin < auto[0], auto[1], auto[0] >	471	1	_	Covered
bin < auto[1], auto[0], auto[0] >	181	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0]$, $\operatorname{auto} [0]$, $\operatorname{auto} [0] >$	233	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[1]$, $\operatorname{auto}[1] >$	42	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[1] >$	105	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	166	1	_	Covered
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [1], \operatorname{auto} [0] >$	583	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	76	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	233	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		_	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.25%	100		Uncovered
covered/total bins:	181	190	_	
missing/total bins:	9	190	_	
% Hit:	95.26%	100	_	C 1
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins: % Hit:	$0\\100.00\%$	$\frac{2}{100}$	_	
bin auto [0]	100.00% 124	100	_	Covered
bin auto[0]	1081	1	_	Covered
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	Covered
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	200	1	_	$\operatorname{Covered}$
bin auto $[1024:2047]$	10	1	_	$\operatorname{Covered}$
bin auto [2048:3071]	7	1	_	$\operatorname{Covered}$
bin auto [3072:4095]	10	1	_	$\operatorname{Covered}$
bin auto [4096:5119]	16	1	_	$\operatorname{Covered}$
bin auto $[5120:6143]$	16	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	9	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	18	1	_	$\operatorname{Covered}$
bin auto [8192:9215]	13	1	_	Covered
bin auto [9216:10239]	14	1	_	Covered
bin auto [10240:11263]	9	1	_	Covered
bin auto [11264:12287]	11	1	_	Covered
bin auto [12288:13311] bin auto [13312:14335]	$\frac{9}{11}$	1	_	Covered Covered
bin auto $[14336:15359]$	$\frac{11}{12}$	1 1	_	Covered
bin auto [14330:15339]	11	1	_	Covered
bin auto [16384:17407]	14	1	_	Covered
bin auto [17408:18431]	7	1	_	Covered
bin auto [18432:19455]	19	1	_	Covered
bin auto [19456:20479]	17	1	_	Covered
bin auto [20480:21503]	11	1	_	$\operatorname{Covered}$
bin auto $[21504:22527]$	16	1	_	$\operatorname{Covered}$
bin auto $[22528:23551]$	8	1	_	$\operatorname{Covered}$
bin auto $[23552:24575]$	14	1	_	$\operatorname{Covered}$
bin auto $[24576:25599]$	15	1	_	$\operatorname{Covered}$
bin auto $[25600:26623]$	10	1	_	$\operatorname{Covered}$
$bin auto \left[26624{:}27647\right]$	19	1	_	$\operatorname{Covered}$
bin auto [27648:28671]	27	1	_	Covered
bin auto [28672:29695]	14	1	_	Covered
bin auto [29696:30719]	13	1	_	Covered
bin auto [30720:31743]	16	1	_	Covered
bin auto [31744:32767]	12	1	_	Covered
bin auto [32768:33791] bin auto [33792:34815]	$9\\12$	1 1	_	Covered Covered
bin auto [34816:35839]	19	1	_	Covered
bin auto [34810:35839]	13	1	_	Covered
bin auto [36864:37887]	20	1	_	Covered
bin auto [37888:38911]	13	1	_	Covered
bin auto [37868.38911]	9	1	_	Covered
bin auto [39936:40959]	9	1		Covered
bin auto [40960:41983]	16	1	_	Covered
	-			

bin auto [41984:43007]	12	1	_	Covered
bin auto [43008:44031]	16	1	_	Covered
bin auto [44032:45055]	15	1	_	Covered
bin auto [45056:46079]	15	1		Covered
			_	
bin auto [46080:47103]	18	1	_	Covered
bin auto [47104:48127]	19	1	_	Covered
bin auto [48128:49151]	10	1	_	Covered
bin auto [49152:50175]	12	1	_	Covered
bin auto [50176:51199]	14	1	_	Covered
bin auto [51200:52223]	10	1	_	Covered
bin auto $[52224:53247]$	18	1	_	Covered
bin auto $[53248:54271]$	9	1	_	Covered
bin auto $[54272 : 55295]$	11	1	_	Covered
bin auto $[55296:56319]$	15	1	_	Covered
bin auto $[56320:57343]$	9	1	_	Covered
bin auto [57344:58367]	9	1	_	Covered
bin auto [58368:59391]	17	1	_	Covered
	16			Covered
bin auto [59392:60415]		1	_	
bin auto $[60416:61439]$	10	1	_	Covered
bin auto $[61440:62463]$	15	1	_	$\operatorname{Covered}$
bin auto [62464:63487]	13	1	_	Covered
bin auto [63488:64511]	6	1	_	Covered
bin auto $[64512:65535]$	188	1	_	Covered
Coverpoint r_en_cp	100.00%	100	_	Covered
			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	816	1	_	Covered
bin auto[1]	389	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
				Covered
covered/total bins:	$\frac{2}{2}$	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	414	1	_	Covered
bin auto [1]	791	1	_	Covered
Coverpoint data_out_cp	85.93%	100	_	Uncovered
				Oncovered
covered/total bins:	55	64	_	
missing/total bins:	9	64	_	
% Hit:	85.93%	100	_	
$\operatorname{bin} \ \operatorname{auto} \left[0:1023\right]$	685	1	_	Covered
bin auto $[1024:2047]$	2	1	_	Covered
bin auto [2048:3071]	0	1	_	ZERO
bin auto [3072:4095]	5	1	_	Covered
i i				
bin auto [4096:5119]	14	1	_	Covered
bin auto [5120:6143]	15	1	_	Covered
bin auto $[6144:7167]$	23	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	20	1	_	Covered
bin auto [8192:9215]	6	1	_	Covered
bin auto $[9216:10239]$	8	1	_	Covered
	1	1		Covered
bin auto [10240:11263]			_	
bin auto $[11264:12287]$	7	1	_	$\operatorname{Covered}$
bin auto $[12288:13311]$	0	1	_	ZERO
bin auto $[13312:14335]$	5	1	_	$\operatorname{Covered}$
bin auto [14336:15359]	5	1	_	Covered
bin auto [15360:16383]	0	1	_	ZERO
bin auto $[16384:17407]$	7	1	_	Covered
· ·				
bin auto [17408:18431]	1	1	_	Covered
bin auto [18432:19455]	8	1	_	Covered
bin auto $[19456:20479]$	1	1	_	$\operatorname{Covered}$
bin auto $[20480:21503]$	3	1	_	Covered
bin auto [21504:22527]	12	1	_	Covered
bin auto $[22528:23551]$	0	1	_	ZERO
bin auto [23552:24575]	$\frac{\sigma}{2}$	1	_	Covered
· ·				
bin auto [24576:25599]	2	1	_	Covered
bin auto [25600:26623]	17	1	_	Covered
bin auto [26624:27647]	17	1	_	Covered
bin auto $[27648:28671]$	13	1	_	Covered
bin auto $[28672:29695]$	9	1	_	Covered
bin auto [29696:30719]	6	1	_	Covered
bin auto [30720:31743]	7	1	_	Covered
bin auto [31744:32767]	$\overset{\prime}{2}$	1	_	Covered
	$\frac{2}{7}$			
bin auto [32768:33791]		1	_	Covered
bin auto [33792:34815]	0	1	_	ZERO
bin auto $[34816:35839]$	19	1	_	Covered
bin auto $[35840:36863]$	1	1	_	Covered
bin auto 36864:37887	0	1	_	ZERO
bin auto [37888:38911]	5	1	_	Covered
bin auto [38912:39935]	9	1	_	Covered
				Covered
bin auto [39936:40959]	3	1	_	
bin auto $[40960:41983]$	3	1	_	Covered
bin auto $[41984:43007]$	11	1	_	Covered
bin auto [43008:44031]	17	1	_	Covered
bin auto $[44032:45055]$	3	1	_	Covered
bin auto [44032.43035]	4	1	_	Covered
bin auto [46080:47103]	2	1	_	Covered
bin auto [47104:48127]	0	1	_	ZERO
bin auto [48128:49151]	0	1	_	ZERO
bin auto [49152:50175]	2	1	_	Covered
bin auto [50176:51199]	3	1	_	Covered
bin auto [51200:52223]	4	1	_	Covered
bin auto [52224:53247]				Covered
	6	1	_	
bin auto $[53248:54271]$	0	1	_	ZERO

bin auto $[54272:55295]$	1	1	_	Covered
bin auto [55296:56319]	21	1	_	Covered
bin auto [56320:57343]	22	1	_	Covered
bin auto [57344:58367]	1	1	_	Covered
bin auto [58368:59391] bin auto [59392:60415]	10 10	1 1	_	Covered Covered
bin auto [60416:61439]	12	1	_	Covered
bin auto [61440:62463]	18	1	_	Covered
bin auto [62464:63487]	$\frac{10}{2}$	1	_	Covered
bin auto [63488:64511]	4	1	_	Covered
bin auto [64512:65535]	102	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	612	1	_	Covered
bin auto[1]	593	1	_	Covered
Coverpoint overflow_cp	100.00%	100	_	Covered
covered/total bins:	$\frac{2}{0}$	$\frac{2}{2}$	_	
missing/total bins: % Hit:	100.00%	100	_	
bin auto[0]	100.00% 1072	100		Covered
bin auto[0]	133	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1047	1	_	Covered
bin auto[1]	158	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{2}{2}$	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	Covered
$egin{array}{ll} egin{array}{ll} egi$	$922 \\ 283$	1 1	_	Covered
Coverpoint almostfull_cp	100.00%	100		Covered
covered/total bins:	$\frac{100.0076}{2}$	2		Covered
missing/total bins:	0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	1113	1	_	Covered
bin auto [1]	92	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	1021	1	_	Covered
bin auto[1]	184	1	_	Covered
Coverpoint underflow_cp	100.00%	100 2	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	0	$\frac{2}{2}$		
% Hit:	100.00%	100		
bin auto[0]	105.00% 1058	1	_	Covered
bin auto[1]	147	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	171	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	37	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	$422 \\ 161$	1 1	_	Covered Covered
$egin{aligned} ext{bin } & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	181	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	$\frac{101}{233}$	1	_	Covered
Illegal and Ignore Bins:		-		00.0104
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	1 4 2	1		Ca 1
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	$145 \\ 13$	1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[1] \rangle$	$\begin{array}{c} 13 \\ 208 \end{array}$	1	_	Covered
$egin{aligned} ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	208 181	1 1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	438	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	$\frac{130}{220}$	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
$Cross\ empty_cross$	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	100.0007	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: bin < auto[1], auto[1] >	20	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	133	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	188	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	526	1	_	Covered
bin < auto[1], auto[0], auto[0] >	48	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	160	1	_	Covered
Illegal and Ignore Bins:				

ignore_bin read_nactv_empty	130		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6		
% Hit:	100.00%	100		
Auto, Default and User Defined Bins:	100.0070	100	_	
·	30	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	30 7			Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	·	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	178	1	_	
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	551	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	174	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ >	210	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	55	100	_	Occurred
Cross almostempty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] > $	64	1	_	Covered
$\mathrm{bin} < \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[0 ight] >$	144	1	_	$\operatorname{Covered}$
$\mathrm{bin} < \mathrm{auto}\left[0 ight], \mathrm{auto}\left[1 ight], \mathrm{auto}\left[1 ight] >$	79	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0 ight], \operatorname{auto} \left[1 ight], \operatorname{auto} \left[0 ight] >$	504	1	_	Covered
$\operatorname{bin}\ < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[0 ight]>$	174	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0 \right], \operatorname{auto} \left[0 \right], \operatorname{auto} \left[0 \right] >$	199	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	41		_	Occurred
Cross overflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	21	1	_	Covered
bin < auto[1], auto[1], auto[0] >	187	1	_	Covered
bin < auto[0], auto[1], auto[1] >	112	1	_	Covered
bin < auto[0], auto[1], auto[0] >	471	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	181	1	_	Covered
bin $<$ auto [0], auto [0], auto [0] $>$	233	1	_	Covered
Illegal and Ignore Bins:	200	-		00.0104
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross underflow_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto[1], auto[1]="" auto[1],=""></auto[1],>	42	1		Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	105	1		Covered
	166	1		Covered
$egin{aligned} ext{bin } < & ext{auto} [1] \ , & ext{auto} [0] > \ & ext{bin } < & ext{auto} [0] \ , & ext{auto} [1] \ , & ext{auto} [0] > \end{aligned}$	583	1	_	Covered
bin $<$ auto [0], auto [1], auto [0] $>$ bin $<$ auto [1], auto [0], auto [0] $>$	76	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	$\frac{76}{233}$	1	_	Covered
	400	1	_	Covered
Illegal and Ignore Bins:	0			ZERO
ignore_bin r_en_nactv_wr_ack	0		_	ZEIO

TOTAL COVERGROUP COVERAGE: 99.25% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.25%

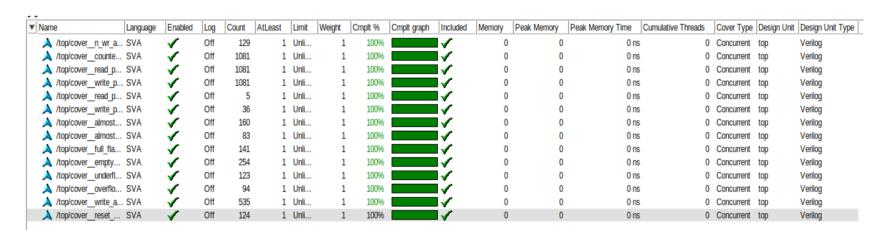


Figure 5: SVA "Seed5"

4 Code Coverage Report

4.1 Code Coverage "seed1" Report

Coverage Report by DU with details

= Design Unit: work.FIFO				
Branch Coverage: Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	$\phantom{aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa$	25	0	100.00%

```
Line
                Item
                                           Count
                                                     Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                           -----IF Branch-
   13
                                            1329
                                                     Count coming in to IF
   13
                   1
                                             261
                                                        if (!fifo_intf.rst_n) begin
                                             630
                                                        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
   18
                   1
                                             438
                                                        else begin
Branch totals: 3 hits of 3 branches = 100.00%
                                 ----IF Branch-
                                             438
                                                     Count coming in to IF
                                                           if (fifo_intf.full & fifo_intf.wr_en)
   25
                                             85
   27
                   1
                                             353
Branch totals: 2 hits of 2 branches = 100.00%
                                 ----IF Branch--
                                            1329
                                                     Count coming in to IF
                   1
                                             261
                                                        if (!fifo_intf.rst_n) begin
   33
                                             237
                                                        else if (fifo_intf.rd_en && count != 0) begin
   38
                   1
                   1
                                             831
                                                        else begin
Branch totals: 3 hits of 3 branches = 100.00%
                                   -IF Branch-
   43
                                             831
                                                     Count coming in to IF
                                                        if (fifo_intf.empty & fifo_intf.rd_en)
                   1
                                             140
   43
                                             691
                   1
Branch totals: 2 hits of 2 branches = 100.00%
                                   -IF Branch-
                                                     Count coming in to IF
                                           1136
                                                        if (!fifo_intf.rst_n) begin
                   1
                                            254
   51
                 1
                                             882
                                                        else begin
Branch totals: 2 hits of 2 branches = 100.00\%
                                   {
m -IF} {
m Branch}-
                                             882
   55
                                                     Count coming in to IF
                                                                if ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
   55
                   1
                                             439
                                                                else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                   1
                                              70
   57
                                                                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
   59
                   1
                                              15
                                                                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                     All False Count
Branch totals: 5 hits of 5 branches = 100.00%
                                 ---IF Branch--
   66
                                             670
                                                     Count coming in to IF
                                                     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
   66
                  1
                                             34
                                                     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
                                   - IF Branch - 
                                             918
                                                     Count coming in to IF
                                                     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
                                             376
                                                     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
                                             670
                                                     Count coming in to IF
                  1
                                             48
                                                     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                   ^{2}
                                                     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
                                  --IF Branch--
                                             670
                                                     Count coming in to IF
                 1
                                             146
                                                     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                 2
                                             524
                                                     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
    Enabled Coverage
                                  Bins Covered
                                                    Misses Coverage
                                                              92.00\%
    Conditions
                                    25
                                              23
                               =Condition Details=
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
               -Focused Condition View-
                     1 (fifo_intf.wr_en && (count < 8))
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
      Input Term
                   Covered Reason for no coverage
                                                      Hint
  fifo_intf.wr_en
                         Y
                          Y
      (count < 8)
                 Hits FEC Target
                                             Non-masking condition(s)
    Rows:
```

```
Row
                        fifo_intf.wr_en_0
  Row
                        fifo_intf.wr_en_1
                                                (count < 8)
  Row
        3:
                        (count < 8)_0
                                                fifo_intf.wr_en
  Row
                        (count < 8)_{-1}
                                                fifo_intf.wr_en
                -Focused Condition View-
           25 Item
Line
                      1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered
                              Reason for no coverage
                                                         Hint
                               ^{,}\_0 ' not hit
                                                         Hit '_0'
   fifo_intf.full
                           Ν
                           Y
  fifo_intf.wr_en
                        FEC Target
                  Hits
                                                Non-masking condition(s)
     Rows:
        1:
               ***0***
                        fifo_intf.full_0
                                                fifo_intf.wr_en
 Row
                        fifo_intf.full_1
                                                fifo_intf.wr_en
  Row
        2:
                     1
  Row
        3:
                        fifo_intf.wr_en_0
                                                fifo_intf.full
                     1
                        fifo_intf.wr_en_1
                                                fifo_intf.full
  Row
        4:
                     1
                 -Focused Condition View-
Line
           38 Item
                     1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00\%
                              Reason for no coverage
       Input Term
                     Covered
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
     (count != 0)
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
                        FEC Target
                        fifo_intf.rd_en_0
  Row
        1:
                     1
  Row
        2:
                        fifo_intf.rd_en_1
                                                (count != 0)
                        (count != 0)_{-0}
  Row
        3:
                                                fifo_intf.rd_en
                     1
                        (count != 0)_{-1}
                                                fifo_intf.rd_en
  Row
        4:
                 -Focused Condition View-
           43 Item
Line
                       1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered
                              Reason for no coverage
                                                         _{
m Hint}
                               '_{0} not hit
                                                         Hit '_0'
  fifo_intf.empty
                           Ν
  fifo_intf.rd_en
                           Y
                  Hits
                                                Non-masking condition(s)
     Rows:
                        FEC Target
  Row
        1:
               ***0***
                        fifo_intf.empty_0
                                                fifo_intf.rd_en
  Row
        2:
                        fifo_intf.empty_1
                                                fifo_intf.rd_en
  Row
        3:
                        fifo_intf.rd_en_0
                                                fifo_intf.empty
                        fifo_intf.rd_en_1
  Row
                                                fifo_intf.empty
                 -Focused Condition View-
Line
           55 Item
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered
                              Reason for no coverage
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           \mathbf{Y}
   fifo_intf.full
                           Y
                        FEC Target
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
        1:
                        fifo_intf.rd_en_0
                                                (~fifo_intf.full && fifo_intf.wr_en)
  Row
        2:
                        fifo_intf.rd_en_1
  Row
        3:
                        fifo_intf.wr_en_0
                                                ~fifo_intf.rd_en
                        fifo_intf.wr_en_1
                                                (~fifo_intf.full && ~fifo_intf.rd_en)
  Row
        4:
                        fifo_intf.full_0
  Row
        5:
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                        fifo_intf.full_1
                                                (~fifo_intf.rd_en && fifo_intf.wr_en)
                 Focused Condition View-
                          ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         _{
m Hint}
                           Y
  fifo_intf.rd_en
  fifo_intf.wr_en
                           Υ
                           Y
  fifo_intf.empty
                       FEC Target
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
                     1
                        fifo_intf.rd_en_0
        1:
        2:
                                                (~fifo_intf.empty && ~fifo_intf.wr_en)
                        fifo_intf.rd_en_1
 Row
                     1
        3:
                                                (~fifo_intf.empty && fifo_intf.rd_en)
  Row
                     1
                        fifo_intf.wr_en_0
        4:
                     1
                        fifo_intf.wr_en_1
                                                fifo_intf.rd_en
  Row
 Row
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
        5:
                     1
                        fifo_intf.empty_0
        6:
                                                (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
                     1
                        fifo_intf.empty_1
                -Focused Condition View-
```

Condition totals: 3 of 3 input terms covered = 100.00%Input Term CoveredReason for no coverage Hintfifo_intf.rd_en Y fifo_intf.wr_en Y Y fifo_intf.full FEC Target Non-masking condition(s) Rows: $_{
m Hits}$ Row fifo_intf.rd_en_0 1: 1 Row 2:fifo_intf.rd_en_1 (fifo_intf.full && fifo_intf.wr_en) 3: fifo_intf.wr_en_0 fifo_intf.rd_en Row (fifo_intf.full && fifo_intf.rd_en) fifo_intf.wr_en_1 Row 4:(fifo_intf.rd_en && fifo_intf.wr_en) fifo_intf.full_0 Row 5:1 (fifo_intf.rd_en && fifo_intf.wr_en) fifo_intf.full_1 Row 6: 1 -Focused Condition View-61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty) Line Condition totals: 3 of 3 input terms covered = 100.00%Input Term Covered Reason for no coverage Hint $fifo_intf.rd_en$ Y Y fifo_intf.wr_en Y fifo_intf.empty Rows: $_{
m Hits}$ FEC Target Non-masking condition(s) fifo_intf.rd_en_0 Row 1: 1 $fifo_intf.rd_en_1$ 2: (fifo_intf.empty && fifo_intf.wr_en) Row 1 $fifo_intf.wr_en_0$ fifo_intf.rd_en Row 3: $fifo_intf.wr_en_1$ (fifo_intf.empty && fifo_intf.rd_en) Row 4: (fifo_intf.rd_en && fifo_intf.wr_en) Row 5:fifo_intf.empty_0 1 $fifo_intf.empty_1$ (fifo_intf.rd_en && fifo_intf.wr_en) Row 6: 1 -Focused Condition View-66 Item Line $1 \quad (count == 8)$ Condition totals: 1 of 1 input term covered = 100.00% Input Term Covered Reason for no coverage HintY (count == 8)Rows: $_{
m Hits}$ FEC Target Non-masking condition(s) Row 1: 1 $(count = 8)_{-0}$ Row 2: $(count = 8)_{-1}$ Focused Condition View-67 Item 1 $((count = 0) | | \tilde{fifo_intf.rst_n})$ Condition totals: 2 of 2 input terms covered = 100.00% Input Term Covered Reason for no coverage Hint (count = 0)Y Y fifo_intf.rst_n Rows: FEC Target Non-masking condition(s) $_{
m Hits}$ Row 1: $(count = 0)_{-}0$ fifo_intf.rst_n $(count = 0)_{-1}$ Row 2: $\tilde{}$ (count == 0) Row 3: $fifo_intf.rst_n_0$ $fifo_intf.rst_n_1$ Row 4: $\tilde{\ }(\text{count} == 0)$ $\operatorname{Focused}$ Condition View-Line 68 Item 1 (count = (8 - 1)) Condition totals: 1 of 1 input term covered = 100.00%Input Term Covered Reason for no coverage 1)) Hits FEC Target Non-masking condition(s) 1 (count = (8 - 1))_0 -Row 1:Row 2: $(count = (8 - 1))_{-1}$ --Focused Condition View----Line 69 Item $1 \quad (count == 1)$ Condition totals: 1 of 1 input term covered = 100.00% Covered Reason for no coverage Input Term Hint Y (count = 1)Hits FEC Target Rows:Non-masking condition(s) $(count = 1)_{-0}$ Row 1: 2: 1 (count = 1)_1 Row

1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)

Line

Statement Coverage:

Enabled Coverage

Statements

Bins
Hits
Misses
Coverage

28
28
0
100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

```
Line
                  Item
                                               Count
                                                          Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                          module FIFO(FIFO_IF.DUT fifo_intf);
    2
                                                          parameter FIFO_WIDTH = 16;
                                                          parameter FIFO_DEPTH = 8;
    3
    4
                                                          localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
    6
                                                          reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
    7
    8
    9
                                                          reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
                                                          reg [max_fifo_addr:0] count;
    10
    11
    12
                     1
                                                1329
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
                                                             if (!fifo_intf.rst_n) begin
    13
                     1
                                                 261
                                                                      wr_ptr \le 0;
    14
                                                 261
                                                                      fifo_intf.wr_ack \ll 0;
                     1
    15
                                                 261
                                                                      fifo_intf.overflow \le 0;
    16
                     1
    17
                                                             _{\mathrm{end}}
                                                             else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                                                                      mem[wr_ptr] \le fifo_intf.data_in;
                     1
                                                 630
    19
    20
                     1
                                                 630
                                                                      fifo_intf.wr_ack \ll 1;
    21
                     1
                                                 630
                                                                      wr_ptr \le wr_ptr + 1;
    22
                                                             _{\mathrm{end}}
                                                             else begin
    23
                                                                      fifo_intf.wr_ack <= 0;
                     1
                                                 438
    24
                                                                      if (fifo_intf.full & fifo_intf.wr_en)
    25
                                                                               fifo_intf.overflow <= 1;
    ^{26}
                     1
                                                  85
    27
                                                                      else
    28
                     1
                                                 353
                                                                               fifo_intf.overflow <= 0;
    29
                                                             _{\mathrm{end}}
    30
                                                          end
    31
                                                1329
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    32
                     1
                                                             if (!fifo_intf.rst_n) begin
    33
    34
                     1
                                                 261
                                                                      rd_ptr \ll 0;
                                                                      fifo_intf.underflow <= 0;
    35
                     1
                                                 261
                                                                      fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    36
                     1
                                                 261
    37
    38
                                                             else if (fifo_intf.rd_en && count != 0) begin
    39
                                                 237
                                                                      fifo_intf.data_out <= mem[rd_ptr];
                     1
                                                 237
                                                                      rd_ptr \ll rd_ptr + 1;
    40
    41
                                                             \operatorname{end}
                                                             else begin
    42
    43
                                                                      if (fifo_intf.empty & fifo_intf.rd_en)
                     1
                                                 140
                                                                               fifo_intf.underflow \ll 1;
    44
                                                                      else
    45
    46
                     1
                                                 691
                                                                               fifo_intf.underflow \le 0;
    47
                                                             _{\mathrm{end}}
    48
                                                          end
    49
    50
                     1
                                                1136
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    51
                                                             if (!fifo_intf.rst_n) begin
    52
                     1
                                                 254
                                                                      count \ll 0;
    53
                                                             end
    54
                                                             else begin
                                                                               (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
    55
                                                                      i f
                                                                               count \ll count + 1;
    56
                     1
                                                 439
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    57
                                                  70
                                                                               count \ll count - 1;
    58
                     1
                                                                      else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
    59
    60
                                                  15
                                                                               count \le count - 1;
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                     1
                                                  39
                                                                               count \le count + 1;
    62
    63
                                                             \operatorname{end}
    64
                                                          end
    65
                     1
                                                          assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                                                 671
                     1
                                                          assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
    67
                                                 919
                                                          assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     1
                                                 671
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                     1
                                                 671
Toggle Coverage:
    Enabled Coverage
                                     Bins
                                                Hits
                                                         Misses
                                                                 Coverage
                                       20
                                                  20
                                                              0
                                                                   100.00\%
    Toggles
```

Toggle Coverage for Design Unit work.FIFO

=Toggle Details=

Node	1H->0L	0L->1H	"Coverage"
$\begin{array}{c} \overline{\text{count} \left[0-3\right]} \\ \text{rd-ptr} \left[0-2\right] \\ \text{wr-ptr} \left[0-2\right] \end{array}$	1	1	100.00
	1	1	100.00
	1	1	100.00

 $\begin{array}{llll} {\rm Total~Node~Count} & = & 10 \\ {\rm Toggled~Node~Count} & = & 10 \\ {\rm Untoggled~Node~Count} & = & 0 \end{array}$

Toggle~Coverage~=~100.00%~(20~of~20~bins)

Branch totals: 2 hits of 2 branches = 100.00%

Total Coverage By Design Unit (filtered view): 98.00%

${\bf 4.2}\quad {\bf Code}\ {\bf Coverage}\ "{\bf seed 2"}\ {\bf Report}$

Coverage Report by DU with details

— Design Unit	· work FIFO					=
Branch Coverage	:					
Enabled Cov	verage	Bins	Hits	Misses	Coverage	
Branches		25	25	0	100.00%	
		Branch Det	ails			
Branch Coverage	for Design	Unit work.FIFO				
Line	Item		Count	Source		
File /home/ta	re/Desktop/s	syn_fifo/uvm_ve IF Bra:		n/FIFO_v1	.0.0.sv	
13 13	1	II Dia	1315 240		coming in to IF	
18	1		612		(!fifo_intf.rst_n) be e if (fifo_intf.wr_en	&& count < FIFO_DEPTH) begin
23 Branch totals:	1 3 hits of 3	branches = 100.0	$\frac{463}{00\%}$	els	e begin	
		IF Bra	nch			_
$\begin{array}{c} 25 \\ 25 \end{array}$	1		$\frac{463}{115}$	Count	coming in to IF	.11 & fifo_intf.wr_en)
27	1		348		else	ir & irro_rmtr.wr_on)
Branch totals:	2 hits of 2	branches $= 100.0$				
33		IF Bra	nch 1315	Count	coming in to IF	
$\frac{33}{38}$	1		$\frac{240}{214}$		(!fifo_intf.rst_n) be	
42	1		861		e if (fifo_intf.rd_en e begin	&& count != 0) begin
Branch totals:	3 hits of 3	branches = 100.0	00%			
43		IF Bra	nch——— 861	Count	coming in to IF	
$\begin{array}{c} 43 \\ 45 \end{array}$	1		$\begin{array}{c} 129 \\ 732 \end{array}$		9	apty & fifo_intf.rd_en)
	2 hits of 2	branches = 100.0			erse	
		IF Bra	nch			_
51 51	1		$\begin{array}{c} 1126 \\ 233 \end{array}$		coming in to IF (!fifo_intf.rst_n) be	gin
54	1	1 1 100.0	893		e begin	0
Branch totals:	2 hits of 2	branches = 100.0				
55		IF Braz	nch——— 893	Count	coming in to IF	_
55 57	1		$\begin{array}{c} 451 \\ 60 \end{array}$		if ({{fifo	_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
59	1		25		else if (({fifo	
61	1		$\begin{array}{c} 32 \\ 325 \end{array}$	All Fa	else if (({ fifo	_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
Branch totals:	5 hits of 5	branches = 100.0				
		IF Bra				_
66 66	1		$\frac{665}{50}$		coming in to IF fifo_intf.full = (co	unt = $FIFO_DEPTH$)? 1 : 0;
66 Branch totals:	2 hits of 2	branches = 100.0	615			unt = $FIFO_DEPTH$)? 1 : 0;
Dianen totals:	2 H165 O1 Z					
67		IF Bra	nch 885	Count	coming in to IF	
67 67	$\frac{1}{2}$		$\frac{328}{557}$	assign	$fifo_intf.empty = (c$	$ount = 0 \mid fifo_intf.rst_n ? 1 : 0;$ $ount = 0 \mid fifo_intf.rst_n ? 1 : 0;$
		branches = 100.0		assign	$1110_{-1} \text{ inti.empty} = (c$	$ount = 0 \mid !fifo_intf.rst_n)? 1 : 0;$
		IF Bra	nch			_
68 68	1		$\frac{665}{68}$		coming in to IF	$= (count = FIFO_DEPTH-1)? 1 : 0;$
68	2		597			$= (count = FIFO_DEPTH-1)? 1 : 0;$ $= (count = FIFO_DEPTH-1)? 1 : 0;$
D 1	0 1 : 4 f 0	branches - 1000	(A) U7			

```
69
                                                665
                                                        Count coming in to IF
                     1
                                                120
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                     2
                                                545
    69
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                            Covered
                                                       Misses
                                                                Coverage
                                                            2
                                                                  92.00\%
    Conditions
                                      25
                                                 23
                                 =Condition Details:
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
                     1 (fifo_intf.wr_en && (count < 8))
Line
           18 Item
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.wr_en
                           Y
      (count < 8)
                           Y
                       FEC Target
     Rows:
                                                Non-masking condition(s)
                  _{
m Hits}
 Row
        1:
                     1
                        fifo_intf.wr_en_0
                        fifo_intf.wr_en_1
  Row
        2:
                                                (count < 8)
                     1
                        (count < 8)_{-0}
  Row
        3:
                                                fifo_intf.wr_en
                     1
                                                fifo_intf.wr_en
        4:
                        (count < 8)_{-1}
  Row
                     1
                 -Focused Condition View-
Line
           25 Item
                     1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
   fifo_intf.full
                           Ν
                               '_{0} not hit
                                                         Hit '_0'
                           Y
  fifo_intf.wr_en
                  _{
m Hits}
                        FEC Target
                                               Non-masking condition(s)
     Rows:
                        fifo_intf.full_0
  Row
        1:
               ***0***
                                                fifo_intf.wr_en
                        fifo_intf.full_1
  Row
        2:
                                                fifo_intf.wr_en
  Row
        3:
                        fifo_intf.wr_en_0
                                                fifo_intf.full
                        fifo_intf.wr_en_1
                                                fifo_intf.full
  Row
        4:
                 -Focused Condition View-
           38 Item
                      1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.rd_en
                           Y
                           Y
     (count != 0)
     Rows:
                  _{
m Hits}
                       FEC Target
                                                Non-masking condition(s)
  Row
        1:
                        fifo_intf.rd_en_0
                        fifo_intf.rd_en_1
  Row
        2:
                                                (count != 0)
  Row
        3:
                        (count != 0)_{-0}
                                                fifo_intf.rd_en
  Row
        4:
                        (count != 0)_{-1}
                                                fifo_intf.rd_en
                 -Focused Condition View-
Line
           43 Item
                     1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00\%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.empty
                                _{-0}, not hit
                           Y
  fifo_intf.rd_en
                        FEC Target
                  _{
m Hits}
                                                Non-masking condition(s)
     Rows:
               ***0***
                        fifo_intf.empty_0
  Row
        1:
                                                fifo_intf.rd_en
                        fifo_intf.empty_1
                                                fifo_intf.rd_en
        2:
  Row
                     1
                        fifo_intf.rd_en_0
        3:
                                                fifo_intf.empty
  Row
                     1
                        fifo_intf.rd_en_1
        4:
                     1
                                                fifo_intf.empty
  Row
                 -Focused Condition View-
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
  fifo_intf.wr_en
                           Y
   fifo_intf.full
```

-IF Branch-

```
Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
  Row
        1:
                     1
                         fifo_intf.rd_en_0
                                                 (~fifo_intf.full && fifo_intf.wr_en)
  Row
        2:
                     1
                         fifo_intf.rd_en_1
                                                 \tilde{f} if o_intf.rd_en
  Row
        3:
                     1
                         fifo_intf.wr_en_0
                                                 (~fifo_intf.full && ~fifo_intf.rd_en)
                         fifo_intf.wr_en_1
  Row
        4:
                     1
                         fifo_intf.full_0
  Row
        5:
                     1
                                                 (~fifo_intf.rd_en && fifo_intf.wr_en)
                                                 (\tilde{fifo_intf.rd_en} \&\& fifo_intf.wr_en)
  Row
        6:
                     1
                         fifo_intf.full_1
                 -Focused Condition View-
           57 Item
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
                               Reason for no coverage
       Input Term
                     Covered
                                                           _{\mathrm{Hint}}
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
  Row
        1:
                     1
                         fifo_intf.rd_{en_0}
                         fifo_intf.rd_en_1
                                                 (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
        2:
                     1
                                                 (~fifo_intf.empty && fifo_intf.rd_en)
  Row
        3:
                         fifo_intf.wr_en_0
                     1
                         fifo_intf.wr_en_1
                                                 fifo_intf.rd_en
  Row
        4:
                     1
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
                         fifo_intf.empty_0
  Row
        5:
                     1
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
        6:
                         fifo_intf.empty_1
  Row
                     1
                 -Focused Condition View—
Line
           59 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            Y
   fifo_intf.full
                            Y
                        FEC Target
                                                 Non-masking condition(s)
     Rows:
                  Hits
  Row
        1:
                     1
                         fifo_intf.rd_en_0
  Row
         2:
                         fifo_intf.rd_en_1
                                                 (fifo_intf.full && fifo_intf.wr_en)
                                                 fifo_intf.rd_en
  Row
        3:
                         fifo_intf.wr_en_0
                                                 (fifo_intf.full && fifo_intf.rd_en)
  Row
        4:
                         fifo_intf.wr_en_1
  Row
        5:
                         fifo_intf.full_0
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                         fifo_intf.full_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
                 -Focused Condition View-
Line
           61 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered
                               Reason for no coverage
                                                           Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
  fifo_intf.empty
                            Y
     Rows:
                        FEC Target
                                                 Non-masking condition(s)
                  _{
m Hits}
  Row
         1:
                         fifo_intf.rd_en_0
  Row
                         fifo_intf.rd_en_1
                                                 (fifo_intf.empty && fifo_intf.wr_en)
  Row
        3:
                         fifo_intf.wr_en_0
                                                 fifo_intf.rd_en
                                                 (fifo_intf.empty && fifo_intf.rd_en)
        4:
                         fifo_intf.wr_en_1
  Row
        5:
                         fifo_intf.empty_0
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                         fifo_intf.empty_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 Focused Condition View-
                       1 \quad (count == 8)
Line
           66 Item
Condition totals: 1 of 1 input term covered = 100.00\%
    Input Term
                  Covered Reason for no coverage
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
  Row
        1:
                     1
                        (count = 8)_{-}0
        2:
                        (count = 8)_{-1}
 Row
                     1
                 \operatorname{-Focused} Condition View\operatorname{-}
                       1 ((count = 0) || \tilde{fifo_intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          \operatorname{Hint}
     (count = 0)
                            Y
                            Y
  fifo_intf.rst_n
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
                                                 fifo_intf.rst_n
  Row
                        (count = 0)_{-0}
        1:
                     1
        2:
                         (count = 0)_{-1}
 Row
                     1
```

```
fifo_intf.rst_n_0
  Row
                                                   \tilde{} (count == 0)
                          fifo_intf.rst_n_1
  Row
                                                    \tilde{\phantom{a}}(\text{count} == 0)
                 —Focused Condition View—
                      1 (count = (8 - 1))
            68 Item
Line
Condition totals: 1 of 1 input term covered = 100.00%
           Input Term
                         Covered Reason for no coverage
                                                                Hint
  (count = (8 - 1))
                                Y
     Rows:
                   Hits
                         FEC Target
                                                   Non-masking condition(s)
  Row
         1:
                          (count = (8 - 1))_{-0}
                      1
                          (count = (8 - 1))_{-1}
  Row
         2:
                  -Focused Condition View-
            69 Item
                       1 \quad (count == 1)
Line
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                   Covered Reason for no coverage
                                                         Hint
                         Υ
  (count == 1)
     Rows:
                   Hits FEC Target
                                                   Non-masking condition(s)
         1:
                         (count = 1)_{-0}
  Row
                      1
                          (count = 1)_{-1}
  Row
         2:
                      1
Statement Coverage:
    Enabled Coverage
                                      _{\mathrm{Bins}}
                                                  Hits
                                                           _{
m Misses}
                                                                   Coverage
    Statements
                                                                     100.00\%
                                         28
                                                    28
                                                                0
                                    =Statement Details:
Statement Coverage for Design Unit work.FIFO —
    Line
                   Item
                                                 Count
                                                            Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                            module FIFO(FIFO_IF.DUT fifo_intf);
                                                            parameter FIFO_WIDTH = 16:
    2
                                                            parameter FIFO_DEPTH = 8;
    3
                                                            localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
                                                            reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
                                                            reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
                                                            reg [max_fifo_addr:0] count;
    10
    11
                      1
                                                  1315
                                                            always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    12
                                                                if (!fifo_intf.rst_n) begin
    13
    14
                                                   240
                                                                         wr_ptr \ll 0;
                                                   240
                                                                         fifo_intf.wr_ack \ll 0;
    15
                      1
    16
                                                   240
                                                                         fifo_intf.overflow <= 0;
    17
                                                               else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
    19
                      1
                                                   612
                                                                        mem[wr_ptr] <= fifo_intf.data_in;
    20
                      1
                                                   612
                                                                        fifo_intf.wr_ack \ll 1;
    21
                                                   612
                                                                         wr_ptr \le wr_ptr + 1;
    22
                                                               \operatorname{end}
    23
                                                               else begin
    24
                      1
                                                   463
                                                                         fifo_intf.wr_ack \ll 0;
    25
                                                                         if (fifo_intf.full & fifo_intf.wr_en)
    ^{26}
                      1
                                                   115
                                                                                  fifo_intf.overflow <= 1;
    27
                                                                         else
    28
                      1
                                                   348
                                                                                  fifo_intf.overflow \ll 0;
    ^{29}
                                                               end
    30
                                                            end
    31
                                                            always \ @(posedge \ fifo\_intf.clk \ or \ negedge \ fifo\_intf.rst\_n) \ begin
    32
                      1
                                                  1315
    33
                                                               if (!fifo_intf.rst_n) begin
                      1
                                                   240
    34
                                                                        rd_ptr \le 0;
    35
                      1
                                                   240
                                                                         fifo_intf.underflow \ll 0;
                                                                         fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    36
                      1
                                                   240
    37
                                                               \operatorname{end}
                                                               else if (fifo_intf.rd_en && count != 0) begin
    38
                      1
                                                   214
                                                                         fifo_intf.data_out <= mem[rd_ptr];
    39
    40
                      1
                                                   214
                                                                         rd_ptr \ll rd_ptr + 1;
    41
                                                               \operatorname{end}
                                                               else begin
    42
                                                                         if (fifo_intf.empty & fifo_intf.rd_en)
    43
                      1
                                                   129
                                                                                  fifo_intf.underflow <= 1;
    44
    45
                                                                         else
                                                                                  \label{eq:fifo_intf.underflow} \text{fifo_intf.underflow} <= 0;
                      1
                                                   732
    46
    47
                                                               _{\mathrm{end}}
                                                            end
    48
```

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin

1126

49

50

1

```
if (!fifo_intf.rst_n) begin
    51
                     1
                                                233
    52
                                                                    count \ll 0;
    53
                                                            end
                                                            else begin
    54
                                                                             (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10) \&\& !fifo\_intf.fu
    55
                                                                     i f
                     1
                                                451
                                                                             count \le count + 1;
    56
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
    57
                                                 60
                     1
    58
                                                                             count \ll count - 1;
                                                                    else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
    59
                     1
                                                 25
    60
                                                                             count \ll count - 1;
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                                                 32
                     1
    62
                                                                             count \ll count + 1;
    63
                                                            end
    64
                                                        end
    65
                     1
                                                666
                                                         assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                                                886
                                                         assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
    67
                     1
                                                666
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                     1
    68
                     1
                                                666
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
Toggle Coverage:
    Enabled Coverage
                                    _{
m Bins}
                                                                Coverage
                                               Hits
                                                       _{
m Misses}
```

Toggle Details—

20

20

Toggle Coverage for Design Unit work.FIFO

	Node	1H—>0L	0L—>1H	"Coverage"
count	[0-3]	1	1	100.00
rd_ptr	[0-2]	1	1	100.00
wr_ptr	[0-2]	1	1	100.00

100.00%

0

Toggles

Toggle Coverage = 100.00% (20 of 20 bins)

Total Coverage By Design Unit (filtered view): 98.00%

4.3 Code Coverage "seed3" Report

Coverage Report by DU with details

anch Coverage:				
Enabled Coverage	Bins	$_{ m Hits}$	Misses	$\operatorname{Coverage}$
Branches	25	$\phantom{00000000000000000000000000000000000$	0	100.00%

Branch Coverage for Design Unit work.FIFO

Liı	ne Item	1	Count	Source
File	/home/tare/De	- sktop/syn_fifo/u		$n/FIFO_v1.0.0.sv$
		I	F Branch———	
13			1312	Count coming in to IF
13		1	230	if (!fifo_intf.rst_n) begin
18		1	624	else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
23		1	458	else begin
Branch	totals: 3 hits	s of 3 branches =	= 100.00%	
		I	F Branch———	
25			458	Count coming in to IF
25		l	84	if (fifo_intf.full & fifo_intf.wr_en)
27		l	374	else
Branch	totals: 2 hits	s of 2 branches =	= 100.00%	
		I	F Branch———	
33			1312	Count coming in to IF
33		1	230	if (!fifo_intf.rst_n) begin
38		l	243	else if (fifo_intf.rd_en && count != 0) begin
42		1	839	else begin
Branch	totals: 3 hits	s of 3 branches =	= 100.00%	
		I	F Branch——	
43			839	Count coming in to IF
43		1	131	if (fifo_intf.empty & fifo_intf.rd_en)
45		1	708	else
${\bf Branch}$	totals: 2 hits	s of 2 branches =	= 100.00%	
			F Branch———	
51		-	1103	Count coming in to IF
51	-	1	219	if (!fifo_intf.rst_n) begin
3.				(,,

```
Branch totals: 2 hits of 2 branches = 100.00\%
                                     -IF Branch
    55
                                               884
                                                        Count coming in to IF
                                                                            (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
    55
                    1
                                               443
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                                                77
    57
                    1
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                    1
                                                15
                                                30
                                                                   else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                    1
                                                        All False Count
                                               319
Branch totals: 5 hits of 5 branches = 100.00\%
                                   ——IF Branch-
    66
                                               658
                                                        Count coming in to IF
                                                37
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                    2
                                               621
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                     –IF Branch-
                                               872
                                                        Count coming in to IF
    67
                    1
                                               325
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                    2
                                               547
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
Branch totals: 2 hits of 2 branches = 100.00\%
                                    --IF Branch-
                                               658
    68
                                                        Count coming in to IF
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                    1
                                                59
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                    2
                                               599
Branch totals: 2 hits of 2 branches = 100.00%
                                    —IF Branch-
    69
                                               658
                                                        Count coming in to IF
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                    1
                                               118
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                    ^{2}
                                               540
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                                              Coverage
                                    _{\mathrm{Bins}}
                                           Covered
                                                       Misses
    Conditions
                                      25
                                                23
                                                            2
                                                                 92.00\%
                                 =Condition Details=
Condition Coverage for Design Unit work.FIFO —
 File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
                     1 (fifo_intf.wr_en && (count < 8))
           18 Item
Condition totals: 2 of 2 input terms covered = 100.00%
                    Covered Reason for no coverage
       Input Term
  fifo_intf.wr_en
                           Y
                           Y
      (count < 8)
                 Hits FEC Target
     Rows:
                                               Non-masking condition(s)
 Row
                        fifo_intf.wr_en_0
 Row
                        fifo_intf.wr_en_1
                                               (count < 8)
 Row
        3:
                        (count < 8)_{-0}
                                               fifo_intf.wr_en
 Row
                        (count < 8)_{-1}
                                               fifo_intf.wr_en
                -Focused Condition View-
           25 Item
                    1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00\%
       Input Term
                     Covered Reason for no coverage
                                                         \operatorname{Hint}
                              ^{\prime}_0 ^{\prime} not hit
                                                         Hit '_0'
   fifo_intf.full
  fifo_intf.wr_en
                 Hits FEC Target
                                               Non-masking \ condition \, (\, s \, )
     Rows:
                        fifo_intf.full_0
 Row
                                               fifo_intf.wr_en
        2:
                        fifo_intf.full_1
 Row
                                               fifo_intf.wr_en
 Row
        3:
                        fifo_intf.wr_en_0
                                               fifo_intf.full
        4:
                        fifo_intf.wr_en_1
                                               fifo_intf.full
 Row
                     1
                -Focused Condition View—
                      1 (fifo_intf.rd_en && (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
                           Y
  fifo_intf.rd_en
                           Y
     (count != 0)
                 Hits FEC Target
                                               Non-masking condition(s)
     Rows:
                        fifo_intf.rd_en_0
 Row
                     1
        1:
        2:
                        fifo_intf.rd_en_1
                                               (count != 0)
 Row
                     1
```

54

1

884

else begin

```
Row
                         (count != 0)_{-1}
                                                  fifo_intf.rd_en
                 -Focused Condition View-
            43 Item
Line
                       1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00\%
       Input Term
                      Covered
                               Reason for no coverage
                                                            Hint
  fifo_intf.empty
                                                            Hit '_0'
                            Ν
                                '_{-0} not hit
                            Y
  fifo_intf.rd_en
     Rows:
                  _{
m Hits}
                         FEC Target
                                                  Non-masking condition(s)
  Row
                                                  fifo_intf.rd_en
               ***0***
                         fifo_intf.empty_0
        1:
        2:
                         fifo_intf.empty_1
                                                  fifo_intf.rd_en
  Row
                      1
                         fifo_intf.rd_en_0
                                                  fifo_intf.empty
  Row
        3:
                      1
                         fifo_intf.rd_en_1
  Row
         4:
                      1
                                                  fifo_intf.empty
                 -Focused Condition View-
Line
            55 Item
                        1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered
                               Reason for no coverage
                                                            Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
   f\,i\,f\,o\,{\scriptscriptstyle \,\_}\,i\,n\,t\,f\,\,.\,\,f\,u\,l\,l
                            Y
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                  _{
m Hits}
                                                  (~fifo_intf.full && fifo_intf.wr_en)
  Row
        1:
                      1
                         fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
  Row
         2:
                      1
  Row
                         fifo_intf.wr_en_0
                                                  ~ fifo_intf.rd_en
         3:
  Row
         4:
                         fifo_intf.wr_en_1
                                                  (~fifo_intf.full && ~fifo_intf.rd_en)
                      1
                         fifo_intf.full_0
                                                  (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
                      1
         6:
                         fifo_intf.full_1
                                                  (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                      1
                 \operatorname{-Focused} Condition View\operatorname{-}
Line
            57 Item
                        1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                            Hint
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            Y
                            Y
  fifo_intf.empty
     Rows:
                   Hits
                         FEC Target
                                                  Non-masking condition(s)
  Row
         1:
                         fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
                                                  (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
                         fifo_intf.wr_en_0
                                                  (~fifo_intf.empty && fifo_intf.rd_en)
  Row
         3:
                         fifo_intf.wr_en_1
  Row
         4:
                                                  fifo_intf.rd_en
                                                  (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                         fifo_intf.empty_0
  Row
                         fifo_intf.empty_1
                                                  (fifo_intf.rd_en && ~fifo_intf.wr_en)
                 \operatorname{-Focused} Condition View\operatorname{-}
Line
                        1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                               Reason for no coverage
                      Covered
                                                            _{
m Hint}
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            \mathbf{Y}
   fifo_intf.full
                            Y
                         FEC Target
     Rows:
                                                  Non-masking condition(s)
                   _{
m Hits}
  Row
                         fifo_intf.rd_en_0
  Row
         2:
                         fifo_intf.rd_en_1
                                                  (fifo_intf.full && fifo_intf.wr_en)
  Row
         3:
                         fifo_intf.wr_en_0
                                                  fifo_intf.rd_en
                          fifo_intf.wr_en_1
  Row
                                                  (fifo_intf.full && fifo_intf.rd_en)
  Row
        5:
                         fifo_intf.full_0
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
                         fifo_intf.full_1
  Row
         6:
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
                 \operatorname{-Focused} Condition View-
            61 Item
                        1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                            Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                         FEC Target
     Rows:
                  _{
m Hits}
                                                  Non-masking condition(s)
                         fifo_intf.rd_en_0
  Row
        1:
                      1
         2:
                         fifo_intf.rd_en_1
                                                  (fifo_intf.empty && fifo_intf.wr_en)
  Row
                      1
        3:
                         fifo_intf.wr_en_0
  Row
                                                  fifo_intf.rd_en
                      1
                                                  (fifo_intf.empty && fifo_intf.rd_en)
         4:
                         fifo_intf.wr_en_1
  Row
                      1
```

Row

 $(count != 0)_{-0}$

fifo_intf.rd_en

```
-Focused Condition View
                     1 \quad (count == 8)
           66 Item
Line
Condition totals: 1 of 1 input term covered = 100.00\%
    Input Term
                  Covered Reason for no coverage
                        Y
  (count == 8)
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
 Row
        1:
                         (count = 8)_{-0}
                     1
 Row
                         (count = 8)_{-1}
                 -Focused Condition View-
           67 Item
                     1 \quad ((count == 0) \mid | \quad \tilde{fifo}_{intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
                            Y
     (count = 0)
  fifo_intf.rst_n
                            Y
                  Hits FEC Target
     Rows:
                                                 Non-masking condition(s)
                         (count = 0)_{-}0
                                                 fifo_intf.rst_n
 Row
        1:
                     1
  Row
                     1
                         (count = 0)_{-1}
 Row
        3:
                         fifo_intf.rst_n_0
                                                 \tilde{} (count == 0)
                     1
                                                 \tilde{\ }(\text{count} == 0)
 Row
                         fifo_intf.rst_n_1
        4:
                     1
                 -Focused Condition View-
                     1 (count = (8 - 1))
           68 Item
Condition totals: 1 of 1 input term covered = 100.00%
                         Covered Reason for no coverage
                                                              Hint
          Input Term
  (count = (8 - 1))
                               Y
     Rows:
                  _{
m Hits}
                       FEC Target
                                                Non-masking condition(s)
                        (count = (8 - 1))_{-0} -
 Row
        1:
                         (count = (8 - 1))_{-1} -
 Row
                 -Focused Condition View-
           69 Item
Line
                     1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
  (count == 1)
                        Y
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
 Row
        1:
                     1
                         (count = 1)_{-0}
 Row
                         (count = 1)_{-1}
Statement Coverage:
    Enabled Coverage
                                     Bins
                                                         _{\mathrm{Misses}}
                                                                 Coverage
                                                                  100.00\%
    Statements
                                       28
                                                  28
                                                              0
                                 =Statement Details=
Statement Coverage for Design Unit work.FIFO —
    Line
                  Item
                                               Count
                                                          Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                          module FIFO(FIFO_IF.DUT fifo_intf);
                                                          parameter FIFO_WIDTH = 16;
    3
                                                          parameter FIFO_DEPTH = 8;
    4
                                                          localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
    6
                                                          reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1—D Array
    7
    8
                                                          reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
    9
                                                          reg [max_fifo_addr:0] count;
    10
    11
                     1
                                                1312
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    12
                                                             if (!fifo_intf.rst_n) begin
    13
                                                 230
                                                                      wr_ptr \ll 0;
                     1
    14
                                                 230
                     1
                                                                      fifo_intf.wr_ack \le 0;
    15
                                                                      \label{eq:fifo_intf.overflow} \textit{ } <= 0;
    16
                     1
                                                 230
    17
                                                             _{\mathrm{end}}
                                                             else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                     1
                                                 624
    19
                                                                      mem[wr_ptr] <= fifo_intf.data_in;
                                                                      fifo_intf.wr_ack \ll 1;
    20
                     1
                                                 624
                     1
    21
                                                 624
                                                                      wr_ptr \ll wr_ptr + 1;
```

(fifo_intf.rd_en && fifo_intf.wr_en)

(fifo_intf.rd_en && fifo_intf.wr_en)

Row

Row

fifo_intf.empty_0

fifo_intf.empty_1

```
22
                                                               \operatorname{end}
    23
                                                                else begin
    24
                      1
                                                   458
                                                                         fifo_intf.wr_ack \le 0;
                                                                         if (fifo_intf.full & fifo_intf.wr_en)
    25
                      1
    26
                                                    84
                                                                                  fifo_intf.overflow <= 1;
    27
                                                                         else
                      1
                                                   374
                                                                                  fifo_intf.overflow \le 0;
    28
    29
                                                               _{\mathrm{end}}
                                                            \operatorname{end}
    30
    31
                      1
                                                  1312
                                                            always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    32
                                                               if (!fifo_intf.rst_n) begin
    33
                                                   230
    34
                      1
                                                                         rd_ptr \le 0;
                                                   230
                                                                         fifo_intf.underflow \ll 0;
    35
                      1
                                                   230
                                                                         fifo_intf.data_out \le \{FIFO_WIDTH\{1'b0\}\};
    36
                      1
    37
                                                               _{\mathrm{end}}
                                                                else if (fifo_intf.rd_en && count != 0) begin
    38
                      1
                                                   243
                                                                         fifo_intf.data_out <= mem[rd_ptr];
    39
    40
                      1
                                                   243
                                                                         rd_ptr \ll rd_ptr + 1;
    41
                                                               _{\mathrm{end}}
    42
                                                                else begin
                                                                         if (fifo_intf.empty & fifo_intf.rd_en)
    43
                                                   131
                      1
                                                                                  fifo_intf.underflow <= 1;
    44
    45
                                                                         else
                      1
                                                   708
                                                                                  fifo_intf.underflow \le 0;
    46
    47
                                                               _{\mathrm{end}}
                                                            end
    48
    49
                      1
                                                  1103
                                                            always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    50
    51
                                                                if (!fifo_intf.rst_n) begin
                      1
                                                   219
    52
                                                                         count \ll 0;
    53
                                                               _{\mathrm{end}}
                                                                else begin
    54
                                                                                  (\{fifo_intf.wr_en, fifo_intf.rd_en\} = 2'b10\} \&\& !fifo_intf.fu
    55
                                                                         i f
    56
                      1
                                                   443
                                                                                  count \ll count + 1;
                                                                         else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b01) && !fifo\_intf.em
    57
                      1
                                                    77
                                                                                  count \ll count - 1;
    58
                                                                         else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
    59
    60
                      1
                                                    15
                                                                                  count \ll count - 1;
                                                                         else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.emp
    61
    62
                      1
                                                    30
                                                                                  count \le count + 1;
    63
                                                               _{\mathrm{end}}
                                                            end
    64
    65
    66
                      1
                                                   659
                                                            assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                                                            assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                      1
                                                   873
                                                            assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                      1
                                                   659
                                                            assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
                                                   659
Toggle Coverage:
    Enabled Coverage
                                      Bins
                                                  Hits
                                                           Misses
                                                                    Coverage
    Toggles
                                         20
                                                    20
                                                                0
                                                                     100.00\%
```

Toggle Details=

Toggle Coverage for Design Unit work.FIFO

No	de $1H$ –> $0L$	0L—>1H	"Coverage"
$\operatorname{count}\left[0-\right]$	3] 1	1	100.00
rd_ptr[0-	2] 1	1	100.00
$\mathrm{wr}_{-}\mathrm{ptr}\left[0-\right]$	2] 1	1	100.00

Toggle Coverage = 100.00% (20 of 20 bins)

Total Coverage By Design Unit (filtered view): 98.00%

4.4 Code Coverage "seed4" Report

Coverage Report by DU with details

anch Coverage:				
Enabled Coverage	Bins	Hits	Misses	${\bf Coverage}$
Branches	25	25	0	100.00%

Branch Coverage for Design Unit work.FIFO

Line Item Count Source

File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv

```
——IF Branch-
    13
                                              1319
                                                        Count coming in to IF
                                                           if (!fifo_intf.rst_n) begin
    13
                    1
                                               244
                                               623
                                                           else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                    1
                                               452
    23
                    1
                                                           else begin
Branch totals: 3 hits of 3 branches = 100.00\%
                                     -IF Branch-
    25
                                               452
                                                        Count coming in to IF
                                                                   if (fifo_intf.full & fifo_intf.wr_en)
    25
                    1
                                                96
    27
                    1
                                               356
Branch totals: 2 hits of 2 branches = 100.00%
                                     -IF Branch-
    33
                                              1319
                                                        Count coming in to IF
                    1
                                               244
                                                           if (!fifo_intf.rst_n) begin
    33
                                               243
                                                           else if (fifo_intf.rd_en && count != 0) begin
    38
                    1
                                                           else begin
                    1
                                               832
Branch totals: 3 hits of 3 branches = 100.00\%
                                    ---IF Branch-
                                                        Count coming in to IF
                                               832
                                                                   if (fifo_intf.empty & fifo_intf.rd_en)
                    1
                                               127
    43
                    1
                                               705
                                                                    else
Branch totals: 2 hits of 2 branches = 100.00\%
                                   ----IF Branch---
                                              1122
                                                        Count coming in to IF
    51
                                               235
    51
                    1
                                                           if (!fifo_intf.rst_n) begin
                    1
                                               887
                                                           else begin
Branch totals: 2 hits of 2 branches = 100.00%
                                    —IF Branch—
    55
                                               887
                                                        Count coming in to IF
                                                                   if ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
    55
                    1
                                               435
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                    1
                                                67
    57
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
                    1
                                                18
                                                30
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                                               337
                                                        All False Count
Branch totals: 5 hits of 5 branches = 100.00\%
                                     {
m -IF} {
m Branch-}
                                               647
                                                        Count coming in to IF
                    1
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66
                                                40
                    2
                                               607
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                     {
m -IF} {
m Branch}{
m -}
                                               875
                                                        Count coming in to IF
                    1
                                               338
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
                    ^{2}
                                               537
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                      \operatorname{-IF} \ \operatorname{Branch} -
                                               647
                                                        Count coming in to IF
                    1
                                                59
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
                    ^{2}
                                               588
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                     {	ext{-IF}} Branch{	ext{-}}
                                               647
                                                        Count coming in to IF
                    1
                                               121
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                    ^{2}
                                               526
Branch totals: 2 hits of 2 branches = 100.00\%
Condition Coverage:
    Enabled Coverage
                                    Bins
                                           Covered
                                                       Misses
                                                               Coverage
                                                            ^{2}
    Conditions
                                      25
                                                 23
                                                                 92.00\%
                             ===Condition Details=
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
Line
           18 Item
                       1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                         Hint
  fifo_intf.wr_en
                           Y
                           Y
      (count < 8)
                  Hits FEC Target
                                               Non-masking condition(s)
     Rows:
 Row
        1:
                        fifo_intf.wr_en_0
        2:
                        fifo_intf.wr_en_1
  Row
                                               (count < 8)
                     1
        3:
                        (count < 8)_{-0}
                                               fifo_intf.wr_en
  Row
                    1
```

fifo_intf.wr_en

Row

4:

 $(count < 8)_{-1}$

Condition totals: 1 of 2 input terms covered = 50.00% Input Term Covered Reason for no coverage Hint $,_0$, not hit fifo_intf.full Hit '_0' Ν Y fifo_intf.wr_en Non-masking condition(s) FEC Target Rows: HitsRow 1: ***0*** fifo_intf.full_0 fifo_intf.wr_en fifo_intf.full_1 Row 2: 1 fifo_intf.wr_en Row 3: fifo_intf.wr_en_0 fifo_intf.full 1 fifo_intf.full fifo_intf.wr_en_1 Row 4:1 -Focused Condition View-1 (fifo_intf.rd_en && (count != 0)) 38 Item Line Condition totals: 2 of 2 input terms covered = 100.00% Input Term Covered Reason for no coverage Hint $fifo_intf.rd_en$ Y (count != 0) Y $_{
m Hits}$ Rows: FEC Target Non-masking condition(s) Row 1: 1 fifo_intf.rd_en_0 fifo_intf.rd_en_1 Row 2: (count != 0) $(count != 0)_{-0}$ Row 3: fifo_intf.rd_en 1 $(count != 0)_{-1}$ fifo_intf.rd_en 4: Row 1 -Focused Condition View-43 Item Line 1 (fifo_intf.empty & fifo_intf.rd_en) Condition totals: 1 of 2 input terms covered = 50.00% Input Term Covered Reason for no coverage Hint fifo_intf.empty Ν $^{\prime}_{-0}$ or not hit Hit '_0' fifo_intf.rd_en Y FEC Target Non-masking condition(s) Rows: Hitsfifo_intf.rd_en Row 1: ***0*** fifo_intf.empty_0 fifo_intf.empty_1 Row 2: fifo_intf.rd_en Row 3: fifo_intf.rd_en_0 fifo_intf.empty fifo_intf.rd_en_1 Row 4:fifo_intf.empty -Focused Condition View-55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full) Condition totals: 3 of 3 input terms covered = 100.00% Input Term Covered Reason for no coverage fifo_intf.rd_en Y fifo_intf.wr_en Y fifo_intf.full Y Rows: Hits FEC Target Non-masking condition(s) Row 1: fifo_intf.rd_en_0 (~fifo_intf.full && fifo_intf.wr_en) 2: fifo_intf.rd_en_1 Row Row ~ fifo_intf.rd_en 3: fifo_intf.wr_en_0 (~fifo_intf.full && ~fifo_intf.rd_en) Row 4: fifo_intf.wr_en_1 Row 5: fifo_intf.full_0 (~fifo_intf.rd_en && fifo_intf.wr_en) Row 6: fifo_intf.full_1 (~fifo_intf.rd_en && fifo_intf.wr_en) $\hbox{-} Focused \quad Condition \quad View-$ 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty) Line 57 Item Condition totals: 3 of 3 input terms covered = 100.00% Input Term Covered Reason for no coverage fifo_intf.rd_en Y fifo_intf.wr_en Υ Y fifo_intf.empty Hits FEC Target Non-masking condition(s) Rows: 1 fifo_intf.rd_en_0 Row 1: $(\tilde{fifo_intf.empty} \&\& \tilde{fifo_intf.wr_en})$ 2: fifo_intf.rd_en_1 Row 1 Row 3: 1 $fifo_intf.wr_en_0$ (~fifo_intf.empty && fifo_intf.rd_en) 4: $fifo_intf.wr_en_1$ fifo_intf.rd_en Row 1 (fifo_intf.rd_en && ~fifo_intf.wr_en) Row 5:fifo_intf.empty_0 1 (fifo_intf.rd_en && ~fifo_intf.wr_en) 6: fifo_intf.empty_1 Row 1 -Focused Condition View-1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full) Line Condition totals: 3 of 3 input terms covered = 100.00%

-Focused Condition View-

1 (fifo_intf.full & fifo_intf.wr_en)

25 Item

Input Term

Covered Reason for no coverage

Line

Hint

```
Y
  fifo_intf.wr_en
                            Y
   fifo_intf.full
                         FEC Target
     Rows:
                  _{
m Hits}
                                                  Non-masking condition(s)
  Row
                     1
                         fifo_intf.rd_en_0
        1:
                         fifo_intf.rd_en_1
  Row
         2:
                      1
                                                  (fifo_intf.full && fifo_intf.wr_en)
         3:
                         fifo_intf.wr_en_0
                                                  fifo_intf.rd_en
  Row
                         fifo_intf.wr_en_1
                                                  (fifo_intf.full && fifo_intf.rd_en)
  Row
         4:
                         fifo_intf.full_0
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
         6:
                         fifo_intf.full_1
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 -Focused Condition View-
            61 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
                      Covered Reason for no coverage
       Input Term
                                                            Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                  _{
m Hits}
  Row
        1:
                     1
                         fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
                                                  (fifo_intf.empty && fifo_intf.wr_en)
         2:
  Row
  Row
         3:
                         fifo_intf.wr_en_0
                                                  fifo_intf.rd_en
                                                  (fifo_intf.empty && fifo_intf.rd_en)
  Row
         4:
                         fifo_intf.wr_en_1
                     1
  Row
                         fifo_intf.empty_0
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
        5:
                      1
                         fifo_intf.empty_1
        6:
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                     1
                 -Focused Condition View-
                       1 \quad (count == 8)
Line
            66 Item
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                   Covered Reason for no coverage
                                                        Hint
  (count == 8)
                         Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
 Row
        1:
                     1
                         (count = 8)_{-}0
 Row
         2:
                         (count = 8)_{-1}
                 -Focused Condition View-
                       1 ((count = 0) || \tilde{fifo_intf.rst_n})
Line
            67 Item
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                      Covered Reason for no coverage
                                                            Hint
     (count = 0)
                            \mathbf{Y}
  fifo_intf.rst_n
                            Y
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                   Hits
                         (count = 0)_{-0}
                                                  fifo_intf.rst_n
 Row
         1:
  Row
         2:
                         (count = 0)_{-1}
  Row
         3:
                         fifo_intf.rst_n_0
                                                  \tilde{\phantom{a}}(\text{count} == 0)
  Row
         4:
                         fifo_intf.rst_n_1
                                                  \tilde{\phantom{a}}(\text{count} == 0)
                 \hbox{-}Focused \quad Condition \quad View-
Line
            68 Item
                        1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00\%
                                  Reason for no coverage
           Input Term
                         Covered
  (count = (8 - 1))
                               \mathbf{Y}
     Rows:
                         FEC Target
                                                 Non-masking condition(s)
                         (count = (8 - 1))_{-0}
  Row
        1:
                      1
  Row
                         (count = (8 - 1))_{-1}
                 -Focused Condition View-
Line
            69 Item
                       1 \quad (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                        _{
m Hint}
                         Y
  (count == 1)
     Rows:
                  Hits FEC Target
                                                 Non-masking condition(s)
                         (count = 1)_{-0}
 Row
        1:
                     1
                         (count = 1)_{-1}
 Row
         2:
                      1
Statement Coverage:
    Enabled Coverage
                                     Bins
                                                 Hits
                                                          Misses Coverage
    Statements\\
                                                   28
                                                               0
                                                                   100.00\%
                                        28
```

Y

fifo_intf.rd_en

Statement Details

Statement Coverage for Design Unit work.FIFO —

```
Line
                  Item
                                               Count
                                                          Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                         module FIFO(FIFO_IF.DUT fifo_intf);
    2
                                                          parameter FIFO_WIDTH = 16;
    3
                                                          parameter FIFO_DEPTH = 8;
    4
                                                          localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    5
    6
                                                          reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
    7
    8
                                                              [max_fifo_addr-1:0] wr_ptr, rd_ptr;
    9
                                                          reg [max_fifo_addr:0] count;
    10
    11
                     1
                                                1319
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    12
                                                             if (!fifo_intf.rst_n) begin
    13
                     1
                                                 244
                                                                      wr_ptr \le 0;
    14
                                                                      fifo_intf.wr_ack \le 0;
    15
                     1
                                                 244
    16
                     1
                                                 244
                                                                      fifo_intf.overflow \ll 0;
    17
                                                             _{\mathrm{end}}
                                                             else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    18
                     1
                                                 623
                                                                     mem[wr_ptr] <= fifo_intf.data_in;
    19
                                                 623
    20
                     1
                                                                      fifo_intf.wr_ack \ll 1;
                                                 623
    21
                     1
                                                                      wr_ptr \le wr_ptr + 1;
    22
                                                             _{\mathrm{end}}
    23
                                                             else begin
                     1
                                                 452
                                                                      fifo_intf.wr_ack \ll 0;
    24
                                                                      if (fifo_intf.full & fifo_intf.wr_en)
    25
                                                                               fifo_intf.overflow <= 1;
    ^{26}
                     1
                                                  96
    27
                                                                      else
                     1
                                                 356
                                                                               fifo_intf.overflow \ll 0;
    28
    ^{29}
                                                             end
    30
                                                          end
    31
    32
                     1
                                                1319
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    33
                                                             if (!fifo_intf.rst_n) begin
    34
                     1
                                                 244
                                                                      rd_ptr \ll 0;
                                                                      fifo_intf.underflow <= 0;
    35
                     1
                                                 244
                                                                      fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    36
                     1
                                                 244
    37
                                                             _{\mathrm{end}}
    38
                                                             else if (fifo_intf.rd_en && count != 0) begin
    39
                     1
                                                 243
                                                                      fifo_intf.data_out <= mem[rd_ptr];
    40
                     1
                                                 243
                                                                      rd_ptr \ll rd_ptr + 1;
    41
                                                             _{\mathrm{end}}
    42
                                                             else begin
    43
                                                                      if (fifo_intf.empty & fifo_intf.rd_en)
                     1
                                                 127
                                                                               fifo_intf.underflow <= 1;
    44
    45
                                                                      else
                     1
                                                 705
                                                                               fifo_intf.underflow \le 0;
    46
    47
                                                             \operatorname{end}
    48
                                                         end
    49
                     1
                                                1122
                                                          always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    50
    51
                                                             if (!fifo_intf.rst_n) begin
    52
                     1
                                                 235
                                                                      count \ll 0;
    53
                                                             end
                                                             else begin
    54
                                                                              (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
    55
                     1
                                                 435
                                                                              count \ll count + 1;
    56
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
    57
    58
                     1
                                                  67
                                                                              count \ll count - 1;
    59
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    60
                     1
                                                  18
                                                                              count \ll count - 1;
    61
                                                                      else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                     1
                                                  30
                                                                              count \ll count + 1;
    63
                                                             end
    64
                                                         end
                                                          assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     1
                                                 648
                                                 876
                                                          assign fifo_intf.empty = (count = 0 \mid | !fifo_intf.rst_n)? 1 : 0;
    67
                     1
                                                 648
                                                          assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     1
    69
                                                 648
                                                          assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Toggle Coverage:
    Enabled Coverage
                                     Bins
                                                Hits
                                                                 Coverage
                                                         _{
m Misses}
                                                                  100.00\%
    Toggles
                                       20
                                                  20
                                                              0
```

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
$\operatorname{count}\left[0-3\right]$	1	1	100.00
$rd_{-}ptr[0-2]$	1	1	100.00
$\operatorname{wr}\operatorname{-ptr}\left[0-2\right]$	1	1	100.00

```
\begin{array}{lll} {\rm Total\ Node\ Count} & = & 10 \\ {\rm Toggled\ Node\ Count} & = & 10 \\ {\rm Untoggled\ Node\ Count} & = & 0 \\ \end{array}
```

Toggle Coverage = 100.00% (20 of 20 bins)

Total Coverage By Design Unit (filtered view): 98.00%

4.5 Code Coverage "seed5" Report

Coverage Report by DU with details

```
— Design Unit: work.FIFO
Branch Coverage:
    Enabled Coverage
                                    Bins
                                              Hits
                                                       _{
m Misses}
                                                               Coverage
    Branches
                                      25
                                                                100.00\%
                                 =Branch Details=
Branch Coverage for Design Unit work.FIFO
                  Item
                                                        Source
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                        Count coming in to IF
                                              1312
    13
                    1
                                               231
                                                           if (!fifo_intf.rst_n) begin
    18
                    1
                                               593
                                                           else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23
                                               488
Branch totals: 3 hits of 3 branches = 100.00\%
                                               488
                                                        Count coming in to IF
                                                                   if (fifo_intf.full & fifo_intf.wr_en)
    25
                     1
                                               121
    27
                    1
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} {
m Branch}
                                              1312
                                                        Count coming in to IF
    33
                                                           if (!fifo_intf.rst_n) begin
    33
                                               231
                                               220
                                                           else if (fifo_intf.rd_en && count != 0) begin
    38
                    1
                                                           else begin
                                               861
Branch totals: 3 hits of 3 branches = 100.00\%
                                     -{
m IF}~{
m Branch}
    43
                                               861
                                                        Count coming in to IF
                                               133
                                                                    if (fifo_intf.empty & fifo_intf.rd_en)
    43
                    1
                                               728
                                                                    else
Branch totals: 2 hits of 2 branches = 100.00\%
                                      {
m -IF} {
m Branch}{
m -}
                                              1070
                                                        Count coming in to IF
    51
                                               225
    51
                    1
                                                           if (!fifo_intf.rst_n) begin
                    1
                                               845
                                                           else begin
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -IF Branch-
                                               845
    55
                                                        Count coming in to IF
                                                                            (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) &&!fifo_intf.fu
                    1
                                               422
    55
                                                                    i f
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
                    1
                                                62
    57
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    59
                    1
                                                17
                                                30
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                                        All False Count
                                               314
Branch totals: 5 hits of 5 branches = 100.00%
                                      IF Branch
    66
                                               627
                                                        Count coming in to IF
                                                41
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                                               586
Branch totals: 2 hits of 2 branches = 100.00%
                                    ---IF Branch
    67
                                               841
                                                        Count coming in to IF
                    1
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                                               324
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                    2
                                               517
Branch totals: 2 hits of 2 branches = 100.00\%
                                  ---IF Branch-
    68
                                               627
                                                        Count coming in to IF
                    1
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                                                56
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                    ^{2}
                                               571
Branch totals: 2 hits of 2 branches = 100.00%
                                   ---IF Branch-
    69
                                                        Count coming in to IF
                                               627
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0:
    69
                    1
                                               116
                    2
                                               511
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
```

```
Condition Coverage:
    Enabled Coverage
                                     Bins
                                            Covered
                                                        Misses
                                                                Coverage
                                                              2
    Conditions
                                       25
                                                                   92.00\%
                                                  23
                                  =Condition Details:
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                -{
m Focused} Condition View-
Line
                      1 (fifo_intf.wr_en && (count < 8))
           18 Item
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
  fifo_intf.wr_en
                            Y
                            Y
      (count < 8)
                       FEC Target
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
                        fifo_intf.wr_en_0
 Row
        1:
                     1
  Row
        2:
                         fifo_intf.wr_en_1
                                                 (count < 8)
                         (count < 8)_{-0}
                                                 fifo_intf.wr_en
  Row
        3:
                         (count < 8)_{-1}
                                                 fifo_intf.wr_en
  Row
        4:
                 -Focused Condition View-
Line
           25 Item
                      1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00\%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
   fifo_intf.full
                            Ν
                               ^{\prime}_{-0} or not hit
                                                          Hit '_0'
                            Y
  fifo_intf.wr_en
     Rows:
                  Hits
                        FEC Target
                                                Non-masking condition(s)
                         fifo_intf.full_0
 Row
        1:
               ***0***
                                                 fifo_intf.wr_en
                         fifo_intf.full_1
                                                 fifo_intf.wr_en
  Row
        2:
                         fifo_intf.wr_en_0
                                                 fifo_intf.full
  Row
        3:
                         fifo_intf.wr_en_1
                                                 fifo_intf.full
  Row
                 -Focused Condition View-
           38 Item
                      1 (fifo_intf.rd_en && (count != 0))
Line
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
  fifo_intf.rd_en
                            Y
     (count != 0)
                            Y
                        FEC Target
                                                Non-masking condition(s)
     Rows:
                  _{
m Hits}
                         fifo_intf.rd_en_0
 Row
        1:
  Row
        2:
                         fifo_intf.rd_en_1
                                                 (count != 0)
  Row
        3:
                        (count != 0)_{-0}
                                                 fifo_intf.rd_en
  Row
        4:
                         (count != 0)_{-1}
                                                 fifo_intf.rd_en
                 \operatorname{-Focused} Condition View\operatorname{-}
Line
                       1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
                              Reason for no coverage
       Input Term
                                                          Hint
                               '_0, not hit
                                                          Hit '_0'
  fifo_intf.empty
                            Ν
                            Y
  fifo_intf.rd_en
                  Hits FEC Target
     Rows:
                                                Non-masking condition(s)
                        fifo_intf.empty_0
                                                 fifo_intf.rd_en
        2:
                         fifo_intf.empty_1
                                                 fifo_intf.rd_en
  Row
        3:
                         fifo_intf.rd_en_0
                                                 fifo_intf.empty
  Row
                        fifo_intf.rd_en_1
 Row
        4:
                     1
                                                 fifo_intf.empty
                 \hbox{-}Focused \quad Condition \quad View-
Line
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                            \mathbf{Y}
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
   fifo_intf.full
                            Y
                                                Non-masking condition(s)
     Rows:
                  Hits FEC Target
                                                (~fifo_intf.full && fifo_intf.wr_en)
  Row
        1:
                     1
                         fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
        2:
  Row
                     1
```

fifo_intf.wr_en_0

1

3:

Row

 \sim fifo_intf.rd_en

```
(~fifo_intf.full && ~fifo_intf.rd_en)
  Row
  Row
                         fifo_intf.full_0
                                                  (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
         6:
                         fifo_intf.full_1
                                                  (~fifo_intf.rd_en && fifo_intf.wr_en)
                 -Focused Condition View-
                        1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
            57 Item
Condition totals: 3 of 3 input terms covered = 100.00\%
       Input Term
                      Covered Reason for no coverage
                                                            Hint
                            Y
  fifo_intf.rd_en
                            \mathbf{Y}
  fifo_intf.wr_en
                            Y
  fifo_intf.empty
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                   Hits
                     1
                         fifo_intf.rd_en_0
  Row
        1:
                                                  (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
         2:
                      1
                         fifo_intf.rd_{en_1}
         3:
                         fifo_intf.wr_en_0
                                                  (~fifo_intf.empty && fifo_intf.rd_en)
  Row
                      1
                         fifo_intf.wr_en_1
                                                  fifo_intf.rd_en
  Row
         4:
                      1
                         fifo_intf.empty_0
                                                  (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                     1
                                                  (fifo_intf.rd_en && ~fifo_intf.wr_en)
         6:
                         fifo_intf.empty_1
  Row
                      1
                 \hbox{-}Focused \quad Condition \quad View-
Line
            59 Item
                        1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                      Covered
                               Reason for no coverage
                                                            Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
   f\,i\,f\,o\,{\scriptscriptstyle \,-}\,i\,n\,t\,f\,\,.\,\,f\,u\,l\,l
                            Y
                         FEC Target
     Rows:
                   _{
m Hits}
                                                  Non-masking condition(s)
  Row
         1:
                     1
                         fifo_intf.rd_en_0
                         fifo_intf.rd_en_1
                                                  (fifo_intf.full && fifo_intf.wr_en)
  Row
         2:
                      1
                         fifo_intf.wr_en_0
                                                  fifo_intf.rd_en
  Row
         3:
                      1
                         fifo_intf.wr_en_1
                                                  (fifo_intf.full && fifo_intf.rd_en)
  Row
         4:
                      1
                         fifo_intf.full_0
  Row
        5:
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
                      1
  Row
         6:
                         fifo_intf.full_1
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
                 -Focused Condition View-
            61 Item
Line
                        1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                      Covered Reason for no coverage
                                                            Hint
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
  fifo_intf.empty
                            Y
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                   Hits
  Row
         1:
                     1
                         fifo_intf.rd_en_0
  Row
         2:
                         fifo_intf.rd_{en_1}
                                                  (fifo_intf.empty && fifo_intf.wr_en)
                         fifo_intf.wr_en_0
                                                  fifo_intf.rd_en
  Row
         3:
         4:
                         fifo_intf.wr_en_1
                                                  (fifo_intf.empty && fifo_intf.rd_en)
  Row
         5:
                         fifo_intf.empty_0
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
         6:
                         fifo_intf.empty_1
                                                  (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 -Focused Condition View-
Line
            66 Item
                        1 \quad (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                   Covered
                           Reason for no coverage
  (count == 8)
                         Y
     Rows:
                         FEC Target
                                                  Non-masking condition(s)
                         (count = 8)_{-0}
  Row
        1:
                      1
  Row
                         (count = 8)_{-1}
                 \operatorname{-Focused} Condition View\operatorname{--}
                      1 \quad ((count = 0) \mid | \quad \tilde{fifo_intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                            Hint
                            Y
     (count = 0)
                            Y
  fifo_intf.rst_n
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
                         (count = 0)_{-}0
 Row
        1:
                      1
                                                  fifo_intf.rst_n
        2:
                         (count = 0)_{-1}
 Row
                      1
 Row
        3:
                         fifo_intf.rst_n_0
                                                  \tilde{\ }(\text{count} == 0)
                      1
                                                   (count == 0)
 Row
        4:
                         fifo_intf.rst_n_1
                      1
                 -Focused Condition View-
                      1 (count = (8 - 1))
Line
            68 Item
```

fifo_intf.wr_en_1

```
Input Term
                          Covered Reason for no coverage
                                                                Hint
  (count = (8 - 1))
                                Y
                         FEC Target
                                                  Non-masking condition(s)
     Rows:
                   _{
m Hits}
                          (count = (8 - 1))_{-0}
  Row
         1:
                      1
                          (count = (8 - 1))_{-1}
         2:
  Row
                      1
                 -Focused Condition View-
            69 Item
                      1 \quad (count == 1)
Line
Condition totals: 1 of 1 input term covered = 100.00%
                   Covered Reason for no coverage
    Input Term
                                                         _{
m Hint}
                         Υ
  (count == 1)
                   Hits FEC Target
                                                   Non-masking condition(s)
     Rows:
                          (count = 1)_{-0}
  Row
         1:
                      1
                          (count = 1)_{-1}
  Row
         2:
                      1
Statement Coverage:
    Enabled Coverage
                                      _{\mathrm{Bins}}
                                                  _{
m Hits}
                                                                   Coverage
                                                           _{\mathrm{Misses}}
    Statements
                                        28
                                                    28
                                                                0
                                                                     100.00\%
```

Statement Details

Statement Coverage for Design Unit work.FIFO —

```
Line
                Item
                                             Count
                                                        Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                        module FIFO(FIFO_IF.DUT fifo_intf);
 ^{2}
                                                        parameter FIFO_WIDTH = 16;
 3
                                                        parameter FIFO_DEPTH = 8;
                                                        localparam max_fifo_addr = $clog2(FIFO_DEPTH);
 5
                                                        reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
  8
                                                        reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
                                                        reg [max_fifo_addr:0] count;
  10
  11
                                              1312
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  12
                   1
                                                            if (!fifo_intf.rst_n) begin
  13
  14
                                               231
                                                                     wr_ptr \ll 0;
                                               231
                                                                     fifo_intf.wr_ack \ll 0;
  15
                   1
                                               231
                                                                     fifo_intf.overflow <= 0;
  16
  17
                                                            else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
  18
  19
                   1
                                               593
                                                                    mem[wr_ptr] <= fifo_intf.data_in;
  20
                                               593
                                                                    fifo_intf.wr_ack \ll 1;
                   1
  21
                                               593
                                                                     wr_ptr \ll wr_ptr + 1;
  22
                                                           end
  23
                                                            else begin
  24
                   1
                                               488
                                                                     fifo_intf.wr_ack \ll 0;
  25
                                                                     if (fifo_intf.full & fifo_intf.wr_en)
                                                                              fifo_intf.overflow <= 1;
  ^{26}
                   1
                                               121
  27
                                                                     else
                                                                              fifo_intf.overflow <= 0;
  28
                   1
                                               367
  ^{29}
                                                           \operatorname{end}
  30
                                                        end
  31
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  32
                   1
                                              1312
                                                            if (!fifo_intf.rst_n) begin
  33
  34
                                               231
                                                                     rd_ptr \le 0;
  35
                   1
                                               231
                                                                     fifo_intf.underflow <= 0;
                                                                     fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
  36
                                               231
  37
                                                           end
                                                            else if (fifo_intf.rd_en && count != 0) begin
  38
                                               220
  39
                   1
                                                                     fifo_intf.data_out <= mem[rd_ptr];
  40
                   1
                                               220
                                                                     rd_ptr \ll rd_ptr + 1;
  41
                                                           \operatorname{end}
  42
                                                            else begin
                                                                     if (fifo_intf.empty & fifo_intf.rd_en)
  43
                   1
  44
                                               133
                                                                              fifo_intf.underflow \ll 1;
  45
                                                                     else
                   1
                                               728
                                                                              fifo_intf.underflow \ll 0;
  46
  47
                                                           _{\mathrm{end}}
  48
                                                        end
  49
                   1
  50
                                              1070
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
                                                            if (!fifo_intf.rst_n) begin
  51
                   1
                                               225
                                                                    count \ll 0;
  52
  53
                                                           _{\mathrm{end}}
                                                            else begin
  54
                                                                              (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10) \&\& !fifo\_intf.fu
  55
                                                                     i f
```

56 57 58 59 60 61 62 63 64 65 66	1 422 1 62 1 17 1 30	end	<pre>count <= count + 1; else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em</pre>
67	1 842	_	$fifo_intf.empty = (count = 0 !fifo_intf.rst_n)? 1 : 0;$
68	1 628		fifo_intf.empty = $(count = 0)$ FIFO_DEPTH-1)? 1 : 0;
69	1 628	_	$fifo_intf.almostempty = (count == 1)? 1 : 0;$
Toggle Coverage: Enabled Coverage	e Bins Hits	s Misses	Coverage
Toggles	20 20	0	100.00%

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L -> 1H	"Coverage"
$\operatorname{count}\left[0-3\right]$	1	1	100.00
$\mathrm{rd}_{-}\mathrm{ptr}\left[0-2\right]$	1	1	100.00
$\operatorname{wr}\operatorname{-ptr}\left[0-2\right]$	1	1	100.00

Toggle~Coverage~=~100.00%~(20~of~20~bins)

Total Coverage By Design Unit (filtered view): 98.00%

5 Waveform

5.1 Waveform & Transcript "seed1" Report

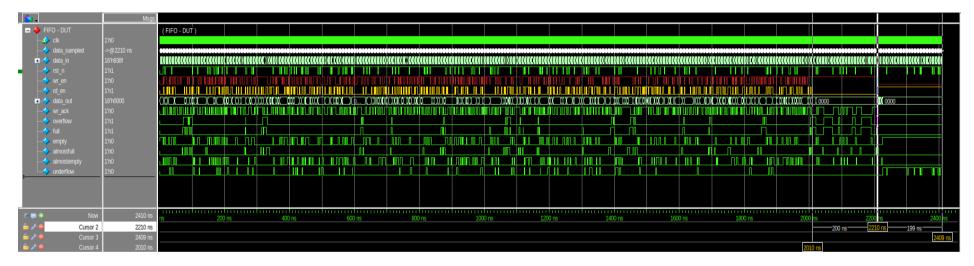


Figure 6: simulation waveform "seed1"

```
2007-2013 Cadence Design Systems, Inc.
      (C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.
           ******
                                                                                                                                  ******
                                                     IMPORTANT RELEASE NOTES
           You are using a version of the UVM library that has been compiled
          with `UVM_NO_DEPRECATED undefined.
           See http://www.eda.org/svdb/view.php?id=3313 for more details.
          You are using a version of the UVM library that has been compiled with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.
                    (Specify +UVM_NO_RELNOTES to turn off this notice)
# (Spectry +UVM_NO_RELNOTES to turn off this notice)

# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(277) @ 0: reporter [Questa UVM] QUESTA_UVM-1.2.3

# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(278) @ 0: reporter [Questa UVM] questa_uvm::init(+struct)

# UVM_INFO @ 0: reporter [RNTST] Running test FIFO_test...

# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv(35) @ 0: uvm_test_top [run_phase] Inside the FIFO test.

# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 2410: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase

# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:

# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205

# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0

# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
 # --- UVM Report Summary ---
 # ** Report counts by severity
 # UVM_INFO :
# UVM_WARNING: 0
# UVM_ERROR: 0
# UVM_FATAL: 0
# ** Report counts by id
     [Questa UVM]
       [REPORT]
      [RNTST]
      [TEST_DONE]
[run_phase]
       ** Note: $finish
                                                      : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
# Time: 2410 ns Iteration: 61 Instance: /top
# End time: 21:40:41 on May 01,2025, Elapsed time: 0:00:07
 # Errors: 0, Warnings: 0
 Running simulation with seed 1111
 Reading pref.tcl
```

Figure 7: Transcript : all test cases passed "seed1"

.2 Waveform & Transcript "seed2" Report

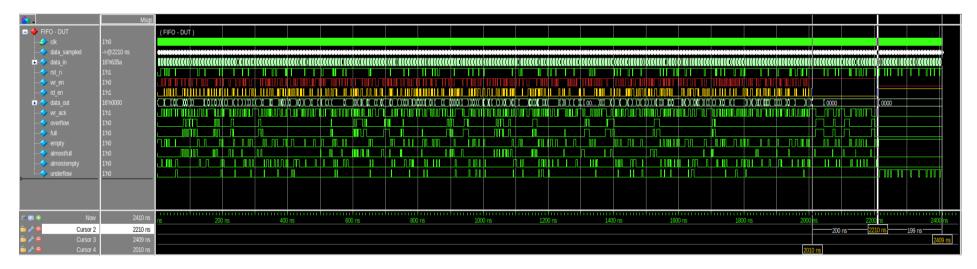


Figure 8: simulation waveform "seed2"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:51:22 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 21:51:22 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:51:22 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIF0_seed1111.ucdb
End time: 21:51:22 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 1511
Reading pref.tcl
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
# --- UVM Report Summary ---
# ** Report counts by severity
# UVM INFO : 8
# UVM WARNING :
# UVM ERROR :
              0
# UVM FATAL :
# ** Report counts by id
# [Questa UVM]
# [REPORT]
# [RNTST]
# [TEST DONE]
# [run phase]
 ** Note: $finish
                  : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh(430)
   Time: 2410 ns Iteration: 61 Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh line 430
```

Figure 9: Transcript : all test cases passed "seed2"

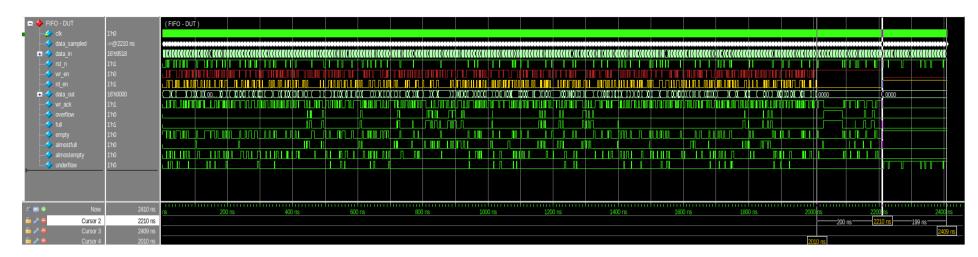


Figure 10: simulation waveform "seed3"

```
Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:55:40 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 21:55:40 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:55:40 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIFO_seed1511.ucdb
End time: 21:55:40 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2515
Reading pref.tcl
# UVM INFO /home/tare/Desktop/syn fifo/uvm verification/FIFO scoreboard pkg.sv(168) @ 2410: uvm test top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
  --- UVM Report Summary ---
# ** Report counts by severity
# UVM INFO :
# UVM_WARNING :
# UVM_ERROR : 0
# UVM_FATAL : 0
  ** Report counts by id
# [Questa UVM]
  [REPORT]
# [RNTST]
  [TEST DONE]
  [run_phase]
  ** Note: $finish
                   : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh(430)
    Time: 2410 ns Iteration: 61 Instance: /top
# Break in Task uvm pkg/uvm root::run test at /usr/local/questasim/linux x86 64/../verilog src/uvm-1.ld/src/base/uvm root.svh line 430
```

Figure 11: Transcript : all test cases passed "seed3"

5.4 Waveform & Transcript "seed4" Report

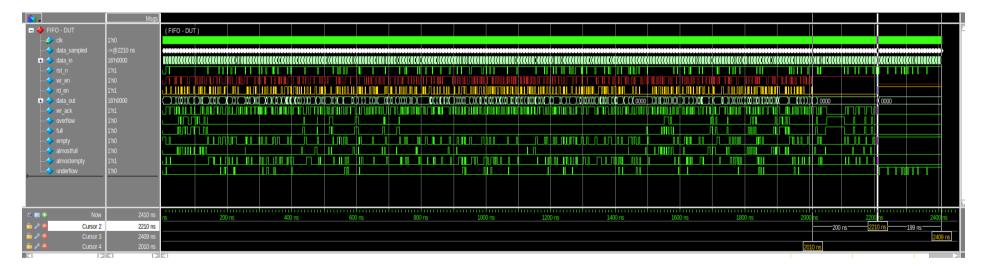


Figure 12: simulation waveform "seed4"

```
Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:58:28 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 21:58:28 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:58:28 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIF0_seed2515.ucdb
End time: 21:58:28 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 2236
Reading pref.tcl
 UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Sum
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
# --- UVM Report Summary --
# ** Report counts by severity
# UVM_INFO : 8
# UVM_WARNING :
# UVM_ERROR : 0
# UVM_FATAL :
              0
# ** Report counts by id
# [Questa UVM]
# [REPORT]
            3
# [RNTST]
            1
# [TEST_DONE]
# [run_phase]
# ** Note: $finish
                   : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh(430)
  Time: 2410 ns Iteration: 61 Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh line 430
VSIM 4>
```

Figure 13: Transcript : all test cases passed "seed4"

5.5 Waveform & Transcript "seed5" Report

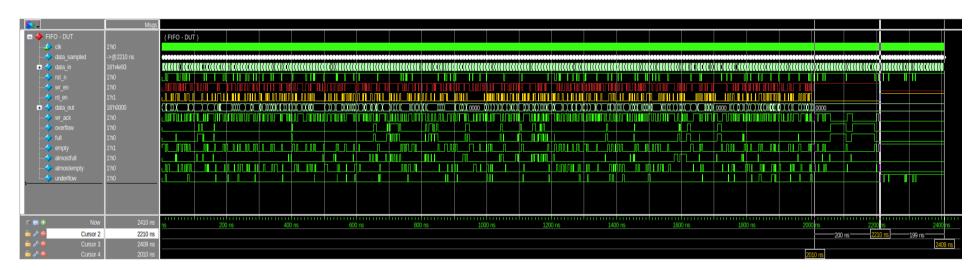


Figure 14: simulation waveform "seed5"

```
Running simulation with seed 2236
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:00:32 on May 01,2025
vcover report FIFO_seed2236.ucdb -details -annotate -all -output code_coverage_rpt_seed2236.txt -du=FIFO
End time: 22:00:32 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:00:32 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2236.txt FIFO_seed2236.ucdb
End time: 22:00:32 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Running simulation with seed 5215
Reading pref.tcl
 UVM INFO /home/tare/Desktop/syn fifo/uvm verification/FIFO scoreboard pkg.sv(169) @ 2410: uvm test top.env.sb [REPORT] Total correct transactions: 1205
 UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
 --- UVM Report Summary ---
 ** Report counts by severity
 UVM INFO: 8
 UVM_WARNING :
 UVM ERROR :
# UVM_FATAL : 0
 ** Report counts by id
 [Questa UVM]
 [REPORT]
# [RNTST]
 [TEST DONE]
 [run_phase]
  ** Note: $finish
                  : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh(430)
   Time: 2410 ns Iteration: 61 Instance: /top
 Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.ld/src/base/uvm_root.svh line 430
```

Figure 15: Transcript : all test cases passed "seed5"

6 Merged Coverage

```
Merging coverage from all seed runs
vcover merge merged.ucdb FIFO_seed*.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:46 on May 01,2025
vcover merge merged.ucdb FIFO_seed1111.ucdb FIFO_seed1511.ucdb FIFO_seed2236.ucdb FIFO_seed2515.ucdb FIFO_seed5215.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Merging file FIFO_seed1111.ucdb
Merging file FIFO_seed1511.ucdb
Merging file FIFO_seed2236.ucdb
Merging file FIFO_seed2515.ucdb
Merging file FIFO_seed5215.ucdb
Writing merged result to merged.ucdb
End time: 22:02:46 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
Reading pref.tcl
# 2021.2_1
# coverage open merged.ucdb
# coverage read -dataset merged merged.ucdb
# merged.ucdb opened as coverage dataset "merged"
# coverage report -output merged_coverage_report.txt -srcfile=* -detail
# quit -f
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:48 on May 01,2025
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
End time: 22:02:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:48 on May 01,2025
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
End time: 22:02:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Coverage merged to merged.ucdb and reports_saved
```

Figure 16: Merge seed



Figure 17: generated files *.ucdb

6.1 Functional Coverage "Merged" Report

Coverage Report by instance with details

== Instance: /FIFO_coverage_pk == Design Unit: work.FIFO_cove					
Covergroup Coverage:					
$\operatorname{Covergroups}$	1	na	na	100.00%	
${ m Coverpoints/Crosses}$	19	na	na	na	
Covergroup Bins	190	190	0	100.00%	

Covergroup	${ m Metric}$	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100		Covered
covered/total bins:	190	190	_	
missing/total bins:	0	190	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	644	1	_	$\operatorname{Covered}$
bin auto[1]	5381	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	976	1	_	$\operatorname{Covered}$
bin auto [1024:2047]	57	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[2048{:}3071 \right]$	62	1	_	$\operatorname{Covered}$
$\operatorname{bin} \ \operatorname{auto} \left[3072 \!:\! 4095 \right]$	64	1	_	$\operatorname{Covered}$
bin auto [4096:5119]	73	1	_	$\operatorname{Covered}$
bin auto [5120:6143]	77	1	_	$\operatorname{Covered}$
bin auto [6144:7167]	60	1	_	$\operatorname{Covered}$
bin auto [7168:8191]	75	1	_	$\operatorname{Covered}$
bin auto [8192:9215]	66	1	_	$\operatorname{Covered}$
bin auto [9216:10239]	62	1	_	Covered

bin auto [10240:11263]	60	1	_	Covered
bin auto [11264:12287]	59	1	_	Covered
bin auto $[12288:13311]$	64	1	_	Covered
bin auto [13312:14335]	62	1	_	Covered
bin auto [14336:15359]	66	1	_	Covered
bin auto $[15360:16383]$	53	1	_	Covered
bin auto [16384:17407]	66	1	_	Covered
•	58			
bin auto [17408:18431]		1	_	Covered
bin auto $[18432:19455]$	79	1	_	$\operatorname{Covered}$
bin auto [19456:20479]	68	1	_	Covered
bin auto $[20480:21503]$	54	1	_	Covered
bin auto [21504:22527]	65	1	_	Covered
bin auto [22528:23551]	72	1	_	Covered
bin auto [23552:24575]	68	1	_	$\operatorname{Covered}$
bin auto [24576:25599]	66	1	_	Covered
bin auto $[25600:26623]$	66	1	_	Covered
bin auto $[26624:27647]$	69	1	_	Covered
bin auto [27648:28671]	78	1	_	Covered
bin auto [28672:29695]	74	1	_	Covered
bin auto [29696:30719]	66	1	_	Covered
bin auto $[30720:31743]$	61	1	_	Covered
bin auto $[31744:32767]$	64	1	_	$\operatorname{Covered}$
bin auto [32768:33791]	77	1	_	Covered
bin auto $[33792:34815]$	61	1	_	Covered
bin auto [34816:35839]	72	1	_	Covered
bin auto 35840:36863	68	1	_	Covered
			_	
bin auto $[36864:37887]$	75	1	_	$\operatorname{Covered}$
bin auto [37888:38911]	70	1	_	Covered
bin auto [38912:39935]	62	1	_	Covered
bin auto $[39936:40959]$	55	1	_	Covered
bin auto [40960:41983]	73	1	_	Covered
bin auto $[41984:43007]$	60	1	_	Covered
bin auto [43008:44031]	70	1	_	Covered
bin auto [44032:45055]	69	1	_	Covered
bin auto $[45056:46079]$	62	1	_	Covered
bin auto [46080:47103]	63	1	_	Covered
		1		
bin auto $[47104:48127]$	62	1	_	Covered
bin auto [48128:49151]	73	1	_	$\operatorname{Covered}$
bin auto [49152:50175]	62	1		Covered
bin auto $[50176:51199]$	65	1	_	Covered
bin auto $[51200:52223]$	69	1	_	$\operatorname{Covered}$
bin auto $[52224:53247]$	70	1		Covered
bin auto $[53248:54271]$	51	1	_	Covered
bin auto $[54272:55295]$	83	1	_	Covered
	70	1		Covered
bin auto $[55296:56319]$			_	
bin auto $[56320:57343]$	60	1	_	Covered
bin auto [57344:58367]	54	1	_	Covered
bin auto $[58368:59391]$	69	1	_	Covered
bin auto [59392:60415]	76	1	_	Covered
bin auto $[60416:61439]$	67	1		Covered
			_	
bin auto $[61440:62463]$	75	1	_	Covered
bin auto [62464:63487]	76	1	_	Covered
bin auto $[63488:64511]$	55	1	_	Covered
bin auto $[64512:65535]$	941	1	_	$\operatorname{Covered}$
Coverpoint r_en_cp	100.00%	100	_	Covered
-				Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
				~ .
bin auto [0]	3991	1	_	$\operatorname{Covered}$
bin auto[1]	2034	1	_	Covered
Coverpoint w_en_cp	100.00%	100		Covered
-			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100		
			_	
$ \text{bin auto} \left[0 \right]$	2017	1	_	Covered
bin auto [1]	4008	1	_	Covered
Coverpoint data_out_cp	100.00%	100		Covered
			_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100		
			_	
bin auto [0:1023]	3334	1	_	Covered
bin auto [1024:2047]	36	1	_	Covered
bin auto [2048:3071]	13	1	_	Covered
bin auto $[3072:4095]$	44	1	_	Covered
bin auto [4096:5119]	53	1	_	Covered
				Covered
bin auto [5120:6143]	57	1	_	
bin auto $[6144:7167]$		1	_	Covered
bin auto [7168:8191]	48		_	Covered
		l l		
hin auto[0100.001E]	50	1	_	Covered
bin auto [8192:9215]	50 43	1		
bin auto [8192:9215] bin auto [9216:10239]	50		_	Covered
bin auto [9216:10239]	$50 \\ 43 \\ 27$	1 1	_	
bin auto [9216:10239] bin auto [10240:11263]	$50 \\ 43 \\ 27 \\ 44$	1 1 1	_	Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287]	50 43 27 44 44	1 1 1 1		$\begin{array}{c} \text{Covered} \\ \text{Covered} \end{array}$
bin auto [9216:10239] bin auto [10240:11263]	$50 \\ 43 \\ 27 \\ 44$	1 1 1	_	Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311]	50 43 27 44 44 33	1 1 1 1	_ _	Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335]	50 43 27 44 44 33 34	1 1 1 1 1	- - -	Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359]	50 43 27 44 44 33 34 25	1 1 1 1 1 1	_ _ _	Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335]	50 43 27 44 44 33 34	1 1 1 1 1	- - -	Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383]	50 43 27 44 44 33 34 25 21	1 1 1 1 1 1 1	- - - -	Covered Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407]	50 43 27 44 44 33 34 25 21	1 1 1 1 1 1 1 1	- - - - -	Covered Covered Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431]	50 43 27 44 44 33 34 25 21 17	1 1 1 1 1 1 1 1 1	- - - -	Covered Covered Covered Covered Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407]	50 43 27 44 44 33 34 25 21	1 1 1 1 1 1 1 1	- - - - -	Covered Covered Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455]	50 43 27 44 44 33 34 25 21 17 19 51	1 1 1 1 1 1 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479]	50 43 27 44 44 33 34 25 21 17 19 51 25	1 1 1 1 1 1 1 1 1 1	- - - - - -	Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503]	50 43 27 44 44 43 33 34 25 21 17 19 51 25 39	1 1 1 1 1 1 1 1 1 1 1	- - - - - -	Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479]	50 43 27 44 44 33 34 25 21 17 19 51 25	1 1 1 1 1 1 1 1 1 1	- - - - - -	Covered
bin auto [9216:10239] bin auto [10240:11263] bin auto [11264:12287] bin auto [12288:13311] bin auto [13312:14335] bin auto [14336:15359] bin auto [15360:16383] bin auto [16384:17407] bin auto [17408:18431] bin auto [18432:19455] bin auto [19456:20479] bin auto [20480:21503]	50 43 27 44 44 43 33 34 25 21 17 19 51 25 39	1 1 1 1 1 1 1 1 1 1 1	- - - - - -	Covered

bin auto[22528:23551]	0	1		Covered
bin auto $[23552:24575]$	$9 \\ 21$	1 1	_	Covered
bin auto [24576:25599]	37	1		Covered
bin auto [25600:26623]	38	1		Covered
bin auto [26624:27647]	35	1	_	Covered
bin auto [27648:28671]	52	1	_	Covered
bin auto [28672:29695]	44	1	_	Covered
bin auto [29696:30719]	31	1	_	Covered
bin auto [30720:31743]	29	1	_	Covered
bin auto [31744:32767]	25	1	_	Covered
bin auto [32768:33791]	46	1	_	Covered
bin auto [33792:34815]	38	1	_	Covered
bin auto [34816:35839]	41	1	_	Covered
bin auto $[35840:36863]$	37	1	_	Covered
bin auto $[36864:37887]$	26	1	_	Covered
bin auto [37888:38911]	32	1	_	Covered
bin auto [38912:39935]	50	1	_	Covered
bin auto $[39936:40959]$	30	1	_	Covered
bin auto [40960:41983]	31	1	_	Covered
bin auto [41984:43007]	33	1	_	Covered
bin auto [43008:44031]	45	1	_	Covered
bin auto [44032:45055]	29	1	_	Covered
bin auto [45056:46079]	26	1	_	Covered Covered
bin auto [46080:47103] bin auto [47104:48127]	$\begin{array}{c} 47 \\ 11 \end{array}$	1 1	_	Covered
bin auto $[47104:48127]$	$\frac{11}{32}$	1	_	Covered
bin auto $[49152:50175]$	28	1	_	Covered
bin auto [50176:51199]	$\frac{25}{25}$	1		Covered
bin auto $[51200:52223]$	61	1	_	Covered
bin auto $[52224:53247]$	$\frac{01}{22}$	1	_	Covered
bin auto $[53248:54271]$	18	1	_	Covered
bin auto $[54272:55295]$	47	1	_	Covered
bin auto [55296:56319]	60	1	_	Covered
bin auto [56320:57343]	41	1	_	Covered
bin auto [57344:58367]	17	1	_	Covered
bin auto [58368:59391]	44	1	_	Covered
bin auto [59392:60415]	82	1	_	Covered
bin auto [60416:61439]	31	1	_	Covered
bin auto [61440:62463]	52	1	_	Covered
bin auto $[62464:63487]$	32	1	_	Covered
bin auto $[63488:64511]$	21	1	_	$\operatorname{Covered}$
bin auto $[64512:65535]$	484	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	G 1
bin auto[0]	2943	1	_	Covered
bin auto[1]	3082	1	_	Covered
Coverpoint overflow_cp	100.00%	100 2	_	Covered
covered/total bins:	0	$\frac{2}{2}$	_	
missing/total bins: % Hit:	100.00%	100	_	
bin auto [0]	5457	100		Covered
bin auto[1]	568	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	00101
missing/total bins:	0	$\frac{-}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	5338	1	_	Covered
bin auto[1]	687	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto $[0]$	4632	1	_	Covered
bin auto[1]	1393	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	100.00%	2	_	
% Hit: bin auto[0]	$100.00\% \ 5570$	100 1	_	Covered
bin auto[1]	$\frac{3570}{455}$	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	$\frac{100}{2}$	_	Covered
missing/total bins:	0	$\overset{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	5044	1	_	Covered
bin auto[1]	981	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	5306	1	_	Covered
bin auto [1]	719	1	_	Covered
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	000	1		Ca 1
bin $<$ auto[1], auto[1], auto[1]>	892 216	1	_	Covered
bin $<$ auto[1], auto[1], auto[0]>	$\frac{216}{2190}$	1 1	_	Covered Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right] >$	2190	1	_	Covered

bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[0],>	710 926	1 1	_ _	Covered Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	1091	1	_	Covered
ignore_bin w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins: bin $<$ auto $[0]$, auto $[1]$, auto $[1]$	613	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	74	1	_	Covered
bin < auto[1], auto[1], auto[0] >	1108	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$926 \\ 2287$	1	_	Covered Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	1017	1	_	Covered
Illegal and Ignore Bins:				TIDD O
ignore_bin r_en_actv_wr_full ignore_bin w_en_r_en_allactv_full	0		_	ZERO ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins: % Hit:	$0 \\ 100.00\%$	$6 \\ 100$	_	
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto [1]="" [1],="" auto=""></auto>	126	1	_	Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	$667 \\ 982$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	2601	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right], \operatorname{auto} \left[0\right] >$	259	1	_	Covered
$\begin{array}{c} \text{bin } < \text{auto} \left[0 \right], \text{auto} \left[0 \right], \text{auto} \left[0 \right] > \\ \text{Illegal and Ignore Bins:} \end{array}$	790	1	_	$\operatorname{Covered}$
ignore_bin read_nactv_empty	600		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	$\frac{6}{0}$	6 6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	$\begin{array}{c} 171 \\ 37 \end{array}$	1 1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[1 ight] > \ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \end{aligned}$	937	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	2737	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	889	1	_	Covered
bin $<$ auto $[0]$, auto $[0]$, auto $[0]$ > Illegal and Ignore Bins:	1007	1	_	Covered
ignore_bin w_en_nactv_almostfull	247		_	Occurred
Cross almostempty_cross	100.00%	100	_	$\operatorname{Covered}$
<pre>covered/total bins: missing/total bins:</pre>	6 0	6 6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	270			
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] \ > \ \end{aligned} \\ ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] \ > \end{aligned}$	$\begin{array}{c} 350 \\ 758 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	401	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right]$, $\operatorname{auto} \left[1\right]$, $\operatorname{auto} \left[0\right] >$	2499	1	_	Covered
$egin{aligned} & ext{bin } < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \ & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	867 920	1 1	_	Covered Covered
Illegal and Ignore Bins:	320	1		Covered
ignore_bin w_en_nactv_almostempty	230	1.00	_	Occurred
Cross overflow_cross covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	$\operatorname{Covered}$
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	109	1		Covered
$egin{aligned} ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [1] > \ \end{aligned} \\ ext{bin} & < ext{auto} [1] \ , ext{auto} [1] \ , ext{auto} [0] > \end{aligned}$	999	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[1\right] >$	459	1	_	Covered
$egin{aligned} ext{bin } & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ \end{aligned} \\ ext{bin } & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\begin{array}{c} 2441 \\ 926 \end{array}$	1 1	_	Covered Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	1091	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack Cross underflow_cross	$0 \\ 100.00\%$	100	_	ZERO Covered
covered/total bins:	100.00%	$\begin{array}{c} 100 \\ 6 \end{array}$	_	Covered
missing/total bins:	0	6	_	
% Hit: Auto, Default and User Defined Bins:	100.00%	100	_	
Auto, Default and User Defined Bins: bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	208	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[1]$, $\operatorname{auto}[0]$, $\operatorname{auto}[1] >$	511	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	900	1	_	Covered Covered
$egin{aligned} ext{bin} & < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ \end{aligned} \\ ext{bin} & < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	$\begin{array}{c} 2900 \\ 415 \end{array}$	1	_	Covered Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[0\right]\!>$	1091	1	_	Covered
Illegal and Ignore Bins:	0			7FDO
ignore_bin r_en_nactv_wr_ack	0		_	ZERO
ERGROUP COVERAGE:				
vergroup	Metric	Goal	Bins	Status
•		J. 2 W.		
PE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100		Covered
covered/total bins:	190	190	_	

missing/total bins:	0	190	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins: missing/total bins:	$\frac{2}{0}$	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	644	1	_	Covered
bin auto[1] Coverpoint data_in_cp	$5381 \\ 100.00\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
covered/total bins:	64	64	_	Covered
missing/total bins:	0	64	_	
% Hit: bin auto[0:1023]	$100.00\% \ 976$	$100 \\ 1$	_	Covered
bin auto $[1024:2047]$	57	1	_	Covered
bin auto [2048:3071]	62	1	_	Covered
bin auto $[3072:4095]$ bin auto $[4096:5119]$	64 73	1 1	_	Covered Covered
bin auto [5120:6143]	77	1	_	Covered
bin auto [6144:7167]	60	1	_	Covered
bin auto [7168:8191] bin auto [8192:9215]	75 66	1 1	_	Covered Covered
bin auto $[9216:10239]$	62	1	_	Covered
bin auto [10240:11263]	60	1	_	Covered
bin auto [11264:12287] bin auto [12288:13311]	$\frac{59}{64}$	1 1	_	Covered Covered
bin auto[13312:14335]	62	1	_	Covered
bin auto [14336:15359]	66	1	_	Covered
bin auto [15360:16383] bin auto [16384:17407]	$\frac{53}{66}$	1 1	_	Covered Covered
bin auto[10384.17407] bin auto[17408:18431]	58	1	_	Covered
bin auto [18432:19455]	79	1	_	Covered
bin auto [19456:20479]	68	1	_	Covered
$egin{array}{ll} ext{bin} & ext{auto} \left[20480 {:} 21503 ight] \ ext{bin} & ext{auto} \left[21504 {:} 22527 ight] \end{array}$	$\frac{54}{65}$	1 1	_	Covered Covered
bin auto [22528:23551]	72	1	_	Covered
bin auto [23552:24575]	68	1	_	Covered
$egin{array}{ll} ext{bin auto} \left[24576 {:} 25599 ight] \ ext{bin auto} \left[25600 {:} 26623 ight] \end{array}$	66 66	1 1	_	Covered Covered
bin auto [26624:27647]	69	1	_	Covered
bin auto [27648:28671]	78	1	_	Covered
$egin{array}{ll} ext{bin auto} \left[28672 {:} 29695 ight] \ ext{bin auto} \left[29696 {:} 30719 ight] \end{array}$	74 66	1 1	_	Covered Covered
bin auto [30720:31743]	61	1	_	Covered
bin auto [31744:32767]	64	1	_	Covered
$\begin{array}{ll} \text{bin auto} \left[32768; 33791 \right] \\ \text{bin auto} \left[33792; 34815 \right] \end{array}$	77 61	1 1	_	Covered Covered
bin auto [34816:35839]	72	1	_	Covered
bin auto [35840:36863]	68	1	_	Covered
bin auto [36864:37887] bin auto [37888:38911]	$\begin{array}{c} 75 \\ 70 \end{array}$	1 1	_	Covered Covered
bin auto [38912:39935]	62	1	_	Covered
bin auto $[39936:40959]$	55	1	_	Covered
$egin{array}{ll} ext{bin auto} & [40960:41983] \ ext{bin auto} & [41984:43007] \end{array}$	$\begin{array}{c} 73 \\ 60 \end{array}$	1 1	_	Covered Covered
bin auto [43008:44031]	70	1	_	Covered
bin auto [44032:45055]	69	1	_	Covered
$egin{array}{ll} ext{bin} & ext{auto} [45056{:}46079] \ ext{bin} & ext{auto} [46080{:}47103] \end{array}$	62 63	1 1	_	Covered Covered
bin auto [47104:48127]	62	1	_	Covered
bin auto [48128:49151]	73	1	_	Covered
$egin{array}{ll} ext{bin auto} & [49152{:}50175] \ ext{bin auto} & [50176{:}51199] \end{array}$	62 65	1 1	_	Covered Covered
bin auto [51200:52223]	69	1	_	Covered
bin auto [52224:53247]	70	1	_	Covered
$egin{array}{ll} { m bin \ auto} [53248;54271] \ { m bin \ auto} [54272;55295] \end{array}$	51 83	1 1	_	Covered Covered
bin auto [55296:56319]	70	1	_	Covered
bin auto [56320:57343]	60	1	_	Covered
$egin{array}{ll} { m bin \ auto} [57344{:}58367] \ { m bin \ auto} [58368{:}59391] \end{array}$	54 69	1 1	_	Covered Covered
bin auto[59392:60415]	76	1	_	Covered
bin auto [60416:61439]	67	1	_	Covered
bin auto [61440:62463] bin auto [62464:63487]	$\begin{array}{c} 75 \\ 76 \end{array}$	1 1	_	Covered Covered
bin auto [63488:64511]	55	1	_	Covered
bin auto [64512:65535]	941	1	_	Covered
Coverpoint r_en_cp covered/total bins:	100.00%	$100 \\ 2$	_	Covered
missing/total bins:	0 = 0	$\frac{2}{2}$	_	
% Hit:	100.00%	100	_	
bin auto[0]	3991	1	_	Covered
bin auto[1] Coverpoint w_en_cp	$2034 \\ 100.00\%$	$\begin{matrix} 1 \\ 100 \end{matrix}$	_	Covered Covered
covered/total bins:	2	2	_	55.0104
missing/total bins:	100.00%	100	_	
% Hit: bin auto [0]	$100.00\%\ 2017$	100 1	_	Covered
bin auto[1]	4008	1	_	Covered
Coverpoint data_out_cp	100.00%	100	_	Covered
<pre>covered/total bins: missing/total bins:</pre>	$\begin{array}{c} 64 \\ 0 \end{array}$	64 64	_	
% Hit:	100.00%	100	_	

1. [0.1020]	2224	4		0 1
bin auto [0:1023]	3334	1	_	Covered
bin auto [1024:2047]	36	1	_	Covered
bin auto [2048:3071]	13	1	_	Covered
bin auto [3072:4095]	44	1	_	Covered
bin auto $[4096:5119]$	53	1	_	Covered
bin auto [5120:6143]	57	1	_	Covered
bin auto [6144:7167]	48	1	_	Covered
bin auto [7168:8191]	50	1	_	Covered
bin auto [8192:9215]	43	1	_	Covered
bin auto [9216:10239]	27	1	_	Covered
bin auto [10240:11263]	44	1	_	Covered
bin auto [11264:12287]	44	1	_	Covered
bin auto [12288:13311]	33	1	_	Covered
bin auto [13312:14335]	34	1	_	Covered
bin auto [14336:15359]	25	1	_	Covered
bin auto [15360:16383]	21	1	_	Covered
bin auto [16384:17407]	17	1	_	Covered
bin auto [17408:18431]	19	1	_	Covered
bin auto [18432:19455]	51	1	_	Covered
bin auto [19456:20479]	$\frac{31}{25}$	1	_	Covered
bin auto [20480:21503]	39	1	_	Covered
· ·				
bin auto [21504:22527]	28	1	_	Covered
bin auto [22528:23551]	9	1	_	Covered
bin auto [23552:24575]	21	1	_	Covered
bin auto [24576:25599]	37	1	_	Covered
bin auto $[25600:26623]$	38	1	_	Covered
$\operatorname{bin} \ \operatorname{auto} \left[26624 \colon\! 27647 \right]$	35	1	_	$\operatorname{Covered}$
bin auto $[27648:28671]$	52	1	_	Covered
bin auto $[28672:29695]$	44	1	_	$\operatorname{Covered}$
bin auto $[29696:30719]$	31	1	_	$\operatorname{Covered}$
bin auto [30720:31743]	29	1	_	Covered
bin auto [31744:32767]	25	1	_	Covered
bin auto [32768:33791]	46	1	_	Covered
bin auto [33792:34815]	38	1	_	Covered
bin auto [34816:35839]	41	1	_	Covered
bin auto [35840:36863]	37	1	_	Covered
bin auto [36864:37887]	26	1	_	Covered
bin auto [37888:38911]	$\frac{20}{32}$	1	_	Covered
bin auto [38912:39935]	50	1		Covered
bin auto [39936:40959]	30	1		Covered
bin auto [40960:41983]	31	1		Covered
	33	1	_	Covered
bin auto [41984:43007]			_	
bin auto [43008:44031]	45	1	_	Covered
bin auto [44032:45055]	29	1	_	Covered
bin auto [45056:46079]	26	1	_	Covered
bin auto [46080:47103]	47	1	_	Covered
bin auto $[47104:48127]$	11	1	_	Covered
bin auto $[48128:49151]$	32	1	_	Covered
bin auto $[49152:50175]$	28	1	_	$\operatorname{Covered}$
bin auto $[50176:51199]$	25	1	_	$\operatorname{Covered}$
${ m bin \ auto} [51200 \!:\! 52223]$	61	1	_	$\operatorname{Covered}$
bin auto [52224:53247]	22	1	_	Covered
bin auto $[53248:54271]$	18	1	_	Covered
bin auto $[54272:55295]$	47	1	_	Covered
bin auto $[55296:56319]$	60	1	_	Covered
bin auto $[56320:57343]$	41	1	_	Covered
bin auto [57344:58367]	17	1	_	Covered
bin auto [58368:59391]	44	1	_	Covered
bin auto [59392:60415]	82	1	_	Covered
bin auto [60416:61439]	31	1	_	Covered
bin auto [61440:62463]	52	1	_	Covered
bin auto [62464:63487]	32	1	_	Covered
bin auto [63488:64511]	21	1	_	Covered
bin auto [64512:65535]	484	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100	_	
bin auto [0]	2943	1	_	Covered
bin auto [1]	3082	1		Covered
Coverpoint overflow_cp	100.00%	100		Covered
covered/total bins:	100.0070	$\frac{100}{2}$		Covered
	0 = 0	$\frac{2}{2}$	_	
missing/total bins:	100.00%	$\frac{2}{100}$	_	
% Hit: bin auto [0]	5457	100	_	Covered
			_	
bin auto[1]	568	1	_	Covered
Coverpoint full_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	5338	1	_	Covered
bin auto[1]	687	1	_	Covered
Coverpoint empty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
${\rm bin \ auto} [0]$	4632	1	_	Covered
bin auto [1]	1393	1	_	Covered
Coverpoint almostfull_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	

bin auto [0]				
1 [4]	5570	1	_	Covered
bin auto[1]	455	1	_	Covered
Coverpoint almostempty_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	$\frac{1}{2}$	_	
% Hit:	100.00%	100	_	
	5044		_	Covered
bin auto [0]		1	_	
bin auto[1]	981	1	_	Covered
Coverpoint underflow_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto[0]	5306	1	_	Covered
t ,				Covered
bin auto[1]	719	1	_	
Cross wr_ack_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$	892	1	_	Covered
	$\begin{array}{c} 332 \\ 216 \end{array}$			Covered
bin < auto[1], auto[1], auto[0] >		1	_	
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight]>$	2190	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[0 \right] \! > \!$	710	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	926	1	_	$\operatorname{Covered}$
bin < auto[0], auto[0], auto[0] >	1091	1	_	Covered
Illegal and Ignore Bins:				
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100		Covered
		100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin $<$ auto [0], auto [1], auto [1]>	613	1		Covered
$\operatorname{bin}\ < \operatorname{auto}\left[0 ight], \operatorname{auto}\left[0 ight], \operatorname{auto}\left[1 ight]>$	74	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right]\!>$	1108	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[0], \operatorname{auto}[0] >$	926	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto} \left[0\right], \operatorname{auto} \left[1\right], \operatorname{auto} \left[0\right] >$	2287	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	1017	1	_	Covered
Illegal and Ignore Bins:	1011	1		Covered
	0			ZEDO
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	0		_	ZERO
Cross empty_cross	100.00%	100	_	$\operatorname{Covered}$
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:	100.0070	100		
	100	1		C 1
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right], \operatorname{auto} \left[1 \right] >$	126	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[0\right], \mathrm{auto} \left[1\right]\!>$	667	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto}[1], \operatorname{auto}[1], \operatorname{auto}[0] >$	982	1	_	$\operatorname{Covered}$
$\operatorname{bin} < \operatorname{auto} [0], \operatorname{auto} [1], \operatorname{auto} [0] >$	2601	1	_	$\operatorname{Covered}$
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$	259	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	790	1		Covered
		1		Covered
Illegal and Ignore Bins:				
Illegal and Ignore Bins: ignore_bin read_nactv_empty	600		_	Occurred
Illegal and Ignore Bins:		100	_ _	Occurred Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross	600	100 6	_ _ _	
Illegal and Ignore Bins:	$600 \\ 100.00\%$	6	_ _ _ _	
Illegal and Ignore Bins:	$600 \\ 100.00\% \\ 6 \\ 0$	6 6	- - - -	
Illegal and Ignore Bins:	$600 \\ 100.00\% \\ 6$	6	- - - -	
Illegal and Ignore Bins:	$600 \\ 100.00\% \\ 6 \\ 0 \\ 100.00\%$	6 6 100	- - - -	Covered
<pre>Illegal and Ignore Bins:</pre>	$600 \\ 100.00\% \\ 6 \\ 0 \\ 100.00\% $	$ \begin{array}{c} 6 \\ 6 \\ 100 \end{array} $	- - - - -	$\operatorname{Covered}$
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- - - - -	Covered Covered Covered
<pre>Illegal and Ignore Bins:</pre>	$600 \\ 100.00\% \\ 6 \\ 0 \\ 100.00\% $	$ \begin{array}{c} 6 \\ 6 \\ 100 \end{array} $	- - - - -	$\operatorname{Covered}$
<pre>Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></pre>	600 $100.00%$ 6 0 $100.00%$ 171 37	$\begin{array}{c} 6 \\ 6 \\ 100 \\ \end{array}$	- - - - - -	Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937	6 6 100 1 1 1	- - - - - - -	Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889	6 6 100 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737	6 6 100 1 1 1	- - - - - - - -	Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007	6 6 100 1 1 1 1	- - - - - - -	Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostfull</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007	6 6 100 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007	6 6 100 1 1 1 1		Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostfull</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007	6 6 100 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross</auto[0],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007	6 6 100 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0	6 6 100 1 1 1 1 1 1 1 1 1 1 1 6 6		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6	6 6 100 1 1 1 1 1 1 1 1 1 1 0 6		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> covered/total bins: covered/total bins:</auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> coveries auto[0], auto[0]> coveries auto[0], auto[0]> coveries auto[0], auto[0]> coveries a</auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: wising/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostempty</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], au<="" auto[0],="" td=""><td>600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6</td><td>6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1</td><td></td><td>Covered Covered Covered</td></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin read_nactv_empty Cross almostfull_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_almostfull Cross almostempty_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins:	600 $100.00%$ 6 0 $100.00%$ 171 37 937 2737 889 1007 247 $100.00%$ 6 0 $100.00%$ 350 758 401 2499 867 920 230 $100.00%$ 6 0 $100.00%$ $100.00%$	6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

```
ignore_bin w_en_nactv_wr_ack
                                                                                                                                                    ZERO
                                                                                                   0
                                                                                         100.00\%
                                                                                                                    100
Cross underflow_cross
                                                                                                                                                    Covered
      covered/total bins:
                                                                                                   6
                                                                                                                       6
      missing/total bins:
                                                                                                   0
                                                                                                                       6
      \% Hit:
                                                                                         100.00\%
                                                                                                                    100
      Auto, Default and User Defined Bins:
                                                                                                                                                    Covered
             \label{eq:bin_section} \mbox{bin } < \mbox{auto} \, [\, 1\, ] \,\, , \, \mbox{auto} \, [\, 1\, ] \,\, , \, \mbox{auto} \, [\, 1\, ] >
                                                                                                208
                                                                                                                       1
             bin <auto [1], auto [1], auto [1] >
bin <auto [1], auto [0], auto [1] >
bin <auto [1], auto [1], auto [0] >
bin <auto [0], auto [1], auto [0] >
bin <auto [1], auto [0], auto [0] >
                                                                                                511
                                                                                                                                                    Covered
                                                                                                                       1
                                                                                                900
                                                                                                                                                    Covered
                                                                                                                       1
                                                                                              2900
                                                                                                                                                    Covered
                                                                                                                       1
                                                                                                                                                    Covered
                                                                                               415
                                                                                                                       1
             bin \langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle
                                                                                              1091
                                                                                                                                                    Covered
                                                                                                                       1
      Illegal and Ignore Bins:
                                                                                                   0
                                                                                                                                                    ZERO
             ignore\_bin \quad r\_en\_nactv\_wr\_ack
```

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%

6.2 Code Coverage "Merged" Report

Coverage Report by DU with details

Coverag	ge Report by DU with d	etails		
De	esign Unit: work.FIFO			
	Coverage: abled Coverage	Bins Hit	ts Misses	s Coverage
$\overline{ m Br}$	anches	$\frac{}{25}$ $\frac{}{2}$	25 0	$0 - \frac{100.00\%}{}$
		Branch Details		
Branch	Coverage for Design U	Jnit work.FIFO		
Lir	ne Item	Coun	$_{ m nt}$ Source	ce
File	/home/tare/Desktop/sy		ation/FIFO_v	$v1.0.0.\mathrm{sv}$
13		IF Branch658	Count	t coming in to IF
13	1	120	06 i f	f (!fifo_intf.rst_n) begin
18		308		lse if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
23 Branch	totals: 3 hits of 3 b	pranches = 100.00%	9 e1s	lse begin
		IF Branch-		
25 25		229		t coming in to IF
$\begin{array}{c} 25 \\ 27 \end{array}$	1	50 179		if (fifo_intf.full & fifo_intf.wr_en) else
	totals: 2 hits of 2 be			
22		IF Branch	Count	t coming in to ID
$\frac{33}{33}$		$658 \\ 120$		t coming in to IF f (!fifo_intf.rst_n) begin
38		115	els els	lse if (fifo_intf.rd_en && count != 0) begin
42Branch	totals: 3 hits of 3 b	$\begin{array}{c} 422 \\ \text{oranches} = 100.00\% \end{array}$	els	lse begin
		IF Branch		
43		422		t coming in to IF
43 45	1	66 356		if (fifo_intf.empty & fifo_intf.rd_en)
	totals: 2 hits of 2 b		4	${ m else}$
		IF Branch		
51		555	7 Count	t coming in to IF
51	1	116		f (!fifo_intf.rst_n) begin
54 Branch	totals: 2 hits of 2 b	439 pranches = 100 00%	-1 els	lse begin
Бтансп	totals. 2 mits of 2 b.			
55		IF Branch439	Ount Count	t coming in to IF
55		219	90	if ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fr
57	1	33		else if (({fifo_intf.wr_en, fifo_intf.rd_en}) == 2'b01) &&!fifo_intf.er
59 61	I 1	$9\\16$	90 31	else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.fu else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.em
01	1	161		False Count
Branch	totals: 5 hits of 5 b	ranches=100.00%		
		IF Branch		
66 66		$\frac{326}{20}$		t coming in to IF gn fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
66		$\frac{20}{306}$	9	$\operatorname{Fifo}_{\operatorname{-intf}}$: 1 : 0; $\operatorname{Fifo}_{\operatorname{-intf}}$: full = (count == FIFO_DEPTH)? 1 : 0;
	totals: 2 hits of 2 b			
		IF Branch-		
67		439		t coming in to IF
67 67	$\frac{1}{2}$	$ \begin{array}{r} 169 \\ 270 \end{array} $		$ \operatorname{fifo_intf.empty} = (\operatorname{count} = 0 \mid !\operatorname{fifo_intf.rst_n})? \ 1 : 0; $ $ \operatorname{fifo_intf.empty} = (\operatorname{count} = 0 \mid !\operatorname{fifo_intf.rst_n})? \ 1 : 0; $
	totals: 2 hits of 2 b		o assign	

-IF Branch-

```
1
                                                         assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                                                290
    68
                     2
                                               2977
                                                         assign fifo_intf.almostfull = (count \Longrightarrow FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00\%
                                      -IF Branch
    69
                                               3267
                                                         Count coming in to IF
    69
                     1
                                                621
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
                                               2646
                     ^{2}
                                                         assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
Branch totals: 2 hits of 2 branches = 100.00%
Condition Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                            Covered
                                                        Misses
                                                                 Coverage
                                                             2
    Conditions
                                       25
                                                  23
                                                                   92.00\%
                                  =Condition Details=
Condition Coverage for Design Unit work.FIFO —
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                -Focused Condition View-
Line
                     1 (fifo_intf.wr_en && (count < 8))
           18 Item
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                          Hint
                           Y
  fifo_intf.wr_en
      (count < 8)
                           Y
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
                        fifo_intf.wr_en_0
  Row
        1:
                     5
  Row
        2:
                        fifo_intf.wr_en_1
                                                 (count < 8)
                     5
  Row
        3:
                        (count < 8)_{-0}
                                                 fifo_intf.wr_en
                     5
                        (count < 8)_{-1}
                                                 fifo_intf.wr_en
  Row
        4:
                     5
                 -Focused Condition View-
Line
           25 Item
                     1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%
                     Covered Reason for no coverage
       Input Term
                                                          Hint
                               ^{\prime}_{-0} or not hit
                                                          Hit '_0'
   fifo_intf.full
                           Ν
  fifo_intf.wr_en
                            Y
                  _{
m Hits}
                                                Non-masking condition(s)
     Rows:
                       FEC Target
               ***0***
                        fifo_intf.full_0
                                                 fifo_intf.wr_en
 Row
        1:
  Row
                     5
                        fifo_intf.full_1
                                                 fifo_intf.wr_en
  Row
        3:
                        fifo_intf.wr_en_0
                                                 fifo_intf.full
                        fifo_intf.wr_en_1
                                                 fifo_intf.full
  Row
        4:
                 \operatorname{-Focused} Condition View-
           38 Item
                      1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                           Y
  fifo_intf.rd_en
     (count != 0)
                            Y
     Rows:
                  Hits FEC Target
                                                Non-masking condition(s)
                        fifo_intf.rd_en_0
  Row
        1:
  Row
        2:
                        fifo_intf.rd_{en_1}
                                                 (count != 0)
                        (count != 0)_{-0}
                                                 fifo_intf.rd_en
  Row
        3:
                        (count != 0)_{-1}
  Row
        4:
                                                 fifo_intf.rd_en
                 \hbox{-}Focused \quad Condition \quad View-
           43 Item 1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%
                     Covered Reason for no coverage
       Input Term
                                                          _{\mathrm{Hint}}
  fifo_intf.empty
                                                          Hit '_0'
                           Ν
                              ^{\prime}_{-0} on not hit
  fifo_intf.rd_en
                            Y
                  Hits FEC Target
                                                Non-masking condition(s)
     Rows:
 Row
        1:
               ***0***
                        fifo_intf.empty_0
                                                 fifo_intf.rd_en
        2:
                        fifo_intf.empty_1
                                                 fifo_intf.rd_en
 Row
                     5
        3:
                        fifo_intf.rd_en_0
                                                 fifo_intf.empty
 Row
                     5
                                                 fifo_intf.empty
 Row
        4:
                     5
                        fifo_intf.rd_en_1
                 -Focused Condition View-
Line
                       1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%
                    Covered Reason for no coverage
       Input Term
                                                          Hint
```

Count coming in to IF

3267

68

```
Y
  fifo_intf.wr_en
   fifo_intf.full
                            Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
                                                 (~fifo_intf.full && fifo_intf.wr_en)
  Row
                         fifo_intf.rd_en_0
        1:
                     5
  Row
        2:
                     5
                         fifo_intf.rd_en_1
                                                 \tilde{f} if o_intf.rd_en
                         fifo_intf.wr_en_0
  Row
        3:
                     5
                                                 (~fifo_intf.full && ~fifo_intf.rd_en)
                         fifo_intf.wr_en_1
  Row
        4:
                     5
                         fifo_intf.full_0
                                                 (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
                     5
        6:
                         fifo_intf.full_1
                                                 (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                     5
                 -Focused Condition View-
           57 Item
                       1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
  fifo_intf.rd_en
                            Y
                            Y
  fifo_intf.wr_en
                            Υ
  fifo_intf.empty
                        FEC Target
     Rows:
                  _{
m Hits}
                                                 Non-masking condition(s)
  Row
        1:
                     5
                         fifo_intf.rd_en_0
        2:
                         fifo_intf.rd_en_1
                                                 (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row
                     5
                                                 ( \tilde{\text{fifo}}_{\text{intf}} .empty && fifo_intf.rd_en)
  Row
        3:
                         fifo_intf.wr_en_0
                     5
  Row
        4:
                         fifo_intf.wr_en_1
                                                 fifo_intf.rd_en
                     5
                         fifo_intf.empty_0
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row
        5:
                     5
                                                 (fifo_intf.rd_en && ~fifo_intf.wr_en)
        6:
                         fifo_intf.empty_1
  Row
                     5
                 -Focused Condition View—
           59 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Line
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered Reason for no coverage
                                                           Hint
                            Y
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
   fifo_intf.full
                            Y
     Rows:
                  _{
m Hits}
                        FEC Target
                                                 Non-masking condition(s)
  Row
        1:
                     5
                         fifo_intf.rd_en_0
  Row
        2:
                         fifo_intf.rd_en_1
                                                 (fifo_intf.full && fifo_intf.wr_en)
                     5
  Row
        3:
                         fifo_intf.wr_en_0
                                                 fifo_intf.rd_en
                     5
  Row
        4:
                         fifo_intf.wr_en_1
                                                 (fifo_intf.full && fifo_intf.rd_en)
  Row
        5:
                         fifo_intf.full_0
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
                     5
                         fifo_intf.full_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
                 \operatorname{-Focused} Condition View-
Line
           61 Item
                       1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%
       Input Term
                     Covered
                               Reason for no coverage
                                                           Hint
  fifo_intf.rd_en
                            Y
  fifo_intf.wr_en
                            \mathbf{Y}
                            Y
  fifo_intf.empty
     Rows:
                        FEC Target
                                                 Non-masking condition(s)
                  _{
m Hits}
  Row
         1:
                         fifo_intf.rd_en_0
                                                 (fifo_intf.empty && fifo_intf.wr_en)
                         fifo_intf.rd_en_1
  Row
                         fifo_intf.wr_en_0
  Row
        3:
                                                 fifo_intf.rd_en
  Row
        4:
                         fifo_intf.wr_en_1
                                                 (fifo_intf.empty && fifo_intf.rd_en)
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        5:
                         fifo_intf.empty_0
                         fifo_intf.empty_1
                                                 (fifo_intf.rd_en && fifo_intf.wr_en)
  Row
        6:
                 \operatorname{Focused} Condition View-
            66 Item
                       1 \quad (count == 8)
Condition totals: 1 of 1 input term covered = 100.00\%
    Input Term
                  Covered Reason for no coverage
                        Y
  (count == 8)
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
                        (count = 8)_{-0}
  Row
        1:
                     5
 Row
        2:
                     5
                         (count = 8)_{-1}
                 -Focused Condition View-
                      1 ((count = 0) || \tilde{fifo_intf.rst_n})
Line
Condition totals: 2 of 2 input terms covered = 100.00\%
       Input Term
                     Covered Reason for no coverage
                                                          \operatorname{Hint}
     (count = 0)
                            Y
                            Y
  fifo_intf.rst_n
```

Y

fifo_intf.rd_en

```
Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
                         (count = 0)_{-0}
                                                 fifo_intf.rst_n
  Row
        1:
                     5
  Row
        2:
                     5
                         (count = 0)_{-1}
                         fifo_intf.rst_n_0
  Row
        3:
                     5
                                                  \tilde{\phantom{a}}(\text{count} == 0)
                         fifo_intf.rst_n_1
 Row
                     5
                                                  (count == 0)
                -Focused Condition View-
           68 Item
Line
                     1 (count = (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%
          Input Term
                        Covered Reason for no coverage
                                                              Hint
  (count = (8 - 1))
                               Y
                        FEC Target
                  Hits
                                                 Non-masking condition(s)
     Rows:
                         (count = (8 - 1))_{-0}
 Row
        1:
                     5
                         (count = (8 - 1))_{-1}
 Row
        2:
                     5
                 -Focused Condition View-
           69 Item
                      1 \quad (count == 1)
Line
Condition totals: 1 of 1 input term covered = 100.00%
    Input Term
                  Covered Reason for no coverage
                                                       _{
m Hint}
                        Y
  (count == 1)
                  Hits FEC Target
                                                 Non-masking condition(s)
     Rows:
        1:
                         (count = 1)_{-0}
 Row
                     5
 Row
        2:
                         (count = 1)_{-1}
                     5
Statement Coverage:
    Enabled Coverage
                                     Bins
                                                Hits
                                                                 Coverage
                                                         Misses
                                                                  100.00\%
    Statements
                                       28
                                                  28
                                                              0
```

Statement Details

Statement Coverage for Design Unit work.FIFO —

Item

 $_{
m Line}$

```
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
                                                       module FIFO(FIFO_IF.DUT fifo_intf);
                                                       parameter FIFO_WIDTH = 16:
                                                       parameter FIFO_DEPTH = 8;
 3
                                                       localparam max_fifo_addr = $clog2(FIFO_DEPTH);
                                                       reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
                                                       reg [max_fifo_addr -1:0] wr_ptr, rd_ptr;
  10
                                                       reg [max_fifo_addr:0] count;
  11
  12
                   1
                                             6587
                                                       always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  13
                                                           if (!fifo_intf.rst_n) begin
                   1
                                             1206
                                                                   wr_ptr \ll 0;
  14
  15
                   1
                                             1206
                                                                   fifo_intf.wr_ack \ll 0;
  16
                   1
                                             1206
                                                                   fifo_intf.overflow \ll 0;
  17
                                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
  18
                                                                   mem[wr_ptr] <= fifo_intf.data_in;
  19
                   1
                                             3082
  20
                   1
                                             3082
                                                                   fifo_intf.wr_ack \ll 1;
  21
                                             3082
                                                                   wr_ptr \ll wr_ptr + 1;
  22
                                                          end
  23
                                                           else begin
                                             2299
  24
                   1
                                                                    fifo_intf.wr_ack \le 0;
  25
                                                                   if (fifo_intf.full & fifo_intf.wr_en)
  ^{26}
                   1
                                              501
                                                                            fifo_intf.overflow <= 1;
  27
  28
                   1
                                             1798
                                                                            fifo_intf.overflow \ll 0;
  29
  30
                                                       end
  31
                   1
                                                       always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
  32
                                             6587
  33
                                                          if (!fifo_intf.rst_n) begin
                   1
                                                                   rd_ptr \ll 0;
  34
                                             1206
                                                                   fifo_intf.underflow \le 0;
  35
                   1
                                             1206
                                                                   fifo_intf.data_out <= \{FIFO_WIDTH\{1'b0\}\};
  36
                   1
                                             1206
  37
                                                          \operatorname{end}
                                                          else if (fifo_intf.rd_en && count != 0) begin
  38
                                                                   fifo_intf.data_out <= mem[rd_ptr];
  39
                   1
                                             1157
                   1
                                                                   rd_ptr \ll rd_ptr + 1;
  40
                                             1157
  41
                                                          _{\mathrm{end}}
                                                          else begin
  42
                                                                   if (fifo_intf.empty & fifo_intf.rd_en)
  43
                   1
                                              660
                                                                            fifo_intf.underflow <= 1;
  44
                                                                   else
  45
                   1
                                                                            fifo_intf.underflow <= 0;
                                             3564
  46
```

Source

Count

```
47
                                                           end
    48
                                                        end
    49
                     1
                                               5557
                                                        always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    50
                                                           if (!fifo_intf.rst_n) begin
    51
                     1
                                               1166
                                                                    count \ll 0;
    52
    53
                                                           end
                                                           else begin
    54
                                                                             ( (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b10) \&\& !fifo\_intf.fu
    55
                                                                    i f
                     1
                                               2190
                                                                             count \ll count + 1;
    56
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) &&!fifo_intf.em
    57
                                                336
                     1
                                                                             count \ll count - 1;
    58
                                                                    else if (\{fifo\_intf.wr\_en, fifo\_intf.rd\_en\} = 2'b11) && fifo\_intf.ful
    59
                                                 90
    60
                     1
                                                                             count \ll count - 1;
                                                                    else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    61
                     1
                                                161
                                                                             count \ll count + 1;
    62
    63
                                                           end
                                                        end
    64
    65
    66
                     1
                                               3272
                                                        assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
                     1
                                               4396
                                                        assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67
                     1
                                               3272
                                                        assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68
                     1
                                               3272
                                                        assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69
Toggle Coverage:
    Enabled Coverage
                                    _{\mathrm{Bins}}
                                               Hits
                                                               Coverage
                                                       Misses
                                      20
                                                            0
                                                                100.00\%
    Toggles
                                                 20
                                 =Toggle Details=
```

Toggle Coverage for Design Unit work.FIFO

Node	1H–> $0L$	0L->1H	"Coverage"
$\operatorname{count}\left[0-3\right]$	5	5	100.00
$\mathrm{rd}_{-}\mathrm{ptr}\left[0-2\right]$	5	5	100.00
$\operatorname{wr}\operatorname{-ptr}\left[0-2\right]$	5	5	100.00

 $\begin{array}{lll} {\rm Total~Node~Count} & = & 10 \\ {\rm Toggled~Node~Count} & = & 10 \\ {\rm Untoggled~Node~Count} & = & 0 \end{array}$

Toggle Coverage = 100.00% (20 of 20 bins)

Total Coverage By Design Unit (filtered view): 98.00%

6.3 Coverage "Merged" Report

Coverage Report by file with details

Statement Coverage: Enabled Coverage	Bins	$_{ m Hits}$	Misses	Coverage	
Statements	1	1	0	100.00%	
	Statement	Details=			
Statement Coverage for file	/home/tare/De	esktop/syn	a_fifo/uvi	m_verification/	FIFO_IF . sv
24 1		6025			
Toggle Coverage: Enabled Coverage	Bins	$_{ m Hits}$	Misses	Coverage	
				100.0007	
Toggles Toggle Coverage for File /ho	86 Toggle Do	op/syn_fi	fo/uvm_v	erification/FIF	
	——Toggle De	etails====	fo/uvm_v	erification/FIF	
Toggle Coverage for File /he Line Total Node Count =	Toggle Deskt	etails———op/syn_fi	fo/uvm_v	erification/FIF	
Toggle Coverage for File /ho	Toggle Do	etails———op/syn_fi	fo/uvm_v	erification/FIF	
Toggle Coverage for File /hc Line Total Node Count = Toggled Node Count = Untoggled Node Count =	Toggle Dome/tare/Deskt	etails——etails——Node	fo/uvm_v	erification/FIF	O_IF.sv — "Coverag
Toggle Coverage for File /he Line Total Node Count = Toggled Node Count = Untoggled Node Count = Toggle Coverage =	Toggle Decome/tare/Deskt 43 43 0 100.00% (86 of	op/syn_fi Node 86 bins)	fo/uvm_v	erification/FIF	
Toggle Coverage for File /hc Line Total Node Count = Toggled Node Count = Untoggled Node Count =	Toggle Decome/tare/Deskt 43 43 0 100.00% (86 of	op/syn_fi Node 86 bins)	fo/uvm_v	erification/FIF	

26	IF Branch5	Count coming in t	o IF
26 1	***0*** 5	All False Count	
Branch totals: 1 hit of		All raise Count	
	IF Branch		
27	***0***	Count coming in t	o IF
27 1	***0*** ***0***	All False Count	
Branch totals: 0 hits of	f 2 branches = 0.00%		
Statement Coverage: Enabled Coverage	Bins Hits	Misses Coverage	
Statements	15 12	$3 \qquad 80.00\%$	
	Statement Details=		
Statement Coverage for i	file /home/tare/Desktop/sy	n_fifo/uvm_verificati	$on/FIFO_agent_pkg.sv$
13 1	***0***		
$ \begin{array}{ccc} 13 & & 2 \\ 13 & & 3 \end{array} $	***0*** 10		
21 1	5		
25 1	5		
27 1	***0***		
28 1	5		
29	5		
30 1	5		
31 1	5		
35 1	5		
$\frac{36}{27}$	5		
$\begin{array}{ccc} 37 & & 1 \\ 38 & & 1 \end{array}$	5		
$ \begin{array}{ccc} 38 & & 1 \\ 39 & & 1 \end{array} $	5 5		
1	9		
Enabled Coverage	Bins Hits	Misses Coverage	
Enabled Coverage Branches	$\begin{array}{ccc} & \operatorname{Bins} & \operatorname{Hits} \\ \hline & 10 & 0 \\ \\ \hline \end{array}$ Branch Details	10 0.00%	
Branches Branch Coverage for file 7 7 1	10 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** ***0***	10 0.00%	
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of	10 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** **0*** **0*** 15 branches = 0.00%	10 0.00% ifo/uvm_verification/ Count coming in t All False Count	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of	10 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** **0*** f 2 branches = 0.00% IF Branch ***0***	10 0.00%	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of	10 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** **0*** **0*** F 2 branches = 0.00% IF Branch ***0*** ***0*** ***0***	10 0.00% ifo/uvm_verification/ Count coming in t All False Count	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of	10 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** ***0*** 1F Branch ***0*** ***0*** ***0*** ***0*** ***0*** IF Branch ***0*** **1 branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***1 branch IF Branch ***1 branch	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t All False Count	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of	To O O O O O O O O O	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of	To 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** ***0*** ***0*** ***0*** F 2 branches = 0.00% IF Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0***	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t All False Count	o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 8 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	To 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0***	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t All False Count	o IF
Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 8 7 9 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	To O O O O O O O O O	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t All False Count Count coming in t	o IF o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 8 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	To 0 Branch Details /home/tare/Desktop/syn_f IF Branch ***0*** ***0** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0***	10 0.00% ifo/uvm_verification/ Count coming in to All False Count Count coming in to All False Count Count coming in to the Count coming in the Count c	o IF o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 8 Branch totals: 0 hits of	### To a control of the control of t	10 0.00% ifo/uvm_verification/ Count coming in t All False Count Count coming in t All False Count Count coming in t	o IF o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 8 Branch totals: 0 hits of	### To a control of the control of t	10 0.00% ifo/uvm_verification/ Count coming in to All False Count Count coming in to All False Count Count coming in to the Count coming in the Count c	o IF o IF
Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 5 Branch totals: 0 hits of	### 10 ##	10 0.00% ifo/uvm_verification/ Count coming in to All False Count Count coming in to All False Count Count coming in to the Count coming in the Count c	o IF o IF o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 5 Branch totals: 0 hits of 7 7 7 6	### To a control of the control of t	10 0.00% ifo/uvm_verification/ Count coming in to All False Count	o IF o IF o IF
Branches Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 5 Branch totals: 0 hits of 7 7 7 6	### To a control of the control of t	10 0.00% ifo/uvm_verification/ Count coming in to All False Count	o IF o IF o IF
Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 5 Branch totals: 0 hits of 7 7 7 6 Branch totals: 0 hits of	### To a control of the control of t	10 0.00% ifo/uvm_verification/ Count coming in to All False Count	o IF o IF o IF
Branch Coverage for file 7 7 7 1 Branch totals: 0 hits of 7 7 7 2 Branch totals: 0 hits of 7 7 7 5 Branch totals: 0 hits of 7 7 7 6 Branch totals: 0 hits of Condition Coverage:	### Details The property of	Count coming in to All False Count	o IF o IF o IF

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_agent_pkg.sv —

 $Condition \ \ Coverage \ \ for \ \ file \ \ /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv \ --- \ /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv \ --- \ /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_ob$

```
-Focused Condition View-
          7 Item
Line
                    1 (name !=0)
Condition totals: 0 of 1 input term covered = 0.00\%
  Input Term
               Covered Reason for no coverage
 (name != 0)
                     N No hits
                                                 Hit '_0' and '_1'
                Hits FEC Target
                                            Non-masking condition(s)
    Rows:
 Row
       1:
                      (name != 0)_{-0}
             ***0***
 Row
       2:
             ***0***
                      (name != 0)_{-1}
               -Focused Condition View-
          7 Item
                    2 \quad (tmp_data_- != null)
Condition totals: 0 of 1 input term covered = 0.00\%
                        Covered Reason for no coverage
                                                          Hint
           Input Term
 (tmp_data__ != null)
                              N No hits
                                                          Hit '_{-}0' and '_{-}1'
                      FEC Target
    Rows:
                _{
m Hits}
                                              Non-masking condition(s)
                      (tmp_data__ != null)_0
 Row
       1:
             ***0***
             ***0***
                      (tmp_data_{--} != null)_1
 Row
       2:
Statement Coverage:
                                 _{
m Bins}
   Enabled Coverage
                                           Hits
                                                           Coverage
                                                   _{
m Misses}
                                                       10
                                                              9.09\%
   Statements
                                   11
                                              1
                               =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv —
                   1
   7
                   ^{2}
                   3
                   10
  = File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_coverage_pkg.sv
Statement Coverage:
   Enabled Coverage
                                 Bins
                                           Hits
                                                   Misses
                                                           Coverage
                                                        2
   Statements
                                   14
                                             12
                                                             85.71\%
                              =Statement Details
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_coverage_pkg.sv —
                   1
                   2
   8
                                             10
   68
   73
    74
    75
    84
                                           6030
   86
                   1
                   1
                                           6025
   87
   File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_driver_pkg.sv
Branch Coverage:
   Enabled Coverage
                                 Bins
                                           Hits
                                                   Misses Coverage
   Branches
                                                        3
                                                             25.00\%
                               =Branch Details==
-IF Branch-
                                                    Count coming in to IF
   21
                   1
   21
```

All False Count

22	1		anch ***0*** ***0***	Count	coming in to IF	
Branch total	ls: 0 hits of 2 h		***0***	All Fa	alse Count	
			,,,			
Statement C Enabled	overage : Coverage	Bins	$_{ m Hits}$	Misses	Coverage	
Statemen	nts	17	14	3	82.35%	
		===Statement	Datails-			
Statement C	overage for file			ı_fifo/uvı	m_verification/F	IFO_driver_pkg.sv
9	1		***0***			
9	2		***0***			
9 16	3 1		$\frac{10}{5}$			
$\frac{10}{20}$	1		5			
22	1		***0***			
27	1		5			
32	1		5			
$\frac{33}{34}$	1		$\begin{matrix} 5 \\ 6030 \end{matrix}$			
$\frac{34}{35}$	1 1		6030			
38	1		6025			
39	1		6025			
40	1		6025			
41	1		6025			
44 46	1 1		6025			
46	1		6025			
— File: /h	nome/tare/Desktop	/syn_fifo/uvr	m_verifica	tion/FIFC)_env_pkg.sv	
Statement C Enabled	overage : Coverage	Bins	Hits	Misses	Coverage	
Statemen	nts	10	8	2	80.00%	
		Statement	Details=			
$\begin{array}{c} 10 \\ 10 \end{array}$	$\frac{1}{2}$		***0***			
10	2 3		***0*** 10			
$\begin{array}{c} 10 \\ 17 \end{array}$			10 5			
10			10			
10 17 21 22 23			10 5 5			
10 17 21 22 23 24			10 5 5 5 5 5			
10 17 21 22 23 24 28	3 1 1 1 1 1		10 5 5 5 5 5 5			
10 17 21 22 23 24 28 29	3 1 1 1 1 1 1		10 5 5 5 5 5 5 5	/DID		
10 17 21 22 23 24 28 29	3 1 1 1 1 1 1 1 1 nome/tare/Desktop		10 5 5 5 5 5 5 5	tion/FIF(O_monitor_pkg.sv	
10 17 21 22 23 24 28 29 File: /h	3 1 1 1 1 1 1 1 1 nome/tare/Desktop		10 5 5 5 5 5 5 5	tion/FIFO	O_monitor_pkg.sv Coverage	
10 17 21 22 23 24 28 29 File: /k	3 1 1 1 1 1 1 1 1 1 overage: Coverage	/syn_fifo/uvr Bins	10 5 5 5 5 5 5 5 m_verifica	Misses	Coverage	
10 17 21 22 23 24 28 29 File: /h	3 1 1 1 1 1 1 1 1 1 overage: Coverage	/ syn_fifo / uvn Bins ————————————————————————————————————	10 5 5 5 5 5 5 5 5 6 4 Thits	Misses 2	$\frac{\text{Coverage}}{92.00\%}$	
10 17 21 22 23 24 28 29 File: /k	3 1 1 1 1 1 1 1 1 1 overage: Coverage	/ syn_fifo / uvn Bins ————————————————————————————————————	10 5 5 5 5 5 5 5 5 6 4 Thits	Misses 2	Coverage	
10 17 21 22 23 24 28 29 File: /h Statement Control Enabled Statement Control Stateme	3 1 1 1 1 1 1 1 1 1 1 owerage: Coverage nts overage for file	Statement Sins Statement State De	10 5 5 5 5 5 5 5 5 7 5 7 7 8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C. Enabled Statement C. 9	3 1 1 1 1 1 1 1 1 1 1 1 verage: Coverage nts overage for file	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 7 5 7 8 10 10 10 10 10 10 10 10 10 10 10 10 10	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9	3 1 1 1 1 1 1 1 1 1 1 1 vertex of the series	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 M_verifica Hits 23 Details= esktop/syn ***0***	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 9	3 1 1 1 1 1 1 1 1 1 1 1 verage: Coverage nts overage for file	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 7 7 8 8 8 8 8 8 8 8	Misses 2	Coverage 92.00%	FO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C. Enabled Statement C. 9 9	3 1 1 1 1 1 1 1 1 1 1 1 vertex of the series	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 M_verifica Hits 23 Details= esktop/syn ***0***	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20	3 1 1 1 1 1 1 1 1 1 1 1 vertical and the second sec	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 7 5 7 8 8 8 8 8 8	Misses 2	Coverage 92.00%	IFO ₋ monitor ₋ pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 7 5 7 8 8 8 8 8 8	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 7 5 7 8 8 8 8 8 8	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 3 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 3 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6030	Misses 2	Coverage 92.00%	FO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28 30	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 3 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6030 6025	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement Control Statement Control Statement Control 9 9 9 15 19 20 24 25 26 28 30 33	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28 30	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 3 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6035 6035 6025 6025	Misses 2	Coverage 92.00%	IFO_monitor_pkg.sv
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28 30 33 36	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025	Misses 2	Coverage 92.00%	FO_monitor_pkg.sv
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28 30 33 36 37 38 39	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 5 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025 6025 6025 6025 6025 6025 602	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement Control Statement Control Statement Control 9 9 9 15 19 20 24 25 26 28 30 33 36 37 38 39 42	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025 6025 6025 6025 6025 6025 602	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement C Enabled Statement C 9 9 9 15 19 20 24 25 26 28 30 33 36 37 38 39 42 43	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025 6025 6025 6025 6025 6025 602	Misses 2	Coverage 92.00%	FO_monitor_pkg.s
10 17 21 22 23 24 28 29 File: /h Statement Control Statement Control Statement Control 9 9 9 15 19 20 24 25 26 28 30 33 36 37 38 39 42	3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Bins 25 ——Statement /home/tare/De	10 5 5 5 5 5 5 5 5 5 5 5 5 5 5 8 m_verifica Hits 23 Details= esktop/syn ***0*** 10 5 5 5 6030 6030 6025 6025 6025 6025 6025 6025 6025 602	Misses 2	Coverage 92.00%	IFO_monitor_pkg.s

47 48	1 1	6	$025 \\ 025$		
49 51	1 1		$025 \\ 025$		
					===
		yn_fifo/uvm_ve	rification/FIF	O_scoreboard_pkg.sv	
Branch Coverage: Enabled Cove		Bins H	lits Misses	Coverage	
Branches		57	19 38	33.33%	
		=Branch Detail	s=		
Branch Coverage	for file /home	/tare/Desktop/s	yn_fifo/uvm_	verification/FIFO_sco	reboard_pkg.s
64		IF Branch-6		coming in to IF	
$\frac{64}{77}$	1 1		$644 \\ 381$		
Branch totals: 2	hits of 2 braz				
84		IF Branch-		coming in to IF	
84 88	1 1	3	082		
88 Branch totals: 2	-		299		
		IF Branch			
90 90	1		299 Count 501	coming in to IF	
93 Branch totals: 2	1		798		
		IF Branch			
99	1	5	381 Count	coming in to IF	
$\frac{99}{102}$	1 1	4	157 224		
Branch totals: 2	hits of 2 braz				
103		IF Branch-		coming in to IF	
103 106	1 1		660 564	5	
Branch totals: 2	_		501		
		IF Branch			
$\begin{array}{c} 112 \\ 112 \end{array}$	1		381 Count 190	coming in to IF	
$\begin{array}{c} 115 \\ 118 \end{array}$	1 1		$336 \\ 161$		
121	1		90	Calca Count	
Branch totals: 5	hits of 5 bra		604 All F	alse Count	
4.44		IF Branch			
$\frac{141}{141}$	1		025 Count 025	coming in to IF	
150 Branch totals: 1	1 hit of 2 bran	***0 ches = $50.00%$	***		
		IF Branch			
$152 \\ 152$	1	***0 ***0	*** Count	coming in to IF	
		***0		Calse Count	
Branch totals: 0	nits of 2 bra				
153		IF Branch- ***0	*** Count	coming in to IF	
153	1	***0 ***0		Calse Count	
Branch totals: 0	hits of 2 braz	_	1111 1		
159		IF Branch		coming in the ID	
$\frac{153}{153}$	2	***0 ***0	***	coming in to IF	
Branch totals: 0	hits of 2 braz	***0 nches = $0.00%$	*** All F	Calse Count	
		IF Branch			
154	1	***0	*** Count	coming in to IF	
154	1	***0 ***0		alse Count	
Branch totals: 0	hits of 2 braz		TTT All F	arse Coull	

——IF Branch——

0

0

Branch totals: 0 hits of 2 branches = 0.00%

2

Branch totals: 0 hits of 2 branches = 0.00%

154

154

Count coming in to IF

All False Count

					-IF Branch			
$155 \\ 155$		1			***0*** ***0***	Count coming in	to	IF
199		1			***0***	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch			
155		0			***0***	Count coming in	to	IF
155		2			***0*** ***0***	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch			
156					***0***	Count coming in	to	IF
156		1			***0*** ***0***	All False Count		
Branch	totals: (hits	of 2	branches		THE TWISE COUNTY		
					-IF Branch			
156					***0***	Count coming in	to	IF
156		2			***0*** ***0***	All False Count		
Branch	totals: (hits	of 2	branches		All False Count		
					-IF Branch			
157					***0***	Count coming in	to	IF
157		1			***0***	A11 F-1 C		
Branch	totals: (hits	of 2	branches	***0*** = 0.00%	All False Count		
157					-IF Branch $***0***$	Count coming in	to	IF
157		2			***0***			
Branch	totals: () hits	of 2	branches	***0*** = 0.00%	All False Count		
Dranen	totals.	, 11105	01 2	branches				
158					-IF Branch $***0***$	Count coming in	+ o	IF
158		1			***0***	Count coming in	to	11
Dranah	totala. () hita	of 9	hnonohoa	***0***	All False Count		
branch	totals: (nits	01 2	branches	= 0.0070			
150					-IF Branch			
158 158		2			***0*** ***0***	Count coming in	to	1F
					0	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch-	~		
$\frac{159}{159}$		1			***0*** ***0***	Count coming in	to	1F
					0	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch-			
$\frac{159}{159}$		2			***0*** ***0***	Count coming in	to	IF
					0	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch			
$\frac{160}{160}$		1			***0*** ***0***	Count coming in	to	IF
					0	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch			
$\frac{160}{160}$		2			***0*** ***0***	Count coming in	to	IF
100		2			***U*** ***0***	All False Count		
Branch	totals: (hits	of 2	branches	= 0.00%			
					-IF Branch			
168					5	Count coming in	to	IF
168		1			5 ***0***	All False Count		
Branch	totals: 1	hit	of 2	branches =		. , , , , , , , , , , , , , , , , , , ,		
					-IF Branch			
169					5	Count coming in	to	IF
169		1			5 ***0***	All False Count		
Branch	totals: 1	hit	of 2	branches =		1111 1 WISC COUIT		
					-IF Branch			
170					5	Count coming in	to	IF
170		1			5 ***0***	All False Count		
Branch	totals: 1	l hit	of 2	branches =		All raise Count		

Condition Coverage:

```
Conditions
                                                           36
                                                                           18
                                                                                            18
                                                                                                      50.00\%
                                                    =Condition Details:
Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —
                        -{
m Focused} Condition View-
                 84 Item
                                1 (\text{seq\_item\_chk.wr\_en \&\& (this.count} < 8))
Condition totals: 2 of 2 input terms covered = 100.00\%
                        —Focused Condition View-
                 90 Item
                                1 (\text{seq\_item\_chk.wr\_en \&\& (this.count} == 8))
Condition totals: 1 of 2 input terms covered = 50.00\%
                Input Term
                                     Covered Reason for no coverage
                                                                                             Hint
                                               Y
   seq_item_chk.wr_en
                                                    ^{,}_{-0} , not hit
                                                                                              Hit '_0'
    (this.count == 8)
                                               Ν
                                                                          Non-masking condition(s)
                           Hits FEC Target
       Rows:
   Row
             1:
                                5
                                    seq\_item\_chk.wr\_en\_0
   Row
                                    seq\_item\_chk.wr\_en\_1
                                                                         (this.count == 8)
                                5
                                     (this.count == 8)_0
   Row
             3:
                                                                         seq_item_chk.wr_en
                       ***0***
                                     (this.count == 8)_{-1}
                                                                         seq_item_chk.wr_en
   Row
             4:
                                5
                         -{
m Focused} Condition View-
                 99 Item
                                1 (\text{seq\_item\_chk.rd\_en \&\& (this.count != 0)})
Line
Condition totals: 2 of 2 input terms covered = 100.00%
                          \operatorname{-Focused} Condition View-
                 103 Item
                                   1 (\text{seq\_item\_chk.rd\_en \&\& (this.count} == 0))
Condition totals: 1 of 2 input terms covered = 50.00%
                                     Covered Reason for no coverage
                Input Term
                                                                                             Hint
   seq_item_chk.rd_en
                                               Y
                                                    ^{\prime}_{-0}, not hit
    (this.count == 0)
                                               Ν
                                                                                              Hit '_0'
       Rows:
                           Hits FEC Target
                                                                         Non-masking condition(s)
   Row
             1:
                                    seq_item_chk.rd_en_0
                                5
   Row
                                5
                                     seq_item_chk.rd_en_1
                                                                         (this.count == 0)
   Row
             3:
                       ***0***
                                     (this.count == 0)_{-0}
                                                                         seq_item_chk.rd_en
   Row
                                     (this.count == 0)_{-1}
                                                                         seq_item_chk.rd_en
                          -Focused Condition View-
                                  1 (~seq_item_chk.rd_en && seq_item_chk.wr_en && ~this.full_ref)
                 112 Item
Condition totals: 3 of 3 input terms covered = 100.00%
                          Focused Condition View-
                                  1 (seq_item_chk.rd_en && ~seq_item_chk.wr_en && ~this.empty_ref)
                 115 Item
Condition totals: 3 of 3 input terms covered = 100.00%
                          Focused Condition View-
                                  1 (seq_item_chk.wr_en && seq_item_chk.rd_en && this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
                          \hbox{-}Focused \quad Condition \quad View-
                 121 Item 1 (seq_item_chk.wr_en && seq_item_chk.rd_en && this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
                          -Focused Condition View-
                 141 Item
                                  1 ((seq_item_chk.data_out === this.data_out_ref) && (seq_item_chk.wr_ack === this.wr_ack_ref) && (seq_item_chk.o
Condition totals: 0 of 8 input terms covered = 0.00\%
                                                                      Input Term
                                                                                            Covered Reason for no coverage
                                                                                                                                                    Hit '_0'
             (seq_item_chk.data_out === this.data_out_ref)
                                                                                                           ^{\prime}_{-0} or not hit
                   (seq_item_chk.wr_ack === this.wr_ack_ref)
                                                                                                     Ν
                                                                                                           ^{\prime}_{-0} or not hit
                                                                                                                                                    Hit '_0'
              seq_item_chk.overflow === this.overflow_ref)
                                                                                                             _{-0}' not hit
                                                                                                                                                    Hit '_0
                                                                                                                                                    Hit '_0'
          (seq_item_chk.underflow === this.underflow_ref)
                                                                                                           , _0 ,
                                                                                                                   not hit
                                                                                                           , _0 ,
                                                                                                                                                    Hit '_0'
                          (seq_item_chk.full == this.full_ref)
                                                                                                     Ν
                                                                                                                   not hit
                                                                                                                                                    Hit '_0'
                       (seq_item_chk.empty === this.empty_ref)
                                                                                                     Ν
                                                                                                           , _0 ,
                                                                                                                   not hit
       (seq_item_chk.almostfull === this.almostfull_ref)
                                                                                                     Ν
                                                                                                           , _0 ,
                                                                                                                   not hit
                                                                                                                                                    Hit '_0'
   (seq_item_chk.almostempty === this.almostempty_ref)
                                                                                                     Ν
                                                                                                           , _0 ,
                                                                                                                  not hit
                                                                                                                                                    Hit '_0'
                            Hits FEC Target
        Rows:
                                                                                                                                Non-masking condition(s)
   Row
             1:
                       ***0***
                                      (seq_item_chk.data_out === this.data_out_ref)_0
             2:
                                                                                                                                ((seg_item_chk.wr_ack == this.wr_ack_ref) && ((seg_item_cl
   Row
                                5
                                      (seq_item_chk.data_out === this.data_out_ref)_1
             3:
                       ***0***
                                      (seq_item_chk.wr_ack == this.wr_ack_ref)_0
                                                                                                                                (seq_item_chk.data_out === this.data_out_ref)
   Row
             4:
                                      (seq_item_chk.wr_ack == this.wr_ack_ref)_1
                                                                                                                                ((seq_item_chk.data_out == this.data_out_ref) && ((seq_item_chk.data_out_ref) & ((seq_item_chk.data_out_ref) & ((seq_item_chk.data_out_ref)) & ((seq_item_chk.
   Row
                                5
                       ***0***
                                      (seq_item_chk.overflow === this.overflow_ref)_0
                                                                                                                                ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
   Row
             5:
                                      (seq_item_chk.overflow === this.overflow_ref)_1
   Row
             6:
                                5
                                                                                                                                ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
             7:
                       ***0***
                                      (seq_item_chk.underflow === this.underflow_ref)_0
                                                                                                                                ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
   Row
```

Misses

Coverage

Bins

Covered

Enabled Coverage

8:

9:

10:

11:

5

0

0

Row

Row

Row

Row

((seq_item_chk.data_out == this.data_out_ref) && (seq_iter

(seq_item_chk.underflow === this.underflow_ref)_1

(seq_item_chk.full == this.full_ref)_0

(seq_item_chk.full == this.full_ref)_1

(seq_item_chk.empty === this.empty_ref)_0

```
(seq_item_chk.empty === this.empty_ref)_1
                                                                                   ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
Row
Row
       13:
                        (seq_item_chk.almostfull == this.almostfull_ref)_0
                                                                                   ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
Row
       14:
                        (seq_item_chk.almostfull === this.almostfull_ref)_1
                                                                                   ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
Row
       15:
                        (\text{seq\_item\_chk.almostempty} = \text{this.almostempty\_ref})_0
                                                                                   ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
               ***0***
Row
       16:
                        (seq_item_chk.almostempty === this.almostempty_ref)_1
                                                                                   ((seq_item_chk.data_out == this.data_out_ref) && (seq_iter
                -Focused Condition View-
           153 Item
Line
                      1 (seq_item_chk.data_out !== this.data_out_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                       Input Term
                                                     Covered
                                                              Reason for no coverage
                                                                                          Hint
                                                                                          Hit ^{\prime}_{-0}, and ^{\prime}_{-1},
  (seq_item_chk.data_out !== this.data_out_ref)
                                                              No hits
                       FEC Target
                                                                             Non-masking condition(s)
     Rows:
                  _{
m Hits}
 Row
        1:
               ***0***
                        (seq_item_chk.data_out !== this.data_out_ref)_0
                        (seq_item_chk.data_out !== this.data_out_ref)_1
 Row
        2:
               ***0***
                 \operatorname{-Focused} Condition View-
           154 Item
                      1 (seq_item_chk.wr_ack !== this.wr_ack_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
                                   Input Term
                                                 Covered
                                                         Reason for no coverage
                                                                                     Hint
                                                                                     Hit '_0' and '_1'
  (seq_item_chk.wr_ack !== this.wr_ack_ref)
                                                       N No hits
                       FEC Target
     Rows:
                  _{
m Hits}
                                                                        Non-masking condition(s)
 Row
        1:
               ***0***
                        (seq_item_chk.wr_ack !== this.wr_ack_ref)_0
        2:
               ***0***
                        (seq_item_chk.wr_ack !== this.wr_ack_ref)_1
  Row
                 \operatorname{-Focused} Condition View\operatorname{-}
           155 Item
                        1 (seq_item_chk.overflow !== this.overflow_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                       Input Term
                                                     Covered Reason for no coverage
                                                                                          Hint
                                                                                          Hit ,0, and ,1,
  (seq_item_chk.overflow !== this.overflow_ref)
                                                           N No hits
     Rows:
                  _{
m Hits}
                       FEC Target
                                                                             Non-masking condition(s)
               ***0***
 Row
        1:
                        (seq_item_chk.overflow !== this.overflow_ref)_0
 Row
        2:
               ***0***
                        (seq_item_chk.overflow !== this.overflow_ref)_1 -
                \operatorname{-Focused} Condition View\operatorname{--}
                        1 (seq_item_chk.underflow !== this.underflow_ref)
           156 Item
Condition totals: 0 of 1 input term covered = 0.00%
                                         Input Term
                                                        Covered
                                                                Reason for no coverage
  (seq_item_chk.underflow !== this.underflow_ref)
                                                             N No hits
                                                                                            Hit '_0' and '_1'
                                                                               Non-masking condition(s)
     Rows:
                  _{
m Hits}
                       FEC Target
 Row
        1:
                        (seq_item_chk.underflow !== this.underflow_ref)_0
                        (seq_item_chk.underflow !== this.underflow_ref)_1
 Row
                 \hbox{-}Focused \quad Condition \quad View-
           157 Item
                        1 (seq_item_chk.full !== this.full_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                            Covered Reason for no coverage
                                                   N No hits
  (seq_item_chk.full !== this.full_ref)
                                                                                 Hit '_0' and '_1'
     Rows:
                  Hits FEC Target
                                                                    Non-masking condition(s)
                        (seq_item_chk.full !== this.full_ref)_0
  Row
        1:
               ***0***
                        (seq_item_chk.full !== this.full_ref)_1
  Row
        2:
                 -Focused Condition View-
            158 Item 1 (seq_item_chk.empty !== this.empty_ref)
Condition totals: 0 of 1 input term covered = 0.00\%
                                 Input Term
                                              Covered Reason for no coverage
                                                                                   _{
m Hint}
                                                                                   Hit '_0' and '_1'
  (seq_item_chk.empty !== this.empty_ref)
                                                     N No hits
                  Hits FEC Target
                                                                      Non-masking condition(s)
     Rows:
  Row
        1:
                        (seq_item_chk.empty !== this.empty_ref)_0
        2:
                        (seq_item_chk.empty !== this.empty_ref)_1
 Row
               ***0***
                -Focused Condition View-
                       1 (seq_item_chk.almostfull !== this.almostfull_ref)
Line
           159 Item
Condition totals: 0 of 1 input term covered = 0.00\%
                                           Input Term
                                                         Covered Reason for no coverage
                                                                                              Hint
  (seq_item_chk.almostfull !== this.almostfull_ref)
                                                                                              Hit '_0' and '_1'
                                                               N No hits
```

12:

```
Hits FEC Target
                                                                                Non-masking condition(s)
     Rows:
                        (seq_item_chk.almostfull !== this.almostfull_ref)_0
 Row
        1:
              ***0***
                        (seq_item_chk.almostfull !== this.almostfull_ref)_1
 Row
        2:
              ***0***
                -Focused Condition View-
           160 Item 1 (seq_item_chk.almostempty !== this.almostempty_ref)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
                                             Input Term
                                                           Covered Reason for no coverage
                                                                                               Hint
                                                                                               Hit ,_0, and ,_1,
 (seq_item_chk.almostempty !== this.almostempty_ref)
                                                                 N No hits
     Rows:
                 Hits FEC Target
                                                                                  Non-masking condition(s)
        1:
                        (seq_item_chk.almostempty !== this.almostempty_ref)_0
 Row
              ***0***
                        (seq_item_chk.almostempty !== this.almostempty_ref)_1
 Row
        2:
              ***0***
Expression Coverage:
    Enabled Coverage
                                   Bins
                                                      Misses
                                           Covered
                                                               Coverage
    Expressions
                                                            0
                                                                100.00\%
                                       4
                                =Expression Details
Expression Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —
                \operatorname{-Focused} Expression View---
Line
           128 Item 1 (this.count = 0)
Expression totals: 1 of 1 input term covered = 100.00%
                -Focused Expression View—
           129 Item 1 (this.count = 8)
Expression totals: 1 of 1 input term covered = 100.00%
                -Focused Expression View—
           130 Item 1 (this.count = (8-1))
Expression totals: 1 of 1 input term covered = 100.00%
                -Focused Expression View-
           131 Item 1 (this.count = 1)
Expression totals: 1 of 1 input term covered = 100.00%
Statement Coverage:
    Enabled Coverage
                                   Bins
                                              Hits
                                                       _{
m Misses}
                                                              Coverage
    Statements
                                     60
                                                           12
                                                                 80.00\%
                                                48
                                \LongrightarrowStatement Details\Longrightarrow
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —
   9
                    1
                    2
                                                10
    17
                                                 5
    22
    23
    24
    ^{29}
                                                 5
                                                 5
    30
    35
                                                 5
    36
                                                 5
    37
                                              6030
    38
                                              6025
    61
                                              6025
                                               644
                                               644
    67
                                               644
    68
                                               644
                                               644
    70
                                               644
                    1
    71
                                               644
                     1
                                               644
    72
    73
                                               644
    74
                                               644
                                               644
    75
    76
                                               644
                                              3082
    85
                                              3082
    86
                                              3082
    87
    89
                                              2299
    92
                                               501
                                              1798
    94
    100
                                              1157
```

1157

660

3564

2190

336

101

105

107

113

116

1

1

```
161
    120
    123
                                                  90
    128
                                                6025
    129
                                                6025
    130
                                                6025
    131
                                                6025
    137
                                                6025
    149
                                                6025
    151
                                             ***0***
    152
    153
    154
    155
    156
    157
    158
    159
    160
    166
    168
                                                   5
    169
                                                   5
    170
                                                   5
  = File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv
Branch Coverage:
    Enabled Coverage
                                                        _{
m Misses}
                                     _{\mathrm{Bins}}
                                                Hits
                                                                 Coverage
                                       10
                                                              8
    Branches
                                                                   20.00\%
                                 ==Branch Details=====
Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —
                                       -IF Branch-
    8
                                                         Count coming in to IF
                     1
                                             ***0***
                                                          All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                       -IF Branch-
    8
                                                         Count coming in to IF
                                                6025
                                             ***0***
                                                6025
                                                          All False Count
Branch totals: 1 hit of 2 branches = 50.00%
                                       -IF Branch-
                                                         Count coming in to IF
Branch totals: 0 hits of 2 branches = 0.00\%
                                       -IF Branch-
                                                6025
                                                          Count coming in to IF
                                             ***0***
                                                6025
                                                          All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                       -IF Branch-
    8
                                                          Count coming in to IF
                                                          All False Count
Branch totals: 0 hits of 2 branches = 0.00%
Condition Coverage:
                                             Covered
    Enabled Coverage
                                     _{\mathrm{Bins}}
                                                         _{\mathrm{Misses}}
                                                                 Coverage
                                        2
                                                              2
    Conditions
                                                                    0.00\%
                                  =Condition Details:
Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —
                 Focused Condition View—
           8 Item
                      1 (\text{name } != 0)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
   Input Term
               Covered Reason for no coverage
                                                      _{
m Hint}
                                                      Hit ,0, and ,1
                       N No hits
  (name != 0)
     Rows:
                  Hits FEC Target
                                                Non-masking condition(s)
        1:
               ***0***
                         (name != 0)_{-0}
  Row
        2:
                         (name != 0)_{-1}
 Row
               ***0***
                -Focused Condition View-
           8 Item 2 (tmp_data_{-} != null)
Line
Condition totals: 0 of 1 input term covered = 0.00\%
```

```
(tmp_data__ != null)
                                     ^{\prime}_{-1} , not hit
                                                                 \operatorname{Hit} \ '_{-1} '
                                  Ν
                  _{
m Hits}
                        FEC Target
                                                    Non-masking condition(s)
     Rows:
                         (tmp_data__ != null)_0
 Row
        1:
                     5
                         (tmp_data__ != null)_1
 Row
        2:
Statement Coverage:
    Enabled Coverage
                                     _{\mathrm{Bins}}
                                                 Hits
                                                                  Coverage
                                                          _{\mathrm{Misses}}
                                        16
    Statements
                                                               8
                                                                    50.00\%
                                   =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —
                     1
                                             ***0***
    8
                     2
    8
                                              ***0***
                                                 6025
                                              ***0***
                                              ***0***
                                                 6025
                     10
                                              ***0***
    16
                                               12065
                                               12065
    22
                                                   15
    63
                                                   15
    64
    65
                                                   15
    69
                                                    5
    File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv
Branch Coverage:
    Enabled Coverage
                                     Bins
                                                 Hits
                                                          _{
m Misses}
                                                                  Coverage
    Branches
                                        ^{26}
                                                              20
                                                                     23.07\%
                                  =Branch Details=
Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv —
                                       -IF Branch-
    8
                                                           Count coming in to IF
                                                           All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                        -IF Branch-
                                                           Count coming in to IF
                                                           All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                       -IF Branch-
                                                           Count coming in to IF
                     3
Branch totals: 0 hits of 2 branches = 0.00\%
                                       -IF Branch-
    8
                                                           Count coming in to IF
                     5
                                                           All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                        {
m -IF} {
m Branch}-
    8
                                                           Count coming in to IF
                                                           All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                      -IF Branch-
    21
                                                   25
                                                           Count coming in to IF
                     1
    21
                                                   25
                                                           All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                       -IF Branch-
    22
                                                           Count coming in to IF
    22
                     1
                                             ***0***
                                                           All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                       -IF Branch-
    30
                                                 5000
                                                           Count coming in to IF
```

Input Term

Covered Reason for no coverage

```
All False Count
                                              5000
Branch totals: 1 hit of 2 branches = 50.00\%
                                    —IF Branch—
    31
                                                        Count coming in to IF
                                           ***0***
    31
                                           ***0***
                                           ***0***
                                                        All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                    ——IF Branch—
    39
                                               500
                                                        Count coming in to IF
    39
                                            ***0***
                                               500
                                                        All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                     -IF Branch-
    40
                                                        Count coming in to IF
                                           ***0***
    40
                                           ***0***
                                                        All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
                                     {
m -IF} Branch{
m -}
    48
                                               500
                                                        Count coming in to IF
    48
                     1
                                           ***0***
                                               500
                                                        All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
                                    —IF Branch—
    49
                                           ***0***
                                                        Count coming in to IF
    49
                     1
                                           ***0***
                                                        All False Count
Branch totals: 0 hits of 2 branches = 0.00\%
Condition Coverage:
    Enabled Coverage
                                                       Misses Coverage
                                    Bins
                                           Covered
    Conditions
                                       2
                                                            2
                                                                   0.00\%
                                -Condition Details
Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv —
               —Focused Condition View—
           8 Item
                   1 (name != 0)
Condition totals: 0 of 1 input term covered = 0.00\%
                Covered Reason for no coverage
  Input Term
  (name != 0)
                       N No hits
                                                     Hit '_0' and '_1'
     Rows:
                  Hits FEC Target
                                               Non-masking condition(s)
 Row
        1:
                        (name != 0)_{-0}
 Row
               ***0***
                        (name != 0)_{-1}
                \operatorname{-Focused} Condition View\operatorname{--}
           8 Item
                   2 \quad (tmp_data_{-} != null)
Condition totals: 0 of 1 input term covered = 0.00\%
            Input Term
                          Covered Reason for no coverage
                                N '_1' not hit
                                                              Hit '_1'
  (tmp_data_{--} != null)
     Rows:
                  Hits FEC Target
                                                 Non-masking condition(s)
                        (tmp_data_{--} != null)_0 -
 Row
        1:
 Row
        2:
                        (tmp_data_{-} != null)_1 -
Statement Coverage:
    Enabled Coverage
                                              Hits Misses Coverage
                                    _{
m Bins}
                                                           12
    Statements
                                      32
                                                 20
                                                                  62.50\%
                                 =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv —
                     1
                                           ***0***
                     2
    8
                                            ***0***
    8
                     3
                                            ***0***
    8
                                            ***0***
                     4
                     5
                     6
                     9
                    10
    12
                    1
                                                  5
```

5

0

30

1

1

16

```
18
                                                   5
    19
                                                  25
    20
                                                  25
    22
    23
                                                  25
    27
                                                5000
    28
                                                5000
    ^{29}
    31
                                             ***0***
    32
                                                5000
    36
                                                   5
    37
                                                 500
    38
                                                 500
    40
                                             ***0***
                                                 500
    41
    45
                                                   5
                                                 500
    46
                                                 500
    47
    49
                                             ***0***
    50
                                                 500
    File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequencer_pkg.sv
Statement Coverage:
                                                _{
m Hits}
    Enabled Coverage
                                     _{\mathrm{Bins}}
                                                                 Coverage
                                                         _{
m Misses}
                                                              2
    Statements
                                        4
                                                                   50.00\%
                                 =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequencer_pkg.sv —
    8
                     1
                     2
    8
    8
                     3
                                                  10
                     1
    11
                                                   5
    File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv
Branch Coverage:
    Enabled Coverage
                                     Bins
                                                Hits
                                                         _{
m Misses}
                                                                 Coverage
    Branches
                                        6
                                                              4
                                                                   33.33\%
                                  =Branch Details=
Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv —
                                       -IF Branch-
    ^{26}
                                                          Count coming in to IF
    ^{26}
                     1
                                                          All False Count
Branch totals: 1 hit of 2 branches = 50.00\%
    27
                                                          Count coming in to IF
                     1
    27
                                                          All False Count
Branch totals: 0 hits of 2 branches = 0.00%
                                       -IF Branch-
    35
                                                   5
                                                          Count coming in to IF
                     1
                                                          All False Count
Branch totals: 1 hit of 2 branches = 50.00%
Statement Coverage:
    Enabled Coverage
                                     Bins
                                                Hits
                                                         Misses Coverage
                                                                   80.00\%
    Statements
                                 =Statement Details=
Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv —
                     1
    10
                                             ***0***
                     2
    10
                     3
                                                  20
    10
    17
                     1
                                                   5
    21
                     1
                                                   5
    22
                                                   5
                                                   5
    23
                                                   5
    24
    27
    29
                                                   5
                                                   5
    33
                                                   5
    34
                                                   5
    35
                     1
                                                   5
                     1
    36
```

37 1 5

	Coverage: abled Coverag	e	Bins	Hits	${\rm Misses}$	Coverage	
Br	anches		25	-25	0	$\overline{100.00\%}$	
			Branch	Details			
Branch	Coverage for	file	, , ,	-, -	fo/uvm_v	verification/	FIFO_v1.0.0.sv -
13			IF	Branch————————————————————————————————————	Count	coming in to	o IF
13 18		1 1		$\frac{1206}{3082}$			
23 Branch	totals: 3 h	1 ts of	3 branches =	$\frac{2299}{100.00\%}$			
Branen	totals. o n	05 01					
25			1F	Branch————————————————————————————————————	Count	coming in to	o IF
$\begin{array}{c} 25 \\ 27 \end{array}$		1 1		$501 \\ 1798$			
	totals: 2 h	ts of	2 branches =				
			IF	Branch-			
33 33		1		$6587 \\ 1206$	Count	coming in to	o IF
$\begin{array}{c} 38 \\ 42 \end{array}$		1		$\begin{array}{c} 1157 \\ 4224 \end{array}$			
	totals: 3 h	ts of	3 branches =				
			IF	Branch			
$\frac{43}{43}$		1		$4224 \\ 660$	Count	coming in to	o IF
45	total= 0.1	1	2 0 hma1	3564			
Branch	totals: 2 h	ts of	2 branches =				
51			IF	Branch————————————————————————————————————	Count	coming in to	
$51 \\ 54$		1 1		$\begin{array}{c} 1166 \\ 4391 \end{array}$		O	
	totals: 2 h		2 branches =				
			IF	Branch-			
55 55		1		$4391 \\ 2190$	Count	coming in to	o IF
57 59		1		336 90			
61		1		161			
Branch	totals: 5 h	ts of	5 branches =	$1614 \\ 100.00\%$	All F	alse Count	
			IF	Branch			
66 66		1		$\frac{3267}{202}$	Count	coming in to	o IF
66		$\frac{1}{2}$		3065			
Branch	totals: 2 h	ts of	2 branches =	100.00%			
67			IF	Branch————————————————————————————————————	Count	coming in to	
67		1		1691	Count		, 11
67 Branch	totals: 2 h	$\frac{2}{\mathrm{ts}}$ of	2 branches =	$2700 \\ 100.00\%$			
			IF	Branch			
68 68		1		$\begin{array}{c} 3267 \\ 290 \end{array}$	Count	coming in to	o IF
68	total= : 0 1	2	2 9 hma1	2977			
oranch	totals: 2 h	is of	2 branches =				
69			IF	Branch————————————————————————————————————	Count	coming in to	o IF
69 69		$\frac{1}{2}$		$621 \\ 2646$		-	
0.0	totals: 2 h	ts of	2 branches =				
Co. 111	ion Co						
	ion Coverage: abled Coverag		Bins	Covered	Misses	Coverage	
Co	onditions		$\phantom{aaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaaa$	23	2	92.00%	
			Condit	ion Details=			

1 (fifo_intf.full & fifo_intf.wr_en) Line 25 Item Condition totals: 1 of 2 input terms covered = 50.00%Input Term Covered Reason for no coverage Hint $'_{-0}$, not hit Hit '_0' fifo_intf.full Ν fifo_intf.wr_en Y Hits FEC Target Non-masking condition(s) Rows: Row 1: ***0*** fifo_intf.full_0 fifo_intf.wr_en fifo_intf.full_1 Row 2:5 fifo_intf.wr_en 3: fifo_intf.wr_en_0 fifo_intf.full Row 5 fifo_intf.wr_en_1 fifo_intf.full Row 4:5 $\operatorname{-Focused}$ Condition View $\operatorname{--}$ 1 (fifo_intf.rd_en && (count != 0)) Line 38 Item Condition totals: 2 of 2 input terms covered = 100.00% -Focused Condition View-43 Item Line 1 (fifo_intf.empty & fifo_intf.rd_en) Condition totals: 1 of 2 input terms covered = 50.00%Input Term Covered Reason for no coverage $_{\mathrm{Hint}}$ fifo_intf.empty $^{\prime}_{-0}$ on not hit Hit '_0' Ν $fifo_intf.rd_en$ Y Hits FEC Target Non-masking condition(s) Rows: Row 1: ***0*** fifo_intf.empty_0 fifo_intf.rd_en fifo_intf.rd_en Row 2: $fifo_intf.empty_1$ 5 Row 3: fifo_intf.rd_en_0 fifo_intf.empty 5 $fifo_intf.rd_{en_1}$ fifo_intf.empty Row 4:5 $\operatorname{-Focused}$ Condition View— 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full) Line 55 Item Condition totals: 3 of 3 input terms covered = 100.00% $\operatorname{-Focused}$ Condition View— 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty) Line Condition totals: 3 of 3 input terms covered = 100.00% Focused Condition View— Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full) Condition totals: 3 of 3 input terms covered = 100.00%-Focused Condition View-Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty) Condition totals: 3 of 3 input terms covered = 100.00% -Focused Condition View-Line 66 Item $1 \quad (count == 8)$ Condition totals: 1 of 1 input term covered = 100.00% -Focused Condition View-Line 1 $((count = 0) | | \tilde{fifo_intf.rst_n})$ Condition totals: 2 of 2 input terms covered = 100.00% -Focused Condition View-1 (count = (8 - 1)) Line 68 Item Condition totals: 1 of 1 input term covered = 100.00% -Focused Condition View-Line 69 Item $1 \quad (count == 1)$ Condition totals: 1 of 1 input term covered = 100.00% Statement Coverage: Enabled Coverage $_{\mathrm{Bins}}$ HitsMisses Coverage Statements 2828100.00%=Statement Details= Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv — 121 6587141 1206 151 1206 161 1206308219 20 3082213082242299 26 501281798 1 3265871 1206341 1 351206

-Focused Condition View-

```
1206
   36
                   1
   39
                                           1157
    40
                                           1157
                                           660
    44
    46
                                           3564
   50
                                           5557
                                           1166
   52
                                           2190
   56
   58
                                           336
   60
                                            90
                                           161
    62
                                           3272
    66
                                           4396
    67
   68
                                           3272
                                           3272
   69
Toggle Coverage:
   Enabled Coverage
                                 _{
m Bins}
                                          _{
m Hits}
                                                          Coverage
                                                  _{
m Misses}
                                   20
                                                           100.00\%
   Toggles
                                            20
                                                       0
                              =Toggle Details=
0L—>1H "Coverage"
      Line
                                            Node
                                                      1H->0L
Total Node Count
                              10
Toggled Node Count
                              10
{\bf Untoggled\ Node\ Count}\,=\,
                               0
Toggle Coverage
                          100.00% (20 of 20 bins)
   File: /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv
                                          _{
m Hits}
                                 _{
m Bins}
                                                  Misses
                                                          Coverage
    Enabled Coverage
   Statements
                                   5
                                                       0
                                                           100.00\%
```

Statement	Coverage:
T2 1-1 -	1 0

=Statement Details=

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv —

10	1		5
11	1		12055
11	2		12050
24	1		5
25	1		5
Toggle Covera	ge:		
Enabled C	Coverage	Bins	$_{ m Hits}$

ggle Coverage: Enabled Coverage	Bins	$_{ m Hits}$	Misses	Coverage
Toggles	2	2	0	100.00%

—Toggle Details—

Toggle Coverage for File /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv —

Node 1H->0L0L—>1H "Coverage" $_{
m Line}$

Total Node Count 1 Toggled Node Count 1 0 Untoggled Node Count =

Toggle Coverage 100.00% (2 of 2 bins)

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	$_{ m Bins}$	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100		Covered
covered/total bins:	190	190	_	
missing/total bins:	0	190	_	
% Hit:	100.00%	100	_	
Coverpoint rst_n_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	644	1	_	Covered
bin auto [1]	5381	1	_	$\operatorname{Covered}$
Coverpoint data_in_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64	_	
% Hit:	100.00%	100	_	
bin auto [0:1023]	976	1	_	Covered
bin auto [1024:2047]	57	1	_	Covered
bin auto [2048:3071]	62	1	_	Covered
bin auto [3072:4095]	64	1	_	Covered
bin auto [4096:5119]	73	1	_	Covered

bin auto $[5120:6143]$	77	1	_	Covered
bin auto [6144:7167]	60	1	_	Covered
bin auto [7168:8191]	75	1	_	Covered
L 3			_	
bin auto [8192:9215]	66	1	_	Covered
bin auto [9216:10239]	62	1	_	Covered
bin auto [10240:11263]	60	1	_	Covered
bin auto [11264:12287]	59	1	_	Covered
bin auto [12288:13311]	64	1	_	Covered
bin auto [13312:14335]	62	1	_	Covered
			_	
bin auto $[14336:15359]$	66	1	_	Covered
bin auto [15360:16383]	53	1	_	Covered
	66	1		Covered
bin auto $[16384:17407]$			_	
bin auto [17408:18431]	58	1	_	Covered
bin auto [18432:19455]	79	1	_	Covered
bin auto $[19456:20479]$	68	1	_	Covered
bin auto $[20480:21503]$	54	1	_	Covered
bin auto [21504:22527]	65	1	_	Covered
$bin auto \left[22528{:}23551\right]$	72	1	_	Covered
bin auto $[23552:24575]$	68	1	_	Covered
bin auto [24576:25599]	66	1	_	Covered
bin auto $[25600:26623]$	66	1	_	Covered
bin auto $[26624:27647]$	69	1	_	Covered
bin auto [27648:28671]	78	1	_	Covered
${ m bin \ auto} [28672 \hbox{:} 29695]$	74	1	_	Covered
bin auto $[29696:30719]$	66	1	_	Covered
bin auto [30720:31743]	61	1	_	Covered
bin auto $[31744:32767]$	64	1	_	Covered
bin auto $[32768:33791]$	77	1	_	Covered
bin auto [33792:34815]	61	1	_	Covered
bin auto $[34816:35839]$	72	1	_	Covered
bin auto $[35840:36863]$	68	1	_	Covered
bin auto [36864:37887]	75	1	_	Covered
bin auto [37888:38911]	70	1	_	Covered
bin auto [38912:39935]	62	1	_	Covered
bin auto $[39936:40959]$	55	1	_	Covered
bin auto $[40960:41983]$	73	1	_	Covered
bin auto $[41984:43007]$	60	1	_	Covered
bin auto $[43008:44031]$	70	1		Covered
· ·			_	
bin auto $[44032:45055]$	69	1	_	Covered
bin auto $[45056:46079]$	62	1	_	Covered
bin auto [46080:47103]	63	1		Covered
		_		
bin auto $[47104:48127]$	62	1	_	Covered
bin auto [48128:49151]	73	1	_	Covered
bin auto [49152:50175]	62	1	_	Covered
bin auto $[50176:51199]$	65	1	_	Covered
bin auto $[51200:52223]$	69	1	_	Covered
bin auto $[52224:53247]$	70	1		Covered
			_	
bin auto $[53248:54271]$	51	1	_	Covered
bin auto [54272:55295]	83	1	_	Covered
	70			Covered
bin auto [55296:56319]		1	_	
${ m bin \ auto} [56320 \!:\! 57343]$	60	1	_	Covered
bin auto [57344:58367]	54	1	_	Covered
,	69	1		Covered
bin auto [58368:59391]			_	
bin auto $[59392:60415]$	76	1	_	Covered
bin auto $[60416:61439]$	67	1	_	Covered
bin auto [61440:62463]	75	1	_	Covered
bin auto $[62464:63487]$	76	1	_	Covered
bin auto $[63488:64511]$	55	1	_	Covered
bin auto $[64512:65535]$	941	1	_	Covered
		_	_	
Coverpoint r_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2		
			_	
% Hit:	100.00%	100	_	
$\operatorname{bin} \operatorname{auto}[0]$	3991	1	_	Covered
bin auto[1]	2034	1	_	Covered
Coverpoint w_en_cp	100.00%	100	_	Covered
covered/total bins:	2	2	_	
missing / total bins:	0	2	_	
% Hit:	100.00%	100	_	
bin auto [0]	2017	1	_	Covered
bin auto [1]	4008	1	_	Covered
			_	
Coverpoint data_out_cp	100.00%	100	_	Covered
covered/total bins:	64	64	_	
missing/total bins:	0	64		
% Hit:	100.00%	100	_	
bin auto $[0:1023]$	3334	1	_	Covered
bin auto [1024:2047]	36	1	_	Covered
bin auto [2048:3071]	13	1	_	Covered
bin auto $[3072:4095]$	44	1	_	Covered
bin auto [4096:5119]	53	1	_	Covered
bin auto [5120:6143]	57	1	_	Covered
bin auto $[6144:7167]$	48	1	_	Covered
bin auto [7168:8191]	50	1	_	Covered
i i				
bin auto $[8192:9215]$	43	1	_	Covered
bin auto [9216:10239]	27	1	_	Covered
bin auto [10240:11263]	44	1	_	Covered
· ·				
bin auto $[11264:12287]$	44	1	_	Covered
bin auto [12288:13311]	33	1	_	Covered
bin auto [13312:14335]	34	1	_	Covered
bin auto $[14336:15359]$	25	1	_	Covered
bin auto [15360:16383]	21	1	_	Covered
bin auto [16384:17407]	17	1	_	Covered
DIII aato [10004.11401]	11	1	_	Oovered

bin auto [17408:18431] bin auto [18432:19455]	19	1		Corrored
hip outo[19429.10455]		1	_	Covered
DIII auto [16452:19455]	51	1	_	Covered
bin auto [19456:20479]	25	1	_	Covered
bin auto [20480:21503]	39	1		Covered
·			_	
bin auto $[21504:22527]$	28	1	_	Covered
bin auto [22528:23551]	9	1	_	Covered
bin auto $[23552:24575]$	21	1	_	Covered
bin auto $[24576:25599]$	37	1		Covered
·			_	
bin auto $[25600:26623]$	38	1	_	Covered
bin auto $[26624:27647]$	35	1	_	Covered
bin auto [27648:28671]	52	1	_	Covered
bin auto [28672:29695]	44	1		Covered
			_	
bin auto $[29696:30719]$	31	1	_	Covered
bin auto [30720:31743]	29	1	_	Covered
bin auto [31744:32767]	25	1	_	Covered
bin auto $[32768:33791]$	46	1	_	Covered
bin auto [33792:34815]	38	1	_	Covered
bin auto [34816:35839]	41	1	_	Covered
	37			
bin auto [35840:36863]		1	_	Covered
bin auto $[36864:37887]$	26	1	_	Covered
bin auto [37888:38911]	32	1	_	Covered
bin auto [38912:39935]	50	1	_	Covered
,				
bin auto $[39936:40959]$	30	1	_	Covered
bin auto $[40960:41983]$	31	1	_	$\operatorname{Covered}$
bin auto [41984:43007]	33	1	_	Covered
bin auto $[43008:44031]$	45	1	_	Covered
bin auto $[44032:45055]$	29	1	_	Covered
bin auto $[45056:46079]$	26	1	_	Covered
bin auto [46080:47103]	47	1	_	Covered
bin auto [47104:48127]	11	1	_	Covered
			_	
bin auto $[48128:49151]$	32	1	_	Covered
bin auto $[49152:50175]$	28	1	_	Covered
bin auto [50176:51199]	25	1	_	Covered
	61			
bin auto [51200:52223]		1	_	Covered
bin auto $[52224:53247]$	22	1	_	Covered
bin auto $[53248:54271]$	18	1	_	Covered
bin auto $[54272:55295]$	47	1	_	Covered
,		1		
bin auto $[55296:56319]$	60	1	_	$\operatorname{Covered}$
bin auto $[56320:57343]$	41	1	_	Covered
bin auto [57344:58367]	17	1	_	Covered
bin auto [58368:59391]	44	1		Covered
		_		
bin auto $[59392:60415]$	82	1	_	Covered
bin auto $[60416:61439]$	31	1	_	Covered
bin auto [61440:62463]	52	1	_	Covered
		_		
bin auto $[62464:63487]$	32	1	_	Covered
bin auto [63488:64511]	21	1	_	Covered
bin auto $[64512:65535]$	484	1	_	Covered
Coverpoint wr_ack_cp	100.00%	100		Covered
			_	Covered
covered/total bins:	2	2	_	
missing/total bins:	0	2	_	
% Hit:	100.00%	100	_	
	2943	1		Covered
bin auto [0]		_	_	
bin auto [1]	3082	1	_	Covered
$\operatorname{Coverpoint}$ $\operatorname{overflow_cp}$	100.00%	100	_	Covered
covered/total bins:	2	2	_	
,	0	$\frac{1}{2}$		
missing/total bins:			_	
% Hit:	100.00%	100	_	
bin auto [0]	5457	1	_	$\operatorname{Covered}$
bin auto[1]	568			
Coverpoint full_cp		1	_	Covered
		1	_	Covered
covered/total bins:	100.00%	$\begin{matrix}1\\100\end{matrix}$	_	Covered Covered
		$100 \\ 2$	_ _ _	
	100.00%	_	_ _ _ _	
missing/total bins:	$100.00\% \ 2 \ 0$	100 2 2	_ _ _ _	
missing/total bins: % Hit:	$100.00\% \ 2 \ 0 \ 100.00\%$	100 2 2 100	- - - -	Covered
missing/total bins: % Hit: bin auto[0]	$100.00\% \ 2 \ 0 \ 100.00\% \ 5338$	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $	- - - -	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687	100 2 2 100 1 1	- - - - -	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp	100.00% 2 0 $100.00%$ 5338 687 $100.00%$	$ \begin{array}{c} 100 \\ 2 \\ 2 \\ 100 \\ 1 \end{array} $	- - - - - -	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687	100 2 2 100 1 1	- - - - - -	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins:	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2	100 2 2 100 1 1 100 2	- - - - - - -	Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins:	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0	100 2 2 100 1 1 100 2	- - - - - - -	Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100	 	Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty-cp covered/total bins: missing/total bins: % Hit: bin auto[0]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632	100 2 2 100 1 1 100 2	- - - - - - - - -	Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty-cp covered/total bins: missing/total bins: % Hit: bin auto[0]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632	100 2 2 100 1 1 100 2 2 100	 	Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393	100 2 2 100 1 1 100 2 2 100 1 1	 	Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$	100 2 2 100 1 1 100 2 2 100 1	 	Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2	100 2 2 100 1 1 100 2 2 100 1 1 100 2	 	Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0	100 2 2 100 1 1 100 2 2 100 1 1 100 2		Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: </pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0	100 2 2 100 1 1 100 2 2 100 1 1 100 2	 	Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100		Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: bin auto[0]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100 1 100 2 2 100 1		Covered Covered Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 4632 1393	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1		Covered Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 1 1 100 1 1 100 1 1 100 1 1 100 1 100		Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 4632 1393	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1		Covered Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] coverpoint almostempty_cp covered/total bins:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2		Covered Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] coverpoint almostempty_cp covered/total bins: missing/total bins: missing</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 2 100 1 1 100 2 2 2 2 100 1 1 100 2 2 2 2 2 2 2 2 2 2 2 2 2		Covered Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered Covered Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.40%$ 2 0 $100.40%$ 2 0 $100.40%$ 2 0 $100.40%$ 2 0 $100.40%$ 2	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 2 100 1 1 100 2 2 2 2 100 1 1 100 2 2 2 2 2 2 2 2 2 2 2 2 2		Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 2 2 100 2 2 100 2 2 100 1 100 2 2 100 100		Covered Covered Covered Covered Covered Covered Covered Covered Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.40%$ 2 0 $100.80%$ 2 0 $100.80%$ 2 0 $100.80%$ 2 0 $100.80%$	100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 100 100		Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] bin auto[1]</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] coverpoint underflow_cp covered/total bins:	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0	100 2 2 100 1 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 2 2 100 2 2 100 2		Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] coverpoint underflow_cp covered/total bins: missing/total bins:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] coverpoint underflow_cp covered/total bins:	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0	100 2 2 100 1 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 1 1 100 2 2 100 2 2 100 2 2 100 2		Covered
<pre>missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit:</pre>	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] coverpoint underflow_cp covered/total bins: missing/total bins: % Hit: bin auto[0] Keypoint underflow_cp covered/total bins: missing/total bins: missing/total bins: Mit: bin auto[0]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 5044 981 $100.00%$ 5044 981 $100.00%$ 5044 981	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[1]	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] bin auto[1] Cross wr_ack_cross	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 5044 981 $100.00%$ 5044 981 $100.00%$ 5044 981	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] bin auto[1] Cross wr_ack_cross	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: % Hit: bin auto[0] bin auto[1] Cross wr_ack_cross covered/total bins:	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 5044 981 $100.00%$ 5044 981 $100.00%$ 6	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered
missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint empty_cp covered/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostfull_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint almostempty_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[1] Coverpoint underflow_cp covered/total bins: missing/total bins: missing/total bins: % Hit: bin auto[0] bin auto[0] bin auto[0] bin auto[1] Cross wr_ack_cross	100.00% 2 0 $100.00%$ 5338 687 $100.00%$ 2 0 $100.00%$ 4632 1393 $100.00%$ 2 0 $100.00%$ 5570 455 $100.00%$ 2 0 $100.00%$ 2 0 $100.00%$ 5044 981 $100.00%$ 5044 981 $100.00%$ 719 $100.00%$	100 2 2 100 1 1 1 100 2 2 100 1 1 1 100 2 2 100 1 1 1 1		Covered

% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
bin < auto[1], auto[1], auto[1] >	892	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	216	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[1] \rangle$	$\begin{array}{c} 2190 \\ 710 \end{array}$	1	_	Covered Covered
$egin{aligned} & ext{bin } < ext{auto} \left[0 ight], ext{auto} \left[1 ight], ext{auto} \left[0 ight] > \ & ext{bin } < ext{auto} \left[1 ight], ext{auto} \left[0 ight], ext{auto} \left[0 ight] > \end{aligned}$	926	1 1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[0] \rangle$ bin $\langle \text{auto}[0], \text{auto}[0] \rangle$	1091	1	_	Covered
Illegal and Ignore Bins:	1031	1		Covered
ignore_bin_w_en_nactv_wr_ack	0		_	ZERO
Cross full_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right], \mathrm{auto} \left[1 \right] >$	613	1	_	Covered
$\mathrm{bin} \ <\! \mathrm{auto} \left[0 \right], \mathrm{auto} \left[0 \right], \mathrm{auto} \left[1 \right] \!>$	74	1	_	Covered
$\operatorname{bin} < \operatorname{auto}\left[1 ight], \operatorname{auto}\left[1 ight], \operatorname{auto}\left[0 ight] >$	1108	1	_	Covered
$\operatorname{bin} < \operatorname{auto} \left[1 \right], \operatorname{auto} \left[0 \right], \operatorname{auto} \left[0 \right] >$	926	1	_	Covered
bin < auto [0], auto [1], auto [0] >	2287	1	_	Covered
bin < auto[0], auto[0], auto[0] >	1017	1	_	Covered
Illegal and Ignore Bins:	0			ZDDO
ignore_bin r_en_actv_wr_full	0		_	ZERO
ignore_bin w_en_r_en_allactv_full	100.00%	100	_	ZERO
Cross empty_cross	100.00%	100	_	Covered
covered/total bins:	6 0	6	_	
missing/total bins: % Hit:	100.00%	$6 \\ 100$	_	
Auto, Default and User Defined Bins:	100.0070	100	_	
bin $<$ auto [1], auto [1] $>$	126	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1] \rangle$ bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	667	1		Covered
bin $\langle \text{auto}[1], \text{auto}[0], \text{auto}[1] \rangle$	982	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	2601	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	259	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[0], \text{auto}[0] \rangle$	790	1	_	Covered
Illegal and Ignore Bins:	, , ,	_		00,0104
ignore_bin read_nactv_empty	600		_	Occurred
Cross almostfull_cross	100.00%	100	_	Covered
covered/total bins:	6	6	_	
missing/total bins:	0	6	_	
% Hit:	100.00%	100	_	
Auto, Default and User Defined Bins:				
$\mathrm{bin} \ <\! \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right], \mathrm{auto} \left[1\right] >$	171	1	_	Covered
$\mathrm{bin}\ <\!\mathrm{auto}\left[1\right],\mathrm{auto}\left[0\right],\mathrm{auto}\left[1\right]>$	37	1	_	$\operatorname{Covered}$
$\mathrm{bin} \ < \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[0 ight] >$	937	1	_	Covered
$\mathrm{bin} \ < \mathrm{auto} \left[0 ight] , \mathrm{auto} \left[1 ight] , \mathrm{auto} \left[0 ight] >$	2737	1	_	Covered
bin < auto[1], auto[0], auto[0] >	889	1	_	Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] >$	1007	1	_	$\operatorname{Covered}$
Illegal and Ignore Bins:	0.47			0 1
ignore_bin w_en_nactv_almostfull	$247 \\ 100.00\%$	100	_	Occurred Covered
Cross almostempty_cross covered/total bins:	6	6	_	Covered
missing/total bins:	0	6	_	
% Hit:	100.00%	100		
Auto, Default and User Defined Bins:	100.0070	100		
bin <auto[1], auto[1]=""></auto[1],>	350	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[0] \rangle$	758	1	_	Covered
bin $\langle \text{auto}[1], \text{auto}[1], \text{auto}[1] \rangle$	401	1	_	Covered
bin $\langle \text{auto}[0], \text{auto}[1], \text{auto}[0] \rangle$	2499	1	_	
bin < auto[1], auto[0], auto[0] >				$\operatorname{Covered}$
	867	1	_	Covered Covered
$\operatorname{bin} < \operatorname{auto}[0], \operatorname{auto}[0], \operatorname{auto}[0] >$	$867 \\ 920$	$1\\1$	_	
Illegal and Ignore Bins:	920			Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty	920 230	1		Covered Covered Occurred
Illegal and Ignore Bins:	920 230 $100.00%$	1	_	Covered Covered
Illegal and Ignore Bins:	920 230 $100.00%$ 6	1 100 6	_	Covered Covered Occurred
Illegal and Ignore Bins:	$920 \ 230 \ 100.00\% \ 6 \ 0$	1 100 6 6	- - -	Covered Covered Occurred
Illegal and Ignore Bins:	920 230 $100.00%$ 6	1 100 6	- - -	Covered Covered Occurred
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins:	920 230 $100.00%$ 6 0 $100.00%$	1 100 6 6 100	- - - - -	Covered Covered Occurred Covered
Illegal and Ignore Bins:	920 230 $100.00%$ 6 0 $100.00%$ 109	$1 \\ 100 \\ 6 \\ 6 \\ 100 \\ 1$	- - - - -	Covered Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999	1 100 6 6 100	- - - - -	Covered Covered Covered Covered Covered
<pre>Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""></auto[0],></auto[1],></auto[1],></pre>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459	1 100 6 6 100 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441	1 100 6 6 100 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926	1 100 6 6 100 1 1 1 1		Covered Covered Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441	1 100 6 6 100 1 1 1	- - - - - -	Covered Covered Covered Covered Covered Covered Covered Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926	1 100 6 6 100 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091	1 100 6 6 100 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091	1 100 6 6 100 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6	1 100 6 6 100 1 1 1 1 1 1 1 1 1 6		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins:</auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 6 6		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]=""></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 6 6		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lilegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0],="" auto[1]=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900 2900	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[0],=""></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900 2900 415	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], a="" auto[0]<=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900 2900	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> Illegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: % Hit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins:</auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900 2900 415 1091	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered
Illegal and Ignore Bins: ignore_bin w_en_nactv_almostempty Cross overflow_cross covered/total bins: missing/total bins: Mit: Auto, Default and User Defined Bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[1],=""> bin <auto[0], auto[0]="" auto[0],=""> bin <auto[0], auto[0]="" auto[0],=""> lllegal and Ignore Bins: ignore_bin w_en_nactv_wr_ack Cross underflow_cross covered/total bins: missing/total bins: missing/total bins: bin <auto[1], auto[1]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[1],=""> bin <auto[1], auto[0]="" auto[0],=""> bin <auto[0], a="" auto[0]<=""></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],></auto[1],></auto[1],></auto[1],></auto[1],></auto[0],></auto[0],></auto[0],></auto[0],></auto[1],>	920 230 $100.00%$ 6 0 $100.00%$ 109 999 459 2441 926 1091 0 $100.00%$ 6 0 $100.00%$ 208 511 900 2900 415	1 100 6 6 100 1 1 1 1 1 1 1 1 1 1 1 1 1		Covered

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

Name	Design Unit	Design UnitType	_	File (Line)	Hits Status	
/top/cover_n_wr_ack_with_FIFO_Full	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/u 546 Covered	verification/top_module.sv(134)
/top/covercounter_threshold	top	Verilog	SVA		op/syn_fifo/u 5381 Covered	avm_verification/top_module.sv(133)
/top/cover_read_ptr_threshold	top	Verilog	SVA		op/syn_fifo/u 5381 Covered	<pre>ivm_verification/top_module.sv(132)</pre>
/top/cover_write_ptr_threshold	top	Verilog	SVA		op/syn_fifo/u 5381 Covered	<pre>ivm_verification/top_module.sv(131)</pre>
$/ top / cover_read_ptr_wrap around$	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/u 25 Covered	uvm_verification/top_module.sv(130)
/top/cover_write_ptr_wraparound	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/u 173 Covered	ivm_verification/top_module.sv(129)
$/top/cover_almost_empty_check$	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/u 881 Covered	avm_verification/top_module.sv(128)
/top/coveralmost_full_check	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/u 408 Covered	uvm_verification/top_module.sv(127)
/top/coverfull_flag_check	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/ι 612 Covered	avm_verification/top_module.sv(126)
/top/coverempty_flag_check	top	Verilog	SVA		op/syn_fifo/u 1234 Covered	avm_verification/top_module.sv(125)
/top/cover_underflow_check	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/ι 591 Covered	avm_verification/top_module.sv(124)
/top/coveroverflow_check	top	Verilog	SVA	/home/tare/Deskt	op/syn_fifo/ι 366 Covered	avm_verification/top_module.sv(123)
/top/cover_write_ack_check	top	Verilog	SVA			avm_verification/top_module.sv(122)
/top/cover_reset_behavior	top	Verilog	SVA			avm_verification/top_module.sv(121)

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 14

ASSERTION RESULTS:

Name	File (Line)	Failure Count	$\begin{array}{c} {\rm Pass} \\ {\rm Count} \end{array}$
/top/assert_n	_wr_ack_with_FIFO_Full /home/tare/Desktop/sy	,	, `
/top/assertc	ounter_threshold /home/tare/Desktop/sy	0 n_fifo/uvm_verific 0	5 ation/top_module.sv(1
/top/assertr	ead_ptr_threshold /home/tare/Desktop/sy	•	
/top/assertv	vrite_ptr_threshold /home/tare/Desktop/sy	v	
/top/assertre	ead_ptr_wraparound /home/tare/Desktop/sy	n_fifo/uvm_verific	
/top/assertw	rite_ptr_wraparound /home/tare/Desktop/sy	n_fifo/uvm_verific	
/top/assert_a	lmost_empty_check /home/tare/Desktop/sy	·	
/top/asserta	almost_full_check /home/tare/Desktop/sy	·	
/top/assertf	full_flag_check /home/tare/Desktop/sy	·	
/top/asserte	mpty_flag_check /home/tare/Desktop/sy		
/top/assertu	nderflow_check /home/tare/Desktop/sy	n_fifo/uvm_verific	ation/top_module.sv(
/top/asserto	verflow_check /home/tare/Desktop/sy	0 rn_fifo/uvm_verific	5 ation/top_module.sv(1
/top/assert_w	vrite_ack_check /home/tare/Desktop/sy	vn_fifo/uvm_verific	· _ ·
/top/assert_r	eset_behavior /home/tare/Desktop/sy	orn_fifo/uvm_verific	5 ation/top_module.sv() 5
Total Coverage	e By File (code coverage only	, filtered view):	75.46%