SV Project

Digital Design Verification

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1 Synchronous FIFO

1.1 Shared package

```
package Shared_pkg;
    // ===== Global parameter for Signal Declaration =====
    parameter FIFO_WIDTH = 16;
    parameter FIFO_DEPTH = 8;

    // ===== Signals For Test Control ======
    // ===== #No of Randomization ======
    parameter TEST_COUNT = 1000;
    // ===== Counter For Failed and Successed Test Transactions ======
    int unsigned error_count = 0;
    int unsigned correct_count = 0;
    // ===== When eq 1 Trim Test =====
    bit test_finished = 0;
endpackage
```

1.2 Top Module

1.3 FIFO_IF

```
import Shared_pkg::*;
import FIFO_test_pkg::*;
import uvm_pkg::*;
`include "uvm_macros.svh"

module top();
   bit clk;

   initial begin
     forever
        #1 clk = ~clk;
   end

   FIFO_IF fifo_intf (clk);

   FIFO #(
    .FIFO_WIDTH(FIFO_WIDTH),
    .FIFO_DEPTH(FIFO_DEPTH)
   ) dut (
    .fifo_intf(fifo_intf)
   );

   initial begin
      uvm_config_db#(virtual FIFO_IF)::set(null, "uvm_test_top", "FIFO_VIF", fifo_intf);
      run_test("FIFO_test");
   end


// ========================================
// Assertions using conditional compilation
// ========================================
`ifdef SIM

    // ===== Reset behavior assertion =====
    property reset_behavior;
        @(posedge fifo_intf.clk) (!fifo_intf.rst_n) |=>  (dut.count == 0 && dut.rd_ptr == 0 && dut.wr_ptr == 0
                  && !fifo_intf.wr_ack && !fifo_intf.overflow  && !fifo_intf.underflow && fifo_intf.data_out <= {FIFO_WIDTH{1'b0}});
    endproperty

    // ===== Whenever the FIFO is full, wr_ack is always = 0 =====
    property n_wr_ack_with_FIFO_Full;
            @(posedge clk) disable iff (!fifo_intf.rst_n) (fifo_intf.full |=> !fifo_intf.wr_ack)
    endproperty

    // ===== Write acknowledge assertion =====
    property write_ack_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full) |=> fifo_intf.wr_ack;
    endproperty

    // ===== Overflow detection assertion =====
    property overflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && fifo_intf.full && !fifo_intf.rd_en) |=>
           fifo_intf.overflow;
    endproperty

    // ===== Underflow detection assertion =====
    property underflow_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && fifo_intf.empty) |=> fifo_intf.underflow;
    endproperty

    // ===== Empty flag assertion =====
    property empty_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.count == 0) |-> fifo_intf.empty;
    endproperty

    // ===== Full flag assertion =====
    property full_flag_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.count == FIFO_DEPTH) |-> fifo_intf.full;
    endproperty

    // ===== Almost full condition assertion =====
    property almost_full_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.count == FIFO_DEPTH-1) |-> fifo_intf.almostfull;
    endproperty
```

```
    // ===== Almost empty condition assertion =====
    property almost_empty_check;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.count == 1) |-> fifo_intf.almostempty;
    endproperty

    // ===== Pointer wraparound assertion for write_ptr =====
    property write_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.wr_en && !fifo_intf.full && dut.wr_ptr == FIFO_DEPTH-1) |=>
            (dut.wr_ptr == 0);
    endproperty

    // ===== Pointer wraparound assertion for read_ptr =====
    property read_ptr_wraparound;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (fifo_intf.rd_en && !fifo_intf.empty && dut.rd_ptr == FIFO_DEPTH-1) |=>
            (dut.rd_ptr == 0);
    endproperty

    // ===== Pointer threshold assertion for write_ptr =====
    property write_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.wr_ptr < FIFO_DEPTH);
    endproperty

    // ===== Pointer threshold assertion for read_ptr =====
    property read_ptr_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.rd_ptr < FIFO_DEPTH);
    endproperty

    // ===== Counter threshold assertion =====
    property counter_threshold;
        @(posedge fifo_intf.clk)  disable iff (!fifo_intf.rst_n) (dut.count <= FIFO_DEPTH);
    endproperty

    // ===== Assert all the properties =====
    assert property (reset_behavior)       else $error("Reset behavior assertion failed!");
    assert property (write_ack_check)      else $error("Write acknowledge assertion failed!");
    assert property (overflow_check)       else $error("Overflow detection assertion failed!");
    assert property (underflow_check)      else $error("Underflow detection assertion failed!");
    assert property (empty_flag_check)     else $error("Empty flag assertion failed!");
    assert property (full_flag_check)      else $error("Full flag assertion failed!");
    assert property (almost_full_check)    else $error("Almost full condition assertion failed!");
    assert property (almost_empty_check)   else $error("Almost empty condition assertion failed!");
    assert property (write_ptr_wraparound) else $error("Write pointer wraparound assertion failed!");
    assert property (read_ptr_wraparound)  else $error("Read pointer wraparound assertion failed!");
    assert property (write_ptr_threshold)  else $error("Write pointer threshold assertion failed!");
    assert property (read_ptr_threshold)   else $error("Read pointer threshold assertion failed!");
    assert property (counter_threshold)    else $error("Counter threshold assertion failed!");
    assert property (n_wr_ack_with_FIFO_Full) else $error("Dasserted Write Ack With FIFO Full assertion failed!");

    cover property (reset_behavior);
    cover property (write_ack_check);
    cover property (overflow_check);
    cover property (underflow_check);
    cover property (empty_flag_check);
    cover property (full_flag_check);
    cover property (almost_full_check);
    cover property (almost_empty_check);
    cover property (write_ptr_wraparound);
    cover property (read_ptr_wraparound);
    cover property (write_ptr_threshold);
    cover property (read_ptr_threshold);
    cover property (counter_threshold);
    cover property (n_wr_ack_with_FIFO_Full);

`endif

endmodule
```

1.4 FIFO_config_obj_pkg

```
package FIFO_config_obj_pkg;

  import uvm_pkg::*;
  `include "uvm_macros.svh"

  class FIFO_config_obj extends uvm_object;
    `uvm_object_utils(FIFO_config_obj)

    virtual FIFO_IF FIFO_config_vif;

    function new (string name = "FIFO_config_obj");
      super.new(name);
    endfunction

  endclass

endpackage
```

1.5 FIFO_test_pkg

```
package FIFO_test_pkg;

import FIFO_env_pkg::*;
import FIFO_config_obj_pkg::*;
import FIFO_sequence_pkg::*;
import uvm_pkg::*;
`include "uvm_macros.svh"

```

```
class FIFO_test extends uvm_test;
   `uvm_component_utils(FIFO_test)

    FIFO_env env;
    FIFO_config_obj FIFO_config_obj_test;
    FIFO_Sequence seq;

    function new (string name = "FIFO_test", uvm_component parent = null);
        super.new(name,parent);
    endfunction

    function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        env = FIFO_env::type_id::create("env",this);
        FIFO_config_obj_test = FIFO_config_obj::type_id::create("FIFO_config_obj_test",this);
        seq = FIFO_Sequence::type_id::create("seq");

        if (!uvm_config_db#(virtual FIFO_IF)::get(this, "", "FIFO_VIF", FIFO_config_obj_test.FIFO_config_vif))
                    `uvm_fatal("NOVIF", "Virtual interface FIFO_test_vif was not found in the configuration database");

        uvm_config_db#(FIFO_config_obj)::set(this,"*","CFG",FIFO_config_obj_test);
    endfunction

    task run_phase(uvm_phase phase);
        super.run_phase(phase);
        phase.raise_objection(this);
        `uvm_info("run_phase","Inside the FIFO test.",UVM_MEDIUM);
    seq.start(env.agt.sqr);
    phase.drop_objection(this);
    endtask : run_phase

endclass : FIFO_test

endpackage
```

1.6 FIFO_sequence_pkg

```
package FIFO_sequence_pkg;

import uvm_pkg::*;
`include "uvm_macros.svh"
import FIFO_sequence_item_pkg::*;

class FIFO_Sequence extends uvm_sequence #(FIFO_seq_item);
    `uvm_object_utils(FIFO_Sequence)
    FIFO_seq_item item;

    function new(string name = "FIFO_Sequence");
        super.new(name);
    endfunction

    virtual task body();
    item = FIFO_seq_item::type_id::create("item");
         // ===== force reset ====
        item.force_rst_item;
        repeat(5) begin
            start_item(item);
        if (!item.randomize())
                `uvm_error("RAND_FAIL", "Failed to force reset randomize FIFO sequence item");
        finish_item(item);
    end

        // ===== simultaneous Read And Write =====
    item.ctrl_seq_item(30,70);
    repeat(1000) begin
        start_item(item);
        if (!item.randomize())
                `uvm_error("RAND_FAIL", "Failed to simultaneous Read And Write randomize FIFO sequence item");
        finish_item(item);
    end

    // ===== Read only =====
    item.ctrl_seq_item(0,100);
    repeat(100) begin
        start_item(item);
        if (!item.randomize())
                `uvm_error("RAND_FAIL", "Failed to Read only randomize FIFO sequence item");
        finish_item(item);
    end

    // ===== Write only =====
    item.ctrl_seq_item(100,0);
    repeat(100) begin
        start_item(item);
        if (!item.randomize())
                `uvm_error("RAND_FAIL", "Failed to Write only randomize FIFO sequence item");
        finish_item(item);
    end

    endtask

endclass

endpackage
```

1.7 FIFO_env_pkg

```
package FIFO_env_pkg;
```

```

import uvm_pkg::*;
`include "uvm_macros.svh"
import FIFO_coverage_pkg::*;
import FIFO_scoreboard_pkg::*;
import FIFO_agent_pkg::*;

    class FIFO_env extends uvm_env;
        `uvm_component_utils(FIFO_env)

        FIFO_agent agt;
        FIFO_scoreboard sb;
        FIFO_coverage cov;

        function new (string name = "FIFO_env", uvm_component parent = null);
        super.new(name,parent);
        endfunction

        function void build_phase(uvm_phase phase);
            super.build_phase(phase);
            agt = FIFO_agent::type_id::create("agt",this);
            sb  = FIFO_scoreboard::type_id::create("sb",this);
            cov = FIFO_coverage::type_id::create("cov",this);
        endfunction: build_phase

            function void connect_phase(uvm_phase phase);
            agt.agt_ap.connect(sb.sb_export);
            agt.agt_ap.connect(cov.cov_export);
        endfunction: connect_phase

    endclass : FIFO_env

endpackage
```

1.8 FIFO_coverage_pkg

```

package FIFO_coverage_pkg;

import uvm_pkg::*;
`include "uvm_macros.svh"
import FIFO_sequence_item_pkg::*;

class FIFO_coverage extends uvm_component;
    `uvm_component_utils(FIFO_coverage)
    uvm_analysis_export #(FIFO_seq_item) cov_export;
    uvm_tlm_analysis_fifo #(FIFO_seq_item) cov_fifo;
    FIFO_seq_item seq_item_cov;

    // ===== Cover Group =====
    covergroup fifo_cg;

        // ====== Cover I/O Ports ======
        rst_n_cp:   coverpoint seq_item_cov.rst_n;
        data_in_cp:     coverpoint seq_item_cov.data_in;
        r_en_cp:    coverpoint seq_item_cov.rd_en;
        w_en_cp:    coverpoint seq_item_cov.wr_en;
        data_out_cp:    coverpoint seq_item_cov.data_out;
        wr_ack_cp:      coverpoint seq_item_cov.wr_ack;
        overflow_cp:    coverpoint seq_item_cov.overflow;
        full_cp:    coverpoint seq_item_cov.full;
        empty_cp:       coverpoint seq_item_cov.empty;
        almostfull_cp:  coverpoint seq_item_cov.almostfull;
        almostempty_cp: coverpoint seq_item_cov.almostempty;
        underflow_cp:   coverpoint seq_item_cov.underflow;


        // ====== "7" Cross Coverage ======
        wr_ack_cross:     cross r_en_cp ,w_en_cp ,wr_ack_cp{
            ignore_bins w_en_nactv_wr_ack        = binsof(w_en_cp) intersect {1'b0} && binsof(wr_ack_cp) intersect {1'b1};
        }
        full_cross:       cross r_en_cp ,w_en_cp ,full_cp{
            // full not asserted when both read and write enabled
            ignore_bins w_en_r_en_allactv_full   = binsof(w_en_cp) intersect {1'b1} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
               intersect {1'b1};
            // full not asserted when read enabled
            ignore_bins r_en_actv_wr_full        = binsof(w_en_cp) intersect {1'b0} && binsof(r_en_cp) intersect {1'b1} && binsof(full_cp)
               intersect {1'b1};
        }

        empty_cross:      cross r_en_cp ,w_en_cp ,empty_cp{
            ignore_bins read_nactv_empty         = binsof(r_en_cp) intersect {1'b0} && binsof(empty_cp) intersect {1'b1};
        }

        almostfull_cross:  cross r_en_cp ,w_en_cp ,almostfull_cp{
                // who almostfull with read
            ignore_bins w_en_nactv_almostfull    = binsof(r_en_cp) intersect {1'b0} && binsof(almostfull_cp) intersect {1'b1};
        }

        almostempty_cross: cross r_en_cp ,w_en_cp ,almostempty_cp{
            // who almostempty with write
            ignore_bins w_en_nactv_almostempty   = binsof(w_en_cp) intersect {1'b0} && binsof(almostempty_cp) intersect {1'b1};
        }

        overflow_cross:    cross r_en_cp ,w_en_cp ,overflow_cp{
            ignore_bins w_en_nactv_wr_ack        = binsof(w_en_cp) intersect {1'b0} && binsof(overflow_cp) intersect {1'b1};
        }

        underflow_cross:   cross r_en_cp ,w_en_cp ,underflow_cp{
            ignore_bins r_en_nactv_wr_ack        = binsof(r_en_cp) intersect {1'b0} && binsof(underflow_cp) intersect {1'b1};
        }
```

```
        endgroup


    function new(string name="FIFO_coverage" , uvm_component parent = null);
        super.new(name,parent);
        fifo_cg = new();
    endfunction

    function void build_phase (uvm_phase phase);
        super.build_phase(phase);
        cov_export = new("cov_export",this);
        cov_fifo = new("cov_fifo",this);
    endfunction: build_phase

    function void connect_phase (uvm_phase phase);
        super.connect_phase(phase);
        cov_export.connect(cov_fifo.analysis_export);
    endfunction: connect_phase

    task run_phase (uvm_phase phase);
        super.run_phase(phase);
        forever begin
            cov_fifo.get(seq_item_cov);
            fifo_cg.sample();
        end
    endtask: run_phase

endclass
endpackage
```

1.9 FIFO_sequence_item_pkg

```
package FIFO_sequence_item_pkg ;

import Shared_pkg::*;
import uvm_pkg::*;
`include "uvm_macros.svh"

class FIFO_seq_item extends uvm_sequence_item;
    `uvm_object_utils(FIFO_seq_item)

    // ====================================================
    // Transaction Distribution "Set to Default Values"
    // ====================================================
    int RD_EN_ON_DIST;
    int WR_EN_ON_DIST;

    bit force_rst = 1;

    // ==================
    // Class Constructor
    // ==================
        function new(string name = "FIFO_seq_item");
        super.new(name);
    endfunction

    // ==== input signals ====
    rand bit rst_n;
    rand bit [FIFO_WIDTH-1:0] data_in;
    rand bit wr_en;
    rand bit rd_en;

    // ==== output signals ====
    bit [FIFO_WIDTH-1:0] data_out;
    bit wr_ack, overflow;
    bit full, empty, almostfull, almostempty, underflow;

        // ====================================================
    // Dassert Reset "Asyn - Active Low" most of the times
    // ====================================================
        constraint rst_c {
            if (!force_rst) {
               rst_n dist {0:/10 , 1:/90};
            }
            if (force_rst) {
               rst_n dist {0:=100, 1:=0};
            }
         }

         constraint data_in_c {
                data_in dist {0:/15 , {FIFO_WIDTH{1'b1}}:/15 , [1:{FIFO_WIDTH{1'b1}}-1] :/ 70};
         }

    // ========================================================
    // Only, Enable Write Enable Signal During "WR_EN_ON_DIST"
    // ========================================================
    constraint wr_en_c { wr_en dist {1 := WR_EN_ON_DIST, 0 := 100-WR_EN_ON_DIST};}

    // ========================================================
    // Only, Enable Read Enable Signal During "RD_EN_ON_DIST"
    // ========================================================
    constraint rd_en_c { rd_en dist {1 := RD_EN_ON_DIST, 0 := 100-RD_EN_ON_DIST};}

    function void ctrl_seq_item (int rd_dist = 30 ,int wr_dist = 70);
        RD_EN_ON_DIST = rd_dist;
        WR_EN_ON_DIST = wr_dist;
        force_rst = 0;
    endfunction

```

```
        function void force_rst_item;
        force_rst = 1;
    endfunction

endclass

endpackage
```

1.10 FIFO_sequencer_pkg

```
package FIFO_sequencer_pkg;

import uvm_pkg::*;
`include "uvm_macros.svh"
import FIFO_sequence_item_pkg::*;

class FIFO_sequencer extends uvm_sequencer #(FIFO_seq_item);
    `uvm_component_utils(FIFO_sequencer)

    function new(string name = "FIFO_sequencer" ,uvm_component parent = null);
        super.new(name ,parent);
    endfunction

endclass

endpackage
```

1.11 FIFO_agent_pkg

```
package FIFO_agent_pkg;

import uvm_pkg::*;
import FIFO_sequencer_pkg::*;
import FIFO_driver_pkg::*;
import FIFO_monitor_pkg::*;
import FIFO_config_obj_pkg::*;
import FIFO_sequence_item_pkg::*;
`include "uvm_macros.svh"

class FIFO_agent extends uvm_agent;

        `uvm_component_utils(FIFO_agent)
    FIFO_sequencer sqr;
    FIFO_driver drv;
    FIFO_monitor mon;
    FIFO_config_obj FIFO_cfg;
        uvm_analysis_port #(FIFO_seq_item) agt_ap;

    function new(string name = "FIFO_agent",uvm_component parent = null);
        super.new(name,parent);
    endfunction

    function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        if(!uvm_config_db #(FIFO_config_obj)::get(this,"","CFG",FIFO_cfg))
            `uvm_fatal("build_phase","unable to get configuration object");
        sqr=FIFO_sequencer::type_id::create("sqr",this);
        drv=FIFO_driver::type_id::create("drv",this);
        mon=FIFO_monitor::type_id::create("mon",this);
        agt_ap = new("agt_ap", this);
    endfunction

    function void connect_phase(uvm_phase phase);
            super.connect_phase(phase);
        drv.FIFO_driver_vif=FIFO_cfg.FIFO_config_vif;
        mon.FIFO_vif=FIFO_cfg.FIFO_config_vif;
        drv.seq_item_port.connect(sqr.seq_item_export);
            mon.mon_ap.connect(agt_ap);
    endfunction

endclass

endpackage
```

1.12 FIFO_driver_pkg

```
package FIFO_driver_pkg;

import uvm_pkg::*;
import FIFO_config_obj_pkg::*;
import FIFO_sequence_item_pkg::*;
`include "uvm_macros.svh"

    class FIFO_driver extends uvm_driver #(FIFO_seq_item);
      `uvm_component_utils(FIFO_driver)

      virtual FIFO_IF FIFO_driver_vif;
      FIFO_config_obj FIFO_cfg_obj_drv;
      FIFO_seq_item stim_seq_item;

      function new(string name = "FIFO_driver", uvm_component parent = null);
        super.new(name, parent);
      endfunction

      function void build_phase(uvm_phase phase);
        super.build_phase(phase);
        if (!uvm_config_db#(FIFO_config_obj)::get(this, "", "CFG", FIFO_cfg_obj_drv)) begin
```

```
          `uvm_fatal("build_phase", "Driver - Unable to get configuration object")
        end
      endfunction

      function void connect_phase(uvm_phase phase);
        FIFO_driver_vif = FIFO_cfg_obj_drv.FIFO_config_vif;
      endfunction


        task run_phase(uvm_phase phase);
            super.run_phase(phase);
            forever begin
                stim_seq_item = FIFO_seq_item::type_id::create("stim_seq_item");
                seq_item_port.get_next_item(stim_seq_item);

                // ==== Input =====
                FIFO_driver_vif.data_in  = stim_seq_item.data_in;
                FIFO_driver_vif.wr_en    = stim_seq_item.wr_en;
                FIFO_driver_vif.rd_en    = stim_seq_item.rd_en;
                FIFO_driver_vif.rst_n    = stim_seq_item.rst_n;

                // Wait for the next negative clock edge
                @(negedge FIFO_driver_vif.clk);

                seq_item_port.item_done();
            end

        endtask

    endclass
endpackage
```

1.13 FIFO_monitor_pkg

```
package FIFO_monitor_pkg;

import uvm_pkg::*;
`include "uvm_macros.svh"
import FIFO_sequence_item_pkg::*;

class FIFO_monitor extends uvm_monitor ;

       `uvm_component_utils(FIFO_monitor)
    virtual FIFO_IF FIFO_vif;
    FIFO_seq_item rsp_seq_item;
    uvm_analysis_port #(FIFO_seq_item) mon_ap;

    function new(string name = "FIFO_monitor", uvm_component parent = null);
        super.new(name ,parent);
    endfunction

    function void build_phase (uvm_phase phase);
        super.build_phase(phase);
        mon_ap = new("mon_ap",this);
    endfunction

    task run_phase (uvm_phase phase);
        super.run_phase(phase);
        forever begin
            rsp_seq_item = FIFO_seq_item::type_id::create("rsp_seq_item");
                // ==== Wait for posedge clock to sample data ====
                @(posedge FIFO_vif.clk);
                // ==== smale delay for stable output ====
                        #1;

                // ==== Wait for sampling event from testbench ====
                FIFO_vif.trigger_sample();
                // ==== Input =====
                rsp_seq_item.data_in = FIFO_vif.data_in;
                rsp_seq_item.wr_en   = FIFO_vif.wr_en;
                rsp_seq_item.rd_en   = FIFO_vif.rd_en;
                rsp_seq_item.rst_n   = FIFO_vif.rst_n;

                // ==== Output =====
                rsp_seq_item.data_out    = FIFO_vif.data_out ;
                rsp_seq_item.full        = FIFO_vif.full;
                rsp_seq_item.empty       = FIFO_vif.empty ;
                rsp_seq_item.almostfull  = FIFO_vif.almostfull;
                rsp_seq_item.almostempty = FIFO_vif.almostempty;
                rsp_seq_item.overflow    = FIFO_vif.overflow ;
                rsp_seq_item.underflow   = FIFO_vif.underflow;
                rsp_seq_item.wr_ack      = FIFO_vif.wr_ack ;

                mon_ap.write(rsp_seq_item);
        end
    endtask

endclass

endpackage
```

1.14 FIFO_scoreboard_pkg

1.15 FIFO

```
module FIFO(FIFO_IF.DUT fifo_intf);
parameter FIFO_WIDTH = 16;
parameter FIFO_DEPTH = 8;

localparam max_fifo_addr = $clog2(FIFO_DEPTH);

reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];  // 1-D Array

reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
reg [max_fifo_addr:0] count;

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        wr_ptr <= 0;
        fifo_intf.wr_ack <= 0;
        fifo_intf.overflow <= 0;
    end
    else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
        mem[wr_ptr] <= fifo_intf.data_in;
        fifo_intf.wr_ack <= 1;
        wr_ptr <= wr_ptr + 1;
    end
    else begin
        fifo_intf.wr_ack <= 0;
        if (fifo_intf.full & fifo_intf.wr_en)
            fifo_intf.overflow <= 1;
        else
            fifo_intf.overflow <= 0;
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        rd_ptr <= 0;
        fifo_intf.underflow <= 0;
        fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
    end
    else if (fifo_intf.rd_en && count != 0) begin
        fifo_intf.data_out <= mem[rd_ptr];
        rd_ptr <= rd_ptr + 1;
    end
    else begin
        if (fifo_intf.empty & fifo_intf.rd_en)
            fifo_intf.underflow <= 1;
        else
            fifo_intf.underflow <= 0;
    end
end

always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    if (!fifo_intf.rst_n) begin
        count <= 0;
    end
    else begin
        if  ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.full)
            count <= count + 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.empty)
            count <= count - 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.full)
            count <= count - 1;
        else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.empty)
            count <= count + 1;
    end
end

assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
assign fifo_intf.almostempty = (count == 1)? 1 : 0;

endmodule
```

2 Makefile Contain Do File

```
VSIM = vsim
VLOG = qverilog

# Define UVM Directory
UVMDIR = ${FIFO_ROOT}/uvm_verification

# Target flist
target = src_files
FLIST = ${target}.list

VPATH = $(UVMDIR)
TBFILES = $(UVMDIR)/$(FLIST)

# Define 5 seed values
SEEDS = 1111 1511 2515 2236 5215

# Targets
clean:
	rm -rf *.log *.dis *.tbl vcs* simv* *.map transcript *.ucdb *.wlf *.txt \
	work dataset.asdb  library.cfg work

###################### Simulation Runs ######################################
questa: ${TBFILES}
```

```
	$(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +cover -covercells -R +nowarn3829
	$(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"

questa+SIM: ${TBFILES}
	$(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
	$(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -do "do wave.do; coverage save FIFO.ucdb -onexit; run -all"

# Run simulation with a specific seed
seed%: ${TBFILES}
	@echo "Running simulation with seed $*"
	$(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
	$(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -sv_seed $* -do "do wave.do; coverage save FIFO_seed$*.ucdb -
	vcover report FIFO_seed$*.ucdb -details -annotate -all -output code_coverage_rpt_seed$*.txt -du=FIFO
	vcover report -details -cvg -output functional_coverage_report_seed$*.txt FIFO_seed$*.ucdb

# Run all seeds in sequence
all_seeds: ${TBFILES}
	@echo "Running simulations with all seeds"
	$(VLOG) -l vlog.log -sv -mfcu -f ${TBFILES} +define+SIM +cover -covercells -R +nowarn3829
	@for seed in $(SEEDS); do \
		echo ""; \
		echo "Running simulation with seed $$seed"; \
		$(VSIM) -voptargs=+acc work.top -classdebug -uvmcontrol=all -cover -sv_seed $$seed -do "do wave.do; coverage save FIFO_s
		vcover report FIFO_seed$$seed.ucdb -details -annotate -all -output code_coverage_rpt_seed$$seed.txt -du=FIFO; \
		vcover report -details -cvg -output functional_coverage_report_seed$$seed.txt FIFO_seed$$seed.ucdb; \
	done
	@echo "All seed runs completed"

# Merge coverage results from all seeds
merge_coverage:
	@echo "Merging coverage from all seed runs"
	vcover merge merged.ucdb FIFO_seed*.ucdb
	$(VSIM) -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
	vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
	vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
	@echo "Coverage merged to merged.ucdb and reports saved"

# Run all seeds and merge coverage
run_seeds: all_seeds merge_coverage
	@echo "Complete seed-based simulation and coverage analysis finished"

help:
	@echo Make sure the environment variable FIFO_ROOT is set.
	@echo Possible targets:
	@echo "  questa         - Run basic simulation"
	@echo "  questa+SIM     - Run simulation with +SIM defined"
	@echo "  seed<number>   - Run simulation with specific seed (e.g., seed1, seed2)"
	@echo "  all_seeds      - Run simulations with all predefined seeds"
	@echo "  merge_coverage- Merge coverage data from all seed runs"
	@echo "  run_seeds      - Run all seeds and merge coverage"
	@echo "  clean          - Clean up simulation files"
```

3 Functional Coverage Report

3.1 Functional Coverage "seed1" Report

Coverage Report by instance with details

```
================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
================================================================================
```

Covergroup Coverage:				
Covergroups	1	na	na	99.58%
Coverpoints/Crosses	19	na	na	na
Covergroup Bins	190	185	5	97.36%

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100	–	Uncovered
covered/total bins:	185	190	–	
missing/total bins:	5	190	–	
% Hit:	97.36%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	137	1	–	Covered
bin auto[1]	1068	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	190	1	–	Covered
bin auto[1024:2047]	9	1	–	Covered
bin auto[2048:3071]	9	1	–	Covered
bin auto[3072:4095]	12	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	12	1	–	Covered

bin auto[6144:7167]	10	1	–	Covered
bin auto[7168:8191]	11	1	–	Covered
bin auto[8192:9215]	12	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	15	1	–	Covered
bin auto[13312:14335]	12	1	–	Covered
bin auto[14336:15359]	17	1	–	Covered
bin auto[15360:16383]	9	1	–	Covered
bin auto[16384:17407]	13	1	–	Covered
bin auto[17408:18431]	14	1	–	Covered
bin auto[18432:19455]	20	1	–	Covered
bin auto[19456:20479]	21	1	–	Covered
bin auto[20480:21503]	7	1	–	Covered
bin auto[21504:22527]	18	1	–	Covered
bin auto[22528:23551]	18	1	–	Covered
bin auto[23552:24575]	13	1	–	Covered
bin auto[24576:25599]	10	1	–	Covered
bin auto[25600:26623]	17	1	–	Covered
bin auto[26624:27647]	17	1	–	Covered
bin auto[27648:28671]	12	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	11	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	12	1	–	Covered
bin auto[32768:33791]	11	1	–	Covered
bin auto[33792:34815]	14	1	–	Covered
bin auto[34816:35839]	13	1	–	Covered
bin auto[35840:36863]	13	1	–	Covered
bin auto[36864:37887]	13	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	19	1	–	Covered
bin auto[41984:43007]	9	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	7	1	–	Covered
bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	11	1	–	Covered
bin auto[48128:49151]	15	1	–	Covered
bin auto[49152:50175]	10	1	–	Covered
bin auto[50176:51199]	11	1	–	Covered
bin auto[51200:52223]	14	1	–	Covered
bin auto[52224:53247]	12	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	20	1	–	Covered
bin auto[55296:56319]	11	1	–	Covered
bin auto[56320:57343]	10	1	–	Covered
bin auto[57344:58367]	16	1	–	Covered
bin auto[58368:59391]	15	1	–	Covered
bin auto[59392:60415]	17	1	–	Covered
bin auto[60416:61439]	18	1	–	Covered
bin auto[61440:62463]	18	1	–	Covered
bin auto[62464:63487]	13	1	–	Covered
bin auto[63488:64511]	14	1	–	Covered
bin auto[64512:65535]	201	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	777	1	–	Covered
bin auto[1]	428	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	396	1	–	Covered
bin auto[1]	809	1	–	Covered
Coverpoint data_out_cp	92.18%	100	–	Uncovered
covered/total bins:	59	64	–	
missing/total bins:	5	64	–	
% Hit:	92.18%	100	–	
bin auto[0:1023]	687	1	–	Covered
bin auto[1024:2047]	1	1	–	Covered
bin auto[2048:3071]	5	1	–	Covered
bin auto[3072:4095]	4	1	–	Covered
bin auto[4096:5119]	15	1	–	Covered
bin auto[5120:6143]	9	1	–	Covered
bin auto[6144:7167]	2	1	–	Covered
bin auto[7168:8191]	4	1	–	Covered
bin auto[8192:9215]	3	1	–	Covered
bin auto[9216:10239]	3	1	–	Covered
bin auto[10240:11263]	30	1	–	Covered
bin auto[11264:12287]	9	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	8	1	–	Covered
bin auto[14336:15359]	6	1	–	Covered
bin auto[15360:16383]	0	1	–	ZERO
bin auto[16384:17407]	0	1	–	ZERO
bin auto[17408:18431]	1	1	–	Covered

bin auto[18432:19455]	7	1	–	Covered
bin auto[19456:20479]	14	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	5	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	0	1	–	ZERO
bin auto[24576:25599]	11	1	–	Covered
bin auto[25600:26623]	13	1	–	Covered
bin auto[26624:27647]	8	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	3	1	–	Covered
bin auto[31744:32767]	3	1	–	Covered
bin auto[32768:33791]	4	1	–	Covered
bin auto[33792:34815]	8	1	–	Covered
bin auto[34816:35839]	4	1	–	Covered
bin auto[35840:36863]	6	1	–	Covered
bin auto[36864:37887]	2	1	–	Covered
bin auto[37888:38911]	1	1	–	Covered
bin auto[38912:39935]	4	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	10	1	–	Covered
bin auto[41984:43007]	2	1	–	Covered
bin auto[43008:44031]	11	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	7	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	1	1	–	Covered
bin auto[49152:50175]	10	1	–	Covered
bin auto[50176:51199]	7	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	1	1	–	Covered
bin auto[53248:54271]	3	1	–	Covered
bin auto[54272:55295]	12	1	–	Covered
bin auto[55296:56319]	14	1	–	Covered
bin auto[56320:57343]	1	1	–	Covered
bin auto[57344:58367]	3	1	–	Covered
bin auto[58368:59391]	6	1	–	Covered
bin auto[59392:60415]	24	1	–	Covered
bin auto[60416:61439]	8	1	–	Covered
bin auto[61440:62463]	16	1	–	Covered
bin auto[62464:63487]	5	1	–	Covered
bin auto[63488:64511]	0	1	–	ZERO
bin auto[64512:65535]	108	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	575	1	–	Covered
bin auto[1]	630	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1109	1	–	Covered
bin auto[1]	96	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1091	1	–	Covered
bin auto[1]	114	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	919	1	–	Covered
bin auto[1]	286	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1128	1	–	Covered
bin auto[1]	77	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	973	1	–	Covered
bin auto[1]	232	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1050	1	–	Covered
bin auto[1]	155	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	

Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	191	1	–	Covered
bin <auto[1],auto[1],auto[0]>	47	1	–	Covered
bin <auto[0],auto[1],auto[1]>	439	1	–	Covered
bin <auto[0],auto[1],auto[0]>	132	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	104	1	–	Covered
bin <auto[0],auto[0],auto[1]>	10	1	–	Covered
bin <auto[1],auto[1],auto[0]>	238	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[1],auto[0]>	467	1	–	Covered
bin <auto[0],auto[0],auto[0]>	196	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	32	1	–	Covered
bin <auto[1],auto[0],auto[1]>	141	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[0],auto[1],auto[0]>	509	1	–	Covered
bin <auto[1],auto[0],auto[0]>	49	1	–	Covered
bin <auto[0],auto[0],auto[0]>	155	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	113		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	32	1	–	Covered
bin <auto[1],auto[0],auto[1]>	4	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[0],auto[1],auto[0]>	542	1	–	Covered
bin <auto[1],auto[0],auto[0]>	186	1	–	Covered
bin <auto[0],auto[0],auto[0]>	194	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	41		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	86	1	–	Covered
bin <auto[1],auto[1],auto[0]>	152	1	–	Covered
bin <auto[0],auto[1],auto[1]>	88	1	–	Covered
bin <auto[0],auto[1],auto[0]>	483	1	–	Covered
bin <auto[1],auto[0],auto[0]>	171	1	–	Covered
bin <auto[0],auto[0],auto[0]>	167	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	58		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	218	1	–	Covered
bin <auto[0],auto[1],auto[1]>	76	1	–	Covered
bin <auto[0],auto[1],auto[0]>	495	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	49	1	–	Covered
bin <auto[1],auto[0],auto[1]>	106	1	–	Covered
bin <auto[1],auto[1],auto[0]>	189	1	–	Covered
bin <auto[0],auto[1],auto[0]>	571	1	–	Covered
bin <auto[1],auto[0],auto[0]>	84	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status

TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100	–	Uncovered
covered/total bins:	185	190	–	
missing/total bins:	5	190	–	
% Hit:	97.36%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	137	1	–	Covered
bin auto[1]	1068	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	190	1	–	Covered
bin auto[1024:2047]	9	1	–	Covered
bin auto[2048:3071]	9	1	–	Covered
bin auto[3072:4095]	12	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	12	1	–	Covered
bin auto[6144:7167]	10	1	–	Covered
bin auto[7168:8191]	11	1	–	Covered
bin auto[8192:9215]	12	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	15	1	–	Covered
bin auto[13312:14335]	12	1	–	Covered
bin auto[14336:15359]	17	1	–	Covered
bin auto[15360:16383]	9	1	–	Covered
bin auto[16384:17407]	13	1	–	Covered
bin auto[17408:18431]	14	1	–	Covered
bin auto[18432:19455]	20	1	–	Covered
bin auto[19456:20479]	21	1	–	Covered
bin auto[20480:21503]	7	1	–	Covered
bin auto[21504:22527]	18	1	–	Covered
bin auto[22528:23551]	18	1	–	Covered
bin auto[23552:24575]	13	1	–	Covered
bin auto[24576:25599]	10	1	–	Covered
bin auto[25600:26623]	17	1	–	Covered
bin auto[26624:27647]	17	1	–	Covered
bin auto[27648:28671]	12	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	11	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	12	1	–	Covered
bin auto[32768:33791]	11	1	–	Covered
bin auto[33792:34815]	14	1	–	Covered
bin auto[34816:35839]	13	1	–	Covered
bin auto[35840:36863]	13	1	–	Covered
bin auto[36864:37887]	13	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	19	1	–	Covered
bin auto[41984:43007]	9	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	7	1	–	Covered
bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	11	1	–	Covered
bin auto[48128:49151]	15	1	–	Covered
bin auto[49152:50175]	10	1	–	Covered
bin auto[50176:51199]	11	1	–	Covered
bin auto[51200:52223]	14	1	–	Covered
bin auto[52224:53247]	12	1	–	Covered
bin auto[53248:54271]	10	1	–	Covered
bin auto[54272:55295]	20	1	–	Covered
bin auto[55296:56319]	11	1	–	Covered
bin auto[56320:57343]	10	1	–	Covered
bin auto[57344:58367]	16	1	–	Covered
bin auto[58368:59391]	15	1	–	Covered
bin auto[59392:60415]	17	1	–	Covered
bin auto[60416:61439]	18	1	–	Covered
bin auto[61440:62463]	18	1	–	Covered
bin auto[62464:63487]	13	1	–	Covered
bin auto[63488:64511]	14	1	–	Covered
bin auto[64512:65535]	201	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	777	1	–	Covered
bin auto[1]	428	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	396	1	–	Covered
bin auto[1]	809	1	–	Covered

Coverpoint data_out_cp	92.18%	100	–	Uncovered
covered/total bins:	59	64	–	
missing/total bins:	5	64	–	
% Hit:	92.18%	100	–	
bin auto[0:1023]	687	1	–	Covered
bin auto[1024:2047]	1	1	–	Covered
bin auto[2048:3071]	5	1	–	Covered
bin auto[3072:4095]	4	1	–	Covered
bin auto[4096:5119]	15	1	–	Covered
bin auto[5120:6143]	9	1	–	Covered
bin auto[6144:7167]	2	1	–	Covered
bin auto[7168:8191]	4	1	–	Covered
bin auto[8192:9215]	3	1	–	Covered
bin auto[9216:10239]	3	1	–	Covered
bin auto[10240:11263]	30	1	–	Covered
bin auto[11264:12287]	9	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	8	1	–	Covered
bin auto[14336:15359]	6	1	–	Covered
bin auto[15360:16383]	0	1	–	ZERO
bin auto[16384:17407]	0	1	–	ZERO
bin auto[17408:18431]	1	1	–	Covered
bin auto[18432:19455]	7	1	–	Covered
bin auto[19456:20479]	14	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	5	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	0	1	–	ZERO
bin auto[24576:25599]	11	1	–	Covered
bin auto[25600:26623]	13	1	–	Covered
bin auto[26624:27647]	8	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	19	1	–	Covered
bin auto[29696:30719]	8	1	–	Covered
bin auto[30720:31743]	3	1	–	Covered
bin auto[31744:32767]	3	1	–	Covered
bin auto[32768:33791]	4	1	–	Covered
bin auto[33792:34815]	8	1	–	Covered
bin auto[34816:35839]	4	1	–	Covered
bin auto[35840:36863]	6	1	–	Covered
bin auto[36864:37887]	2	1	–	Covered
bin auto[37888:38911]	1	1	–	Covered
bin auto[38912:39935]	4	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	10	1	–	Covered
bin auto[41984:43007]	2	1	–	Covered
bin auto[43008:44031]	11	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	7	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	1	1	–	Covered
bin auto[49152:50175]	10	1	–	Covered
bin auto[50176:51199]	7	1	–	Covered
bin auto[51200:52223]	13	1	–	Covered
bin auto[52224:53247]	1	1	–	Covered
bin auto[53248:54271]	3	1	–	Covered
bin auto[54272:55295]	12	1	–	Covered
bin auto[55296:56319]	14	1	–	Covered
bin auto[56320:57343]	1	1	–	Covered
bin auto[57344:58367]	3	1	–	Covered
bin auto[58368:59391]	6	1	–	Covered
bin auto[59392:60415]	24	1	–	Covered
bin auto[60416:61439]	8	1	–	Covered
bin auto[61440:62463]	16	1	–	Covered
bin auto[62464:63487]	5	1	–	Covered
bin auto[63488:64511]	0	1	–	ZERO
bin auto[64512:65535]	108	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	575	1	–	Covered
bin auto[1]	630	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1109	1	–	Covered
bin auto[1]	96	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1091	1	–	Covered
bin auto[1]	114	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	919	1	–	Covered
bin auto[1]	286	1	–	Covered

Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1128	1	–	Covered
bin auto[1]	77	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	973	1	–	Covered
bin auto[1]	232	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1050	1	–	Covered
bin auto[1]	155	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	191	1	–	Covered
bin <auto[1],auto[1],auto[0]>	47	1	–	Covered
bin <auto[0],auto[1],auto[1]>	439	1	–	Covered
bin <auto[0],auto[1],auto[0]>	132	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	104	1	–	Covered
bin <auto[0],auto[0],auto[1]>	10	1	–	Covered
bin <auto[1],auto[1],auto[0]>	238	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[1],auto[0]>	467	1	–	Covered
bin <auto[0],auto[0],auto[0]>	196	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	32	1	–	Covered
bin <auto[1],auto[0],auto[1]>	141	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[0],auto[1],auto[0]>	509	1	–	Covered
bin <auto[1],auto[0],auto[0]>	49	1	–	Covered
bin <auto[0],auto[0],auto[0]>	155	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	113		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	32	1	–	Covered
bin <auto[1],auto[0],auto[1]>	4	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[0],auto[1],auto[0]>	542	1	–	Covered
bin <auto[1],auto[0],auto[0]>	186	1	–	Covered
bin <auto[0],auto[0],auto[0]>	194	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	41		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	86	1	–	Covered
bin <auto[1],auto[1],auto[0]>	152	1	–	Covered
bin <auto[0],auto[1],auto[1]>	88	1	–	Covered
bin <auto[0],auto[1],auto[0]>	483	1	–	Covered
bin <auto[1],auto[0],auto[0]>	171	1	–	Covered
bin <auto[0],auto[0],auto[0]>	167	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	58		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	218	1	–	Covered
bin <auto[0],auto[1],auto[1]>	76	1	–	Covered

bin <auto[0],auto[1],auto[0]>	495	1	–	Covered
bin <auto[1],auto[0],auto[0]>	190	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	49	1	–	Covered
bin <auto[1],auto[0],auto[1]>	106	1	–	Covered
bin <auto[1],auto[1],auto[0]>	189	1	–	Covered
bin <auto[0],auto[1],auto[0]>	571	1	–	Covered
bin <auto[1],auto[0],auto[0]>	84	1	–	Covered
bin <auto[0],auto[0],auto[0]>	206	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 99.58% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.58%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover__n_wr_a...	SVA	✓	Off	86	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__counte...	SVA	✓	Off	1068	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	1068	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	1068	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	6	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	34	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	203	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	69	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__full_fla...	SVA	✓	Off	99	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__empty...	SVA	✓	Off	255	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__underfl...	SVA	✓	Off	122	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__overflo...	SVA	✓	Off	62	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_a...	SVA	✓	Off	553	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__reset_...	SVA	✓	Off	137	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 1: SVA "Seed1"

3.2 Functional Coverage "seed2" Report

Coverage Report by instance with details

```
================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.50%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   190       184         6    96.84%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.50%	100	–	Uncovered
covered/total bins:	184	190	–	
missing/total bins:	6	190	–	
% Hit:	96.84%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	130	1	–	Covered
bin auto[1]	1075	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	195	1	–	Covered
bin auto[1024:2047]	15	1	–	Covered
bin auto[2048:3071]	17	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	12	1	–	Covered
bin auto[5120:6143]	13	1	–	Covered
bin auto[6144:7167]	8	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	15	1	–	Covered
bin auto[9216:10239]	13	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	16	1	–	Covered
bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	17	1	–	Covered
bin auto[14336:15359]	11	1	–	Covered
bin auto[15360:16383]	11	1	–	Covered
bin auto[16384:17407]	14	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered

bin auto[18432:19455]	12	1	–	Covered
bin auto[19456:20479]	12	1	–	Covered
bin auto[20480:21503]	11	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	16	1	–	Covered
bin auto[23552:24575]	17	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	11	1	–	Covered
bin auto[26624:27647]	7	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	16	1	–	Covered
bin auto[29696:30719]	12	1	–	Covered
bin auto[30720:31743]	15	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	19	1	–	Covered
bin auto[33792:34815]	11	1	–	Covered
bin auto[34816:35839]	15	1	–	Covered
bin auto[35840:36863]	12	1	–	Covered
bin auto[36864:37887]	14	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	16	1	–	Covered
bin auto[39936:40959]	10	1	–	Covered
bin auto[40960:41983]	17	1	–	Covered
bin auto[41984:43007]	15	1	–	Covered
bin auto[43008:44031]	18	1	–	Covered
bin auto[44032:45055]	10	1	–	Covered
bin auto[45056:46079]	8	1	–	Covered
bin auto[46080:47103]	8	1	–	Covered
bin auto[47104:48127]	10	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	12	1	–	Covered
bin auto[50176:51199]	17	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	13	1	–	Covered
bin auto[53248:54271]	12	1	–	Covered
bin auto[54272:55295]	15	1	–	Covered
bin auto[55296:56319]	15	1	–	Covered
bin auto[56320:57343]	13	1	–	Covered
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	8	1	–	Covered
bin auto[59392:60415]	10	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	17	1	–	Covered
bin auto[63488:64511]	16	1	–	Covered
bin auto[64512:65535]	174	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	816	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	401	1	–	Covered
bin auto[1]	804	1	–	Covered
Coverpoint data_out_cp	90.62%	100	–	Uncovered
covered/total bins:	58	64	–	
missing/total bins:	6	64	–	
% Hit:	90.62%	100	–	
bin auto[0:1023]	666	1	–	Covered
bin auto[1024:2047]	3	1	–	Covered
bin auto[2048:3071]	6	1	–	Covered
bin auto[3072:4095]	12	1	–	Covered
bin auto[4096:5119]	6	1	–	Covered
bin auto[5120:6143]	11	1	–	Covered
bin auto[6144:7167]	0	1	–	ZERO
bin auto[7168:8191]	6	1	–	Covered
bin auto[8192:9215]	10	1	–	Covered
bin auto[9216:10239]	6	1	–	Covered
bin auto[10240:11263]	3	1	–	Covered
bin auto[11264:12287]	12	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	5	1	–	Covered
bin auto[14336:15359]	3	1	–	Covered
bin auto[15360:16383]	5	1	–	Covered
bin auto[16384:17407]	1	1	–	Covered
bin auto[17408:18431]	4	1	–	Covered
bin auto[18432:19455]	13	1	–	Covered
bin auto[19456:20479]	2	1	–	Covered
bin auto[20480:21503]	27	1	–	Covered
bin auto[21504:22527]	10	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	7	1	–	Covered
bin auto[24576:25599]	5	1	–	Covered
bin auto[25600:26623]	2	1	–	Covered
bin auto[26624:27647]	0	1	–	ZERO
bin auto[27648:28671]	9	1	–	Covered
bin auto[28672:29695]	3	1	–	Covered
bin auto[29696:30719]	14	1	–	Covered

bin auto[30720:31743]	1	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	6	1	–	Covered
bin auto[34816:35839]	11	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	15	1	–	Covered
bin auto[37888:38911]	11	1	–	Covered
bin auto[38912:39935]	14	1	–	Covered
bin auto[39936:40959]	0	1	–	ZERO
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	7	1	–	Covered
bin auto[43008:44031]	1	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered
bin auto[46080:47103]	11	1	–	Covered
bin auto[47104:48127]	2	1	–	Covered
bin auto[48128:49151]	7	1	–	Covered
bin auto[49152:50175]	0	1	–	ZERO
bin auto[50176:51199]	10	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	8	1	–	Covered
bin auto[53248:54271]	4	1	–	Covered
bin auto[54272:55295]	8	1	–	Covered
bin auto[55296:56319]	16	1	–	Covered
bin auto[56320:57343]	14	1	–	Covered
bin auto[57344:58367]	4	1	–	Covered
bin auto[58368:59391]	6	1	–	Covered
bin auto[59392:60415]	25	1	–	Covered
bin auto[60416:61439]	0	1	–	ZERO
bin auto[61440:62463]	0	1	–	ZERO
bin auto[62464:63487]	12	1	–	Covered
bin auto[63488:64511]	5	1	–	Covered
bin auto[64512:65535]	78	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	593	1	–	Covered
bin auto[1]	612	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1067	1	–	Covered
bin auto[1]	138	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1045	1	–	Covered
bin auto[1]	160	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	932	1	–	Covered
bin auto[1]	273	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1105	1	–	Covered
bin auto[1]	100	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1023	1	–	Covered
bin auto[1]	182	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1068	1	–	Covered
bin auto[1]	137	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	161	1	–	Covered
bin <auto[1],auto[1],auto[0]>	45	1	–	Covered
bin <auto[0],auto[1],auto[1]>	451	1	–	Covered
bin <auto[0],auto[1],auto[0]>	147	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	

% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	140	1	–	Covered
bin <auto[0],auto[0],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[1],auto[0]>	458	1	–	Covered
bin <auto[0],auto[0],auto[0]>	198	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[0],auto[1]>	134	1	–	Covered
bin <auto[1],auto[1],auto[0]>	186	1	–	Covered
bin <auto[0],auto[1],auto[0]>	541	1	–	Covered
bin <auto[1],auto[0],auto[0]>	49	1	–	Covered
bin <auto[0],auto[0],auto[0]>	156	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	119		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	40	1	–	Covered
bin <auto[1],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	166	1	–	Covered
bin <auto[0],auto[1],auto[0]>	563	1	–	Covered
bin <auto[1],auto[0],auto[0]>	175	1	–	Covered
bin <auto[0],auto[0],auto[0]>	201	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	52		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	60	1	–	Covered
bin <auto[1],auto[1],auto[0]>	146	1	–	Covered
bin <auto[0],auto[1],auto[1]>	75	1	–	Covered
bin <auto[0],auto[1],auto[0]>	523	1	–	Covered
bin <auto[1],auto[0],auto[0]>	170	1	–	Covered
bin <auto[0],auto[0],auto[0]>	184	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	47		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	30	1	–	Covered
bin <auto[1],auto[1],auto[0]>	176	1	–	Covered
bin <auto[0],auto[1],auto[1]>	108	1	–	Covered
bin <auto[0],auto[1],auto[0]>	490	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	39	1	–	Covered
bin <auto[1],auto[0],auto[1]>	98	1	–	Covered
bin <auto[1],auto[1],auto[0]>	167	1	–	Covered
bin <auto[0],auto[1],auto[0]>	598	1	–	Covered
bin <auto[1],auto[0],auto[0]>	85	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.50%	100	–	Uncovered
covered/total bins:	184	190	–	
missing/total bins:	6	190	–	
% Hit:	96.84%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	130	1	–	Covered
bin auto[1]	1075	1	–	Covered

Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	195	1	–	Covered
bin auto[1024:2047]	15	1	–	Covered
bin auto[2048:3071]	17	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	12	1	–	Covered
bin auto[5120:6143]	13	1	–	Covered
bin auto[6144:7167]	8	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	15	1	–	Covered
bin auto[9216:10239]	13	1	–	Covered
bin auto[10240:11263]	16	1	–	Covered
bin auto[11264:12287]	16	1	–	Covered
bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	17	1	–	Covered
bin auto[14336:15359]	11	1	–	Covered
bin auto[15360:16383]	11	1	–	Covered
bin auto[16384:17407]	14	1	–	Covered
bin auto[17408:18431]	15	1	–	Covered
bin auto[18432:19455]	12	1	–	Covered
bin auto[19456:20479]	12	1	–	Covered
bin auto[20480:21503]	11	1	–	Covered
bin auto[21504:22527]	13	1	–	Covered
bin auto[22528:23551]	16	1	–	Covered
bin auto[23552:24575]	17	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	11	1	–	Covered
bin auto[26624:27647]	7	1	–	Covered
bin auto[27648:28671]	11	1	–	Covered
bin auto[28672:29695]	16	1	–	Covered
bin auto[29696:30719]	12	1	–	Covered
bin auto[30720:31743]	15	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	19	1	–	Covered
bin auto[33792:34815]	11	1	–	Covered
bin auto[34816:35839]	15	1	–	Covered
bin auto[35840:36863]	12	1	–	Covered
bin auto[36864:37887]	14	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	16	1	–	Covered
bin auto[39936:40959]	10	1	–	Covered
bin auto[40960:41983]	17	1	–	Covered
bin auto[41984:43007]	15	1	–	Covered
bin auto[43008:44031]	18	1	–	Covered
bin auto[44032:45055]	10	1	–	Covered
bin auto[45056:46079]	8	1	–	Covered
bin auto[46080:47103]	8	1	–	Covered
bin auto[47104:48127]	10	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	12	1	–	Covered
bin auto[50176:51199]	17	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	13	1	–	Covered
bin auto[53248:54271]	12	1	–	Covered
bin auto[54272:55295]	15	1	–	Covered
bin auto[55296:56319]	15	1	–	Covered
bin auto[56320:57343]	13	1	–	Covered
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	8	1	–	Covered
bin auto[59392:60415]	10	1	–	Covered
bin auto[60416:61439]	11	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	17	1	–	Covered
bin auto[63488:64511]	16	1	–	Covered
bin auto[64512:65535]	174	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	816	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	401	1	–	Covered
bin auto[1]	804	1	–	Covered
Coverpoint data_out_cp	90.62%	100	–	Uncovered
covered/total bins:	58	64	–	
missing/total bins:	6	64	–	
% Hit:	90.62%	100	–	
bin auto[0:1023]	666	1	–	Covered
bin auto[1024:2047]	3	1	–	Covered
bin auto[2048:3071]	6	1	–	Covered
bin auto[3072:4095]	12	1	–	Covered
bin auto[4096:5119]	6	1	–	Covered
bin auto[5120:6143]	11	1	–	Covered
bin auto[6144:7167]	0	1	–	ZERO
bin auto[7168:8191]	6	1	–	Covered

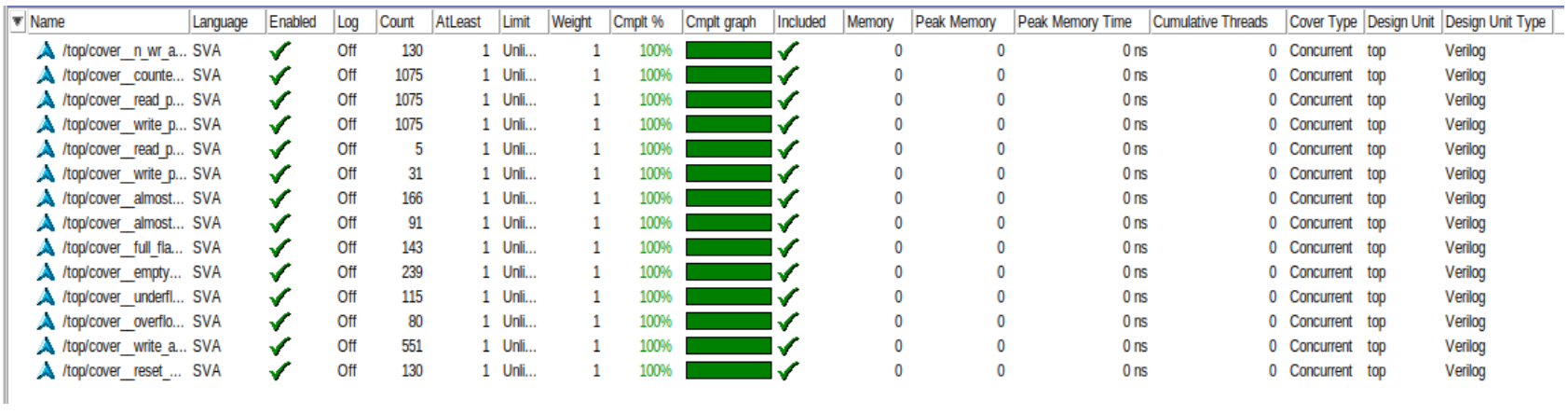
bin auto[8192:9215]	10	1	–	Covered
bin auto[9216:10239]	6	1	–	Covered
bin auto[10240:11263]	3	1	–	Covered
bin auto[11264:12287]	12	1	–	Covered
bin auto[12288:13311]	7	1	–	Covered
bin auto[13312:14335]	5	1	–	Covered
bin auto[14336:15359]	3	1	–	Covered
bin auto[15360:16383]	5	1	–	Covered
bin auto[16384:17407]	1	1	–	Covered
bin auto[17408:18431]	4	1	–	Covered
bin auto[18432:19455]	13	1	–	Covered
bin auto[19456:20479]	2	1	–	Covered
bin auto[20480:21503]	27	1	–	Covered
bin auto[21504:22527]	10	1	–	Covered
bin auto[22528:23551]	1	1	–	Covered
bin auto[23552:24575]	7	1	–	Covered
bin auto[24576:25599]	5	1	–	Covered
bin auto[25600:26623]	2	1	–	Covered
bin auto[26624:27647]	0	1	–	ZERO
bin auto[27648:28671]	9	1	–	Covered
bin auto[28672:29695]	3	1	–	Covered
bin auto[29696:30719]	14	1	–	Covered
bin auto[30720:31743]	1	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	8	1	–	Covered
bin auto[33792:34815]	6	1	–	Covered
bin auto[34816:35839]	11	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	15	1	–	Covered
bin auto[37888:38911]	11	1	–	Covered
bin auto[38912:39935]	14	1	–	Covered
bin auto[39936:40959]	0	1	–	ZERO
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	7	1	–	Covered
bin auto[43008:44031]	1	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered
bin auto[46080:47103]	11	1	–	Covered
bin auto[47104:48127]	2	1	–	Covered
bin auto[48128:49151]	7	1	–	Covered
bin auto[49152:50175]	0	1	–	ZERO
bin auto[50176:51199]	10	1	–	Covered
bin auto[51200:52223]	20	1	–	Covered
bin auto[52224:53247]	8	1	–	Covered
bin auto[53248:54271]	4	1	–	Covered
bin auto[54272:55295]	8	1	–	Covered
bin auto[55296:56319]	16	1	–	Covered
bin auto[56320:57343]	14	1	–	Covered
bin auto[57344:58367]	4	1	–	Covered
bin auto[58368:59391]	6	1	–	Covered
bin auto[59392:60415]	25	1	–	Covered
bin auto[60416:61439]	0	1	–	ZERO
bin auto[61440:62463]	0	1	–	ZERO
bin auto[62464:63487]	12	1	–	Covered
bin auto[63488:64511]	5	1	–	Covered
bin auto[64512:65535]	78	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	593	1	–	Covered
bin auto[1]	612	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1067	1	–	Covered
bin auto[1]	138	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1045	1	–	Covered
bin auto[1]	160	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	932	1	–	Covered
bin auto[1]	273	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1105	1	–	Covered
bin auto[1]	100	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1023	1	–	Covered
bin auto[1]	182	1	–	Covered

Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1068	1	–	Covered
bin auto[1]	137	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	161	1	–	Covered
bin <auto[1],auto[1],auto[0]>	45	1	–	Covered
bin <auto[0],auto[1],auto[1]>	451	1	–	Covered
bin <auto[0],auto[1],auto[0]>	147	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	140	1	–	Covered
bin <auto[0],auto[0],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[1],auto[0]>	458	1	–	Covered
bin <auto[0],auto[0],auto[0]>	198	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[0],auto[1]>	134	1	–	Covered
bin <auto[1],auto[1],auto[0]>	186	1	–	Covered
bin <auto[0],auto[1],auto[0]>	541	1	–	Covered
bin <auto[1],auto[0],auto[0]>	49	1	–	Covered
bin <auto[0],auto[0],auto[0]>	156	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	119		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	40	1	–	Covered
bin <auto[1],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	166	1	–	Covered
bin <auto[0],auto[1],auto[0]>	563	1	–	Covered
bin <auto[1],auto[0],auto[0]>	175	1	–	Covered
bin <auto[0],auto[0],auto[0]>	201	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	52		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	60	1	–	Covered
bin <auto[1],auto[1],auto[0]>	146	1	–	Covered
bin <auto[0],auto[1],auto[1]>	75	1	–	Covered
bin <auto[0],auto[1],auto[0]>	523	1	–	Covered
bin <auto[1],auto[0],auto[0]>	170	1	–	Covered
bin <auto[0],auto[0],auto[0]>	184	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	47		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	30	1	–	Covered
bin <auto[1],auto[1],auto[0]>	176	1	–	Covered
bin <auto[0],auto[1],auto[1]>	108	1	–	Covered
bin <auto[0],auto[1],auto[0]>	490	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	39	1	–	Covered
bin <auto[1],auto[0],auto[1]>	98	1	–	Covered

bin <auto[1],auto[1],auto[0]>	167	1	–	Covered
bin <auto[0],auto[1],auto[0]>	598	1	–	Covered
bin <auto[1],auto[0],auto[0]>	85	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 99.50% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.50%



Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover__n_wr_a...	SVA	✓	Off	130	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__counte...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	5	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	31	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	166	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	91	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__full_fla...	SVA	✓	Off	143	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__empty...	SVA	✓	Off	239	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__underfl...	SVA	✓	Off	115	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__overflo...	SVA	✓	Off	80	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_a...	SVA	✓	Off	551	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__reset_...	SVA	✓	Off	130	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 2: SVA "Seed2"

3.3 Functional Coverage "seed3" Report

Coverage Report by instance with details

```
=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.42%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   190       183         7    96.31%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.42%	100	–	Uncovered
covered/total bins:	183	190	–	
missing/total bins:	7	190	–	
% Hit:	96.31%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	123	1	–	Covered
bin auto[1]	1082	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	205	1	–	Covered
bin auto[1024:2047]	9	1	–	Covered
bin auto[2048:3071]	14	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	15	1	–	Covered
bin auto[5120:6143]	16	1	–	Covered
bin auto[6144:7167]	17	1	–	Covered
bin auto[7168:8191]	14	1	–	Covered
bin auto[8192:9215]	9	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	4	1	–	Covered
bin auto[11264:12287]	8	1	–	Covered
bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	14	1	–	Covered
bin auto[14336:15359]	7	1	–	Covered
bin auto[15360:16383]	8	1	–	Covered
bin auto[16384:17407]	15	1	–	Covered
bin auto[17408:18431]	12	1	–	Covered
bin auto[18432:19455]	11	1	–	Covered
bin auto[19456:20479]	11	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	9	1	–	Covered
bin auto[22528:23551]	18	1	–	Covered
bin auto[23552:24575]	14	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	14	1	–	Covered
bin auto[27648:28671]	14	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	11	1	–	Covered
bin auto[30720:31743]	14	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	13	1	–	Covered

bin auto[33792:34815]	10	1	–	Covered
bin auto[34816:35839]	10	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	7	1	–	Covered
bin auto[37888:38911]	22	1	–	Covered
bin auto[38912:39935]	12	1	–	Covered
bin auto[39936:40959]	16	1	–	Covered
bin auto[40960:41983]	7	1	–	Covered
bin auto[41984:43007]	12	1	–	Covered
bin auto[43008:44031]	11	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	20	1	–	Covered
bin auto[46080:47103]	14	1	–	Covered
bin auto[47104:48127]	13	1	–	Covered
bin auto[48128:49151]	14	1	–	Covered
bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	12	1	–	Covered
bin auto[51200:52223]	15	1	–	Covered
bin auto[52224:53247]	11	1	–	Covered
bin auto[53248:54271]	12	1	–	Covered
bin auto[54272:55295]	15	1	–	Covered
bin auto[55296:56319]	17	1	–	Covered
bin auto[56320:57343]	13	1	–	Covered
bin auto[57344:58367]	5	1	–	Covered
bin auto[58368:59391]	12	1	–	Covered
bin auto[59392:60415]	17	1	–	Covered
bin auto[60416:61439]	16	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	19	1	–	Covered
bin auto[63488:64511]	8	1	–	Covered
bin auto[64512:65535]	212	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	787	1	–	Covered
bin auto[1]	418	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	411	1	–	Covered
bin auto[1]	794	1	–	Covered
Coverpoint data_out_cp	89.06%	100	–	Uncovered
covered/total bins:	57	64	–	
missing/total bins:	7	64	–	
% Hit:	89.06%	100	–	
bin auto[0:1023]	656	1	–	Covered
bin auto[1024:2047]	10	1	–	Covered
bin auto[2048:3071]	2	1	–	Covered
bin auto[3072:4095]	18	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	5	1	–	Covered
bin auto[7168:8191]	7	1	–	Covered
bin auto[8192:9215]	10	1	–	Covered
bin auto[9216:10239]	6	1	–	Covered
bin auto[10240:11263]	0	1	–	ZERO
bin auto[11264:12287]	1	1	–	Covered
bin auto[12288:13311]	2	1	–	Covered
bin auto[13312:14335]	4	1	–	Covered
bin auto[14336:15359]	0	1	–	ZERO
bin auto[15360:16383]	13	1	–	Covered
bin auto[16384:17407]	8	1	–	Covered
bin auto[17408:18431]	9	1	–	Covered
bin auto[18432:19455]	2	1	–	Covered
bin auto[19456:20479]	8	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	0	1	–	ZERO
bin auto[22528:23551]	2	1	–	Covered
bin auto[23552:24575]	8	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	0	1	–	ZERO
bin auto[26624:27647]	5	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	12	1	–	Covered
bin auto[29696:30719]	2	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	1	1	–	Covered
bin auto[32768:33791]	5	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	0	1	–	ZERO
bin auto[35840:36863]	5	1	–	Covered
bin auto[36864:37887]	3	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	4	1	–	Covered
bin auto[39936:40959]	13	1	–	Covered
bin auto[40960:41983]	8	1	–	Covered
bin auto[41984:43007]	2	1	–	Covered
bin auto[43008:44031]	3	1	–	Covered
bin auto[44032:45055]	11	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered

bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	9	1	–	Covered
bin auto[48128:49151]	8	1	–	Covered
bin auto[49152:50175]	9	1	–	Covered
bin auto[50176:51199]	1	1	–	Covered
bin auto[51200:52223]	8	1	–	Covered
bin auto[52224:53247]	0	1	–	ZERO
bin auto[53248:54271]	11	1	–	Covered
bin auto[54272:55295]	17	1	–	Covered
bin auto[55296:56319]	6	1	–	Covered
bin auto[56320:57343]	4	1	–	Covered
bin auto[57344:58367]	0	1	–	ZERO
bin auto[58368:59391]	11	1	–	Covered
bin auto[59392:60415]	12	1	–	Covered
bin auto[60416:61439]	4	1	–	Covered
bin auto[61440:62463]	12	1	–	Covered
bin auto[62464:63487]	10	1	–	Covered
bin auto[63488:64511]	3	1	–	Covered
bin auto[64512:65535]	128	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	581	1	–	Covered
bin auto[1]	624	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1110	1	–	Covered
bin auto[1]	95	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1084	1	–	Covered
bin auto[1]	121	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	925	1	–	Covered
bin auto[1]	280	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1110	1	–	Covered
bin auto[1]	95	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1025	1	–	Covered
bin auto[1]	180	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1060	1	–	Covered
bin auto[1]	145	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	181	1	–	Covered
bin <auto[1],auto[1],auto[0]>	44	1	–	Covered
bin <auto[0],auto[1],auto[1]>	443	1	–	Covered
bin <auto[0],auto[1],auto[0]>	126	1	–	Covered
bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	106	1	–	Covered
bin <auto[0],auto[0],auto[1]>	15	1	–	Covered
bin <auto[1],auto[1],auto[0]>	225	1	–	Covered
bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	203	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	

Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	29	1	–	Covered
bin <auto[1],auto[0],auto[1]>	134	1	–	Covered
bin <auto[1],auto[1],auto[0]>	196	1	–	Covered
bin <auto[0],auto[1],auto[0]>	512	1	–	Covered
bin <auto[1],auto[0],auto[0]>	59	1	–	Covered
bin <auto[0],auto[0],auto[0]>	158	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	117		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	33	1	–	Covered
bin <auto[1],auto[0],auto[1]>	10	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[0],auto[1],auto[0]>	535	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	200	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	52		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	67	1	–	Covered
bin <auto[1],auto[1],auto[0]>	158	1	–	Covered
bin <auto[0],auto[1],auto[1]>	80	1	–	Covered
bin <auto[0],auto[1],auto[0]>	489	1	–	Covered
bin <auto[1],auto[0],auto[0]>	185	1	–	Covered
bin <auto[0],auto[0],auto[0]>	193	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	33		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	205	1	–	Covered
bin <auto[0],auto[1],auto[1]>	75	1	–	Covered
bin <auto[0],auto[1],auto[0]>	494	1	–	Covered
bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	42	1	–	Covered
bin <auto[1],auto[0],auto[1]>	103	1	–	Covered
bin <auto[1],auto[1],auto[0]>	183	1	–	Covered
bin <auto[0],auto[1],auto[0]>	569	1	–	Covered
bin <auto[1],auto[0],auto[0]>	90	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.42%	100	–	Uncovered
covered/total bins:	183	190	–	
missing/total bins:	7	190	–	
% Hit:	96.31%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	123	1	–	Covered
bin auto[1]	1082	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	205	1	–	Covered
bin auto[1024:2047]	9	1	–	Covered
bin auto[2048:3071]	14	1	–	Covered
bin auto[3072:4095]	15	1	–	Covered
bin auto[4096:5119]	15	1	–	Covered
bin auto[5120:6143]	16	1	–	Covered
bin auto[6144:7167]	17	1	–	Covered
bin auto[7168:8191]	14	1	–	Covered
bin auto[8192:9215]	9	1	–	Covered
bin auto[9216:10239]	12	1	–	Covered
bin auto[10240:11263]	4	1	–	Covered

bin auto[11264:12287]	8	1	–	Covered
bin auto[12288:13311]	13	1	–	Covered
bin auto[13312:14335]	14	1	–	Covered
bin auto[14336:15359]	7	1	–	Covered
bin auto[15360:16383]	8	1	–	Covered
bin auto[16384:17407]	15	1	–	Covered
bin auto[17408:18431]	12	1	–	Covered
bin auto[18432:19455]	11	1	–	Covered
bin auto[19456:20479]	11	1	–	Covered
bin auto[20480:21503]	17	1	–	Covered
bin auto[21504:22527]	9	1	–	Covered
bin auto[22528:23551]	18	1	–	Covered
bin auto[23552:24575]	14	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	14	1	–	Covered
bin auto[27648:28671]	14	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	11	1	–	Covered
bin auto[30720:31743]	14	1	–	Covered
bin auto[31744:32767]	14	1	–	Covered
bin auto[32768:33791]	13	1	–	Covered
bin auto[33792:34815]	10	1	–	Covered
bin auto[34816:35839]	10	1	–	Covered
bin auto[35840:36863]	11	1	–	Covered
bin auto[36864:37887]	7	1	–	Covered
bin auto[37888:38911]	22	1	–	Covered
bin auto[38912:39935]	12	1	–	Covered
bin auto[39936:40959]	16	1	–	Covered
bin auto[40960:41983]	7	1	–	Covered
bin auto[41984:43007]	12	1	–	Covered
bin auto[43008:44031]	11	1	–	Covered
bin auto[44032:45055]	13	1	–	Covered
bin auto[45056:46079]	20	1	–	Covered
bin auto[46080:47103]	14	1	–	Covered
bin auto[47104:48127]	13	1	–	Covered
bin auto[48128:49151]	14	1	–	Covered
bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	12	1	–	Covered
bin auto[51200:52223]	15	1	–	Covered
bin auto[52224:53247]	11	1	–	Covered
bin auto[53248:54271]	12	1	–	Covered
bin auto[54272:55295]	15	1	–	Covered
bin auto[55296:56319]	17	1	–	Covered
bin auto[56320:57343]	13	1	–	Covered
bin auto[57344:58367]	5	1	–	Covered
bin auto[58368:59391]	12	1	–	Covered
bin auto[59392:60415]	17	1	–	Covered
bin auto[60416:61439]	16	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	19	1	–	Covered
bin auto[63488:64511]	8	1	–	Covered
bin auto[64512:65535]	212	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	787	1	–	Covered
bin auto[1]	418	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	411	1	–	Covered
bin auto[1]	794	1	–	Covered
Coverpoint data_out_cp	89.06%	100	–	Uncovered
covered/total bins:	57	64	–	
missing/total bins:	7	64	–	
% Hit:	89.06%	100	–	
bin auto[0:1023]	656	1	–	Covered
bin auto[1024:2047]	10	1	–	Covered
bin auto[2048:3071]	2	1	–	Covered
bin auto[3072:4095]	18	1	–	Covered
bin auto[4096:5119]	13	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	5	1	–	Covered
bin auto[7168:8191]	7	1	–	Covered
bin auto[8192:9215]	10	1	–	Covered
bin auto[9216:10239]	6	1	–	Covered
bin auto[10240:11263]	0	1	–	ZERO
bin auto[11264:12287]	1	1	–	Covered
bin auto[12288:13311]	2	1	–	Covered
bin auto[13312:14335]	4	1	–	Covered
bin auto[14336:15359]	0	1	–	ZERO
bin auto[15360:16383]	13	1	–	Covered
bin auto[16384:17407]	8	1	–	Covered
bin auto[17408:18431]	9	1	–	Covered
bin auto[18432:19455]	2	1	–	Covered
bin auto[19456:20479]	8	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	0	1	–	ZERO
bin auto[22528:23551]	2	1	–	Covered

bin auto[23552:24575]	8	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	0	1	–	ZERO
bin auto[26624:27647]	5	1	–	Covered
bin auto[27648:28671]	6	1	–	Covered
bin auto[28672:29695]	12	1	–	Covered
bin auto[29696:30719]	2	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	1	1	–	Covered
bin auto[32768:33791]	5	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	0	1	–	ZERO
bin auto[35840:36863]	5	1	–	Covered
bin auto[36864:37887]	3	1	–	Covered
bin auto[37888:38911]	12	1	–	Covered
bin auto[38912:39935]	4	1	–	Covered
bin auto[39936:40959]	13	1	–	Covered
bin auto[40960:41983]	8	1	–	Covered
bin auto[41984:43007]	2	1	–	Covered
bin auto[43008:44031]	3	1	–	Covered
bin auto[44032:45055]	11	1	–	Covered
bin auto[45056:46079]	9	1	–	Covered
bin auto[46080:47103]	13	1	–	Covered
bin auto[47104:48127]	9	1	–	Covered
bin auto[48128:49151]	8	1	–	Covered
bin auto[49152:50175]	9	1	–	Covered
bin auto[50176:51199]	1	1	–	Covered
bin auto[51200:52223]	8	1	–	Covered
bin auto[52224:53247]	0	1	–	ZERO
bin auto[53248:54271]	11	1	–	Covered
bin auto[54272:55295]	17	1	–	Covered
bin auto[55296:56319]	6	1	–	Covered
bin auto[56320:57343]	4	1	–	Covered
bin auto[57344:58367]	0	1	–	ZERO
bin auto[58368:59391]	11	1	–	Covered
bin auto[59392:60415]	12	1	–	Covered
bin auto[60416:61439]	4	1	–	Covered
bin auto[61440:62463]	12	1	–	Covered
bin auto[62464:63487]	10	1	–	Covered
bin auto[63488:64511]	3	1	–	Covered
bin auto[64512:65535]	128	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	581	1	–	Covered
bin auto[1]	624	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1110	1	–	Covered
bin auto[1]	95	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1084	1	–	Covered
bin auto[1]	121	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	925	1	–	Covered
bin auto[1]	280	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1110	1	–	Covered
bin auto[1]	95	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1025	1	–	Covered
bin auto[1]	180	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1060	1	–	Covered
bin auto[1]	145	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	181	1	–	Covered
bin <auto[1],auto[1],auto[0]>	44	1	–	Covered
bin <auto[0],auto[1],auto[1]>	443	1	–	Covered
bin <auto[0],auto[1],auto[0]>	126	1	–	Covered

bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	106	1	–	Covered
bin <auto[0],auto[0],auto[1]>	15	1	–	Covered
bin <auto[1],auto[1],auto[0]>	225	1	–	Covered
bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[1],auto[0]>	463	1	–	Covered
bin <auto[0],auto[0],auto[0]>	203	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	29	1	–	Covered
bin <auto[1],auto[0],auto[1]>	134	1	–	Covered
bin <auto[1],auto[1],auto[0]>	196	1	–	Covered
bin <auto[0],auto[1],auto[0]>	512	1	–	Covered
bin <auto[1],auto[0],auto[0]>	59	1	–	Covered
bin <auto[0],auto[0],auto[0]>	158	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	117		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	33	1	–	Covered
bin <auto[1],auto[0],auto[1]>	10	1	–	Covered
bin <auto[1],auto[1],auto[0]>	192	1	–	Covered
bin <auto[0],auto[1],auto[0]>	535	1	–	Covered
bin <auto[1],auto[0],auto[0]>	183	1	–	Covered
bin <auto[0],auto[0],auto[0]>	200	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	52		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	67	1	–	Covered
bin <auto[1],auto[1],auto[0]>	158	1	–	Covered
bin <auto[0],auto[1],auto[1]>	80	1	–	Covered
bin <auto[0],auto[1],auto[0]>	489	1	–	Covered
bin <auto[1],auto[0],auto[0]>	185	1	–	Covered
bin <auto[0],auto[0],auto[0]>	193	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	33		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[1],auto[0]>	205	1	–	Covered
bin <auto[0],auto[1],auto[1]>	75	1	–	Covered
bin <auto[0],auto[1],auto[0]>	494	1	–	Covered
bin <auto[1],auto[0],auto[0]>	193	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	42	1	–	Covered
bin <auto[1],auto[0],auto[1]>	103	1	–	Covered
bin <auto[1],auto[1],auto[0]>	183	1	–	Covered
bin <auto[0],auto[1],auto[0]>	569	1	–	Covered
bin <auto[1],auto[0],auto[0]>	90	1	–	Covered
bin <auto[0],auto[0],auto[0]>	218	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 99.42% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.42%

3.4 Functional Coverage "seed4" Report

Coverage Report by instance with details

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover__n_wr_a...	SVA	✓	Off	96	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__counte...	SVA	✓	Off	1082	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	1082	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	1082	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	3	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	34	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	170	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	84	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__full_fla...	SVA	✓	Off	109	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__empty...	SVA	✓	Off	249	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__underfl...	SVA	✓	Off	119	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__overflo...	SVA	✓	Off	63	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_a...	SVA	✓	Off	571	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__reset_...	SVA	✓	Off	123	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 3: SVA "Seed3"

```
=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.58%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   190       185         5    97.36%

---------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status
---------------------------------------------------------------------------------
 TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg      99.58%        100          -    Uncovered
 covered/total bins:                                  185        190          -
 missing/total bins:                                    5        190          -
 % Hit:                                            97.36%        100          -
 Coverpoint rst_n_cp                               100.00%        100          -    Covered
     covered/total bins:                                 2          2          -
     missing/total bins:                                 0          2          -
     % Hit:                                        100.00%        100          -
     bin auto[0]                                       130          1          -    Covered
     bin auto[1]                                      1075          1          -    Covered
 Coverpoint data_in_cp                             100.00%        100          -    Covered
     covered/total bins:                                64         64          -
     missing/total bins:                                 0         64          -
     % Hit:                                        100.00%        100          -
     bin auto[0:1023]                                  186          1          -    Covered
     bin auto[1024:2047]                                14          1          -    Covered
     bin auto[2048:3071]                                15          1          -    Covered
     bin auto[3072:4095]                                12          1          -    Covered
     bin auto[4096:5119]                                17          1          -    Covered
     bin auto[5120:6143]                                20          1          -    Covered
     bin auto[6144:7167]                                16          1          -    Covered
     bin auto[7168:8191]                                14          1          -    Covered
     bin auto[8192:9215]                                17          1          -    Covered
     bin auto[9216:10239]                               11          1          -    Covered
     bin auto[10240:11263]                              15          1          -    Covered
     bin auto[11264:12287]                              13          1          -    Covered
     bin auto[12288:13311]                              14          1          -    Covered
     bin auto[13312:14335]                               8          1          -    Covered
     bin auto[14336:15359]                              19          1          -    Covered
     bin auto[15360:16383]                              14          1          -    Covered
     bin auto[16384:17407]                              10          1          -    Covered
     bin auto[17408:18431]                              10          1          -    Covered
     bin auto[18432:19455]                              17          1          -    Covered
     bin auto[19456:20479]                               7          1          -    Covered
     bin auto[20480:21503]                               8          1          -    Covered
     bin auto[21504:22527]                               9          1          -    Covered
     bin auto[22528:23551]                              12          1          -    Covered
     bin auto[23552:24575]                              10          1          -    Covered
     bin auto[24576:25599]                              11          1          -    Covered
     bin auto[25600:26623]                              18          1          -    Covered
     bin auto[26624:27647]                              12          1          -    Covered
     bin auto[27648:28671]                              14          1          -    Covered
     bin auto[28672:29695]                              16          1          -    Covered
     bin auto[29696:30719]                              19          1          -    Covered
     bin auto[30720:31743]                               7          1          -    Covered
     bin auto[31744:32767]                              12          1          -    Covered
     bin auto[32768:33791]                              25          1          -    Covered
     bin auto[33792:34815]                              14          1          -    Covered
     bin auto[34816:35839]                              15          1          -    Covered
     bin auto[35840:36863]                              19          1          -    Covered
     bin auto[36864:37887]                              21          1          -    Covered
     bin auto[37888:38911]                              10          1          -    Covered
     bin auto[38912:39935]                              16          1          -    Covered
     bin auto[39936:40959]                              11          1          -    Covered
     bin auto[40960:41983]                              14          1          -    Covered
     bin auto[41984:43007]                              12          1          -    Covered
     bin auto[43008:44031]                              12          1          -    Covered
     bin auto[44032:45055]                              18          1          -    Covered
     bin auto[45056:46079]                              12          1          -    Covered
     bin auto[46080:47103]                              10          1          -    Covered
     bin auto[47104:48127]                               9          1          -    Covered
     bin auto[48128:49151]                              17          1          -    Covered
```

bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	11	1	–	Covered
bin auto[51200:52223]	10	1	–	Covered
bin auto[52224:53247]	16	1	–	Covered
bin auto[53248:54271]	8	1	–	Covered
bin auto[54272:55295]	22	1	–	Covered
bin auto[55296:56319]	12	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	15	1	–	Covered
bin auto[58368:59391]	17	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	12	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	14	1	–	Covered
bin auto[63488:64511]	11	1	–	Covered
bin auto[64512:65535]	166	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	795	1	–	Covered
bin auto[1]	410	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	395	1	–	Covered
bin auto[1]	810	1	–	Covered
Coverpoint data_out_cp	92.18%	100	–	Uncovered
covered/total bins:	59	64	–	
missing/total bins:	5	64	–	
% Hit:	92.18%	100	–	
bin auto[0:1023]	640	1	–	Covered
bin auto[1024:2047]	20	1	–	Covered
bin auto[2048:3071]	0	1	–	ZERO
bin auto[3072:4095]	5	1	–	Covered
bin auto[4096:5119]	5	1	–	Covered
bin auto[5120:6143]	7	1	–	Covered
bin auto[6144:7167]	18	1	–	Covered
bin auto[7168:8191]	13	1	–	Covered
bin auto[8192:9215]	14	1	–	Covered
bin auto[9216:10239]	4	1	–	Covered
bin auto[10240:11263]	10	1	–	Covered
bin auto[11264:12287]	15	1	–	Covered
bin auto[12288:13311]	17	1	–	Covered
bin auto[13312:14335]	12	1	–	Covered
bin auto[14336:15359]	11	1	–	Covered
bin auto[15360:16383]	3	1	–	Covered
bin auto[16384:17407]	1	1	–	Covered
bin auto[17408:18431]	4	1	–	Covered
bin auto[18432:19455]	21	1	–	Covered
bin auto[19456:20479]	0	1	–	ZERO
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	4	1	–	Covered
bin auto[24576:25599]	4	1	–	Covered
bin auto[25600:26623]	6	1	–	Covered
bin auto[26624:27647]	5	1	–	Covered
bin auto[27648:28671]	13	1	–	Covered
bin auto[28672:29695]	1	1	–	Covered
bin auto[29696:30719]	1	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	5	1	–	Covered
bin auto[32768:33791]	22	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	7	1	–	Covered
bin auto[35840:36863]	14	1	–	Covered
bin auto[36864:37887]	6	1	–	Covered
bin auto[37888:38911]	3	1	–	Covered
bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	5	1	–	Covered
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	11	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	9	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	14	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	16	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	4	1	–	Covered
bin auto[51200:52223]	16	1	–	Covered
bin auto[52224:53247]	7	1	–	Covered
bin auto[53248:54271]	0	1	–	ZERO
bin auto[54272:55295]	9	1	–	Covered
bin auto[55296:56319]	3	1	–	Covered
bin auto[56320:57343]	0	1	–	ZERO
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	11	1	–	Covered
bin auto[59392:60415]	11	1	–	Covered
bin auto[60416:61439]	7	1	–	Covered

bin auto[61440:62463]	6	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	9	1	–	Covered
bin auto[64512:65535]	68	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	582	1	–	Covered
bin auto[1]	623	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1099	1	–	Covered
bin auto[1]	106	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1071	1	–	Covered
bin auto[1]	134	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	934	1	–	Covered
bin auto[1]	271	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1114	1	–	Covered
bin auto[1]	91	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1002	1	–	Covered
bin auto[1]	203	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1070	1	–	Covered
bin auto[1]	135	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	188	1	–	Covered
bin <auto[1],auto[1],auto[0]>	43	1	–	Covered
bin <auto[0],auto[1],auto[1]>	435	1	–	Covered
bin <auto[0],auto[1],auto[0]>	144	1	–	Covered
bin <auto[1],auto[0],auto[0]>	179	1	–	Covered
bin <auto[0],auto[0],auto[0]>	216	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	118	1	–	Covered
bin <auto[0],auto[0],auto[1]>	16	1	–	Covered
bin <auto[1],auto[1],auto[0]>	231	1	–	Covered
bin <auto[1],auto[0],auto[0]>	179	1	–	Covered
bin <auto[0],auto[1],auto[0]>	461	1	–	Covered
bin <auto[0],auto[0],auto[0]>	200	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	25	1	–	Covered
bin <auto[1],auto[0],auto[1]>	125	1	–	Covered
bin <auto[1],auto[1],auto[0]>	206	1	–	Covered
bin <auto[0],auto[1],auto[0]>	513	1	–	Covered
bin <auto[1],auto[0],auto[0]>	54	1	–	Covered
bin <auto[0],auto[0],auto[0]>	161	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	121		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	36	1	–	Covered

bin <auto[1],auto[0],auto[1]>	8	1	–	Covered
bin <auto[1],auto[1],auto[0]>	195	1	–	Covered
bin <auto[0],auto[1],auto[0]>	546	1	–	Covered
bin <auto[1],auto[0],auto[0]>	171	1	–	Covered
bin <auto[0],auto[0],auto[0]>	202	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	47		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	73	1	–	Covered
bin <auto[1],auto[1],auto[0]>	158	1	–	Covered
bin <auto[0],auto[1],auto[1]>	79	1	–	Covered
bin <auto[0],auto[1],auto[0]>	500	1	–	Covered
bin <auto[1],auto[0],auto[0]>	167	1	–	Covered
bin <auto[0],auto[0],auto[0]>	177	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	51		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	18	1	–	Covered
bin <auto[1],auto[1],auto[0]>	213	1	–	Covered
bin <auto[0],auto[1],auto[1]>	88	1	–	Covered
bin <auto[0],auto[1],auto[0]>	491	1	–	Covered
bin <auto[1],auto[0],auto[0]>	179	1	–	Covered
bin <auto[0],auto[0],auto[0]>	216	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	36	1	–	Covered
bin <auto[1],auto[0],auto[1]>	99	1	–	Covered
bin <auto[1],auto[1],auto[0]>	195	1	–	Covered
bin <auto[0],auto[1],auto[0]>	579	1	–	Covered
bin <auto[1],auto[0],auto[0]>	80	1	–	Covered
bin <auto[0],auto[0],auto[0]>	216	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.58%	100	–	Uncovered
covered/total bins:	185	190	–	
missing/total bins:	5	190	–	
% Hit:	97.36%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	130	1	–	Covered
bin auto[1]	1075	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	186	1	–	Covered
bin auto[1024:2047]	14	1	–	Covered
bin auto[2048:3071]	15	1	–	Covered
bin auto[3072:4095]	12	1	–	Covered
bin auto[4096:5119]	17	1	–	Covered
bin auto[5120:6143]	20	1	–	Covered
bin auto[6144:7167]	16	1	–	Covered
bin auto[7168:8191]	14	1	–	Covered
bin auto[8192:9215]	17	1	–	Covered
bin auto[9216:10239]	11	1	–	Covered
bin auto[10240:11263]	15	1	–	Covered
bin auto[11264:12287]	13	1	–	Covered
bin auto[12288:13311]	14	1	–	Covered
bin auto[13312:14335]	8	1	–	Covered
bin auto[14336:15359]	19	1	–	Covered
bin auto[15360:16383]	14	1	–	Covered
bin auto[16384:17407]	10	1	–	Covered
bin auto[17408:18431]	10	1	–	Covered
bin auto[18432:19455]	17	1	–	Covered
bin auto[19456:20479]	7	1	–	Covered
bin auto[20480:21503]	8	1	–	Covered
bin auto[21504:22527]	9	1	–	Covered
bin auto[22528:23551]	12	1	–	Covered
bin auto[23552:24575]	10	1	–	Covered
bin auto[24576:25599]	11	1	–	Covered
bin auto[25600:26623]	18	1	–	Covered

bin auto[26624:27647]	12	1	–	Covered
bin auto[27648:28671]	14	1	–	Covered
bin auto[28672:29695]	16	1	–	Covered
bin auto[29696:30719]	19	1	–	Covered
bin auto[30720:31743]	7	1	–	Covered
bin auto[31744:32767]	12	1	–	Covered
bin auto[32768:33791]	25	1	–	Covered
bin auto[33792:34815]	14	1	–	Covered
bin auto[34816:35839]	15	1	–	Covered
bin auto[35840:36863]	19	1	–	Covered
bin auto[36864:37887]	21	1	–	Covered
bin auto[37888:38911]	10	1	–	Covered
bin auto[38912:39935]	16	1	–	Covered
bin auto[39936:40959]	11	1	–	Covered
bin auto[40960:41983]	14	1	–	Covered
bin auto[41984:43007]	12	1	–	Covered
bin auto[43008:44031]	12	1	–	Covered
bin auto[44032:45055]	18	1	–	Covered
bin auto[45056:46079]	12	1	–	Covered
bin auto[46080:47103]	10	1	–	Covered
bin auto[47104:48127]	9	1	–	Covered
bin auto[48128:49151]	17	1	–	Covered
bin auto[49152:50175]	14	1	–	Covered
bin auto[50176:51199]	11	1	–	Covered
bin auto[51200:52223]	10	1	–	Covered
bin auto[52224:53247]	16	1	–	Covered
bin auto[53248:54271]	8	1	–	Covered
bin auto[54272:55295]	22	1	–	Covered
bin auto[55296:56319]	12	1	–	Covered
bin auto[56320:57343]	15	1	–	Covered
bin auto[57344:58367]	15	1	–	Covered
bin auto[58368:59391]	17	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	12	1	–	Covered
bin auto[61440:62463]	14	1	–	Covered
bin auto[62464:63487]	14	1	–	Covered
bin auto[63488:64511]	11	1	–	Covered
bin auto[64512:65535]	166	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	795	1	–	Covered
bin auto[1]	410	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	395	1	–	Covered
bin auto[1]	810	1	–	Covered
Coverpoint data_out_cp	92.18%	100	–	Uncovered
covered/total bins:	59	64	–	
missing/total bins:	5	64	–	
% Hit:	92.18%	100	–	
bin auto[0:1023]	640	1	–	Covered
bin auto[1024:2047]	20	1	–	Covered
bin auto[2048:3071]	0	1	–	ZERO
bin auto[3072:4095]	5	1	–	Covered
bin auto[4096:5119]	5	1	–	Covered
bin auto[5120:6143]	7	1	–	Covered
bin auto[6144:7167]	18	1	–	Covered
bin auto[7168:8191]	13	1	–	Covered
bin auto[8192:9215]	14	1	–	Covered
bin auto[9216:10239]	4	1	–	Covered
bin auto[10240:11263]	10	1	–	Covered
bin auto[11264:12287]	15	1	–	Covered
bin auto[12288:13311]	17	1	–	Covered
bin auto[13312:14335]	12	1	–	Covered
bin auto[14336:15359]	11	1	–	Covered
bin auto[15360:16383]	3	1	–	Covered
bin auto[16384:17407]	1	1	–	Covered
bin auto[17408:18431]	4	1	–	Covered
bin auto[18432:19455]	21	1	–	Covered
bin auto[19456:20479]	0	1	–	ZERO
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	1	1	–	Covered
bin auto[22528:23551]	5	1	–	Covered
bin auto[23552:24575]	4	1	–	Covered
bin auto[24576:25599]	4	1	–	Covered
bin auto[25600:26623]	6	1	–	Covered
bin auto[26624:27647]	5	1	–	Covered
bin auto[27648:28671]	13	1	–	Covered
bin auto[28672:29695]	1	1	–	Covered
bin auto[29696:30719]	1	1	–	Covered
bin auto[30720:31743]	9	1	–	Covered
bin auto[31744:32767]	5	1	–	Covered
bin auto[32768:33791]	22	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	7	1	–	Covered
bin auto[35840:36863]	14	1	–	Covered
bin auto[36864:37887]	6	1	–	Covered
bin auto[37888:38911]	3	1	–	Covered

bin auto[38912:39935]	19	1	–	Covered
bin auto[39936:40959]	5	1	–	Covered
bin auto[40960:41983]	5	1	–	Covered
bin auto[41984:43007]	11	1	–	Covered
bin auto[43008:44031]	13	1	–	Covered
bin auto[44032:45055]	9	1	–	Covered
bin auto[45056:46079]	2	1	–	Covered
bin auto[46080:47103]	14	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	16	1	–	Covered
bin auto[49152:50175]	7	1	–	Covered
bin auto[50176:51199]	4	1	–	Covered
bin auto[51200:52223]	16	1	–	Covered
bin auto[52224:53247]	7	1	–	Covered
bin auto[53248:54271]	0	1	–	ZERO
bin auto[54272:55295]	9	1	–	Covered
bin auto[55296:56319]	3	1	–	Covered
bin auto[56320:57343]	0	1	–	ZERO
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	11	1	–	Covered
bin auto[59392:60415]	11	1	–	Covered
bin auto[60416:61439]	7	1	–	Covered
bin auto[61440:62463]	6	1	–	Covered
bin auto[62464:63487]	3	1	–	Covered
bin auto[63488:64511]	9	1	–	Covered
bin auto[64512:65535]	68	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	582	1	–	Covered
bin auto[1]	623	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1099	1	–	Covered
bin auto[1]	106	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1071	1	–	Covered
bin auto[1]	134	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	934	1	–	Covered
bin auto[1]	271	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1114	1	–	Covered
bin auto[1]	91	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1002	1	–	Covered
bin auto[1]	203	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1070	1	–	Covered
bin auto[1]	135	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	188	1	–	Covered
bin <auto[1],auto[1],auto[0]>	43	1	–	Covered
bin <auto[0],auto[1],auto[1]>	435	1	–	Covered
bin <auto[0],auto[1],auto[0]>	144	1	–	Covered
bin <auto[1],auto[0],auto[0]>	179	1	–	Covered
bin <auto[0],auto[0],auto[0]>	216	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	118	1	–	Covered
bin <auto[0],auto[0],auto[1]>	16	1	–	Covered
bin <auto[1],auto[1],auto[0]>	231	1	–	Covered
bin <auto[1],auto[0],auto[0]>	179	1	–	Covered
bin <auto[0],auto[1],auto[0]>	461	1	–	Covered
bin <auto[0],auto[0],auto[0]>	200	1	–	Covered

```
    Illegal and Ignore Bins:
        ignore_bin r_en_actv_wr_full                0                          -    ZERO
        ignore_bin w_en_r_en_allactv_full           0                          -    ZERO
Cross empty_cross                                 100.00%      100             -    Covered
    covered/total bins:                                6        6             -
    missing/total bins:                                0        6             -
    % Hit:                                        100.00%      100             -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 25        1             -    Covered
        bin <auto[1],auto[0],auto[1]>                125        1             -    Covered
        bin <auto[1],auto[1],auto[0]>                206        1             -    Covered
        bin <auto[0],auto[1],auto[0]>                513        1             -    Covered
        bin <auto[1],auto[0],auto[0]>                 54        1             -    Covered
        bin <auto[0],auto[0],auto[0]>                161        1             -    Covered
    Illegal and Ignore Bins:
        ignore_bin read_nactv_empty                  121                      -    Occurred
Cross almostfull_cross                            100.00%      100             -    Covered
    covered/total bins:                                6        6             -
    missing/total bins:                                0        6             -
    % Hit:                                        100.00%      100             -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 36        1             -    Covered
        bin <auto[1],auto[0],auto[1]>                  8        1             -    Covered
        bin <auto[1],auto[1],auto[0]>                195        1             -    Covered
        bin <auto[0],auto[1],auto[0]>                546        1             -    Covered
        bin <auto[1],auto[0],auto[0]>                171        1             -    Covered
        bin <auto[0],auto[0],auto[0]>                202        1             -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_almostfull              47                      -    Occurred
Cross almostempty_cross                           100.00%      100             -    Covered
    covered/total bins:                                6        6             -
    missing/total bins:                                0        6             -
    % Hit:                                        100.00%      100             -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 73        1             -    Covered
        bin <auto[1],auto[1],auto[0]>                158        1             -    Covered
        bin <auto[0],auto[1],auto[1]>                 79        1             -    Covered
        bin <auto[0],auto[1],auto[0]>                500        1             -    Covered
        bin <auto[1],auto[0],auto[0]>                167        1             -    Covered
        bin <auto[0],auto[0],auto[0]>                177        1             -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_almostempty             51                      -    Occurred
Cross overflow_cross                              100.00%      100             -    Covered
    covered/total bins:                                6        6             -
    missing/total bins:                                0        6             -
    % Hit:                                        100.00%      100             -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 18        1             -    Covered
        bin <auto[1],auto[1],auto[0]>                213        1             -    Covered
        bin <auto[0],auto[1],auto[1]>                 88        1             -    Covered
        bin <auto[0],auto[1],auto[0]>                491        1             -    Covered
        bin <auto[1],auto[0],auto[0]>                179        1             -    Covered
        bin <auto[0],auto[0],auto[0]>                216        1             -    Covered
    Illegal and Ignore Bins:
        ignore_bin w_en_nactv_wr_ack                   0                      -    ZERO
Cross underflow_cross                             100.00%      100             -    Covered
    covered/total bins:                                6        6             -
    missing/total bins:                                0        6             -
    % Hit:                                        100.00%      100             -
    Auto, Default and User Defined Bins:
        bin <auto[1],auto[1],auto[1]>                 36        1             -    Covered
        bin <auto[1],auto[0],auto[1]>                 99        1             -    Covered
        bin <auto[1],auto[1],auto[0]>                195        1             -    Covered
        bin <auto[0],auto[1],auto[0]>                579        1             -    Covered
        bin <auto[1],auto[0],auto[0]>                 80        1             -    Covered
        bin <auto[0],auto[0],auto[0]>                216        1             -    Covered
    Illegal and Ignore Bins:
        ignore_bin r_en_nactv_wr_ack                   0                      -    ZERO
```

TOTAL COVERGROUP COVERAGE: 99.58% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.58%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover__n_wr_a...	SVA	✓	Off	105	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__counte...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	1075	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	6	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	38	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	182	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	81	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__full_fla...	SVA	✓	Off	120	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__empty...	SVA	✓	Off	237	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__underfl...	SVA	✓	Off	112	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__overflo...	SVA	✓	Off	67	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_a...	SVA	✓	Off	562	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__reset_...	SVA	✓	Off	130	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 4: SVA "Seed4"

3.5 Functional Coverage "seed5" Report

Coverage Report by instance with details

```
=================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
=================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na    99.25%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   190       181         9    95.26%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.25%	100	–	Uncovered
covered/total bins:	181	190	–	
missing/total bins:	9	190	–	
% Hit:	95.26%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	124	1	–	Covered
bin auto[1]	1081	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	200	1	–	Covered
bin auto[1024:2047]	10	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	10	1	–	Covered
bin auto[4096:5119]	16	1	–	Covered
bin auto[5120:6143]	16	1	–	Covered
bin auto[6144:7167]	9	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	13	1	–	Covered
bin auto[9216:10239]	14	1	–	Covered
bin auto[10240:11263]	9	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	11	1	–	Covered
bin auto[14336:15359]	12	1	–	Covered
bin auto[15360:16383]	11	1	–	Covered
bin auto[16384:17407]	14	1	–	Covered
bin auto[17408:18431]	7	1	–	Covered
bin auto[18432:19455]	19	1	–	Covered
bin auto[19456:20479]	17	1	–	Covered
bin auto[20480:21503]	11	1	–	Covered
bin auto[21504:22527]	16	1	–	Covered
bin auto[22528:23551]	8	1	–	Covered
bin auto[23552:24575]	14	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	19	1	–	Covered
bin auto[27648:28671]	27	1	–	Covered
bin auto[28672:29695]	14	1	–	Covered
bin auto[29696:30719]	13	1	–	Covered
bin auto[30720:31743]	16	1	–	Covered
bin auto[31744:32767]	12	1	–	Covered
bin auto[32768:33791]	9	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	19	1	–	Covered
bin auto[35840:36863]	13	1	–	Covered
bin auto[36864:37887]	20	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	16	1	–	Covered
bin auto[41984:43007]	12	1	–	Covered
bin auto[43008:44031]	16	1	–	Covered
bin auto[44032:45055]	15	1	–	Covered
bin auto[45056:46079]	15	1	–	Covered
bin auto[46080:47103]	18	1	–	Covered
bin auto[47104:48127]	19	1	–	Covered
bin auto[48128:49151]	10	1	–	Covered
bin auto[49152:50175]	12	1	–	Covered
bin auto[50176:51199]	14	1	–	Covered
bin auto[51200:52223]	10	1	–	Covered
bin auto[52224:53247]	18	1	–	Covered
bin auto[53248:54271]	9	1	–	Covered
bin auto[54272:55295]	11	1	–	Covered
bin auto[55296:56319]	15	1	–	Covered
bin auto[56320:57343]	9	1	–	Covered
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	17	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	10	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered
bin auto[62464:63487]	13	1	–	Covered
bin auto[63488:64511]	6	1	–	Covered

bin auto[64512:65535]	188	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	816	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	414	1	–	Covered
bin auto[1]	791	1	–	Covered
Coverpoint data_out_cp	85.93%	100	–	Uncovered
covered/total bins:	55	64	–	
missing/total bins:	9	64	–	
% Hit:	85.93%	100	–	
bin auto[0:1023]	685	1	–	Covered
bin auto[1024:2047]	2	1	–	Covered
bin auto[2048:3071]	0	1	–	ZERO
bin auto[3072:4095]	5	1	–	Covered
bin auto[4096:5119]	14	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	23	1	–	Covered
bin auto[7168:8191]	20	1	–	Covered
bin auto[8192:9215]	6	1	–	Covered
bin auto[9216:10239]	8	1	–	Covered
bin auto[10240:11263]	1	1	–	Covered
bin auto[11264:12287]	7	1	–	Covered
bin auto[12288:13311]	0	1	–	ZERO
bin auto[13312:14335]	5	1	–	Covered
bin auto[14336:15359]	5	1	–	Covered
bin auto[15360:16383]	0	1	–	ZERO
bin auto[16384:17407]	7	1	–	Covered
bin auto[17408:18431]	1	1	–	Covered
bin auto[18432:19455]	8	1	–	Covered
bin auto[19456:20479]	1	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	12	1	–	Covered
bin auto[22528:23551]	0	1	–	ZERO
bin auto[23552:24575]	2	1	–	Covered
bin auto[24576:25599]	2	1	–	Covered
bin auto[25600:26623]	17	1	–	Covered
bin auto[26624:27647]	17	1	–	Covered
bin auto[27648:28671]	13	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	6	1	–	Covered
bin auto[30720:31743]	7	1	–	Covered
bin auto[31744:32767]	2	1	–	Covered
bin auto[32768:33791]	7	1	–	Covered
bin auto[33792:34815]	0	1	–	ZERO
bin auto[34816:35839]	19	1	–	Covered
bin auto[35840:36863]	1	1	–	Covered
bin auto[36864:37887]	0	1	–	ZERO
bin auto[37888:38911]	5	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	3	1	–	Covered
bin auto[40960:41983]	3	1	–	Covered
bin auto[41984:43007]	11	1	–	Covered
bin auto[43008:44031]	17	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	4	1	–	Covered
bin auto[46080:47103]	2	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	0	1	–	ZERO
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	3	1	–	Covered
bin auto[51200:52223]	4	1	–	Covered
bin auto[52224:53247]	6	1	–	Covered
bin auto[53248:54271]	0	1	–	ZERO
bin auto[54272:55295]	1	1	–	Covered
bin auto[55296:56319]	21	1	–	Covered
bin auto[56320:57343]	22	1	–	Covered
bin auto[57344:58367]	1	1	–	Covered
bin auto[58368:59391]	10	1	–	Covered
bin auto[59392:60415]	10	1	–	Covered
bin auto[60416:61439]	12	1	–	Covered
bin auto[61440:62463]	18	1	–	Covered
bin auto[62464:63487]	2	1	–	Covered
bin auto[63488:64511]	4	1	–	Covered
bin auto[64512:65535]	102	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	612	1	–	Covered
bin auto[1]	593	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1072	1	–	Covered

bin auto[1]	133	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1047	1	–	Covered
bin auto[1]	158	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	922	1	–	Covered
bin auto[1]	283	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1113	1	–	Covered
bin auto[1]	92	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1021	1	–	Covered
bin auto[1]	184	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1058	1	–	Covered
bin auto[1]	147	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	171	1	–	Covered
bin <auto[1],auto[1],auto[0]>	37	1	–	Covered
bin <auto[0],auto[1],auto[1]>	422	1	–	Covered
bin <auto[0],auto[1],auto[0]>	161	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	145	1	–	Covered
bin <auto[0],auto[0],auto[1]>	13	1	–	Covered
bin <auto[1],auto[1],auto[0]>	208	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	438	1	–	Covered
bin <auto[0],auto[0],auto[0]>	220	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[0],auto[1]>	133	1	–	Covered
bin <auto[1],auto[1],auto[0]>	188	1	–	Covered
bin <auto[0],auto[1],auto[0]>	526	1	–	Covered
bin <auto[1],auto[0],auto[0]>	48	1	–	Covered
bin <auto[0],auto[0],auto[0]>	160	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	130		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	30	1	–	Covered
bin <auto[1],auto[0],auto[1]>	7	1	–	Covered
bin <auto[1],auto[1],auto[0]>	178	1	–	Covered
bin <auto[0],auto[1],auto[0]>	551	1	–	Covered
bin <auto[1],auto[0],auto[0]>	174	1	–	Covered
bin <auto[0],auto[0],auto[0]>	210	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	55		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	64	1	–	Covered
bin <auto[1],auto[1],auto[0]>	144	1	–	Covered
bin <auto[0],auto[1],auto[1]>	79	1	–	Covered

bin <auto[0],auto[1],auto[0]>	504	1	–	Covered
bin <auto[1],auto[0],auto[0]>	174	1	–	Covered
bin <auto[0],auto[0],auto[0]>	199	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	41		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	21	1	–	Covered
bin <auto[1],auto[1],auto[0]>	187	1	–	Covered
bin <auto[0],auto[1],auto[1]>	112	1	–	Covered
bin <auto[0],auto[1],auto[0]>	471	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	42	1	–	Covered
bin <auto[1],auto[0],auto[1]>	105	1	–	Covered
bin <auto[1],auto[1],auto[0]>	166	1	–	Covered
bin <auto[0],auto[1],auto[0]>	583	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	99.25%	100	–	Uncovered
covered/total bins:	181	190	–	
missing/total bins:	9	190	–	
% Hit:	95.26%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	124	1	–	Covered
bin auto[1]	1081	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	200	1	–	Covered
bin auto[1024:2047]	10	1	–	Covered
bin auto[2048:3071]	7	1	–	Covered
bin auto[3072:4095]	10	1	–	Covered
bin auto[4096:5119]	16	1	–	Covered
bin auto[5120:6143]	16	1	–	Covered
bin auto[6144:7167]	9	1	–	Covered
bin auto[7168:8191]	18	1	–	Covered
bin auto[8192:9215]	13	1	–	Covered
bin auto[9216:10239]	14	1	–	Covered
bin auto[10240:11263]	9	1	–	Covered
bin auto[11264:12287]	11	1	–	Covered
bin auto[12288:13311]	9	1	–	Covered
bin auto[13312:14335]	11	1	–	Covered
bin auto[14336:15359]	12	1	–	Covered
bin auto[15360:16383]	11	1	–	Covered
bin auto[16384:17407]	14	1	–	Covered
bin auto[17408:18431]	7	1	–	Covered
bin auto[18432:19455]	19	1	–	Covered
bin auto[19456:20479]	17	1	–	Covered
bin auto[20480:21503]	11	1	–	Covered
bin auto[21504:22527]	16	1	–	Covered
bin auto[22528:23551]	8	1	–	Covered
bin auto[23552:24575]	14	1	–	Covered
bin auto[24576:25599]	15	1	–	Covered
bin auto[25600:26623]	10	1	–	Covered
bin auto[26624:27647]	19	1	–	Covered
bin auto[27648:28671]	27	1	–	Covered
bin auto[28672:29695]	14	1	–	Covered
bin auto[29696:30719]	13	1	–	Covered
bin auto[30720:31743]	16	1	–	Covered
bin auto[31744:32767]	12	1	–	Covered
bin auto[32768:33791]	9	1	–	Covered
bin auto[33792:34815]	12	1	–	Covered
bin auto[34816:35839]	19	1	–	Covered
bin auto[35840:36863]	13	1	–	Covered
bin auto[36864:37887]	20	1	–	Covered
bin auto[37888:38911]	13	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	9	1	–	Covered
bin auto[40960:41983]	16	1	–	Covered

bin auto[41984:43007]	12	1	–	Covered
bin auto[43008:44031]	16	1	–	Covered
bin auto[44032:45055]	15	1	–	Covered
bin auto[45056:46079]	15	1	–	Covered
bin auto[46080:47103]	18	1	–	Covered
bin auto[47104:48127]	19	1	–	Covered
bin auto[48128:49151]	10	1	–	Covered
bin auto[49152:50175]	12	1	–	Covered
bin auto[50176:51199]	14	1	–	Covered
bin auto[51200:52223]	10	1	–	Covered
bin auto[52224:53247]	18	1	–	Covered
bin auto[53248:54271]	9	1	–	Covered
bin auto[54272:55295]	11	1	–	Covered
bin auto[55296:56319]	15	1	–	Covered
bin auto[56320:57343]	9	1	–	Covered
bin auto[57344:58367]	9	1	–	Covered
bin auto[58368:59391]	17	1	–	Covered
bin auto[59392:60415]	16	1	–	Covered
bin auto[60416:61439]	10	1	–	Covered
bin auto[61440:62463]	15	1	–	Covered
bin auto[62464:63487]	13	1	–	Covered
bin auto[63488:64511]	6	1	–	Covered
bin auto[64512:65535]	188	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	816	1	–	Covered
bin auto[1]	389	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	414	1	–	Covered
bin auto[1]	791	1	–	Covered
Coverpoint data_out_cp	85.93%	100	–	Uncovered
covered/total bins:	55	64	–	
missing/total bins:	9	64	–	
% Hit:	85.93%	100	–	
bin auto[0:1023]	685	1	–	Covered
bin auto[1024:2047]	2	1	–	Covered
bin auto[2048:3071]	0	1	–	ZERO
bin auto[3072:4095]	5	1	–	Covered
bin auto[4096:5119]	14	1	–	Covered
bin auto[5120:6143]	15	1	–	Covered
bin auto[6144:7167]	23	1	–	Covered
bin auto[7168:8191]	20	1	–	Covered
bin auto[8192:9215]	6	1	–	Covered
bin auto[9216:10239]	8	1	–	Covered
bin auto[10240:11263]	1	1	–	Covered
bin auto[11264:12287]	7	1	–	Covered
bin auto[12288:13311]	0	1	–	ZERO
bin auto[13312:14335]	5	1	–	Covered
bin auto[14336:15359]	5	1	–	Covered
bin auto[15360:16383]	0	1	–	ZERO
bin auto[16384:17407]	7	1	–	Covered
bin auto[17408:18431]	1	1	–	Covered
bin auto[18432:19455]	8	1	–	Covered
bin auto[19456:20479]	1	1	–	Covered
bin auto[20480:21503]	3	1	–	Covered
bin auto[21504:22527]	12	1	–	Covered
bin auto[22528:23551]	0	1	–	ZERO
bin auto[23552:24575]	2	1	–	Covered
bin auto[24576:25599]	2	1	–	Covered
bin auto[25600:26623]	17	1	–	Covered
bin auto[26624:27647]	17	1	–	Covered
bin auto[27648:28671]	13	1	–	Covered
bin auto[28672:29695]	9	1	–	Covered
bin auto[29696:30719]	6	1	–	Covered
bin auto[30720:31743]	7	1	–	Covered
bin auto[31744:32767]	2	1	–	Covered
bin auto[32768:33791]	7	1	–	Covered
bin auto[33792:34815]	0	1	–	ZERO
bin auto[34816:35839]	19	1	–	Covered
bin auto[35840:36863]	1	1	–	Covered
bin auto[36864:37887]	0	1	–	ZERO
bin auto[37888:38911]	5	1	–	Covered
bin auto[38912:39935]	9	1	–	Covered
bin auto[39936:40959]	3	1	–	Covered
bin auto[40960:41983]	3	1	–	Covered
bin auto[41984:43007]	11	1	–	Covered
bin auto[43008:44031]	17	1	–	Covered
bin auto[44032:45055]	3	1	–	Covered
bin auto[45056:46079]	4	1	–	Covered
bin auto[46080:47103]	2	1	–	Covered
bin auto[47104:48127]	0	1	–	ZERO
bin auto[48128:49151]	0	1	–	ZERO
bin auto[49152:50175]	2	1	–	Covered
bin auto[50176:51199]	3	1	–	Covered
bin auto[51200:52223]	4	1	–	Covered
bin auto[52224:53247]	6	1	–	Covered
bin auto[53248:54271]	0	1	–	ZERO

bin auto[54272:55295]	1	1	–	Covered
bin auto[55296:56319]	21	1	–	Covered
bin auto[56320:57343]	22	1	–	Covered
bin auto[57344:58367]	1	1	–	Covered
bin auto[58368:59391]	10	1	–	Covered
bin auto[59392:60415]	10	1	–	Covered
bin auto[60416:61439]	12	1	–	Covered
bin auto[61440:62463]	18	1	–	Covered
bin auto[62464:63487]	2	1	–	Covered
bin auto[63488:64511]	4	1	–	Covered
bin auto[64512:65535]	102	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	612	1	–	Covered
bin auto[1]	593	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1072	1	–	Covered
bin auto[1]	133	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1047	1	–	Covered
bin auto[1]	158	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	922	1	–	Covered
bin auto[1]	283	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1113	1	–	Covered
bin auto[1]	92	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1021	1	–	Covered
bin auto[1]	184	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	1058	1	–	Covered
bin auto[1]	147	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	171	1	–	Covered
bin <auto[1],auto[1],auto[0]>	37	1	–	Covered
bin <auto[0],auto[1],auto[1]>	422	1	–	Covered
bin <auto[0],auto[1],auto[0]>	161	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	145	1	–	Covered
bin <auto[0],auto[0],auto[1]>	13	1	–	Covered
bin <auto[1],auto[1],auto[0]>	208	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[1],auto[0]>	438	1	–	Covered
bin <auto[0],auto[0],auto[0]>	220	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	20	1	–	Covered
bin <auto[1],auto[0],auto[1]>	133	1	–	Covered
bin <auto[1],auto[1],auto[0]>	188	1	–	Covered
bin <auto[0],auto[1],auto[0]>	526	1	–	Covered
bin <auto[1],auto[0],auto[0]>	48	1	–	Covered
bin <auto[0],auto[0],auto[0]>	160	1	–	Covered
Illegal and Ignore Bins:				

ignore_bin read_nactv_empty	130		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	30	1	–	Covered
bin <auto[1],auto[0],auto[1]>	7	1	–	Covered
bin <auto[1],auto[1],auto[0]>	178	1	–	Covered
bin <auto[0],auto[1],auto[0]>	551	1	–	Covered
bin <auto[1],auto[0],auto[0]>	174	1	–	Covered
bin <auto[0],auto[0],auto[0]>	210	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	55		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	64	1	–	Covered
bin <auto[1],auto[1],auto[0]>	144	1	–	Covered
bin <auto[0],auto[1],auto[1]>	79	1	–	Covered
bin <auto[0],auto[1],auto[0]>	504	1	–	Covered
bin <auto[1],auto[0],auto[0]>	174	1	–	Covered
bin <auto[0],auto[0],auto[0]>	199	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	41		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	21	1	–	Covered
bin <auto[1],auto[1],auto[0]>	187	1	–	Covered
bin <auto[0],auto[1],auto[1]>	112	1	–	Covered
bin <auto[0],auto[1],auto[0]>	471	1	–	Covered
bin <auto[1],auto[0],auto[0]>	181	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	42	1	–	Covered
bin <auto[1],auto[0],auto[1]>	105	1	–	Covered
bin <auto[1],auto[1],auto[0]>	166	1	–	Covered
bin <auto[0],auto[1],auto[0]>	583	1	–	Covered
bin <auto[1],auto[0],auto[0]>	76	1	–	Covered
bin <auto[0],auto[0],auto[0]>	233	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 99.25% COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 99.25%

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	Cover Type	Design Unit	Design Unit Type
/top/cover__n_wr_a...	SVA	✓	Off	129	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__counte...	SVA	✓	Off	1081	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	1081	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	1081	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__read_p...	SVA	✓	Off	5	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_p...	SVA	✓	Off	36	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	160	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__almost...	SVA	✓	Off	83	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__full_fla...	SVA	✓	Off	141	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__empty...	SVA	✓	Off	254	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__underfl...	SVA	✓	Off	123	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__overflo...	SVA	✓	Off	94	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__write_a...	SVA	✓	Off	535	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog
/top/cover__reset_...	SVA	✓	Off	124	1	Unli...	1	100%		✓	0	0	0 ns	0	Concurrent	top	Verilog

Figure 5: SVA "Seed5"

4 Code Coverage Report

4.1 Code Coverage "seed1" Report

Coverage Report by DU with details

Design Unit: work.FIFO

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	25	25	0	100.00%

Branch Details

```
Branch Coverage for Design Unit work.FIFO

    Line         Item                      Count      Source
    ____         ____                      _____      ______

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                      1329      Count coming in to IF
    13              1                        261         if (!fifo_intf.rst_n) begin
    18              1                        630         else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                        438         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                       438      Count coming in to IF
    25              1                         85                 if (fifo_intf.full & fifo_intf.wr_en)
    27              1                        353                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                      1329      Count coming in to IF
    33              1                        261         if (!fifo_intf.rst_n) begin
    38              1                        237         else if (fifo_intf.rd_en && count != 0) begin
    42              1                        831         else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                       831      Count coming in to IF
    43              1                        140                 if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                        691                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                      1136      Count coming in to IF
    51              1                        254         if (!fifo_intf.rst_n) begin
    54              1                        882         else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                       882      Count coming in to IF
    55              1                        439                 if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                         70                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                         15                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                         39                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                              319      All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                       670      Count coming in to IF
    66              1                         34      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                        636      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                       918      Count coming in to IF
    67              1                        376      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                        542      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                       670      Count coming in to IF
    68              1                         48      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                        622      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                       670      Count coming in to IF
    69              1                        146      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                        524      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ________________                 ____    _____       ______  ________
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO —

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
----------Focused Condition View----------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      __________   _______  ______________________   ____
  fifo_intf.wr_en        Y
     (count < 8)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
     _____       ____  __________            ________________________
```

Row 1:	1	fifo_intf.wr_en_0	–
Row 2:	1	fifo_intf.wr_en_1	(count < 8)
Row 3:	1	(count < 8)_0	fifo_intf.wr_en
Row 4:	1	(count < 8)_1	fifo_intf.wr_en

----------Focused Condition View----------
Line 25 Item 1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.full	N	'_0' not hit	Hit '_0'
fifo_intf.wr_en	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	fifo_intf.full_0	fifo_intf.wr_en
Row 2:	1	fifo_intf.full_1	fifo_intf.wr_en
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.full
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.full

----------Focused Condition View----------
Line 38 Item 1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
(count != 0)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(count != 0)
Row 3:	1	(count != 0)_0	fifo_intf.rd_en
Row 4:	1	(count != 0)_1	fifo_intf.rd_en

----------Focused Condition View----------
Line 43 Item 1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.empty	N	'_0' not hit	Hit '_0'
fifo_intf.rd_en	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	fifo_intf.empty_0	fifo_intf.rd_en
Row 2:	1	fifo_intf.empty_1	fifo_intf.rd_en
Row 3:	1	fifo_intf.rd_en_0	fifo_intf.empty
Row 4:	1	fifo_intf.rd_en_1	fifo_intf.empty

----------Focused Condition View----------
Line 55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	–
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------

Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 8)_0	-
Row 2:	1	(count == 8)_1	-

----------Focused Condition View----------
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	-
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == (8 - 1))_0	-
Row 2:	1	(count == (8 - 1))_1	-

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 1)_0	-
Row 2:	1	(count == 1)_1	-

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

Statement Details

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1329	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	261	wr_ptr <= 0;
15	1	261	fifo_intf.wr_ack <= 0;
16	1	261	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	630	mem[wr_ptr] <= fifo_intf.data_in;
20	1	630	fifo_intf.wr_ack <= 1;
21	1	630	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	438	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	85	fifo_intf.overflow <= 1;
27			else
28	1	353	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	1329	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	261	rd_ptr <= 0;
35	1	261	fifo_intf.underflow <= 0;
36	1	261	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	237	fifo_intf.data_out <= mem[rd_ptr];
40	1	237	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	140	fifo_intf.underflow <= 1;
45			else
46	1	691	fifo_intf.underflow <= 0;
47			end
48			end
49			
50	1	1136	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51			if (!fifo_intf.rst_n) begin
52	1	254	count <= 0;
53			end
54			else begin
55			if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56	1	439	count <= count + 1;
57			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58	1	70	count <= count - 1;
59			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60	1	15	count <= count - 1;
61			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62	1	39	count <= count + 1;
63			end
64			end
65			
66	1	671	assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67	1	919	assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68	1	671	assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69	1	671	assign fifo_intf.almostempty = (count == 1)? 1 : 0;

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H–>0L	0L–>1H	"Coverage"
count[0–3]	1	1	100.00
rd_ptr[0–2]	1	1	100.00
wr_ptr[0–2]	1	1	100.00

```
Total Node Count        =         10
Toggled Node Count      =         10
Untoggled Node Count    =          0

Toggle Coverage         =     100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

4.2 Code Coverage "seed2" Report

```
Coverage Report by DU with details

================================================================================
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                     1315     Count coming in to IF
    13              1                       240        if (!fifo_intf.rst_n) begin
    18              1                       612        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                       463        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                      463     Count coming in to IF
    25              1                       115                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                       348                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                     1315     Count coming in to IF
    33              1                       240        if (!fifo_intf.rst_n) begin
    38              1                       214        else if (fifo_intf.rd_en && count != 0) begin
    42              1                       861        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                      861     Count coming in to IF
    43              1                       129                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                       732                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                     1126     Count coming in to IF
    51              1                       233        if (!fifo_intf.rst_n) begin
    54              1                       893        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                      893     Count coming in to IF
    55              1                       451                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                        60                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                        25                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                        32                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                             325     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                      665     Count coming in to IF
    66              1                        50     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                       615     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                      885     Count coming in to IF
    67              1                       328     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                       557     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                      665     Count coming in to IF
    68              1                        68     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                       597     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    69                                    665     Count coming in to IF
    69              1                     120     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                     545     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.wr_en         Y
     (count < 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          1  fifo_intf.wr_en_0       -
  Row    2:          1  fifo_intf.wr_en_1       (count < 8)
  Row    3:          1  (count < 8)_0           fifo_intf.wr_en
  Row    4:          1  (count < 8)_1           fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
   fifo_intf.full          N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.full_0       fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1       fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0      fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1      fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.rd_en         Y
    (count != 0)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
  Row    3:          1  (count != 0)_0          fifo_intf.rd_en
  Row    4:          1  (count != 0)_1          fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.empty_0      fifo_intf.rd_en
  Row    2:          1  fifo_intf.empty_1      fifo_intf.rd_en
  Row    3:          1  fifo_intf.rd_en_0      fifo_intf.empty
  Row    4:          1  fifo_intf.rd_en_1      fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.rd_en         Y
  fifo_intf.wr_en         Y
   fifo_intf.full         Y
```

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	–
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

----------Focused Condition View----------
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	–

Row 3:	1	fifo_intf.rst_n_0	~(count == 0)	
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)	

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == (8 - 1))_0	-
Row 2:	1	(count == (8 - 1))_1	-

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 1)_0	-
Row 2:	1	(count == 1)_1	-

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1315	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	240	wr_ptr <= 0;
15	1	240	fifo_intf.wr_ack <= 0;
16	1	240	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	612	mem[wr_ptr] <= fifo_intf.data_in;
20	1	612	fifo_intf.wr_ack <= 1;
21	1	612	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	463	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	115	fifo_intf.overflow <= 1;
27			else
28	1	348	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	1315	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	240	rd_ptr <= 0;
35	1	240	fifo_intf.underflow <= 0;
36	1	240	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	214	fifo_intf.data_out <= mem[rd_ptr];
40	1	214	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	129	fifo_intf.underflow <= 1;
45			else
46	1	732	fifo_intf.underflow <= 0;
47			end
48			end
49			
50	1	1126	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin

```
    51                                          if (!fifo_intf.rst_n) begin
    52              1                    233                count <= 0;
    53                                          end
    54                                          else begin
    55                                                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    56              1                    451                   count <= count + 1;
    57                                                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    58              1                     60                   count <= count - 1;
    59                                                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    60              1                     25                   count <= count - 1;
    61                                                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    62              1                     32                   count <= count + 1;
    63                                          end
    64                                        end
    65
    66              1                    666      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    67              1                    886      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    68              1                    666      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    69              1                    666      assign fifo_intf.almostempty = (count == 1)? 1 : 0;

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         20        20         0   100.00%

================================Toggle Details================================

Toggle Coverage for Design Unit work.FIFO

                                          Node         1H->0L         0L->1H    "Coverage"
                                          ----------------------------------------------
                                          count[0-3]        1              1        100.00
                                          rd_ptr[0-2]       1              1        100.00
                                          wr_ptr[0-2]       1              1        100.00

Total Node Count        =         10
Toggled Node Count      =         10
Untoggled Node Count    =          0

Toggle Coverage         =     100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

4.3 Code Coverage "seed3" Report

```
Coverage Report by DU with details

================================================================================
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                           Count     Source
    ----         ----                           -----     ------
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                          1312     Count coming in to IF
    13              1                            230        if (!fifo_intf.rst_n) begin
    18              1                            624        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                            458        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                           458     Count coming in to IF
    25              1                             84                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                            374                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                          1312     Count coming in to IF
    33              1                            230        if (!fifo_intf.rst_n) begin
    38              1                            243        else if (fifo_intf.rd_en && count != 0) begin
    42              1                            839        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                           839     Count coming in to IF
    43              1                            131                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                            708                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                          1103     Count coming in to IF
    51              1                            219        if (!fifo_intf.rst_n) begin
```

```
    54              1                          884          else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                         884      Count coming in to IF
    55              1                          443                  if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                           77                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                           15                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                           30                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                               319      All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                         658      Count coming in to IF
    66              1                           37      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                          621      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                         872      Count coming in to IF
    67              1                          325      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                          547      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                         658      Count coming in to IF
    68              1                           59      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                          599      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                         658      Count coming in to IF
    69              1                          118      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                          540      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.wr_en         Y
     (count < 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  fifo_intf.wr_en_0       -
  Row    2:          1  fifo_intf.wr_en_1       (count < 8)
  Row    3:          1  (count < 8)_0           fifo_intf.wr_en
  Row    4:          1  (count < 8)_1           fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
   fifo_intf.full          N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:     ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0       fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1       fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
       ----------   -------  ----------------------   ----
  fifo_intf.rd_en          Y
    (count != 0)           Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
```

Row 3:	1	(count != 0)_0	fifo_intf.rd_en
Row 4:	1	(count != 0)_1	fifo_intf.rd_en

----------Focused Condition View----------
Line 43 Item 1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.empty	N	'_0' not hit	Hit '_0'
fifo_intf.rd_en	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	fifo_intf.empty_0	fifo_intf.rd_en
Row 2:	1	fifo_intf.empty_1	fifo_intf.rd_en
Row 3:	1	fifo_intf.rd_en_0	fifo_intf.empty
Row 4:	1	fifo_intf.rd_en_1	fifo_intf.empty

----------Focused Condition View----------
Line 55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	-
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)

```
  Row    5:          1  fifo_intf.empty_0     (fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:          1  fifo_intf.empty_1     (fifo_intf.rd_en && fifo_intf.wr_en)

------------------Focused Condition View-------------------
Line       66 Item    1  (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ------------------------  ---------------
  (count == 8)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  (count == 8)_0         -
  Row    2:          1  (count == 8)_1         -

------------------Focused Condition View-------------------
Line       67 Item    1  ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
  ---------------  --------  ------------------------  ---------------
    (count == 0)          Y
  fifo_intf.rst_n         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  (count == 0)_0         fifo_intf.rst_n
  Row    2:          1  (count == 0)_1         -
  Row    3:          1  fifo_intf.rst_n_0      ~(count == 0)
  Row    4:          1  fifo_intf.rst_n_1      ~(count == 0)

------------------Focused Condition View-------------------
Line       68 Item    1  (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

          Input Term   Covered  Reason for no coverage   Hint
  -----------------  --------  ------------------------  ---------------
  (count == (8 - 1))         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  (count == (8 - 1))_0   -
  Row    2:          1  (count == (8 - 1))_1   -

------------------Focused Condition View-------------------
Line       69 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ------------------------  ---------------
  (count == 1)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          1  (count == 1)_0         -
  Row    2:          1  (count == 1)_1         -


Statement Coverage:
    Enabled Coverage                Bins      Hits    Misses  Coverage
    ----------------                ----      ----    ------  --------
    Statements                        28        28         0   100.00%

================================Statement Details================================

Statement Coverage for Design Unit work.FIFO —

    Line           Item                           Count      Source
    ----           ----                           -----      ------
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
    1                                                       module FIFO(FIFO_IF.DUT fifo_intf);
    2                                                       parameter FIFO_WIDTH = 16;
    3                                                       parameter FIFO_DEPTH = 8;
    4
    5                                                       localparam max_fifo_addr = $clog2(FIFO_DEPTH);
    6
    7                                                       reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0];  // 1-D Array
    8
    9                                                       reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
    10                                                      reg [max_fifo_addr:0] count;
    11
    12              1                               1312    always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    13                                                          if (!fifo_intf.rst_n) begin
    14              1                                230                 wr_ptr <= 0;
    15              1                                230                 fifo_intf.wr_ack <= 0;
    16              1                                230                 fifo_intf.overflow <= 0;
    17                                                          end
    18                                                          else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    19              1                                624                 mem[wr_ptr] <= fifo_intf.data_in;
    20              1                                624                 fifo_intf.wr_ack <= 1;
    21              1                                624                 wr_ptr <= wr_ptr + 1;
```

```
22                                          end
23                                          else begin
24              1                  458              fifo_intf.wr_ack <= 0;
25                                                  if (fifo_intf.full & fifo_intf.wr_en)
26              1                   84                      fifo_intf.overflow <= 1;
27                                                  else
28              1                  374                      fifo_intf.overflow <= 0;
29                                          end
30                                      end
31
32              1                 1312      always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33                                          if (!fifo_intf.rst_n) begin
34              1                  230              rd_ptr <= 0;
35              1                  230              fifo_intf.underflow <= 0;
36              1                  230              fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37                                          end
38                                          else if (fifo_intf.rd_en && count != 0) begin
39              1                  243              fifo_intf.data_out <= mem[rd_ptr];
40              1                  243              rd_ptr <= rd_ptr + 1;
41                                          end
42                                          else begin
43                                                  if (fifo_intf.empty & fifo_intf.rd_en)
44              1                  131                      fifo_intf.underflow <= 1;
45                                                  else
46              1                  708                      fifo_intf.underflow <= 0;
47                                          end
48                                      end
49
50              1                 1103      always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51                                          if (!fifo_intf.rst_n) begin
52              1                  219              count <= 0;
53                                          end
54                                          else begin
55                                                  if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56              1                  443                      count <= count + 1;
57                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58              1                   77                      count <= count - 1;
59                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60              1                   15                      count <= count - 1;
61                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62              1                   30                      count <= count + 1;
63                                          end
64                                      end
65
66              1                  659      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67              1                  873      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68              1                  659      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69              1                  659      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

```
Total Node Count        =         10
Toggled Node Count      =         10
Untoggled Node Count    =          0

Toggle Coverage         =    100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

4.4 Code Coverage "seed4" Report

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.FIFO
================================================================================
```

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	25	25	0	100.00%

==========Branch Details==========

Branch Coverage for Design Unit work.FIFO

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			

```
------------------------------------IF Branch------------------------------------
    13                                  1319     Count coming in to IF
    13              1                    244        if (!fifo_intf.rst_n) begin
    18              1                    623        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                    452        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                   452     Count coming in to IF
    25              1                     96                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                    356                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                  1319     Count coming in to IF
    33              1                    244        if (!fifo_intf.rst_n) begin
    38              1                    243        else if (fifo_intf.rd_en && count != 0) begin
    42              1                    832        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                   832     Count coming in to IF
    43              1                    127                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                    705                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                  1122     Count coming in to IF
    51              1                    235        if (!fifo_intf.rst_n) begin
    54              1                    887        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                   887     Count coming in to IF
    55              1                    435                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                     67                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                     18                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                     30                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                          337     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                   647     Count coming in to IF
    66              1                     40     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                    607     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                   875     Count coming in to IF
    67              1                    338     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                    537     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                   647     Count coming in to IF
    68              1                     59     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                    588     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                   647     Count coming in to IF
    69              1                    121     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                    526     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%
```

```
Condition Coverage:
    Enabled Coverage                    Bins    Covered     Misses   Coverage
    ----------------                    ----    -------     ------   --------
    Conditions                            25         23          2     92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO —

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------Focused Condition View-------------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

        Input Term   Covered  Reason for no coverage   Hint
        ----------   -------  ----------------------   ----
  fifo_intf.wr_en          Y
      (count < 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  --------------------  -------------------------
  Row    1:          1  fifo_intf.wr_en_0      -
  Row    2:          1  fifo_intf.wr_en_1      (count < 8)
  Row    3:          1  (count < 8)_0          fifo_intf.wr_en
  Row    4:          1  (count < 8)_1          fifo_intf.wr_en
```

```
----------Focused Condition View----------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
    fifo_intf.full         N  '_0' not hit            Hit '_0'
  fifo_intf.wr_en          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:    ***0***  fifo_intf.full_0        fifo_intf.wr_en
  Row    2:          1  fifo_intf.full_1        fifo_intf.wr_en
  Row    3:          1  fifo_intf.wr_en_0      fifo_intf.full
  Row    4:          1  fifo_intf.wr_en_1      fifo_intf.full

----------Focused Condition View----------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
  fifo_intf.rd_en          Y
    (count != 0)           Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (count != 0)
  Row    3:          1  (count != 0)_0          fifo_intf.rd_en
  Row    4:          1  (count != 0)_1          fifo_intf.rd_en

----------Focused Condition View----------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
  fifo_intf.empty          N  '_0' not hit            Hit '_0'
  fifo_intf.rd_en          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:    ***0***  fifo_intf.empty_0       fifo_intf.rd_en
  Row    2:          1  fifo_intf.empty_1       fifo_intf.rd_en
  Row    3:          1  fifo_intf.rd_en_0       fifo_intf.empty
  Row    4:          1  fifo_intf.rd_en_1       fifo_intf.empty

----------Focused Condition View----------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
   fifo_intf.full          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       (~fifo_intf.full && fifo_intf.wr_en)
  Row    2:          1  fifo_intf.rd_en_1       -
  Row    3:          1  fifo_intf.wr_en_0       ~fifo_intf.rd_en
  Row    4:          1  fifo_intf.wr_en_1       (~fifo_intf.full && ~fifo_intf.rd_en)
  Row    5:          1  fifo_intf.full_0        (~fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:          1  fifo_intf.full_1        (~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line       57 Item    1  ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
  fifo_intf.empty          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ---------  ----------------------  --------------------------
  Row    1:          1  fifo_intf.rd_en_0       -
  Row    2:          1  fifo_intf.rd_en_1       (~fifo_intf.empty && ~fifo_intf.wr_en)
  Row    3:          1  fifo_intf.wr_en_0       (~fifo_intf.empty && fifo_intf.rd_en)
  Row    4:          1  fifo_intf.wr_en_1       fifo_intf.rd_en
  Row    5:          1  fifo_intf.empty_0       (fifo_intf.rd_en && ~fifo_intf.wr_en)
  Row    6:          1  fifo_intf.empty_1       (fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line       59 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
     ------------  --------  ----------------------  --------------
```

```
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
   fifo_intf.full          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       -
  Row    2:           1  fifo_intf.rd_en_1       (fifo_intf.full && fifo_intf.wr_en)
  Row    3:           1  fifo_intf.wr_en_0       fifo_intf.rd_en
  Row    4:           1  fifo_intf.wr_en_1       (fifo_intf.full && fifo_intf.rd_en)
  Row    5:           1  fifo_intf.full_0        (fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:           1  fifo_intf.full_1        (fifo_intf.rd_en && fifo_intf.wr_en)

------------------Focused Condition View-------------------
Line       61 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
  ----------  ----------  ------------------------  --------------
  fifo_intf.rd_en          Y
  fifo_intf.wr_en          Y
  fifo_intf.empty          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  fifo_intf.rd_en_0       -
  Row    2:           1  fifo_intf.rd_en_1       (fifo_intf.empty && fifo_intf.wr_en)
  Row    3:           1  fifo_intf.wr_en_0       fifo_intf.rd_en
  Row    4:           1  fifo_intf.wr_en_1       (fifo_intf.empty && fifo_intf.rd_en)
  Row    5:           1  fifo_intf.empty_0       (fifo_intf.rd_en && fifo_intf.wr_en)
  Row    6:           1  fifo_intf.empty_1       (fifo_intf.rd_en && fifo_intf.wr_en)

------------------Focused Condition View-------------------
Line       66 Item    1  (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
  ------------  ----------  ------------------------  --------------
  (count == 8)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  (count == 8)_0          -
  Row    2:           1  (count == 8)_1          -

------------------Focused Condition View-------------------
Line       67 Item    1  ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

       Input Term   Covered  Reason for no coverage   Hint
  ------------  ----------  ------------------------  --------------
    (count == 0)          Y
  fifo_intf.rst_n          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  (count == 0)_0          fifo_intf.rst_n
  Row    2:           1  (count == 0)_1          -
  Row    3:           1  fifo_intf.rst_n_0       ~(count == 0)
  Row    4:           1  fifo_intf.rst_n_1       ~(count == 0)

------------------Focused Condition View-------------------
Line       68 Item    1  (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

         Input Term   Covered  Reason for no coverage   Hint
  ----------------  ----------  ------------------------  --------------
  (count == (8 - 1))          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  (count == (8 - 1))_0    -
  Row    2:           1  (count == (8 - 1))_1    -

------------------Focused Condition View-------------------
Line       69 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
  ------------  ----------  ------------------------  --------------
  (count == 1)          Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ----------  ----------  ----------------------  --------------------------
  Row    1:           1  (count == 1)_0          -
  Row    2:           1  (count == 1)_1          -


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      28        28         0   100.00%
```

Statement Details

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1319	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	244	wr_ptr <= 0;
15	1	244	fifo_intf.wr_ack <= 0;
16	1	244	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	623	mem[wr_ptr] <= fifo_intf.data_in;
20	1	623	fifo_intf.wr_ack <= 1;
21	1	623	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	452	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	96	fifo_intf.overflow <= 1;
27			else
28	1	356	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	1319	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	244	rd_ptr <= 0;
35	1	244	fifo_intf.underflow <= 0;
36	1	244	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	243	fifo_intf.data_out <= mem[rd_ptr];
40	1	243	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	127	fifo_intf.underflow <= 1;
45			else
46	1	705	fifo_intf.underflow <= 0;
47			end
48			end
49			
50	1	1122	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51			if (!fifo_intf.rst_n) begin
52	1	235	count <= 0;
53			end
54			else begin
55			if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
56	1	435	count <= count + 1;
57			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
58	1	67	count <= count - 1;
59			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
60	1	18	count <= count - 1;
61			else if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
62	1	30	count <= count + 1;
63			end
64			end
65			
66	1	648	assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
67	1	876	assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
68	1	648	assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
69	1	648	assign fifo_intf.almostempty = (count == 1)? 1 : 0;

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

Toggle Details

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

```
Total Node Count     =         10
Toggled Node Count   =         10
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

4.5 Code Coverage "seed5" Report

```
Coverage Report by DU with details

================================================================================
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        25        25         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                           Count     Source
    ----         ----                           -----     ------
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                      1312     Count coming in to IF
    13              1                        231        if (!fifo_intf.rst_n) begin
    18              1                        593        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                        488        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                       488     Count coming in to IF
    25              1                        121                if (fifo_intf.full & fifo_intf.wr_en)
    27              1                        367                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                      1312     Count coming in to IF
    33              1                        231        if (!fifo_intf.rst_n) begin
    38              1                        220        else if (fifo_intf.rd_en && count != 0) begin
    42              1                        861        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                       861     Count coming in to IF
    43              1                        133                if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                        728                else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                      1070     Count coming in to IF
    51              1                        225        if (!fifo_intf.rst_n) begin
    54              1                        845        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                       845     Count coming in to IF
    55              1                        422                if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                         62                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                         17                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                         30                else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                              314     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                       627     Count coming in to IF
    66              1                         41     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                        586     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                       841     Count coming in to IF
    67              1                        324     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                        517     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                       627     Count coming in to IF
    68              1                         56     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                        571     assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                       627     Count coming in to IF
    69              1                        116     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                        511     assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Branch totals: 2 hits of 2 branches = 100.00%

Condition Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Conditions	25	23	2	92.00%

==========Condition Details==========

Condition Coverage for Design Unit work.FIFO —

File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv

----------Focused Condition View----------
Line 18 Item 1 (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.wr_en	Y		
(count < 8)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.wr_en_0	-
Row 2:	1	fifo_intf.wr_en_1	(count < 8)
Row 3:	1	(count < 8)_0	fifo_intf.wr_en
Row 4:	1	(count < 8)_1	fifo_intf.wr_en

----------Focused Condition View----------
Line 25 Item 1 (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.full	N	'_0' not hit	Hit '_0'
fifo_intf.wr_en	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	fifo_intf.full_0	fifo_intf.wr_en
Row 2:	1	fifo_intf.full_1	fifo_intf.wr_en
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.full
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.full

----------Focused Condition View----------
Line 38 Item 1 (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
(count != 0)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	-
Row 2:	1	fifo_intf.rd_en_1	(count != 0)
Row 3:	1	(count != 0)_0	fifo_intf.rd_en
Row 4:	1	(count != 0)_1	fifo_intf.rd_en

----------Focused Condition View----------
Line 43 Item 1 (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.empty	N	'_0' not hit	Hit '_0'
fifo_intf.rd_en	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	fifo_intf.empty_0	fifo_intf.rd_en
Row 2:	1	fifo_intf.empty_1	fifo_intf.rd_en
Row 3:	1	fifo_intf.rd_en_0	fifo_intf.empty
Row 4:	1	fifo_intf.rd_en_1	fifo_intf.empty

----------Focused Condition View----------
Line 55 Item 1 ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	1	fifo_intf.rd_en_1	-
Row 3:	1	fifo_intf.wr_en_0	~fifo_intf.rd_en

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 4:	1	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	1	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

----------Focused Condition View----------
Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	1	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	fifo_intf.rd_en_0	–
Row 2:	1	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	1	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	1	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	1	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	1	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

----------Focused Condition View----------
Line 66 Item 1 (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 8)_0	–
Row 2:	1	(count == 8)_1	–

----------Focused Condition View----------
Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	1	(count == 0)_0	fifo_intf.rst_n
Row 2:	1	(count == 0)_1	–
Row 3:	1	fifo_intf.rst_n_0	~(count == 0)
Row 4:	1	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))

Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == (8 - 1))_0	-
Row 2:	1	(count == (8 - 1))_1	-

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(count == 1)_0	-
Row 2:	1	(count == 1)_1	-

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO ---

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	1312	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	231	wr_ptr <= 0;
15	1	231	fifo_intf.wr_ack <= 0;
16	1	231	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	593	mem[wr_ptr] <= fifo_intf.data_in;
20	1	593	fifo_intf.wr_ack <= 1;
21	1	593	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	488	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	121	fifo_intf.overflow <= 1;
27			else
28	1	367	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	1312	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	231	rd_ptr <= 0;
35	1	231	fifo_intf.underflow <= 0;
36	1	231	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	220	fifo_intf.data_out <= mem[rd_ptr];
40	1	220	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	133	fifo_intf.underflow <= 1;
45			else
46	1	728	fifo_intf.underflow <= 0;
47			end
48			end
49			
50	1	1070	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
51			if (!fifo_intf.rst_n) begin
52	1	225	count <= 0;
53			end
54			else begin
55			if (({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu

```
    56              1                    422                    count <= count + 1;
    57                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    58              1                     62                    count <= count - 1;
    59                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    60              1                     17                    count <= count - 1;
    61                                                  else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    62              1                     30                    count <= count + 1;
    63                                              end
    64                                          end
    65
    66              1                    628      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    67              1                    842      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    68              1                    628      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    69              1                    628      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
```

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for Design Unit work.FIFO

Node	1H->0L	0L->1H	"Coverage"
count[0-3]	1	1	100.00
rd_ptr[0-2]	1	1	100.00
wr_ptr[0-2]	1	1	100.00

```
Total Node Count        =         10
Toggled Node Count      =         10
Untoggled Node Count    =          0

Toggle Coverage         =    100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

5 Waveform

5.1 Waveform & Transcript "seed1" Report

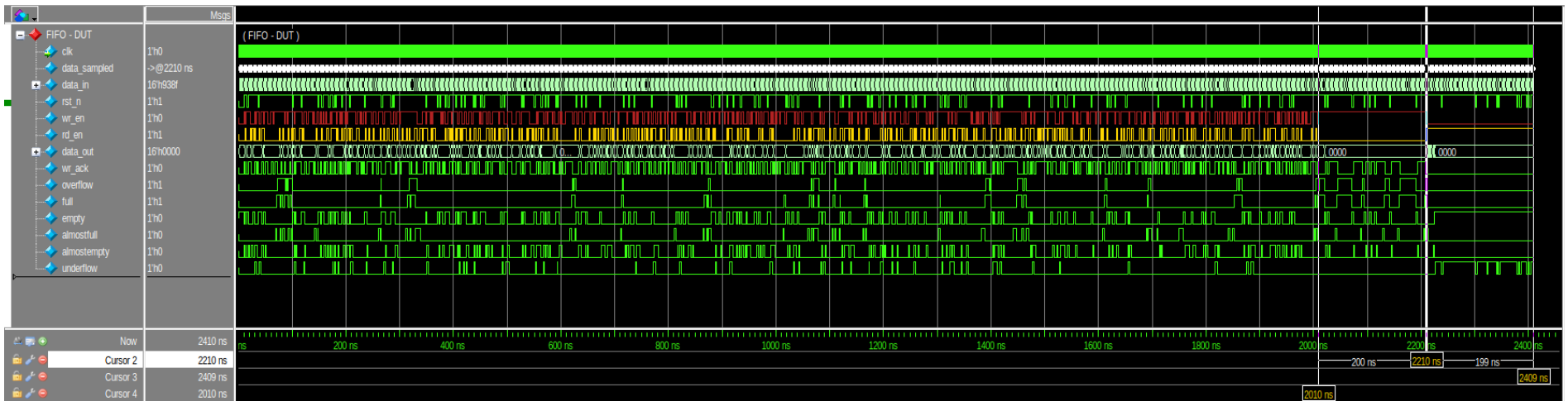


Figure 6: simulation waveform "seed1"

```
# (C) 2007-2013 Cadence Design Systems, Inc.
# (C) 2006-2013 Synopsys, Inc.
# (C) 2011-2013 Cypress Semiconductor Corp.
# ------------------------------------------------------------
#
#   ***********       IMPORTANT RELEASE NOTES         ************
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_NO_DEPRECATED undefined.
#   See http://www.eda.org/svdb/view.php?id=3313 for more details.
#
#   You are using a version of the UVM library that has been compiled
#   with `UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
#   See http://www.eda.org/svdb/view.php?id=3770 for more details.
#
#       (Specify +UVM_NO_RELNOTES to turn off this notice)
#
# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(277) @ 0: reporter [Questa UVM] QUESTA_UVM-1.2.3
# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(278) @ 0: reporter [Questa UVM]  questa_uvm::init(+struct)
# UVM_INFO @ 0: reporter [RNTST] Running test FIFO_test...
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv(35) @ 0: uvm_test_top [run_phase] Inside the FIFO test.
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 2410: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    8
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [REPORT]     3
# [RNTST]     1
# [TEST_DONE]     1
# [run_phase]     1
# ** Note: $finish    : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2410 ns  Iteration: 61  Instance: /top
# End time: 21:40:41 on May 01,2025, Elapsed time: 0:00:07
# Errors: 0, Warnings: 0

Running simulation with seed 1111
Reading pref.tcl
```

Figure 7: Transcript : all test cases passed "seed1"

5.2 Waveform & Transcript "seed2" Report

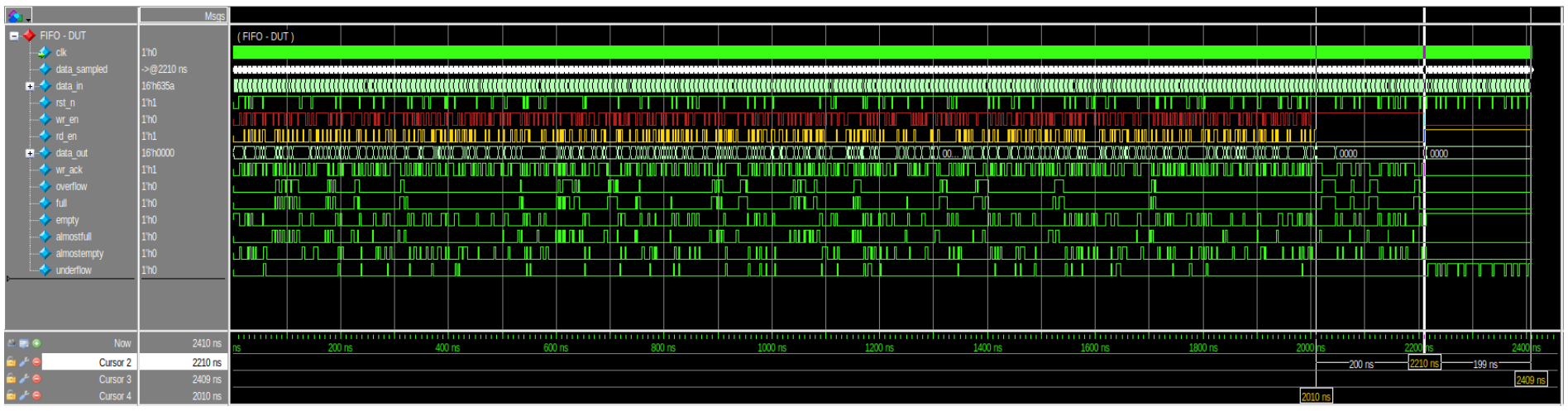


Figure 8: simulation waveform "seed2"

```
Running simulation with seed 1111
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:51:22 on May 01,2025
vcover report FIFO_seed1111.ucdb -details -annotate -all -output code_coverage_rpt_seed1111.txt -du=FIFO
End time: 21:51:22 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:51:22 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1111.txt FIFO_seed1111.ucdb
End time: 21:51:22 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 1511
Reading pref.tcl
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    8
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [REPORT]     3
# [RNTST]     1
# [TEST_DONE]     1
# [run_phase]     1
# ** Note: $finish    : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2410 ns  Iteration: 61  Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
```

Figure 9: Transcript : all test cases passed "seed2"

5.3 Waveform & Transcript "seed3" Report

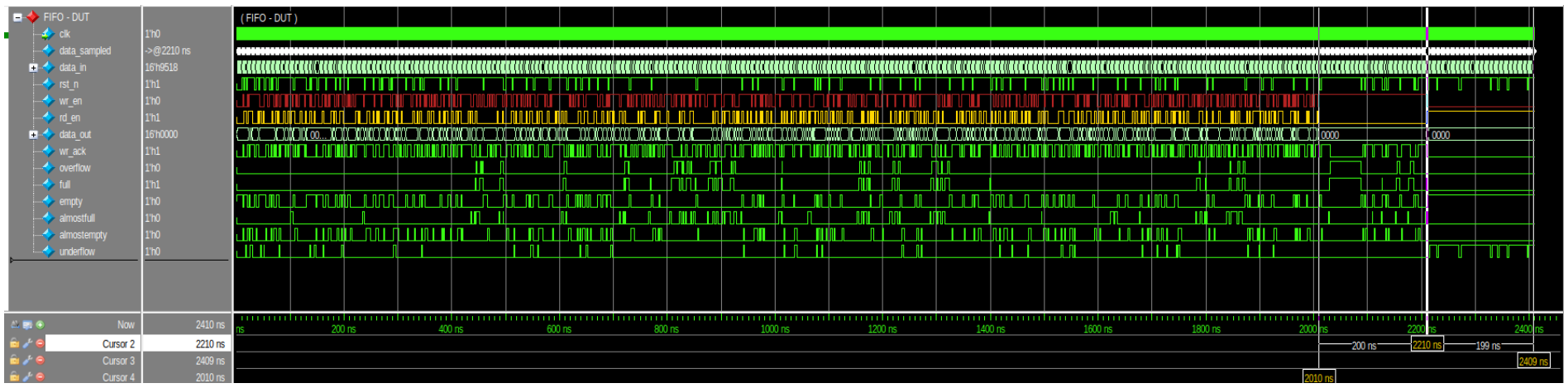


Figure 10: simulation waveform "seed3"

```
Running simulation with seed 1511
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:55:40 on May 01,2025
vcover report FIFO_seed1511.ucdb -details -annotate -all -output code_coverage_rpt_seed1511.txt -du=FIFO
End time: 21:55:40 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:55:40 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed1511.txt FIFO_seed1511.ucdb
End time: 21:55:40 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2515
Reading pref.tcl
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    8
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [REPORT]     3
# [RNTST]     1
# [TEST_DONE]     1
# [run_phase]     1
# ** Note: $finish    : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2410 ns  Iteration: 61  Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
```

Figure 11: Transcript : all test cases passed "seed3"

5.4 Waveform & Transcript "seed4" Report

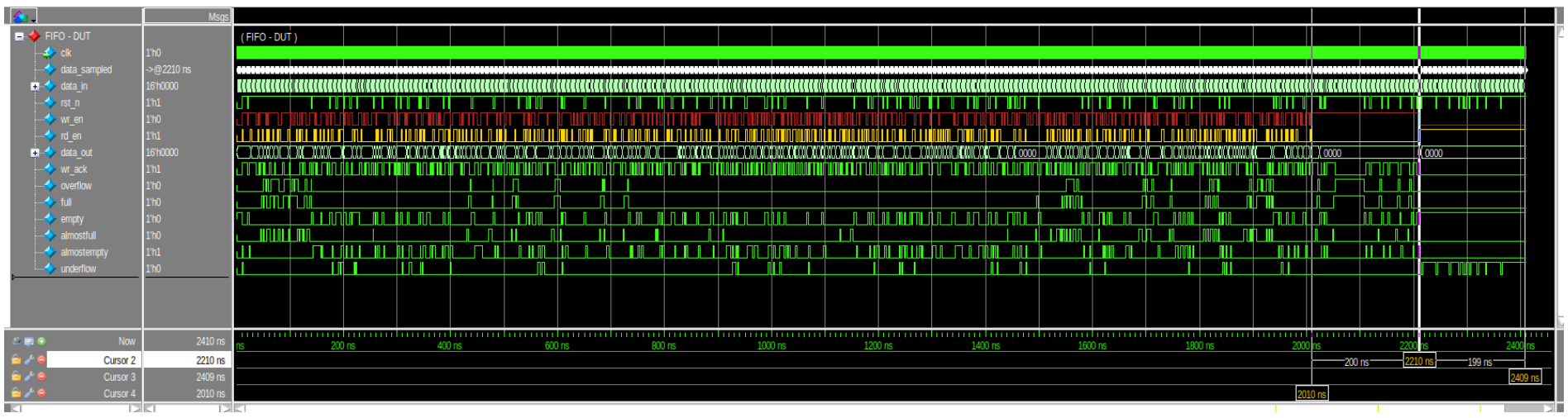


Figure 12: simulation waveform "seed4"

```
Running simulation with seed 2515
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:58:28 on May 01,2025
vcover report FIFO_seed2515.ucdb -details -annotate -all -output code_coverage_rpt_seed2515.txt -du=FIFO
End time: 21:58:28 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 21:58:28 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2515.txt FIFO_seed2515.ucdb
End time: 21:58:28 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 2236
Reading pref.tcl
```

```
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    8
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [REPORT]     3
# [RNTST]     1
# [TEST_DONE]     1
# [run_phase]     1
# ** Note: $finish    : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2410 ns  Iteration: 61  Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430

VSIM 4>
```

Figure 13: Transcript : all test cases passed ”seed4”

5.5 Waveform & Transcript ”seed5” Report

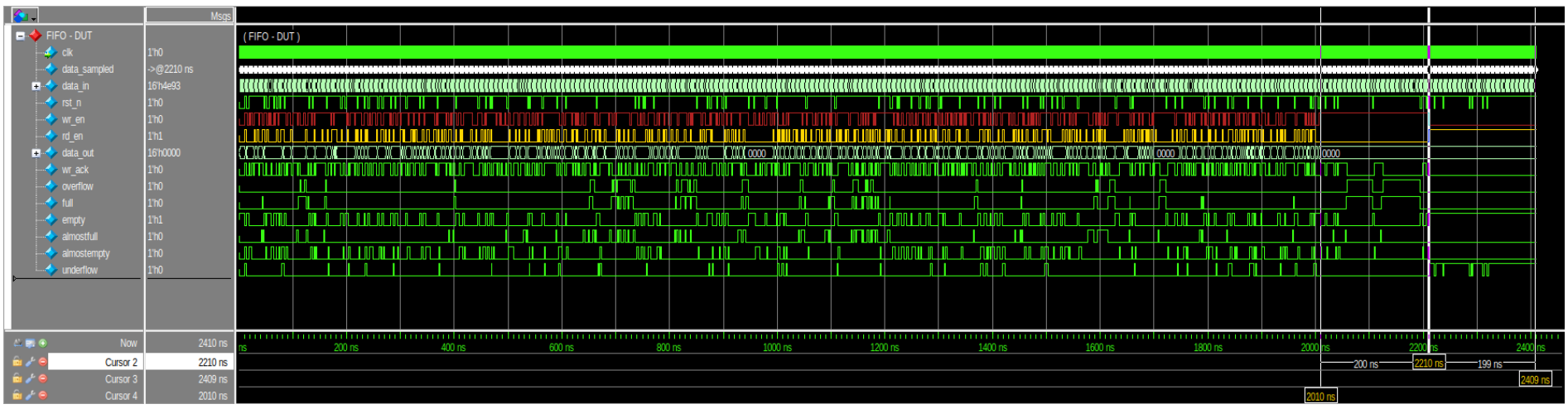


Figure 14: simulation waveform ”seed5”

```
Running simulation with seed 2236
Reading pref.tcl
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:00:32 on May 01,2025
vcover report FIFO_seed2236.ucdb -details -annotate -all -output code_coverage_rpt_seed2236.txt -du=FIFO
End time: 22:00:32 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:00:32 on May 01,2025
vcover report -details -cvg -output functional_coverage_report_seed2236.txt FIFO_seed2236.ucdb
End time: 22:00:32 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

Running simulation with seed 5215
Reading pref.tcl
```

```
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(168) @ 2410: uvm_test_top.env.sb [REPORT] Test Summary:
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(169) @ 2410: uvm_test_top.env.sb [REPORT] Total correct transactions: 1205
# UVM_INFO /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv(170) @ 2410: uvm_test_top.env.sb [REPORT] Total mismatches: 0
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :    8
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [Questa UVM]     2
# [REPORT]     3
# [RNTST]     1
# [TEST_DONE]     1
# [run_phase]     1
# ** Note: $finish    : /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#    Time: 2410 ns  Iteration: 61  Instance: /top
# Break in Task uvm_pkg/uvm_root::run_test at /usr/local/questasim/linux_x86_64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh line 430
```

Figure 15: Transcript : all test cases passed ”seed5”

```
Merging coverage from all seed runs
vcover merge merged.ucdb FIFO_seed*.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:46 on May 01,2025
vcover merge merged.ucdb FIFO_seed1111.ucdb FIFO_seed1511.ucdb FIFO_seed2236.ucdb FIFO_seed2515.ucdb FIFO_seed5215.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Merging file FIFO_seed1111.ucdb
Merging file FIFO_seed1511.ucdb
Merging file FIFO_seed2236.ucdb
Merging file FIFO_seed2515.ucdb
Merging file FIFO_seed5215.ucdb
Writing merged result to merged.ucdb

End time: 22:02:46 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -c -do "coverage open merged.ucdb; coverage report -output merged_coverage_report.txt -srcfile=* -detail; quit -f"
Reading pref.tcl

# 2021.2_1

# coverage open merged.ucdb
# coverage read -dataset merged merged.ucdb
# merged.ucdb opened as coverage dataset "merged"
#  coverage report -output merged_coverage_report.txt -srcfile=* -detail
#  quit -f
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:48 on May 01,2025
vcover report merged.ucdb -details -annotate -all -output merged_code_coverage_rpt.txt -du=FIFO
End time: 22:02:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
QuestaSim-64 vcover 2021.2_1 Coverage Utility 2021.05 May 15 2021
Start time: 22:02:48 on May 01,2025
vcover report -details -cvg -output merged_functional_coverage_report.txt merged.ucdb
End time: 22:02:48 on May 01,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Coverage merged to merged.ucdb and reports saved
```

Figure 16: Merge seed

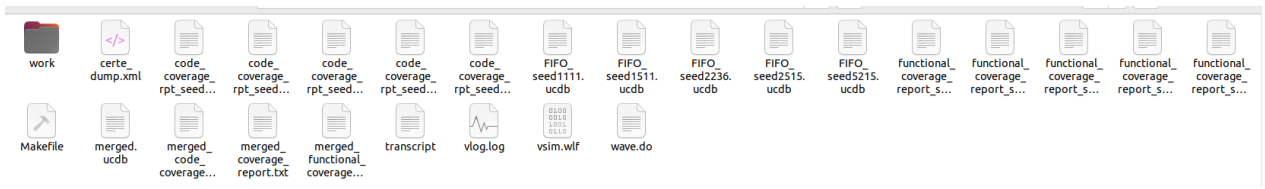


Figure 17: generated files *.ucdb

6.1 Functional Coverage "Merged" Report

Coverage Report by instance with details

```
================================================================================
=== Instance: /FIFO_coverage_pkg
=== Design Unit: work.FIFO_coverage_pkg
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses    19        na        na        na
            Covergroup Bins   190       190         0   100.00%
```

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	–	Covered
covered/total bins:	190	190	–	
missing/total bins:	0	190	–	
% Hit:	100.00%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	644	1	–	Covered
bin auto[1]	5381	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	976	1	–	Covered
bin auto[1024:2047]	57	1	–	Covered
bin auto[2048:3071]	62	1	–	Covered
bin auto[3072:4095]	64	1	–	Covered
bin auto[4096:5119]	73	1	–	Covered
bin auto[5120:6143]	77	1	–	Covered
bin auto[6144:7167]	60	1	–	Covered
bin auto[7168:8191]	75	1	–	Covered
bin auto[8192:9215]	66	1	–	Covered
bin auto[9216:10239]	62	1	–	Covered

bin auto[10240:11263]	60	1	–	Covered
bin auto[11264:12287]	59	1	–	Covered
bin auto[12288:13311]	64	1	–	Covered
bin auto[13312:14335]	62	1	–	Covered
bin auto[14336:15359]	66	1	–	Covered
bin auto[15360:16383]	53	1	–	Covered
bin auto[16384:17407]	66	1	–	Covered
bin auto[17408:18431]	58	1	–	Covered
bin auto[18432:19455]	79	1	–	Covered
bin auto[19456:20479]	68	1	–	Covered
bin auto[20480:21503]	54	1	–	Covered
bin auto[21504:22527]	65	1	–	Covered
bin auto[22528:23551]	72	1	–	Covered
bin auto[23552:24575]	68	1	–	Covered
bin auto[24576:25599]	66	1	–	Covered
bin auto[25600:26623]	66	1	–	Covered
bin auto[26624:27647]	69	1	–	Covered
bin auto[27648:28671]	78	1	–	Covered
bin auto[28672:29695]	74	1	–	Covered
bin auto[29696:30719]	66	1	–	Covered
bin auto[30720:31743]	61	1	–	Covered
bin auto[31744:32767]	64	1	–	Covered
bin auto[32768:33791]	77	1	–	Covered
bin auto[33792:34815]	61	1	–	Covered
bin auto[34816:35839]	72	1	–	Covered
bin auto[35840:36863]	68	1	–	Covered
bin auto[36864:37887]	75	1	–	Covered
bin auto[37888:38911]	70	1	–	Covered
bin auto[38912:39935]	62	1	–	Covered
bin auto[39936:40959]	55	1	–	Covered
bin auto[40960:41983]	73	1	–	Covered
bin auto[41984:43007]	60	1	–	Covered
bin auto[43008:44031]	70	1	–	Covered
bin auto[44032:45055]	69	1	–	Covered
bin auto[45056:46079]	62	1	–	Covered
bin auto[46080:47103]	63	1	–	Covered
bin auto[47104:48127]	62	1	–	Covered
bin auto[48128:49151]	73	1	–	Covered
bin auto[49152:50175]	62	1	–	Covered
bin auto[50176:51199]	65	1	–	Covered
bin auto[51200:52223]	69	1	–	Covered
bin auto[52224:53247]	70	1	–	Covered
bin auto[53248:54271]	51	1	–	Covered
bin auto[54272:55295]	83	1	–	Covered
bin auto[55296:56319]	70	1	–	Covered
bin auto[56320:57343]	60	1	–	Covered
bin auto[57344:58367]	54	1	–	Covered
bin auto[58368:59391]	69	1	–	Covered
bin auto[59392:60415]	76	1	–	Covered
bin auto[60416:61439]	67	1	–	Covered
bin auto[61440:62463]	75	1	–	Covered
bin auto[62464:63487]	76	1	–	Covered
bin auto[63488:64511]	55	1	–	Covered
bin auto[64512:65535]	941	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3991	1	–	Covered
bin auto[1]	2034	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2017	1	–	Covered
bin auto[1]	4008	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	3334	1	–	Covered
bin auto[1024:2047]	36	1	–	Covered
bin auto[2048:3071]	13	1	–	Covered
bin auto[3072:4095]	44	1	–	Covered
bin auto[4096:5119]	53	1	–	Covered
bin auto[5120:6143]	57	1	–	Covered
bin auto[6144:7167]	48	1	–	Covered
bin auto[7168:8191]	50	1	–	Covered
bin auto[8192:9215]	43	1	–	Covered
bin auto[9216:10239]	27	1	–	Covered
bin auto[10240:11263]	44	1	–	Covered
bin auto[11264:12287]	44	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	34	1	–	Covered
bin auto[14336:15359]	25	1	–	Covered
bin auto[15360:16383]	21	1	–	Covered
bin auto[16384:17407]	17	1	–	Covered
bin auto[17408:18431]	19	1	–	Covered
bin auto[18432:19455]	51	1	–	Covered
bin auto[19456:20479]	25	1	–	Covered
bin auto[20480:21503]	39	1	–	Covered
bin auto[21504:22527]	28	1	–	Covered

bin auto[22528:23551]	9	1	–	Covered
bin auto[23552:24575]	21	1	–	Covered
bin auto[24576:25599]	37	1	–	Covered
bin auto[25600:26623]	38	1	–	Covered
bin auto[26624:27647]	35	1	–	Covered
bin auto[27648:28671]	52	1	–	Covered
bin auto[28672:29695]	44	1	–	Covered
bin auto[29696:30719]	31	1	–	Covered
bin auto[30720:31743]	29	1	–	Covered
bin auto[31744:32767]	25	1	–	Covered
bin auto[32768:33791]	46	1	–	Covered
bin auto[33792:34815]	38	1	–	Covered
bin auto[34816:35839]	41	1	–	Covered
bin auto[35840:36863]	37	1	–	Covered
bin auto[36864:37887]	26	1	–	Covered
bin auto[37888:38911]	32	1	–	Covered
bin auto[38912:39935]	50	1	–	Covered
bin auto[39936:40959]	30	1	–	Covered
bin auto[40960:41983]	31	1	–	Covered
bin auto[41984:43007]	33	1	–	Covered
bin auto[43008:44031]	45	1	–	Covered
bin auto[44032:45055]	29	1	–	Covered
bin auto[45056:46079]	26	1	–	Covered
bin auto[46080:47103]	47	1	–	Covered
bin auto[47104:48127]	11	1	–	Covered
bin auto[48128:49151]	32	1	–	Covered
bin auto[49152:50175]	28	1	–	Covered
bin auto[50176:51199]	25	1	–	Covered
bin auto[51200:52223]	61	1	–	Covered
bin auto[52224:53247]	22	1	–	Covered
bin auto[53248:54271]	18	1	–	Covered
bin auto[54272:55295]	47	1	–	Covered
bin auto[55296:56319]	60	1	–	Covered
bin auto[56320:57343]	41	1	–	Covered
bin auto[57344:58367]	17	1	–	Covered
bin auto[58368:59391]	44	1	–	Covered
bin auto[59392:60415]	82	1	–	Covered
bin auto[60416:61439]	31	1	–	Covered
bin auto[61440:62463]	52	1	–	Covered
bin auto[62464:63487]	32	1	–	Covered
bin auto[63488:64511]	21	1	–	Covered
bin auto[64512:65535]	484	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2943	1	–	Covered
bin auto[1]	3082	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5457	1	–	Covered
bin auto[1]	568	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5338	1	–	Covered
bin auto[1]	687	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4632	1	–	Covered
bin auto[1]	1393	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5570	1	–	Covered
bin auto[1]	455	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5044	1	–	Covered
bin auto[1]	981	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5306	1	–	Covered
bin auto[1]	719	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	892	1	–	Covered
bin <auto[1],auto[1],auto[0]>	216	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2190	1	–	Covered

bin <auto[0],auto[1],auto[0]>	710	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	613	1	–	Covered
bin <auto[0],auto[0],auto[1]>	74	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1108	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2287	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1017	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	126	1	–	Covered
bin <auto[1],auto[0],auto[1]>	667	1	–	Covered
bin <auto[1],auto[1],auto[0]>	982	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2601	1	–	Covered
bin <auto[1],auto[0],auto[0]>	259	1	–	Covered
bin <auto[0],auto[0],auto[0]>	790	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	600		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	171	1	–	Covered
bin <auto[1],auto[0],auto[1]>	37	1	–	Covered
bin <auto[1],auto[1],auto[0]>	937	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2737	1	–	Covered
bin <auto[1],auto[0],auto[0]>	889	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1007	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	247		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	350	1	–	Covered
bin <auto[1],auto[1],auto[0]>	758	1	–	Covered
bin <auto[0],auto[1],auto[1]>	401	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2499	1	–	Covered
bin <auto[1],auto[0],auto[0]>	867	1	–	Covered
bin <auto[0],auto[0],auto[0]>	920	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	230		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	999	1	–	Covered
bin <auto[0],auto[1],auto[1]>	459	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2441	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	208	1	–	Covered
bin <auto[1],auto[0],auto[1]>	511	1	–	Covered
bin <auto[1],auto[1],auto[0]>	900	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2900	1	–	Covered
bin <auto[1],auto[0],auto[0]>	415	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	–	Covered
covered/total bins:	190	190	–	

missing/total bins:	0	190	–	
% Hit:	100.00%	100	–	
Coverpoint rst_n_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	644	1	–	Covered
bin auto[1]	5381	1	–	Covered
Coverpoint data_in_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	976	1	–	Covered
bin auto[1024:2047]	57	1	–	Covered
bin auto[2048:3071]	62	1	–	Covered
bin auto[3072:4095]	64	1	–	Covered
bin auto[4096:5119]	73	1	–	Covered
bin auto[5120:6143]	77	1	–	Covered
bin auto[6144:7167]	60	1	–	Covered
bin auto[7168:8191]	75	1	–	Covered
bin auto[8192:9215]	66	1	–	Covered
bin auto[9216:10239]	62	1	–	Covered
bin auto[10240:11263]	60	1	–	Covered
bin auto[11264:12287]	59	1	–	Covered
bin auto[12288:13311]	64	1	–	Covered
bin auto[13312:14335]	62	1	–	Covered
bin auto[14336:15359]	66	1	–	Covered
bin auto[15360:16383]	53	1	–	Covered
bin auto[16384:17407]	66	1	–	Covered
bin auto[17408:18431]	58	1	–	Covered
bin auto[18432:19455]	79	1	–	Covered
bin auto[19456:20479]	68	1	–	Covered
bin auto[20480:21503]	54	1	–	Covered
bin auto[21504:22527]	65	1	–	Covered
bin auto[22528:23551]	72	1	–	Covered
bin auto[23552:24575]	68	1	–	Covered
bin auto[24576:25599]	66	1	–	Covered
bin auto[25600:26623]	66	1	–	Covered
bin auto[26624:27647]	69	1	–	Covered
bin auto[27648:28671]	78	1	–	Covered
bin auto[28672:29695]	74	1	–	Covered
bin auto[29696:30719]	66	1	–	Covered
bin auto[30720:31743]	61	1	–	Covered
bin auto[31744:32767]	64	1	–	Covered
bin auto[32768:33791]	77	1	–	Covered
bin auto[33792:34815]	61	1	–	Covered
bin auto[34816:35839]	72	1	–	Covered
bin auto[35840:36863]	68	1	–	Covered
bin auto[36864:37887]	75	1	–	Covered
bin auto[37888:38911]	70	1	–	Covered
bin auto[38912:39935]	62	1	–	Covered
bin auto[39936:40959]	55	1	–	Covered
bin auto[40960:41983]	73	1	–	Covered
bin auto[41984:43007]	60	1	–	Covered
bin auto[43008:44031]	70	1	–	Covered
bin auto[44032:45055]	69	1	–	Covered
bin auto[45056:46079]	62	1	–	Covered
bin auto[46080:47103]	63	1	–	Covered
bin auto[47104:48127]	62	1	–	Covered
bin auto[48128:49151]	73	1	–	Covered
bin auto[49152:50175]	62	1	–	Covered
bin auto[50176:51199]	65	1	–	Covered
bin auto[51200:52223]	69	1	–	Covered
bin auto[52224:53247]	70	1	–	Covered
bin auto[53248:54271]	51	1	–	Covered
bin auto[54272:55295]	83	1	–	Covered
bin auto[55296:56319]	70	1	–	Covered
bin auto[56320:57343]	60	1	–	Covered
bin auto[57344:58367]	54	1	–	Covered
bin auto[58368:59391]	69	1	–	Covered
bin auto[59392:60415]	76	1	–	Covered
bin auto[60416:61439]	67	1	–	Covered
bin auto[61440:62463]	75	1	–	Covered
bin auto[62464:63487]	76	1	–	Covered
bin auto[63488:64511]	55	1	–	Covered
bin auto[64512:65535]	941	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3991	1	–	Covered
bin auto[1]	2034	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2017	1	–	Covered
bin auto[1]	4008	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	

bin auto[0:1023]	3334	1	–	Covered
bin auto[1024:2047]	36	1	–	Covered
bin auto[2048:3071]	13	1	–	Covered
bin auto[3072:4095]	44	1	–	Covered
bin auto[4096:5119]	53	1	–	Covered
bin auto[5120:6143]	57	1	–	Covered
bin auto[6144:7167]	48	1	–	Covered
bin auto[7168:8191]	50	1	–	Covered
bin auto[8192:9215]	43	1	–	Covered
bin auto[9216:10239]	27	1	–	Covered
bin auto[10240:11263]	44	1	–	Covered
bin auto[11264:12287]	44	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	34	1	–	Covered
bin auto[14336:15359]	25	1	–	Covered
bin auto[15360:16383]	21	1	–	Covered
bin auto[16384:17407]	17	1	–	Covered
bin auto[17408:18431]	19	1	–	Covered
bin auto[18432:19455]	51	1	–	Covered
bin auto[19456:20479]	25	1	–	Covered
bin auto[20480:21503]	39	1	–	Covered
bin auto[21504:22527]	28	1	–	Covered
bin auto[22528:23551]	9	1	–	Covered
bin auto[23552:24575]	21	1	–	Covered
bin auto[24576:25599]	37	1	–	Covered
bin auto[25600:26623]	38	1	–	Covered
bin auto[26624:27647]	35	1	–	Covered
bin auto[27648:28671]	52	1	–	Covered
bin auto[28672:29695]	44	1	–	Covered
bin auto[29696:30719]	31	1	–	Covered
bin auto[30720:31743]	29	1	–	Covered
bin auto[31744:32767]	25	1	–	Covered
bin auto[32768:33791]	46	1	–	Covered
bin auto[33792:34815]	38	1	–	Covered
bin auto[34816:35839]	41	1	–	Covered
bin auto[35840:36863]	37	1	–	Covered
bin auto[36864:37887]	26	1	–	Covered
bin auto[37888:38911]	32	1	–	Covered
bin auto[38912:39935]	50	1	–	Covered
bin auto[39936:40959]	30	1	–	Covered
bin auto[40960:41983]	31	1	–	Covered
bin auto[41984:43007]	33	1	–	Covered
bin auto[43008:44031]	45	1	–	Covered
bin auto[44032:45055]	29	1	–	Covered
bin auto[45056:46079]	26	1	–	Covered
bin auto[46080:47103]	47	1	–	Covered
bin auto[47104:48127]	11	1	–	Covered
bin auto[48128:49151]	32	1	–	Covered
bin auto[49152:50175]	28	1	–	Covered
bin auto[50176:51199]	25	1	–	Covered
bin auto[51200:52223]	61	1	–	Covered
bin auto[52224:53247]	22	1	–	Covered
bin auto[53248:54271]	18	1	–	Covered
bin auto[54272:55295]	47	1	–	Covered
bin auto[55296:56319]	60	1	–	Covered
bin auto[56320:57343]	41	1	–	Covered
bin auto[57344:58367]	17	1	–	Covered
bin auto[58368:59391]	44	1	–	Covered
bin auto[59392:60415]	82	1	–	Covered
bin auto[60416:61439]	31	1	–	Covered
bin auto[61440:62463]	52	1	–	Covered
bin auto[62464:63487]	32	1	–	Covered
bin auto[63488:64511]	21	1	–	Covered
bin auto[64512:65535]	484	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2943	1	–	Covered
bin auto[1]	3082	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5457	1	–	Covered
bin auto[1]	568	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5338	1	–	Covered
bin auto[1]	687	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4632	1	–	Covered
bin auto[1]	1393	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	

bin auto[0]	5570	1	–	Covered
bin auto[1]	455	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5044	1	–	Covered
bin auto[1]	981	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5306	1	–	Covered
bin auto[1]	719	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	892	1	–	Covered
bin <auto[1],auto[1],auto[0]>	216	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2190	1	–	Covered
bin <auto[0],auto[1],auto[0]>	710	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	613	1	–	Covered
bin <auto[0],auto[0],auto[1]>	74	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1108	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2287	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1017	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	126	1	–	Covered
bin <auto[1],auto[0],auto[1]>	667	1	–	Covered
bin <auto[1],auto[1],auto[0]>	982	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2601	1	–	Covered
bin <auto[1],auto[0],auto[0]>	259	1	–	Covered
bin <auto[0],auto[0],auto[0]>	790	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	600		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	171	1	–	Covered
bin <auto[1],auto[0],auto[1]>	37	1	–	Covered
bin <auto[1],auto[1],auto[0]>	937	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2737	1	–	Covered
bin <auto[1],auto[0],auto[0]>	889	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1007	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	247		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	350	1	–	Covered
bin <auto[1],auto[1],auto[0]>	758	1	–	Covered
bin <auto[0],auto[1],auto[1]>	401	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2499	1	–	Covered
bin <auto[1],auto[0],auto[0]>	867	1	–	Covered
bin <auto[0],auto[0],auto[0]>	920	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	230		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	999	1	–	Covered
bin <auto[0],auto[1],auto[1]>	459	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2441	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				

```
        ignore_bin w_en_nactv_wr_ack                    0                      -    ZERO
    Cross underflow_cross                             100.00%          100     -    Covered
        covered/total bins:                             6                6     -
        missing/total bins:                             0                6     -
        % Hit:                                        100.00%          100     -
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1],auto[1]>             208              1       -    Covered
            bin <auto[1],auto[0],auto[1]>             511              1       -    Covered
            bin <auto[1],auto[1],auto[0]>             900              1       -    Covered
            bin <auto[0],auto[1],auto[0]>             2900             1       -    Covered
            bin <auto[1],auto[0],auto[0]>             415              1       -    Covered
            bin <auto[0],auto[0],auto[0]>             1091             1       -    Covered
        Illegal and Ignore Bins:
            ignore_bin r_en_nactv_wr_ack              0                      -    ZERO

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1

Total Coverage By Instance (filtered view): 100.00%
```

6.2 Code Coverage "Merged" Report

```
Coverage Report by DU with details

================================================================================
=== Design Unit: work.FIFO
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits      Misses  Coverage
    ----------------              ----      ----      ------  --------
    Branches                        25        25           0  100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.FIFO

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
------------------------------------IF Branch------------------------------------
    13                                     6587     Count coming in to IF
    13              1                      1206        if (!fifo_intf.rst_n) begin
    18              1                      3082        else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
    23              1                      2299        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                     2299     Count coming in to IF
    25              1                       501                 if (fifo_intf.full & fifo_intf.wr_en)
    27              1                      1798                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                     6587     Count coming in to IF
    33              1                      1206        if (!fifo_intf.rst_n) begin
    38              1                      1157        else if (fifo_intf.rd_en && count != 0) begin
    42              1                      4224        else begin
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                     4224     Count coming in to IF
    43              1                       660                 if (fifo_intf.empty & fifo_intf.rd_en)
    45              1                      3564                 else
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                     5557     Count coming in to IF
    51              1                      1166        if (!fifo_intf.rst_n) begin
    54              1                      4391        else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                     4391     Count coming in to IF
    55              1                      2190                 if      ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    57              1                       336                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    59              1                        90                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    61              1                       161                 else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
                                           1614     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                     3267     Count coming in to IF
    66              1                       202     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    66              2                      3065     assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                     4391     Count coming in to IF
    67              1                      1691     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    67              2                      2700     assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
```

```
    68                                  3267      Count coming in to IF
    68              1                    290      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    68              2                   2977      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                  3267      Count coming in to IF
    69              1                    621      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
    69              2                   2646      assign fifo_intf.almostempty = (count == 1)? 1 : 0;
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for Design Unit work.FIFO --

  File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----
  fifo_intf.wr_en        Y
     (count < 8)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          5  fifo_intf.wr_en_0      -
  Row    2:          5  fifo_intf.wr_en_1      (count < 8)
  Row    3:          5  (count < 8)_0          fifo_intf.wr_en
  Row    4:          5  (count < 8)_1          fifo_intf.wr_en

----------------Focused Condition View----------------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----
   fifo_intf.full         N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.full_0      fifo_intf.wr_en
  Row    2:          5  fifo_intf.full_1      fifo_intf.wr_en
  Row    3:          5  fifo_intf.wr_en_0     fifo_intf.full
  Row    4:          5  fifo_intf.wr_en_1     fifo_intf.full

----------------Focused Condition View----------------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----
  fifo_intf.rd_en        Y
    (count != 0)         Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:          5  fifo_intf.rd_en_0      -
  Row    2:          5  fifo_intf.rd_en_1      (count != 0)
  Row    3:          5  (count != 0)_0          fifo_intf.rd_en
  Row    4:          5  (count != 0)_1          fifo_intf.rd_en

----------------Focused Condition View----------------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----
  fifo_intf.empty        N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en        Y

     Rows:       Hits  FEC Target              Non-masking condition(s)
     -----       ----  ----------              ------------------------
  Row    1:     ***0***  fifo_intf.empty_0     fifo_intf.rd_en
  Row    2:          5  fifo_intf.empty_1     fifo_intf.rd_en
  Row    3:          5  fifo_intf.rd_en_0     fifo_intf.empty
  Row    4:          5  fifo_intf.rd_en_1     fifo_intf.empty

----------------Focused Condition View----------------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

      Input Term   Covered  Reason for no coverage   Hint
      ----------   -------  ----------------------   ----
```

fifo_intf.rd_en	Y
fifo_intf.wr_en	Y
fifo_intf.full	Y

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	(~fifo_intf.full && fifo_intf.wr_en)
Row 2:	5	fifo_intf.rd_en_1	–
Row 3:	5	fifo_intf.wr_en_0	~fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(~fifo_intf.full && ~fifo_intf.rd_en)
Row 5:	5	fifo_intf.full_0	(~fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.full_1	(~fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 57 Item 1 ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(~fifo_intf.empty && ~fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	(~fifo_intf.empty && fifo_intf.rd_en)
Row 4:	5	fifo_intf.wr_en_1	fifo_intf.rd_en
Row 5:	5	fifo_intf.empty_0	(fifo_intf.rd_en && ~fifo_intf.wr_en)
Row 6:	5	fifo_intf.empty_1	(fifo_intf.rd_en && ~fifo_intf.wr_en)

Focused Condition View

Line 59 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.full	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(fifo_intf.full && fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(fifo_intf.full && fifo_intf.rd_en)
Row 5:	5	fifo_intf.full_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.full_1	(fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 61 Item 1 ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)

Condition totals: 3 of 3 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
fifo_intf.rd_en	Y		
fifo_intf.wr_en	Y		
fifo_intf.empty	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	fifo_intf.rd_en_0	–
Row 2:	5	fifo_intf.rd_en_1	(fifo_intf.empty && fifo_intf.wr_en)
Row 3:	5	fifo_intf.wr_en_0	fifo_intf.rd_en
Row 4:	5	fifo_intf.wr_en_1	(fifo_intf.empty && fifo_intf.rd_en)
Row 5:	5	fifo_intf.empty_0	(fifo_intf.rd_en && fifo_intf.wr_en)
Row 6:	5	fifo_intf.empty_1	(fifo_intf.rd_en && fifo_intf.wr_en)

Focused Condition View

Line 66 Item 1 (count == 8)

Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 8)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == 8)_0	–
Row 2:	5	(count == 8)_1	–

Focused Condition View

Line 67 Item 1 ((count == 0) || ~fifo_intf.rst_n)

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 0)	Y		
fifo_intf.rst_n	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == 0)_0	fifo_intf.rst_n
Row 2:	5	(count == 0)_1	–
Row 3:	5	fifo_intf.rst_n_0	~(count == 0)
Row 4:	5	fifo_intf.rst_n_1	~(count == 0)

----------Focused Condition View----------
Line 68 Item 1 (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == (8 - 1))	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == (8 - 1))_0	–
Row 2:	5	(count == (8 - 1))_1	–

----------Focused Condition View----------
Line 69 Item 1 (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(count == 1)	Y		

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	(count == 1)_0	–
Row 2:	5	(count == 1)_1	–

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	28	28	0	100.00%

==========Statement Details==========

Statement Coverage for Design Unit work.FIFO —

Line	Item	Count	Source
File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv			
1			module FIFO(FIFO_IF.DUT fifo_intf);
2			parameter FIFO_WIDTH = 16;
3			parameter FIFO_DEPTH = 8;
4			
5			localparam max_fifo_addr = $clog2(FIFO_DEPTH);
6			
7			reg [FIFO_WIDTH-1:0] mem [FIFO_DEPTH-1:0]; // 1-D Array
8			
9			reg [max_fifo_addr-1:0] wr_ptr, rd_ptr;
10			reg [max_fifo_addr:0] count;
11			
12	1	6587	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
13			if (!fifo_intf.rst_n) begin
14	1	1206	wr_ptr <= 0;
15	1	1206	fifo_intf.wr_ack <= 0;
16	1	1206	fifo_intf.overflow <= 0;
17			end
18			else if (fifo_intf.wr_en && count < FIFO_DEPTH) begin
19	1	3082	mem[wr_ptr] <= fifo_intf.data_in;
20	1	3082	fifo_intf.wr_ack <= 1;
21	1	3082	wr_ptr <= wr_ptr + 1;
22			end
23			else begin
24	1	2299	fifo_intf.wr_ack <= 0;
25			if (fifo_intf.full & fifo_intf.wr_en)
26	1	501	fifo_intf.overflow <= 1;
27			else
28	1	1798	fifo_intf.overflow <= 0;
29			end
30			end
31			
32	1	6587	always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
33			if (!fifo_intf.rst_n) begin
34	1	1206	rd_ptr <= 0;
35	1	1206	fifo_intf.underflow <= 0;
36	1	1206	fifo_intf.data_out <= {FIFO_WIDTH{1'b0}};
37			end
38			else if (fifo_intf.rd_en && count != 0) begin
39	1	1157	fifo_intf.data_out <= mem[rd_ptr];
40	1	1157	rd_ptr <= rd_ptr + 1;
41			end
42			else begin
43			if (fifo_intf.empty & fifo_intf.rd_en)
44	1	660	fifo_intf.underflow <= 1;
45			else
46	1	3564	fifo_intf.underflow <= 0;

```
    47                                                   end
    48                                                end
    49
    50              1                       5557      always @(posedge fifo_intf.clk or negedge fifo_intf.rst_n) begin
    51                                                   if (!fifo_intf.rst_n) begin
    52              1                       1166                 count <= 0;
    53                                                   end
    54                                                   else begin
    55                                                          if       ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b10) && !fifo_intf.fu
    56              1                       2190                         count <= count + 1;
    57                                                          else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b01) && !fifo_intf.em
    58              1                        336                         count <= count - 1;
    59                                                          else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.ful
    60              1                         90                         count <= count - 1;
    61                                                          else if ( ({fifo_intf.wr_en, fifo_intf.rd_en} == 2'b11) && fifo_intf.emp
    62              1                        161                         count <= count + 1;
    63                                                   end
    64                                                end
    65
    66              1                       3272      assign fifo_intf.full = (count == FIFO_DEPTH)? 1 : 0;
    67              1                       4396      assign fifo_intf.empty = (count == 0 || !fifo_intf.rst_n)? 1 : 0;
    68              1                       3272      assign fifo_intf.almostfull = (count == FIFO_DEPTH-1)? 1 : 0;
    69              1                       3272      assign fifo_intf.almostempty = (count == 1)? 1 : 0;

Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         20        20         0   100.00%

================================Toggle Details================================

Toggle Coverage for Design Unit work.FIFO

                                               Node      1H->0L      0L->1H   "Coverage"
                                              ---------------------------------------------
                                         count[0-3]           5           5       100.00
                                        rd_ptr[0-2]           5           5       100.00
                                        wr_ptr[0-2]           5           5       100.00

Total Node Count     =         10
Toggled Node Count   =         10
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (20 of 20 bins)


Total Coverage By Design Unit (filtered view): 98.00%
```

6.3 Coverage "Merged" Report

```
Coverage Report by file with details

=================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_IF.sv
=================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                       1         1         0   100.00%

================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_IF.sv --

    24              1                       6025
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         86        86         0   100.00%

================================Toggle Details================================

Toggle Coverage for File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_IF.sv --

       Line                                    Node      1H->0L      0L->1H   "Coverage"
---------------------------------------------------------------------------------------------

Total Node Count     =         43
Toggled Node Count   =         43
Untoggled Node Count =          0

Toggle Coverage      =     100.00% (86 of 86 bins)

=================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_agent_pkg.sv
=================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         4         1         3    25.00%

================================Branch Details================================
```

```
Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_agent_pkg.sv --

------------------------------------IF Branch------------------------------------
    26                                     5     Count coming in to IF
    26              1                  ***0***
                                           5     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    27                                  ***0***  Count coming in to IF
    27              1                  ***0***
                                       ***0***  All False Count
Branch totals: 0 hits of 2 branches = 0.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      15        12         3    80.00%

====================================Statement Details====================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_agent_pkg.sv --

    13              1                  ***0***
    13              2                  ***0***
    13              3                      10
    21              1                       5
    25              1                       5
    27              1                  ***0***
    28              1                       5
    29              1                       5
    30              1                       5
    31              1                       5
    35              1                       5
    36              1                       5
    37              1                       5
    38              1                       5
    39              1                       5

================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        10         0        10     0.00%

====================================Branch Details====================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv --

------------------------------------IF Branch------------------------------------
    7                                   ***0***  Count coming in to IF
    7               1                   ***0***
                                        ***0***  All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    7                                   ***0***  Count coming in to IF
    7               2                   ***0***
                                        ***0***  All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    7                                   ***0***  Count coming in to IF
    7               3                   ***0***
    7               4                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    7                                   ***0***  Count coming in to IF
    7               5                   ***0***
                                        ***0***  All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    7                                   ***0***  Count coming in to IF
    7               6                   ***0***
                                        ***0***  All False Count
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----   -------    ------  --------
    Conditions                       2         0         2     0.00%

====================================Condition Details====================================

Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv --
```

```
----------Focused Condition View----------
Line       7 Item    1  (name != 0)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
  -----------  -------  ----------------------  ---------------
  (name != 0)        N  No hits                 Hit '_0' and '_1'

    Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  --------  ----------------------  ------------------------
  Row    1:    ***0***  (name != 0)_0          -
  Row    2:    ***0***  (name != 0)_1          -

----------Focused Condition View----------
Line       7 Item    2  (tmp_data__ != null)
Condition totals: 0 of 1 input term covered = 0.00%

            Input Term   Covered  Reason for no coverage   Hint
            -----------  -------  ----------------------  ---------------
  (tmp_data__ != null)         N  No hits                 Hit '_0' and '_1'

    Rows:       Hits  FEC Target                 Non-masking condition(s)
  ---------  --------  -------------------------  ------------------------
  Row    1:    ***0***  (tmp_data__ != null)_0    -
  Row    2:    ***0***  (tmp_data__ != null)_1    -


Statement Coverage:
    Enabled Coverage                 Bins      Hits    Misses  Coverage
    ----------------                 ----      ----    ------  --------
    Statements                         11         1        10     9.09%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_config_obj_pkg.sv --

    7                1                    ***0***
    7                2                    ***0***
    7                3                    ***0***
    7                4                    ***0***
    7                5                    ***0***
    7                6                    ***0***
    7                7                    ***0***
    7                8                    ***0***
    7                9                    ***0***
    7               10                    ***0***
    12               1                        5

================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_coverage_pkg.sv
================================================================================
Statement Coverage:
    Enabled Coverage                 Bins      Hits    Misses  Coverage
    ----------------                 ----      ----    ------  --------
    Statements                         14        12         2    85.71%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_coverage_pkg.sv --

    8                1                    ***0***
    8                2                    ***0***
    8                3                        10
    68               1                        5
    69               1                        5
    73               1                        5
    74               1                        5
    75               1                        5
    79               1                        5
    80               1                        5
    84               1                        5
    85               1                        5
    86               1                     6030
    87               1                     6025

================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_driver_pkg.sv
================================================================================
Branch Coverage:
    Enabled Coverage                 Bins      Hits    Misses  Coverage
    ----------------                 ----      ----    ------  --------
    Branches                            4         1         3    25.00%

==========Branch Details==========

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_driver_pkg.sv --

----------IF Branch----------
    21                                   5     Count coming in to IF
    21               1                ***0***
                                         5     All False Count
```

Branch totals: 1 hit of 2 branches = 50.00%

IF Branch

22		***0***	Count coming in to IF
22	1	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	17	14	3	82.35%

Statement Details

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_driver_pkg.sv —

9	1	***0***
9	2	***0***
9	3	10
16	1	5
20	1	5
22	1	***0***
27	1	5
32	1	5
33	1	5
34	1	6030
35	1	6030
38	1	6025
39	1	6025
40	1	6025
41	1	6025
44	1	6025
46	1	6025

File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_env_pkg.sv

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	10	8	2	80.00%

Statement Details

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_env_pkg.sv —

10	1	***0***
10	2	***0***
10	3	10
17	1	5
21	1	5
22	1	5
23	1	5
24	1	5
28	1	5
29	1	5

File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_monitor_pkg.sv

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	25	23	2	92.00%

Statement Details

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_monitor_pkg.sv —

9	1	***0***
9	2	***0***
9	3	10
15	1	5
19	1	5
20	1	5
24	1	5
25	1	5
26	1	6030
28	1	6030
30	1	6025
33	1	6025
36	1	6025
37	1	6025
38	1	6025
39	1	6025
42	1	6025
43	1	6025
44	1	6025
45	1	6025
46	1	6025

```
    47              1                       6025
    48              1                       6025
    49              1                       6025
    51              1                       6025

================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        57        19        38    33.33%

================================Branch Details================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv --

------------------------------------IF Branch------------------------------------
    64                                      6025     Count coming in to IF
    64              1                        644
    77              1                       5381
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    84                                      5381     Count coming in to IF
    84              1                       3082
    88              1                       2299
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    90                                      2299     Count coming in to IF
    90              1                        501
    93              1                       1798
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    99                                      5381     Count coming in to IF
    99              1                       1157
    102             1                       4224
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    103                                     4224     Count coming in to IF
    103             1                        660
    106             1                       3564
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    112                                     5381     Count coming in to IF
    112             1                       2190
    115             1                        336
    118             1                        161
    121             1                         90
                                            2604     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    141                                     6025     Count coming in to IF
    141             1                       6025
    150             1                     ***0***
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    152                                   ***0***    Count coming in to IF
    152             1                     ***0***
                                          ***0***    All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    153                                   ***0***    Count coming in to IF
    153             1                     ***0***
                                          ***0***    All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    153                                   ***0***    Count coming in to IF
    153             2                     ***0***
                                          ***0***    All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    154                                   ***0***    Count coming in to IF
    154             1                     ***0***
                                          ***0***    All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    154                                   ***0***    Count coming in to IF
    154             2                     ***0***
                                          ***0***    All False Count
Branch totals: 0 hits of 2 branches = 0.00%
```

```
------------------------------------IF Branch------------------------------------
    155                                 ***0***     Count coming in to IF
    155             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    155                                 ***0***     Count coming in to IF
    155             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    156                                 ***0***     Count coming in to IF
    156             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    156                                 ***0***     Count coming in to IF
    156             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    157                                 ***0***     Count coming in to IF
    157             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    157                                 ***0***     Count coming in to IF
    157             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    158                                 ***0***     Count coming in to IF
    158             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    158                                 ***0***     Count coming in to IF
    158             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    159                                 ***0***     Count coming in to IF
    159             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    159                                 ***0***     Count coming in to IF
    159             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    160                                 ***0***     Count coming in to IF
    160             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    160                                 ***0***     Count coming in to IF
    160             2                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------IF Branch------------------------------------
    168                                     5       Count coming in to IF
    168             1                       5
                                        ***0***     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    169                                     5       Count coming in to IF
    169             1                       5
                                        ***0***     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    170                                     5       Count coming in to IF
    170             1                       5
                                        ***0***     All False Count
Branch totals: 1 hit of 2 branches = 50.00%


Condition Coverage:
```

Enabled Coverage	Bins	Covered	Misses	Coverage
Conditions	36	18	18	50.00%

Condition Details

Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —

Focused Condition View

```
Line       84 Item    1  (seq_item_chk.wr_en && (this.count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
```

Focused Condition View

```
Line       90 Item    1  (seq_item_chk.wr_en && (this.count == 8))
Condition totals: 1 of 2 input terms covered = 50.00%
```

Input Term	Covered	Reason for no coverage	Hint
seq_item_chk.wr_en	Y		
(this.count == 8)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	seq_item_chk.wr_en_0	–
Row 2:	5	seq_item_chk.wr_en_1	(this.count == 8)
Row 3:	***0***	(this.count == 8)_0	seq_item_chk.wr_en
Row 4:	5	(this.count == 8)_1	seq_item_chk.wr_en

Focused Condition View

```
Line       99 Item    1  (seq_item_chk.rd_en && (this.count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%
```

Focused Condition View

```
Line       103 Item    1  (seq_item_chk.rd_en && (this.count == 0))
Condition totals: 1 of 2 input terms covered = 50.00%
```

Input Term	Covered	Reason for no coverage	Hint
seq_item_chk.rd_en	Y		
(this.count == 0)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	5	seq_item_chk.rd_en_0	–
Row 2:	5	seq_item_chk.rd_en_1	(this.count == 0)
Row 3:	***0***	(this.count == 0)_0	seq_item_chk.rd_en
Row 4:	5	(this.count == 0)_1	seq_item_chk.rd_en

Focused Condition View

```
Line       112 Item    1  (~seq_item_chk.rd_en && seq_item_chk.wr_en && ~this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
```

Focused Condition View

```
Line       115 Item    1  (seq_item_chk.rd_en && ~seq_item_chk.wr_en && ~this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
```

Focused Condition View

```
Line       118 Item    1  (seq_item_chk.wr_en && seq_item_chk.rd_en && this.empty_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
```

Focused Condition View

```
Line       121 Item    1  (seq_item_chk.wr_en && seq_item_chk.rd_en && this.full_ref)
Condition totals: 3 of 3 input terms covered = 100.00%
```

Focused Condition View

```
Line       141 Item    1  ((seq_item_chk.data_out == this.data_out_ref) && (seq_item_chk.wr_ack == this.wr_ack_ref) && (seq_item_chk.o
Condition totals: 0 of 8 input terms covered = 0.00%
```

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.data_out == this.data_out_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.wr_ack == this.wr_ack_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.overflow == this.overflow_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.underflow == this.underflow_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.full == this.full_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.empty == this.empty_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.almostfull == this.almostfull_ref)	N	'_0' not hit	Hit '_0'
(seq_item_chk.almostempty == this.almostempty_ref)	N	'_0' not hit	Hit '_0'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	***0***	(seq_item_chk.data_out == this.data_out_ref)_0	–
Row 2:	5	(seq_item_chk.data_out == this.data_out_ref)_1	((seq_item_chk.wr_ack == this.wr_ack_ref) && ((seq_item_cl
Row 3:	***0***	(seq_item_chk.wr_ack == this.wr_ack_ref)_0	(seq_item_chk.data_out == this.data_out_ref)
Row 4:	5	(seq_item_chk.wr_ack == this.wr_ack_ref)_1	((seq_item_chk.data_out == this.data_out_ref) && ((seq_ite
Row 5:	***0***	(seq_item_chk.overflow == this.overflow_ref)_0	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 6:	5	(seq_item_chk.overflow == this.overflow_ref)_1	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 7:	***0***	(seq_item_chk.underflow == this.underflow_ref)_0	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 8:	5	(seq_item_chk.underflow == this.underflow_ref)_1	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 9:	***0***	(seq_item_chk.full == this.full_ref)_0	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 10:	5	(seq_item_chk.full == this.full_ref)_1	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten
Row 11:	***0***	(seq_item_chk.empty == this.empty_ref)_0	((seq_item_chk.data_out == this.data_out_ref) && (seq_iten

Row 12:	5	(seq_item_chk.empty === this.empty_ref)_1	((seq_item_chk.data_out === this.data_out_ref) && (seq_iten
Row 13:	***0***	(seq_item_chk.almostfull === this.almostfull_ref)_0	((seq_item_chk.data_out === this.data_out_ref) && (seq_iten
Row 14:	5	(seq_item_chk.almostfull === this.almostfull_ref)_1	((seq_item_chk.data_out === this.data_out_ref) && (seq_iten
Row 15:	***0***	(seq_item_chk.almostempty === this.almostempty_ref)_0	((seq_item_chk.data_out === this.data_out_ref) && (seq_iten
Row 16:	5	(seq_item_chk.almostempty === this.almostempty_ref)_1	((seq_item_chk.data_out === this.data_out_ref) && (seq_iten

----------Focused Condition View----------
Line 153 Item 1 (seq_item_chk.data_out !== this.data_out_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.data_out !== this.data_out_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.data_out !== this.data_out_ref)_0	-
Row 2:	***0***	(seq_item_chk.data_out !== this.data_out_ref)_1	-

----------Focused Condition View----------
Line 154 Item 1 (seq_item_chk.wr_ack !== this.wr_ack_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.wr_ack !== this.wr_ack_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.wr_ack !== this.wr_ack_ref)_0	-
Row 2:	***0***	(seq_item_chk.wr_ack !== this.wr_ack_ref)_1	-

----------Focused Condition View----------
Line 155 Item 1 (seq_item_chk.overflow !== this.overflow_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.overflow !== this.overflow_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.overflow !== this.overflow_ref)_0	-
Row 2:	***0***	(seq_item_chk.overflow !== this.overflow_ref)_1	-

----------Focused Condition View----------
Line 156 Item 1 (seq_item_chk.underflow !== this.underflow_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.underflow !== this.underflow_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.underflow !== this.underflow_ref)_0	-
Row 2:	***0***	(seq_item_chk.underflow !== this.underflow_ref)_1	-

----------Focused Condition View----------
Line 157 Item 1 (seq_item_chk.full !== this.full_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.full !== this.full_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.full !== this.full_ref)_0	-
Row 2:	***0***	(seq_item_chk.full !== this.full_ref)_1	-

----------Focused Condition View----------
Line 158 Item 1 (seq_item_chk.empty !== this.empty_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.empty !== this.empty_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(seq_item_chk.empty !== this.empty_ref)_0	-
Row 2:	***0***	(seq_item_chk.empty !== this.empty_ref)_1	-

----------Focused Condition View----------
Line 159 Item 1 (seq_item_chk.almostfull !== this.almostfull_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.almostfull !== this.almostfull_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	***0***	(seq_item_chk.almostfull !== this.almostfull_ref)_0	–
Row 2:	***0***	(seq_item_chk.almostfull !== this.almostfull_ref)_1	–

----------Focused Condition View----------
Line 160 Item 1 (seq_item_chk.almostempty !== this.almostempty_ref)
Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(seq_item_chk.almostempty !== this.almostempty_ref)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	***0***	(seq_item_chk.almostempty !== this.almostempty_ref)_0	–
Row 2:	***0***	(seq_item_chk.almostempty !== this.almostempty_ref)_1	–

Expression Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Expressions	4	4	0	100.00%

==========Expression Details==========

Expression Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —

----------Focused Expression View----------
Line 128 Item 1 (this.count == 0)
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 129 Item 1 (this.count == 8)
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 130 Item 1 (this.count == (8 - 1))
Expression totals: 1 of 1 input term covered = 100.00%

----------Focused Expression View----------
Line 131 Item 1 (this.count == 1)
Expression totals: 1 of 1 input term covered = 100.00%

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	60	48	12	80.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_scoreboard_pkg.sv —

9	1	***0***
9	2	***0***
9	3	10
17	1	5
22	1	5
23	1	5
24	1	5
29	1	5
30	1	5
35	1	5
36	1	5
37	1	6030
38	1	6025
61	1	6025
65	1	644
66	1	644
67	1	644
68	1	644
69	1	644
70	1	644
71	1	644
72	1	644
73	1	644
74	1	644
75	1	644
76	1	644
85	1	3082
86	1	3082
87	1	3082
89	1	2299
92	1	501
94	1	1798
100	1	1157
101	1	1157
105	1	660
107	1	3564
113	1	2190
116	1	336

120	1	161
123	1	90
128	1	6025
129	1	6025
130	1	6025
131	1	6025
137	1	6025
149	1	6025
151	1	***0***
152	1	***0***
153	1	***0***
154	1	***0***
155	1	***0***
156	1	***0***
157	1	***0***
158	1	***0***
159	1	***0***
160	1	***0***
166	1	5
168	1	5
169	1	5
170	1	5

==========
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv
==========

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	10	2	8	20.00%

==========Branch Details==========

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —

----------IF Branch----------

8		***0***	Count coming in to IF
8	1	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

8		6025	Count coming in to IF
8	2	***0***	
		6025	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

8		***0***	Count coming in to IF
8	3	***0***	
8	4	***0***	

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

8		6025	Count coming in to IF
8	5	***0***	
		6025	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

8		***0***	Count coming in to IF
8	6	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

Condition Coverage:

Enabled Coverage	Bins	Covered	Misses	Coverage
Conditions	2	0	2	0.00%

==========Condition Details==========

Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —

----------Focused Condition View----------

Line 8 Item 1 (name != 0)

Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(name != 0)	N	No hits	Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non–masking condition(s)
Row 1:	***0***	(name != 0)_0	–
Row 2:	***0***	(name != 0)_1	–

----------Focused Condition View----------

Line 8 Item 2 (tmp_data__ != null)

Condition totals: 0 of 1 input term covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(tmp_data__ != null)	N	'_1' not hit	Hit '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	5	(tmp_data__ != null)_0	-
Row 2:	***0***	(tmp_data__ != null)_1	-

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	16	8	8	50.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_item_pkg.sv —

8	1	***0***
8	2	***0***
8	3	***0***
8	4	***0***
8	5	***0***
8	6	6025
8	7	***0***
8	8	***0***
8	9	6025
8	10	***0***
16	1	12065
22	1	12065
63	1	15
64	1	15
65	1	15
69	1	5

==========
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv
==========

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	26	6	20	23.07%

==========Branch Details==========

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv —

----------IF Branch----------

8		***0***	Count coming in to IF
8	1	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

8		5	Count coming in to IF
8	2	***0***	
		5	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

8		***0***	Count coming in to IF
8	3	***0***	
8	4	***0***	

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

8		5	Count coming in to IF
8	5	***0***	
		5	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

8		***0***	Count coming in to IF
8	6	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

21		25	Count coming in to IF
21	1	***0***	
		25	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

22		***0***	Count coming in to IF
22	1	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

30		5000	Count coming in to IF

```
    30              1                      ***0***
                                           5000      All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------------IF Branch------------------------------------------
    31                                     ***0***      Count coming in to IF
    31              1                      ***0***
                                           ***0***      All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------------IF Branch------------------------------------------
    39                                        500      Count coming in to IF
    39              1                      ***0***
                                              500      All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------------IF Branch------------------------------------------
    40                                     ***0***      Count coming in to IF
    40              1                      ***0***
                                           ***0***      All False Count
Branch totals: 0 hits of 2 branches = 0.00%

------------------------------------------IF Branch------------------------------------------
    48                                        500      Count coming in to IF
    48              1                      ***0***
                                              500      All False Count
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------------IF Branch------------------------------------------
    49                                     ***0***      Count coming in to IF
    49              1                      ***0***
                                           ***0***      All False Count
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
    Enabled Coverage                  Bins    Covered     Misses  Coverage
    ----------------                  ----    -------     ------  --------
    Conditions                           2          0          2     0.00%

================================Condition Details================================

Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv --

----------------Focused Condition View----------------
Line       8 Item    1  (name != 0)
Condition totals: 0 of 1 input term covered = 0.00%

   Input Term   Covered  Reason for no coverage   Hint
   ----------   -------  ----------------------   ----
  (name != 0)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
  ---------  ---------  --------------------  ------------------------
  Row    1:     ***0***  (name != 0)_0         -
  Row    2:     ***0***  (name != 0)_1         -

----------------Focused Condition View----------------
Line       8 Item    2  (tmp_data__ != null)
Condition totals: 0 of 1 input term covered = 0.00%

            Input Term   Covered  Reason for no coverage   Hint
            ----------   -------  ----------------------   ----
  (tmp_data__ != null)         N  '_1' not hit             Hit '_1'

     Rows:       Hits  FEC Target              Non-masking condition(s)
  ---------  ---------  ----------------------  ------------------------
  Row    1:          5  (tmp_data__ != null)_0  -
  Row    2:     ***0***  (tmp_data__ != null)_1  -


Statement Coverage:
    Enabled Coverage                  Bins      Hits     Misses  Coverage
    ----------------                  ----      ----     ------  --------
    Statements                          32        20         12    62.50%

================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequence_pkg.sv --

    8               1                      ***0***
    8               2                      ***0***
    8               3                      ***0***
    8               4                      ***0***
    8               5                      ***0***
    8               6                           5
    8               7                      ***0***
    8               8                      ***0***
    8               9                           5
    8              10                      ***0***
    12              1                           5
    16              1                           5
```

18	1	5
19	1	25
20	1	25
22	1	***0***
23	1	25
27	1	5
28	1	5000
29	1	5000
31	1	***0***
32	1	5000
36	1	5
37	1	500
38	1	500
40	1	***0***
41	1	500
45	1	5
46	1	500
47	1	500
49	1	***0***
50	1	500

==
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequencer_pkg.sv
==

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	4	2	2	50.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_sequencer_pkg.sv —

8	1	***0***
8	2	***0***
8	3	10
11	1	5

==
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv
==

Branch Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Branches	6	2	4	33.33%

==========Branch Details==========

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv —

----------IF Branch----------

26		5	Count coming in to IF
26	1	***0***	
		5	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

----------IF Branch----------

27		***0***	Count coming in to IF
27	1	***0***	
		0	All False Count

Branch totals: 0 hits of 2 branches = 0.00%

----------IF Branch----------

35		5	Count coming in to IF
35	1	5	
		0	All False Count

Branch totals: 1 hit of 2 branches = 50.00%

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	15	12	3	80.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_test_pkg.sv —

10	1	***0***
10	2	***0***
10	3	20
17	1	5
21	1	5
22	1	5
23	1	5
24	1	5
27	1	***0***
29	1	5
33	1	5
34	1	5
35	1	5
36	1	5

```
    37                1                                5

================================================================================
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv
================================================================================
Branch Coverage:
    Enabled Coverage                 Bins      Hits     Misses  Coverage
    ----------------                 ----      ----     ------  --------
    Branches                           25        25          0   100.00%

================================Branch Details================================

Branch Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv --

------------------------------------IF Branch------------------------------------
    13                                      6587     Count coming in to IF
    13                1                     1206
    18                1                     3082
    23                1                     2299
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    25                                      2299     Count coming in to IF
    25                1                      501
    27                1                     1798
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    33                                      6587     Count coming in to IF
    33                1                     1206
    38                1                     1157
    42                1                     4224
Branch totals: 3 hits of 3 branches = 100.00%

------------------------------------IF Branch------------------------------------
    43                                      4224     Count coming in to IF
    43                1                      660
    45                1                     3564
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    51                                      5557     Count coming in to IF
    51                1                     1166
    54                1                     4391
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    55                                      4391     Count coming in to IF
    55                1                     2190
    57                1                      336
    59                1                       90
    61                1                      161
                                            1614     All False Count
Branch totals: 5 hits of 5 branches = 100.00%

------------------------------------IF Branch------------------------------------
    66                                      3267     Count coming in to IF
    66                1                      202
    66                2                     3065
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    67                                      4391     Count coming in to IF
    67                1                     1691
    67                2                     2700
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    68                                      3267     Count coming in to IF
    68                1                      290
    68                2                     2977
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    69                                      3267     Count coming in to IF
    69                1                      621
    69                2                     2646
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage                 Bins    Covered     Misses  Coverage
    ----------------                 ----    -------     ------  --------
    Conditions                         25         23          2    92.00%

================================Condition Details================================

Condition Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv --

----------------Focused Condition View----------------
Line       18 Item    1  (fifo_intf.wr_en && (count < 8))
Condition totals: 2 of 2 input terms covered = 100.00%
```

```
----------Focused Condition View----------
Line       25 Item    1  (fifo_intf.full & fifo_intf.wr_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
     -------------  -------  ----------------------  ---------------
    fifo_intf.full        N  '_0' not hit             Hit '_0'
  fifo_intf.wr_en         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:    ***0***  fifo_intf.full_0      fifo_intf.wr_en
  Row    2:          5  fifo_intf.full_1      fifo_intf.wr_en
  Row    3:          5  fifo_intf.wr_en_0     fifo_intf.full
  Row    4:          5  fifo_intf.wr_en_1     fifo_intf.full

----------Focused Condition View----------
Line       38 Item    1  (fifo_intf.rd_en && (count != 0))
Condition totals: 2 of 2 input terms covered = 100.00%

----------Focused Condition View----------
Line       43 Item    1  (fifo_intf.empty & fifo_intf.rd_en)
Condition totals: 1 of 2 input terms covered = 50.00%

       Input Term   Covered  Reason for no coverage   Hint
     -------------  -------  ----------------------  ---------------
  fifo_intf.empty         N  '_0' not hit             Hit '_0'
  fifo_intf.rd_en         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ----------  ---------  --------------------  --------------------------
  Row    1:    ***0***  fifo_intf.empty_0     fifo_intf.rd_en
  Row    2:          5  fifo_intf.empty_1     fifo_intf.rd_en
  Row    3:          5  fifo_intf.rd_en_0     fifo_intf.empty
  Row    4:          5  fifo_intf.rd_en_1     fifo_intf.empty

----------Focused Condition View----------
Line       55 Item    1  ((~fifo_intf.rd_en && fifo_intf.wr_en) && ~fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line       57 Item    1  ((fifo_intf.rd_en && ~fifo_intf.wr_en) && ~fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line       59 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.full)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line       61 Item    1  ((fifo_intf.rd_en && fifo_intf.wr_en) && fifo_intf.empty)
Condition totals: 3 of 3 input terms covered = 100.00%

----------Focused Condition View----------
Line       66 Item    1  (count == 8)
Condition totals: 1 of 1 input term covered = 100.00%

----------Focused Condition View----------
Line       67 Item    1  ((count == 0) || ~fifo_intf.rst_n)
Condition totals: 2 of 2 input terms covered = 100.00%

----------Focused Condition View----------
Line       68 Item    1  (count == (8 - 1))
Condition totals: 1 of 1 input term covered = 100.00%

----------Focused Condition View----------
Line       69 Item    1  (count == 1)
Condition totals: 1 of 1 input term covered = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      28        28         0  100.00%

================================Statement Details================================

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv --

    12                  1                    6587
    14                  1                    1206
    15                  1                    1206
    16                  1                    1206
    19                  1                    3082
    20                  1                    3082
    21                  1                    3082
    24                  1                    2299
    26                  1                     501
    28                  1                    1798
    32                  1                    6587
    34                  1                    1206
    35                  1                    1206
```

36	1	1206
39	1	1157
40	1	1157
44	1	660
46	1	3564
50	1	5557
52	1	1166
56	1	2190
58	1	336
60	1	90
62	1	161
66	1	3272
67	1	4396
68	1	3272
69	1	3272

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	20	20	0	100.00%

==========Toggle Details==========

Toggle Coverage for File /home/tare/Desktop/syn_fifo/uvm_verification/FIFO_v1.0.0.sv —

Line	Node	1H->0L	0L->1H	"Coverage"

Total Node Count = 10
Toggled Node Count = 10
Untoggled Node Count = 0

Toggle Coverage = 100.00% (20 of 20 bins)

==========
=== File: /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv
==========

Statement Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	5	5	0	100.00%

==========Statement Details==========

Statement Coverage for file /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv —

10	1	5
11	1	12055
11	2	12050
24	1	5
25	1	5

Toggle Coverage:

Enabled Coverage	Bins	Hits	Misses	Coverage
Toggles	2	2	0	100.00%

==========Toggle Details==========

Toggle Coverage for File /home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv —

Line	Node	1H->0L	0L->1H	"Coverage"

Total Node Count = 1
Toggled Node Count = 1
Untoggled Node Count = 0

Toggle Coverage = 100.00% (2 of 2 bins)

COVERGROUP COVERAGE:

Covergroup	Metric	Goal	Bins	Status
TYPE /FIFO_coverage_pkg/FIFO_coverage/fifo_cg	100.00%	100	—	Covered
covered/total bins:	190	190	—	
missing/total bins:	0	190	—	
% Hit:	100.00%	100	—	
Coverpoint rst_n_cp	100.00%	100	—	Covered
covered/total bins:	2	2	—	
missing/total bins:	0	2	—	
% Hit:	100.00%	100	—	
bin auto[0]	644	1	—	Covered
bin auto[1]	5381	1	—	Covered
Coverpoint data_in_cp	100.00%	100	—	Covered
covered/total bins:	64	64	—	
missing/total bins:	0	64	—	
% Hit:	100.00%	100	—	
bin auto[0:1023]	976	1	—	Covered
bin auto[1024:2047]	57	1	—	Covered
bin auto[2048:3071]	62	1	—	Covered
bin auto[3072:4095]	64	1	—	Covered
bin auto[4096:5119]	73	1	—	Covered

bin auto[5120:6143]	77	1	–	Covered
bin auto[6144:7167]	60	1	–	Covered
bin auto[7168:8191]	75	1	–	Covered
bin auto[8192:9215]	66	1	–	Covered
bin auto[9216:10239]	62	1	–	Covered
bin auto[10240:11263]	60	1	–	Covered
bin auto[11264:12287]	59	1	–	Covered
bin auto[12288:13311]	64	1	–	Covered
bin auto[13312:14335]	62	1	–	Covered
bin auto[14336:15359]	66	1	–	Covered
bin auto[15360:16383]	53	1	–	Covered
bin auto[16384:17407]	66	1	–	Covered
bin auto[17408:18431]	58	1	–	Covered
bin auto[18432:19455]	79	1	–	Covered
bin auto[19456:20479]	68	1	–	Covered
bin auto[20480:21503]	54	1	–	Covered
bin auto[21504:22527]	65	1	–	Covered
bin auto[22528:23551]	72	1	–	Covered
bin auto[23552:24575]	68	1	–	Covered
bin auto[24576:25599]	66	1	–	Covered
bin auto[25600:26623]	66	1	–	Covered
bin auto[26624:27647]	69	1	–	Covered
bin auto[27648:28671]	78	1	–	Covered
bin auto[28672:29695]	74	1	–	Covered
bin auto[29696:30719]	66	1	–	Covered
bin auto[30720:31743]	61	1	–	Covered
bin auto[31744:32767]	64	1	–	Covered
bin auto[32768:33791]	77	1	–	Covered
bin auto[33792:34815]	61	1	–	Covered
bin auto[34816:35839]	72	1	–	Covered
bin auto[35840:36863]	68	1	–	Covered
bin auto[36864:37887]	75	1	–	Covered
bin auto[37888:38911]	70	1	–	Covered
bin auto[38912:39935]	62	1	–	Covered
bin auto[39936:40959]	55	1	–	Covered
bin auto[40960:41983]	73	1	–	Covered
bin auto[41984:43007]	60	1	–	Covered
bin auto[43008:44031]	70	1	–	Covered
bin auto[44032:45055]	69	1	–	Covered
bin auto[45056:46079]	62	1	–	Covered
bin auto[46080:47103]	63	1	–	Covered
bin auto[47104:48127]	62	1	–	Covered
bin auto[48128:49151]	73	1	–	Covered
bin auto[49152:50175]	62	1	–	Covered
bin auto[50176:51199]	65	1	–	Covered
bin auto[51200:52223]	69	1	–	Covered
bin auto[52224:53247]	70	1	–	Covered
bin auto[53248:54271]	51	1	–	Covered
bin auto[54272:55295]	83	1	–	Covered
bin auto[55296:56319]	70	1	–	Covered
bin auto[56320:57343]	60	1	–	Covered
bin auto[57344:58367]	54	1	–	Covered
bin auto[58368:59391]	69	1	–	Covered
bin auto[59392:60415]	76	1	–	Covered
bin auto[60416:61439]	67	1	–	Covered
bin auto[61440:62463]	75	1	–	Covered
bin auto[62464:63487]	76	1	–	Covered
bin auto[63488:64511]	55	1	–	Covered
bin auto[64512:65535]	941	1	–	Covered
Coverpoint r_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	3991	1	–	Covered
bin auto[1]	2034	1	–	Covered
Coverpoint w_en_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2017	1	–	Covered
bin auto[1]	4008	1	–	Covered
Coverpoint data_out_cp	100.00%	100	–	Covered
covered/total bins:	64	64	–	
missing/total bins:	0	64	–	
% Hit:	100.00%	100	–	
bin auto[0:1023]	3334	1	–	Covered
bin auto[1024:2047]	36	1	–	Covered
bin auto[2048:3071]	13	1	–	Covered
bin auto[3072:4095]	44	1	–	Covered
bin auto[4096:5119]	53	1	–	Covered
bin auto[5120:6143]	57	1	–	Covered
bin auto[6144:7167]	48	1	–	Covered
bin auto[7168:8191]	50	1	–	Covered
bin auto[8192:9215]	43	1	–	Covered
bin auto[9216:10239]	27	1	–	Covered
bin auto[10240:11263]	44	1	–	Covered
bin auto[11264:12287]	44	1	–	Covered
bin auto[12288:13311]	33	1	–	Covered
bin auto[13312:14335]	34	1	–	Covered
bin auto[14336:15359]	25	1	–	Covered
bin auto[15360:16383]	21	1	–	Covered
bin auto[16384:17407]	17	1	–	Covered

bin auto[17408:18431]	19	1	–	Covered
bin auto[18432:19455]	51	1	–	Covered
bin auto[19456:20479]	25	1	–	Covered
bin auto[20480:21503]	39	1	–	Covered
bin auto[21504:22527]	28	1	–	Covered
bin auto[22528:23551]	9	1	–	Covered
bin auto[23552:24575]	21	1	–	Covered
bin auto[24576:25599]	37	1	–	Covered
bin auto[25600:26623]	38	1	–	Covered
bin auto[26624:27647]	35	1	–	Covered
bin auto[27648:28671]	52	1	–	Covered
bin auto[28672:29695]	44	1	–	Covered
bin auto[29696:30719]	31	1	–	Covered
bin auto[30720:31743]	29	1	–	Covered
bin auto[31744:32767]	25	1	–	Covered
bin auto[32768:33791]	46	1	–	Covered
bin auto[33792:34815]	38	1	–	Covered
bin auto[34816:35839]	41	1	–	Covered
bin auto[35840:36863]	37	1	–	Covered
bin auto[36864:37887]	26	1	–	Covered
bin auto[37888:38911]	32	1	–	Covered
bin auto[38912:39935]	50	1	–	Covered
bin auto[39936:40959]	30	1	–	Covered
bin auto[40960:41983]	31	1	–	Covered
bin auto[41984:43007]	33	1	–	Covered
bin auto[43008:44031]	45	1	–	Covered
bin auto[44032:45055]	29	1	–	Covered
bin auto[45056:46079]	26	1	–	Covered
bin auto[46080:47103]	47	1	–	Covered
bin auto[47104:48127]	11	1	–	Covered
bin auto[48128:49151]	32	1	–	Covered
bin auto[49152:50175]	28	1	–	Covered
bin auto[50176:51199]	25	1	–	Covered
bin auto[51200:52223]	61	1	–	Covered
bin auto[52224:53247]	22	1	–	Covered
bin auto[53248:54271]	18	1	–	Covered
bin auto[54272:55295]	47	1	–	Covered
bin auto[55296:56319]	60	1	–	Covered
bin auto[56320:57343]	41	1	–	Covered
bin auto[57344:58367]	17	1	–	Covered
bin auto[58368:59391]	44	1	–	Covered
bin auto[59392:60415]	82	1	–	Covered
bin auto[60416:61439]	31	1	–	Covered
bin auto[61440:62463]	52	1	–	Covered
bin auto[62464:63487]	32	1	–	Covered
bin auto[63488:64511]	21	1	–	Covered
bin auto[64512:65535]	484	1	–	Covered
Coverpoint wr_ack_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	2943	1	–	Covered
bin auto[1]	3082	1	–	Covered
Coverpoint overflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5457	1	–	Covered
bin auto[1]	568	1	–	Covered
Coverpoint full_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5338	1	–	Covered
bin auto[1]	687	1	–	Covered
Coverpoint empty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	4632	1	–	Covered
bin auto[1]	1393	1	–	Covered
Coverpoint almostfull_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5570	1	–	Covered
bin auto[1]	455	1	–	Covered
Coverpoint almostempty_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5044	1	–	Covered
bin auto[1]	981	1	–	Covered
Coverpoint underflow_cp	100.00%	100	–	Covered
covered/total bins:	2	2	–	
missing/total bins:	0	2	–	
% Hit:	100.00%	100	–	
bin auto[0]	5306	1	–	Covered
bin auto[1]	719	1	–	Covered
Cross wr_ack_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	

% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	892	1	–	Covered
bin <auto[1],auto[1],auto[0]>	216	1	–	Covered
bin <auto[0],auto[1],auto[1]>	2190	1	–	Covered
bin <auto[0],auto[1],auto[0]>	710	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross full_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[0],auto[1],auto[1]>	613	1	–	Covered
bin <auto[0],auto[0],auto[1]>	74	1	–	Covered
bin <auto[1],auto[1],auto[0]>	1108	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2287	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1017	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_actv_wr_full	0		–	ZERO
ignore_bin w_en_r_en_allactv_full	0		–	ZERO
Cross empty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	126	1	–	Covered
bin <auto[1],auto[0],auto[1]>	667	1	–	Covered
bin <auto[1],auto[1],auto[0]>	982	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2601	1	–	Covered
bin <auto[1],auto[0],auto[0]>	259	1	–	Covered
bin <auto[0],auto[0],auto[0]>	790	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin read_nactv_empty	600		–	Occurred
Cross almostfull_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	171	1	–	Covered
bin <auto[1],auto[0],auto[1]>	37	1	–	Covered
bin <auto[1],auto[1],auto[0]>	937	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2737	1	–	Covered
bin <auto[1],auto[0],auto[0]>	889	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1007	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostfull	247		–	Occurred
Cross almostempty_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	350	1	–	Covered
bin <auto[1],auto[1],auto[0]>	758	1	–	Covered
bin <auto[0],auto[1],auto[1]>	401	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2499	1	–	Covered
bin <auto[1],auto[0],auto[0]>	867	1	–	Covered
bin <auto[0],auto[0],auto[0]>	920	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_almostempty	230		–	Occurred
Cross overflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	109	1	–	Covered
bin <auto[1],auto[1],auto[0]>	999	1	–	Covered
bin <auto[0],auto[1],auto[1]>	459	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2441	1	–	Covered
bin <auto[1],auto[0],auto[0]>	926	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin w_en_nactv_wr_ack	0		–	ZERO
Cross underflow_cross	100.00%	100	–	Covered
covered/total bins:	6	6	–	
missing/total bins:	0	6	–	
% Hit:	100.00%	100	–	
Auto, Default and User Defined Bins:				
bin <auto[1],auto[1],auto[1]>	208	1	–	Covered
bin <auto[1],auto[0],auto[1]>	511	1	–	Covered
bin <auto[1],auto[1],auto[0]>	900	1	–	Covered
bin <auto[0],auto[1],auto[0]>	2900	1	–	Covered
bin <auto[1],auto[0],auto[0]>	415	1	–	Covered
bin <auto[0],auto[0],auto[0]>	1091	1	–	Covered
Illegal and Ignore Bins:				
ignore_bin r_en_nactv_wr_ack	0		–	ZERO

TOTAL COVERGROUP COVERAGE: 100.00% COVERGROUP TYPES: 1

DIRECTIVE COVERAGE:

Name	Design Unit	Design UnitType	Lang	File(Line)	Hits	Status
/top/cover__n_wr_ack_with_FIFO_Full	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(134)	546	Covered
/top/cover__counter_threshold	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(133)	5381	Covered
/top/cover__read_ptr_threshold	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(132)	5381	Covered
/top/cover__write_ptr_threshold	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(131)	5381	Covered
/top/cover__read_ptr_wraparound	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(130)	25	Covered
/top/cover__write_ptr_wraparound	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(129)	173	Covered
/top/cover__almost_empty_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(128)	881	Covered
/top/cover__almost_full_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(127)	408	Covered
/top/cover__full_flag_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(126)	612	Covered
/top/cover__empty_flag_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(125)	1234	Covered
/top/cover__underflow_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(124)	591	Covered
/top/cover__overflow_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(123)	366	Covered
/top/cover__write_ack_check	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(122)	2772	Covered
/top/cover__reset_behavior	top	Verilog	SVA	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(121)	644	Covered

TOTAL DIRECTIVE COVERAGE: 100.00% COVERS: 14

ASSERTION RESULTS:

Name	File(Line)	Failure Count	Pass Count
/top/assert__n_wr_ack_with_FIFO_Full	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(119)	0	5
/top/assert__counter_threshold	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(118)	0	5
/top/assert__read_ptr_threshold	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(117)	0	5
/top/assert__write_ptr_threshold	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(116)	0	5
/top/assert__read_ptr_wraparound	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(115)	0	5
/top/assert__write_ptr_wraparound	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(114)	0	5
/top/assert__almost_empty_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(113)	0	5
/top/assert__almost_full_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(112)	0	5
/top/assert__full_flag_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(111)	0	5
/top/assert__empty_flag_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(110)	0	5
/top/assert__underflow_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(109)	0	5
/top/assert__overflow_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(108)	0	5
/top/assert__write_ack_check	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(107)	0	5
/top/assert__reset_behavior	/home/tare/Desktop/syn_fifo/uvm_verification/top_module.sv(106)	0	5

Total Coverage By File (code coverage only, filtered view): 75.46%