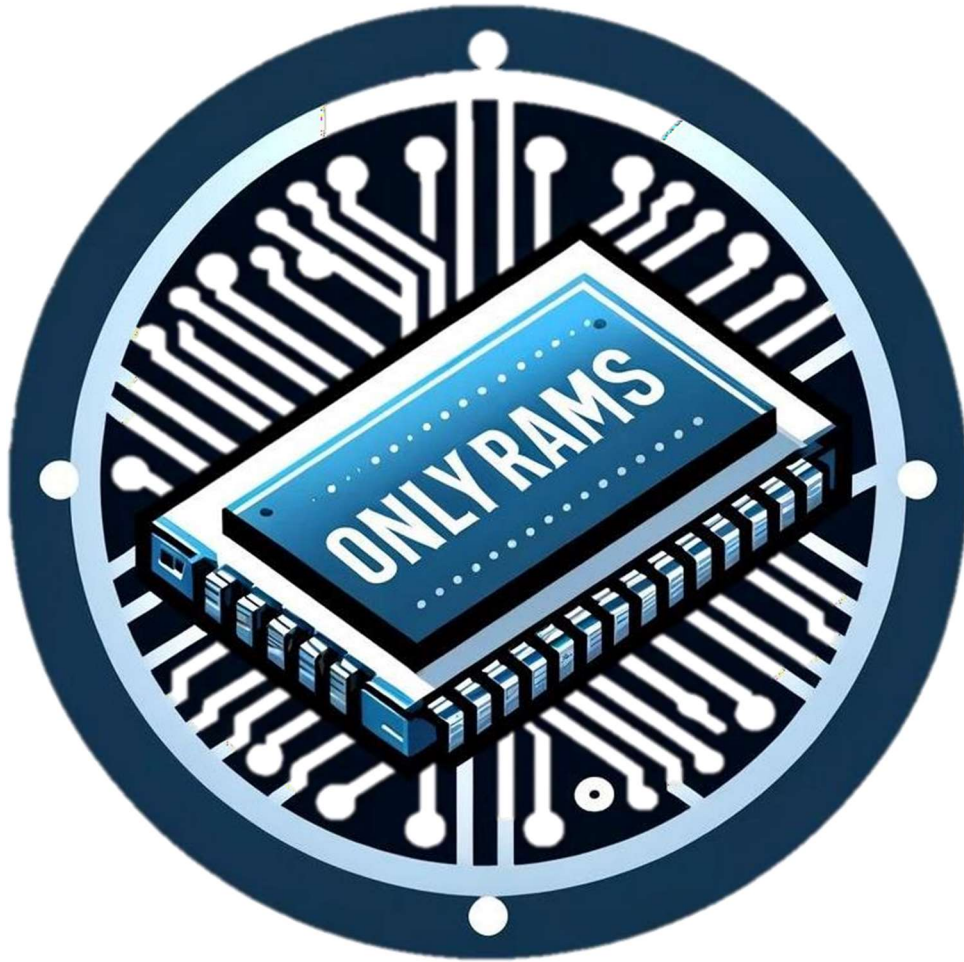


Project 1: DSP

Team: OnlyRAMs



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RTL Code:

```
module sel_reg(D,clk,E,rst,out);
parameter size=18;
parameter z=1;
parameter RSTTYPE="SYNC";
input [size-1:0] D;
input clk,rst,E;
output [size-1:0]out;
reg [size-1:0]temp;
generate
    if (z) begin
        if(RSTTYPE=="SYNC")begin
            always @(posedge clk ) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        else begin
            always @(posedge clk or posedge rst) begin
                if(rst)temp<=0;
                else if(E)temp<=D;
            end
        end
        assign out = temp;
    end
else assign out=D;
endgenerate
endmodule
```

```
module DSP48A1(A,B,Bcin,C,D,carryin,M,P,carryout,
carryoutF,clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode
,ceP,rstA,rstB,rstC,rstcarryin,rstD,rstM,rstopmode,rstP,Bcout,Pcin,Pcout);
```

```
//parameters
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
parameter RSTTYPE = "SYNC";
```

```
//inputs
input [17:0] A,B,D;
input [47:0] C,Pcin;
input [17:0] Bcin;
input clk,carryin;
input [7:0] opmode;
input rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
input ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;
```

```
//outputs
output [17:0] Bcout;
output [47:0] Pcout,P;
output [35:0] M;
output carryout,carryoutF;
```

```
//wires
wire [17:0] Bmux_out;
wire [17:0] A0REG_out,B0REG_out,DREG_out,A1REG_out,adder1,adder1_mux_out,B1REG_out;
wire [47:0] CREG_out,PREG_out;
wire [35:0] multiply_out,MREG_out,M_buff;
wire carryin_MUX_out,CIN;
wire [7:0] opmode_reg_out;
wire [47:0] DAB_conc;
wire [47:0] Xmux_out,Zmux_out,adder2_out;
```

```

//reg
reg [47:0] reg_X_temp, reg_Z_temp;

//
// verilog design
//

assign Bmux_out=(B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? Bcin:0;

sel_reg #(18,A0REG,RSTTYPE) _A0REG(A,clk,ceA,rstA,A0REG_out);//A0REG
sel_reg #(18,A1REG,RSTTYPE) _A1REG(A0REG_out,clk,ceA,rstA,A1REG_out);//A1REG
sel_reg #(18,B0REG,RSTTYPE) _B0REG(Bmux_out,clk,ceB,rstB,B0REG_out);//B0REG
sel_reg #(48,CREG,RSTTYPE) _CREG (C,clk,ceC,rstC,CREG_out);//CREG
sel_reg #(18,DREG,RSTTYPE) _DREG (D,clk,ceD,rstD,DREG_out);//DREG
sel_reg #(8,OPMODEREG,RSTTYPE) _OPMODEREG(opmode,clk,ceopmode,rstopmode,opmode_reg_out);//opcodereg

assign adder1=(opmode_reg_out[6])? (DREG_out-B0REG_out) : (DREG_out+B0REG_out);//first adder
assign adder1_mux_out=(opmode_reg_out[4])? adder1 : B0REG_out;

sel_reg #(18,B1REG,RSTTYPE) _B1REG(adder1_mux_out,clk,ceB,rstB,B1REG_out); //B1REG

assign Bcout=B1REG_out;

assign multiply_out=A1REG_out*B1REG_out;

sel_reg #(36,MREG,RSTTYPE) _MREG (multiply_out,clk,ceM,rstM,MREG_out);//MREG
assign M_buff=MREG_out;
assign M=M_buff;
assign carryin_MUX_out=(CARRYINSEL == "OPMODE5")? opmode_reg_out[5]:(CARRYINSEL == "CARRYIN")? carryin : 0;

sel_reg #(1,CARRYINREG,RSTTYPE) _CYI(carryin_MUX_out,clk,cecarryin,rstcarryin,CIN);
//

```

```

//
//
always @(*) begin
    case (opmode_reg_out[1:0])
        0:reg_X_temp=0;
        1:reg_X_temp={12'b0,MREG_out};
        2:reg_X_temp=Pcout;
        3:reg_X_temp=DAB_conc;
    endcase
end
assign DAB_conc={DREG_out[11:0],A1REG_out,B1REG_out};
assign Xmux_out=reg_X_temp;
//
//
always @(*) begin
    case (opmode_reg_out[3:2])
        0:reg_Z_temp=0;
        1:reg_Z_temp=Pcin;
        2:reg_Z_temp=Pcout;
        3:reg_Z_temp=CREG_out;
    endcase
end
assign Zmux_out=reg_Z_temp;
assign {carry,adder2_out}=(opmode_reg_out[7])?(Zmux_out-(Xmux_out+carryin)):(Zmux_out+Xmux_out+carryin);

sel_reg #(48,PREG,RSTTYPE) _PREG (adder2_out,clk,ceP,rstP,P);

assign Pcout=P;

sel_reg #(1,CARRYOUTREG,RSTTYPE) _CARRYOUTREG (carry,clk,cecarryin,rstcarryin,carryout);
assign carryoutF=carryout;
assign Pcout=P;
endmodule

```


Testbench Code:

```
module DSP_TB();
    reg [17:0] A,B,D;
    reg [47:0] C,Pcin;
    reg [17:0] Bcin;
    reg clk,carryin;
    reg [7:0] opmode;
    reg rstA,rstB,rstM,rstP,rstC,rstD,rstcarryin,rstopmode;
    reg ceA,ceB,ceM,ceP,ceC,ceD,cecarryin,ceopmode;

    wire [17:0] Bcout_dut;
    wire [47:0] Pcout_dut,P_dut;
    wire [35:0] M_dut;
    wire carryout_dut,carryoutF_dut;

    DSP48A1 dut(A,B,Bcin,C,D,carryin,M_dut,P_dut,carryout_dut,carryoutF_dut,
        clk,opmode,ceA,ceB,ceC,cecarryin,ceD,ceM,ceopmode,ceP,rstA,
        rstB,rstC,rstcarryin,rstD,rstM,rstopmode
        ,rstP,Bcout_dut,Pcin,Pcout_dut);

    initial begin
        clk=0;
        forever begin
            #5;
            clk=~clk;
        end
    end
end
```

```

initial begin
    rstA=1;
    rstB=1;
    rstM=1;
    rstP=1;
    rstC=1;
    rstD=1;
    rstcarryin=1;
    rstopmode=1;
    repeat(50)begin
        ceA=$random;
        ceB=$random;
        ceM=$random;
        ceP=$random;
        ceC=$random;
        ceD=$random;
        cecarryin=$random;
        ceopmode=$random;
        A=$random;
        B=$random;
        D=$random;
        C=$random;
        Pcin=$random;
        Bcin=$random;
        carryin=$random;
        opmode=$random;
        @(negedge clk);
        if(M_dut!=0 || P_dut!=0 || Bcout_dut!=0 || carryout_dut!=0 || carryoutF_dut!=0 || P_dut!=0)begin
            $display("Error");
            $stop;
        end
    end
end

```

```

rstA=0;
rstB=0;
rstM=0;
rstP=0;
rstC=0;
rstD=0;
rstcarryin=0;
rstopmode=0;
ceA=1;
ceB=1;
ceM=1;
ceP=1;
ceC=1;
ceD=1;
cecarryin=1;
ceopmode=1;
A=2;
C=0;
D=1;
B=1;
opmode[6] = 0; //adder1 = D+B
opmode[4] = 1; //adder1_mux_out
opmode[1:0] = 1;
opmode[3:2] = 0;
opmode[7] = 0;
carryin = 0;
@(negedge clk);
//output Bcout =2 , p=2 ,M =2 ,PCout =2
repeat(100) begin
    A=$random;
    B=$random;
    D=$random;
    C=$random;
    Pcin=$random;
    Bcin=$random;
    carryin=$random;
    opmode=$random;
    @(negedge clk);
end
$stop;
end

```

Do file:

```
run_dsp_tb.do
1  vlib work
2  vlog DSP48A1.v sel_reg.v DSP_TB.v
3  vsim -voptargs=+acc work.DSP_TB
4  add wave *
5  run -all
```

QuestaSim Snippets:

QSP_78A	QSP_78B	QSP_78C	QSP_78D	QSP_78E	QSP_78F	QSP_78G	QSP_78H	QSP_78I	QSP_78J	QSP_78K	QSP_78L	QSP_78M	QSP_78N	QSP_78O	QSP_78P	QSP_78Q	QSP_78R	QSP_78S	QSP_78T	QSP_78U	QSP_78V	QSP_78W	QSP_78X	QSP_78Y	QSP_78Z	QSP_78AA	QSP_78AB	QSP_78AC	QSP_78AD	QSP_78AE	QSP_78AF	QSP_78AG	QSP_78AH	QSP_78AI	QSP_78AJ	QSP_78AK	QSP_78AL	QSP_78AM	QSP_78AN	QSP_78AO	QSP_78AP	QSP_78AQ	QSP_78AR	QSP_78AS	QSP_78AT	QSP_78AU	QSP_78AV	QSP_78AW	QSP_78AX	QSP_78AY	QSP_78AZ	QSP_78BA	QSP_78BB	QSP_78BC	QSP_78BD	QSP_78BE	QSP_78BF	QSP_78BG	QSP_78BH	QSP_78BI	QSP_78BJ	QSP_78BK	QSP_78BL	QSP_78BM	QSP_78BN	QSP_78BO	QSP_78BP	QSP_78BQ	QSP_78BR	QSP_78BS	QSP_78BT	QSP_78BU	QSP_78BV	QSP_78BW	QSP_78BX	QSP_78BY	QSP_78BZ	QSP_78CA	QSP_78CB	QSP_78CC	QSP_78CD	QSP_78CE	QSP_78CF	QSP_78CG	QSP_78CH	QSP_78CI	QSP_78CJ	QSP_78CK	QSP_78CL	QSP_78CM	QSP_78CN	QSP_78CO	QSP_78CP	QSP_78CQ	QSP_78CR	QSP_78CS	QSP_78CT	QSP_78CU	QSP_78CV	QSP_78CW	QSP_78CX	QSP_78CY	QSP_78CZ	QSP_78DA	QSP_78DB	QSP_78DC	QSP_78DD	QSP_78DE	QSP_78DF	QSP_78DG	QSP_78DH	QSP_78DI	QSP_78DJ	QSP_78DK	QSP_78DL	QSP_78DM	QSP_78DN	QSP_78DO	QSP_78DP	QSP_78DQ	QSP_78DR	QSP_78DS	QSP_78DT	QSP_78DU	QSP_78DV	QSP_78DW	QSP_78DX	QSP_78DY	QSP_78DZ	QSP_78EA	QSP_78EB	QSP_78EC	QSP_78ED	QSP_78EE	QSP_78EF	QSP_78EG	QSP_78EH	QSP_78EI	QSP_78EJ	QSP_78EK	QSP_78EL	QSP_78EM	QSP_78EN	QSP_78EO	QSP_78EP	QSP_78EQ	QSP_78ER	QSP_78ES	QSP_78ET	QSP_78EU	QSP_78EV	QSP_78EW	QSP_78EX	QSP_78EY	QSP_78EZ	QSP_78FA	QSP_78FB	QSP_78FC	QSP_78FD	QSP_78FE	QSP_78FF	QSP_78FG	QSP_78FH	QSP_78FI	QSP_78FJ	QSP_78FK	QSP_78FL	QSP_78FM	QSP_78FN	QSP_78FO	QSP_78FP	QSP_78FQ	QSP_78FR	QSP_78FS	QSP_78FT	QSP_78FU	QSP_78FV	QSP_78FW	QSP_78FX	QSP_78FY	QSP_78FZ	QSP_78GA	QSP_78GB	QSP_78GC	QSP_78GD	QSP_78GE	QSP_78GF	QSP_78GG	QSP_78GH	QSP_78GI	QSP_78GJ	QSP_78GK	QSP_78GL	QSP_78GM	QSP_78GN	QSP_78GO	QSP_78GP	QSP_78GQ	QSP_78GR	QSP_78GS	QSP_78GT	QSP_78GU	QSP_78GV	QSP_78GW	QSP_78GX	QSP_78GY	QSP_78GZ	QSP_78HA	QSP_78HB	QSP_78HC	QSP_78HD	QSP_78HE	QSP_78HF	QSP_78HG	QSP_78HH	QSP_78HI	QSP_78HJ	QSP_78HK	QSP_78HL	QSP_78HM	QSP_78HN	QSP_78HO	QSP_78HP	QSP_78HQ	QSP_78HR	QSP_78HS	QSP_78HT	QSP_78HU	QSP_78HV	QSP_78HW	QSP_78HX	QSP_78HY	QSP_78HZ	QSP_78IA	QSP_78IB	QSP_78IC	QSP_78ID	QSP_78IE	QSP_78IF	QSP_78IG	QSP_78IH	QSP_78II	QSP_78IJ	QSP_78IK	QSP_78IL	QSP_78IM	QSP_78IN	QSP_78IO	QSP_78IP	QSP_78IQ	QSP_78IR	QSP_78IS	QSP_78IT	QSP_78IU	QSP_78IV	QSP_78IW	QSP_78IX	QSP_78IY	QSP_78IZ	QSP_78JA	QSP_78JB	QSP_78JC	QSP_78JD	QSP_78JE	QSP_78JF	QSP_78JG	QSP_78JH	QSP_78JI	QSP_78JJ	QSP_78JK	QSP_78JL	QSP_78JM	QSP_78JN	QSP_78JO	QSP_78JP	QSP_78JQ	QSP_78JR	QSP_78JS	QSP_78JT	QSP_78JU	QSP_78JV	QSP_78JW	QSP_78JX	QSP_78JY	QSP_78JZ	QSP_78KA	QSP_78KB	QSP_78KC	QSP_78KD	QSP_78KE	QSP_78KF	QSP_78KG	QSP_78KH	QSP_78KI	QSP_78KJ	QSP_78KK	QSP_78KL	QSP_78KM	QSP_78KN	QSP_78KO	QSP_78KP	QSP_78KQ	QSP_78KR	QSP_78KS	QSP_78KT	QSP_78KU	QSP_78KV	QSP_78KW	QSP_78KX	QSP_78KY	QSP_78KZ	QSP_78LA	QSP_78LB	QSP_78LC	QSP_78LD	QSP_78LE	QSP_78LF	QSP_78LG	QSP_78LH	QSP_78LI	QSP_78LJ	QSP_78LK	QSP_78LL	QSP_78LM	QSP_78LN	QSP_78LO	QSP_78LP	QSP_78LQ	QSP_78LR	QSP_78LS	QSP_78LT	QSP_78LU	QSP_78LV	QSP_78LW	QSP_78LX	QSP_78LY	QSP_78LZ	QSP_78MA	QSP_78MB	QSP_78MC	QSP_78MD	QSP_78ME	QSP_78MF	QSP_78MG	QSP_78MH	QSP_78MI	QSP_78MJ	QSP_78MK	QSP_78ML	QSP_78MM	QSP_78MN	QSP_78MO	QSP_78MP	QSP_78MQ	QSP_78MR	QSP_78MS	QSP_78MT	QSP_78MU	QSP_78MV	QSP_78MW	QSP_78MX	QSP_78MY	QSP_78MZ	QSP_78NA	QSP_78NB	QSP_78NC	QSP_78ND	QSP_78NE	QSP_78NF	QSP_78NG	QSP_78NH	QSP_78NI	QSP_78NJ	QSP_78NK	QSP_78NL	QSP_78NM	QSP_78NN	QSP_78NO	QSP_78NP	QSP_78NQ	QSP_78NR	QSP_78NS	QSP_78NT	QSP_78NU	QSP_78NV	QSP_78NW	QSP_78NX	QSP_78NY	QSP_78NZ	QSP_78OA	QSP_78OB	QSP_78OC	QSP_78OD	QSP_78OE	QSP_78OF	QSP_78OG	QSP_78OH	QSP_78OI	QSP_78OJ	QSP_78OK	QSP_78OL	QSP_78OM	QSP_78ON	QSP_78OO	QSP_78OP	QSP_78OQ	QSP_78OR	QSP_78OS	QSP_78OT	QSP_78OU	QSP_78OV	QSP_78OW	QSP_78OX	QSP_78OY	QSP_78OZ	QSP_78PA	QSP_78PB	QSP_78PC	QSP_78PD	QSP_78PE	QSP_78PF	QSP_78PG	QSP_78PH	QSP_78PI	QSP_78PJ	QSP_78PK	QSP_78PL	QSP_78PM	QSP_78PN	QSP_78PO	QSP_78PP	QSP_78PQ	QSP_78PR	QSP_78PS	QSP_78PT	QSP_78PU	QSP_78PV	QSP_78PW	QSP_78PX	QSP_78PY	QSP_78PZ	QSP_78QA	QSP_78QB	QSP_78QC	QSP_78QD	QSP_78QE	QSP_78QF	QSP_78QG	QSP_78QH	QSP_78QI	QSP_78QJ	QSP_78QK	QSP_78QL	QSP_78QM	QSP_78QN	QSP_78QO	QSP_78QP	QSP_78QQ	QSP_78QR	QSP_78QS	QSP_78QT	QSP_78QU	QSP_78QV	QSP_78QW	QSP_78QX	QSP_78QY	QSP_78QZ	QSP_78RA	QSP_78RB	QSP_78RC	QSP_78RD	QSP_78RE	QSP_78RF	QSP_78RG	QSP_78RH	QSP_78RI	QSP_78RJ	QSP_78RK	QSP_78RL	QSP_78RM	QSP_78RN	QSP_78RO	QSP_78RP	QSP_78RQ	QSP_78RR	QSP_78RS	QSP_78RT	QSP_78RU	QSP_78RV	QSP_78RW	QSP_78RX	QSP_78RY	QSP_78RZ	QSP_78SA	QSP_78SB	QSP_78SC	QSP_78SD	QSP_78SE	QSP_78SF	QSP_78SG	QSP_78SH	QSP_78SI	QSP_78SJ	QSP_78SK	QSP_78SL	QSP_78SM	QSP_78SN	QSP_78SO	QSP_78SP	QSP_78SQ	QSP_78SR	QSP_78SS	QSP_78ST	QSP_78SU	QSP_78SV	QSP_78SW	QSP_78SX	QSP_78SY	QSP_78SZ	QSP_78TA	QSP_78TB	QSP_78TC	QSP_78TD	QSP_78TE	QSP_78TF	QSP_78TG	QSP_78TH	QSP_78TI	QSP_78TJ	QSP_78TK	QSP_78TL	QSP_78TM	QSP_78TN	QSP_78TO	QSP_78TP	QSP_78TQ	QSP_78TR	QSP_78TS	QSP_78TT	QSP_78TU	QSP_78TV	QSP_78TW	QSP_78TX	QSP_78TY	QSP_78TZ	QSP_78UA	QSP_78UB	QSP_78UC	QSP_78UD	QSP_78UE	QSP_78UF	QSP_78UG	QSP_78UH	QSP_78UI	QSP_78UJ	QSP_78UK	QSP_78UL	QSP_78UM	QSP_78UN	QSP_78UO	QSP_78UP	QSP_78UQ	QSP_78UR	QSP_78US	QSP_78UT	QSP_78UU	QSP_78UV	QSP_78UW	QSP_78UX	QSP_78UY	QSP_78UZ	QSP_78VA	QSP_78VB	QSP_78VC	QSP_78VD	QSP_78VE	QSP_78VF	QSP_78VG	QSP_78VH	QSP_78VI	QSP_78VJ	QSP_78VK	QSP_78VL	QSP_78VM	QSP_78VN	QSP_78VO	QSP_78VP	QSP_78VQ	QSP_78VR	QSP_78VS	QSP_78VT	QSP_78VU	QSP_78VV	QSP_78VW	QSP_78VX	QSP_78VY	QSP_78VZ	QSP_78WA	QSP_78WB	QSP_78WC	QSP_78WD	QSP_78WE	QSP_78WF	QSP_78WG	QSP_78WH	QSP_78WI	QSP_78WJ	QSP_78WK	QSP_78WL	QSP_78WM	QSP_78WN	QSP_78WO	QSP_78WP	QSP_78WQ	QSP_78WR	QSP_78WS	QSP_78WT	QSP_78WU	QSP_78WV	QSP_78WW	QSP_78WX	QSP_78WY	QSP_78WZ	QSP_78XA	QSP_78XB	QSP_78XC	QSP_78XD	QSP_78XE	QSP_78XF	QSP_78XG	QSP_78XH	QSP_78XI	QSP_78XJ	QSP_78XK	QSP_78XL	QSP_78XM	QSP_78XN	QSP_78XO	QSP_78XP	QSP_78XQ	QSP_78XR	QSP_78XS	QSP_78XT	QSP_78XU	QSP_78XV	QSP_78XW	QSP_78XX	QSP_78XY	QSP_78XZ	QSP_78YA	QSP_78YB	QSP_78YC	QSP_78YD	QSP_78YE	QSP_78YF	QSP_78YG	QSP_78YH	QSP_78YI	QSP_78YJ	QSP_78YK	QSP_78YL	QSP_78YM	QSP_78YN	QSP_78YO	QSP_78YP	QSP_78YQ	QSP_78YR	QSP_78YS	QSP_78YT	QSP_78YU	QSP_78YV	QSP_78YW	QSP_78YX	QSP_78YY	QSP_78YZ	QSP_78ZA	QSP_78ZB	QSP_78ZC	QSP_78ZD	QSP_78ZE	QSP_78ZF	QSP_78ZG	QSP_78ZH	QSP_78ZI	QSP_78ZJ	QSP_78ZK	QSP_78ZL	QSP_78ZM	QSP_78ZN	QSP_78ZO	QSP_78ZP	QSP_78ZQ	QSP_78ZR	QSP_78ZS	QSP_78ZT	QSP_78ZU	QSP_78ZV	QSP_78ZW	QSP_78ZX	QSP_78ZY	QSP_78ZZ
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# input: A = 178975 B = 112491 C = 1263109014 D = 196221 PCin = 281472921665547 Carryin = 1 opmode = 63
# output: Bcout = 92077 PCout = 281474706953440 P = 281474706953440 M = 17205382324 Carry_Out = 0 Carry_OutF = 0
# input: A = 178975 B = 112491 C = 1263109014 D = 196221 PCin = 281472921665547 Carryin = 1 opmode = 63
# output: Bcout = 83987 PCout = 281474706953441 P = 281474706953441 M = 11727018797 Carry_Out = 0 Carry_OutF = 0
# input: A = 120586 B = 146043 C = 281474488630981 D = 243245 PCin = 281474970659583 Carryin = 0 opmode = 215
# output: Bcout = 83987 PCout = 281474706953441 P = 281474706953441 M = 11727018797 Carry_Out = 0 Carry_OutF = 0
# input: A = 120586 B = 146043 C = 281474488630981 D = 243245 PCin = 281474970659583 Carryin = 0 opmode = 215
# output: Bcout = 80120 PCout = 254928719629225 P = 254928719629225 M = 15031573325 Carry_Out = 0 Carry_OutF = 0
# input: A = 239421 B = 202205 C = 281474802871019 D = 72474 PCin = 1766210002 Carryin = 1 opmode = 38
# output: Bcout = 80120 PCout = 254928719629225 P = 254928719629225 M = 15031573325 Carry_Out = 0 Carry_OutF = 0
# input: A = 239421 B = 202205 C = 281474802871019 D = 72474 PCin = 1766210002 Carryin = 1 opmode = 38
# output: Bcout = 41040 PCout = 172799639224537 P = 172799639224537 M = 9661350320 Carry_Out = 1 Carry_OutF = 1
# input: A = 35357 B = 75990 C = 281474026841742 D = 166898 PCin = 281474061863058 Carryin = 0 opmode = 69
# output: Bcout = 41040 PCout = 172799639224537 P = 172799639224537 M = 9661350320 Carry_Out = 1 Carry_OutF = 1
# input: A = 35357 B = 75990 C = 281474026841742 D = 166898 PCin = 281474061863058 Carryin = 0 opmode = 69
# output: Bcout = 75990 PCout = 172798724376939 P = 172798724376939 M = 9825837840 Carry_Out = 1 Carry_OutF = 1
# input: A = 57854 B = 86125 C = 281472867536900 D = 222375 PCin = 281473120009250 Carryin = 0 opmode = 141
# output: Bcout = 75990 PCout = 172798724376939 P = 172798724376939 M = 9825837840 Carry_Out = 1 Carry_OutF = 1
# input: A = 57854 B = 86125 C = 281472867536900 D = 222375 PCin = 281473120009250 Carryin = 0 opmode = 141
# output: Bcout = 86125 PCout = 7969136434 P = 7969136434 M = 2686778430 Carry_Out = 1 Carry_OutF = 1
# input: A = 67845 B = 28987 C = 281473470335052 D = 199119 PCin = 1703015371 Carryin = 0 opmode = 227
# output: Bcout = 86125 PCout = 7969136434 P = 7969136434 M = 2686778430 Carry_Out = 1 Carry_OutF = 1
# input: A = 67845 B = 28987 C = 281473470335052 D = 199119 PCin = 1703015371 Carryin = 0 opmode = 227
# output: Bcout = 28987 PCout = 281470180758470 P = 281470180758470 M = 4982675750 Carry_Out = 0 Carry_OutF = 0
# input: A = 92012 B = 223247 C = 1749545424 D = 55643 PCin = 397528367 Carryin = 0 opmode = 238
# output: Bcout = 28987 PCout = 281470180758470 P = 281470180758470 M = 4982675750 Carry_Out = 0 Carry_OutF = 0
# input: A = 92012 B = 223247 C = 1749545424 D = 55643 PCin = 397528367 Carryin = 0 opmode = 238
# output: Bcout = 223247 PCout = 108902585437893 P = 108902585437893 M = 1966623015 Carry_Out = 1 Carry_OutF = 1
# input: A = 152613 B = 202610 C = 39102212 D = 12980 PCin = 281474173692064 Carryin = 1 opmode = 31
# output: Bcout = 223247 PCout = 108902585437893 P = 108902585437893 M = 1966623015 Carry_Out = 1 Carry_OutF = 1
# input: A = 152613 B = 202610 C = 39102212 D = 12980 PCin = 281474173692064 Carryin = 1 opmode = 31
# output: Bcout = 202610 PCout = 172574140818186 P = 172574140818186 M = 20541402964 Carry_Out = 1 Carry_OutF = 1
# input: A = 14300 B = 23572 C = 281474749205732 D = 30773 PCin = 1730128334 Carryin = 1 opmode = 164
# output: Bcout = 202610 PCout = 172574140818186 P = 172574140818186 M = 20541402964 Carry_Out = 1 Carry_OutF = 1
# input: A = 14300 B = 23572 C = 281474749205732 D = 30773 PCin = 1730128334 Carryin = 1 opmode = 164
# output: Bcout = 36552 PCout = 47593923788407 P = 47593923788407 M = 30920919930 Carry_Out = 0 Carry_OutF = 0
# input: A = 224346 B = 6157 C = 711689044 D = 68102 PCin = 281474683005660 Carryin = 0 opmode = 55
# output: Bcout = 36552 PCout = 47593923788407 P = 47593923788407 M = 30920919930 Carry_Out = 0 Carry_OutF = 0
# input: A = 224346 B = 6157 C = 711689044 D = 68102 PCin = 281474683005660 Carryin = 0 opmode = 55
# output: Bcout = 6157 PCout = 281474683005660 P = 281474683005660 M = 522693600 Carry_Out = 0 Carry_OutF = 0
# input: A = 21579 B = 207623 C = 793864030 D = 83545 PCin = 1797362134 Carryin = 1 opmode = 202
# output: Bcout = 6157 PCout = 281474683005660 P = 281474683005660 M = 522693600 Carry_Out = 0 Carry_OutF = 0
# input: A = 21579 B = 207623 C = 793864030 D = 83545 PCin = 1797362134 Carryin = 1 opmode = 202
# output: Bcout = 13581 PCout = 176394785630692 P = 176394785630692 M = 1381298322 Carry_Out = 0 Carry_OutF = 0
# input: A = 216923 B = 161096 C = 686430545 D = 36096 PCin = 281473877244540 Carryin = 1 opmode = 25
# output: Bcout = 13581 PCout = 176394785630692 P = 176394785630692 M = 1381298322 Carry_Out = 0 Carry_OutF = 0
# input: A = 216923 B = 161096 C = 686430545 D = 36096 PCin = 281473877244540 Carryin = 1 opmode = 25
# output: Bcout = 161096 PCout = 281474976710655 P = 281474976710655 M = 293064399 Carry_Out = 1 Carry_OutF = 1
# input: A = 48319 B = 186257 C = 281474460383938 D = 147055 PCin = 281473902609535 Carryin = 1 opmode = 24
# output: Bcout = 161096 PCout = 281474976710655 P = 281474976710655 M = 293064399 Carry_Out = 1 Carry_OutF = 1
# input: A = 48319 B = 186257 C = 281474460383938 D = 147055 PCin = 281473902609535 Carryin = 1 opmode = 24
# output: Bcout = 222353 PCout = 293064399 P = 293064399 M = 34945427608 Carry_Out = 1 Carry_OutF = 1
# input: A = 65047 B = 77806 C = 281473701604455 D = 113169 PCin = 281472941495309 Carryin = 1 opmode = 66
# output: Bcout = 222353 PCout = 293064399 P = 293064399 M = 34945427608 Carry_Out = 1 Carry_OutF = 1
# input: A = 65047 B = 77806 C = 281473701604455 D = 113169 PCin = 281472941495309 Carryin = 1 opmode = 66
# output: Bcout = 224861 PCout = 293064400 P = 293064400 M = 10743874607 Carry_Out = 0 Carry_OutF = 0
# ** Note: $stop : DSP_TB.v(102)
# Time: 1510 ns Iteration: 1 Instance: /DSP_TB
# Break in Module DSP_TB at DSP_TB.v line 102

```

Constraint File:

```

6  ## Clock signal
7  set_property -dict { PACKAGE_PIN W5    IOSTANDARD LVCMOS33 } [get_ports clk]
8  create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10

```

The screenshot shows the 'Messages' window in Vivado. The top bar has tabs for 'Tcl Console', 'Messages', 'Log', 'Reports', 'Design Runs', and 'Find Results'. Below the tabs is a search bar and a list of message types: 'Warning (65)', 'Info (53)', and 'Status (24)'. A 'Show All' button is on the right. The message list is expanded to show 'Vivado Commands (3 infos)', which is further expanded to 'General Messages (3 infos)'. These three messages are all 'Info' type and relate to IP repositories. Below this, 'Elaborated Design (22 warnings, 18 infos)' is expanded to 'General Messages (22 warnings, 18 infos)'. The first message in this list is a 'Warning' (yellow icon) about overwriting the definition of module DSP48A1. The second message is an 'Info' (blue icon) about synthesizing the module DSP48A1.

Tcl Console Messages x Log Reports Design Runs Find Results

Warning (65) Info (53) Status (24) Show All

Vivado Commands (3 infos)

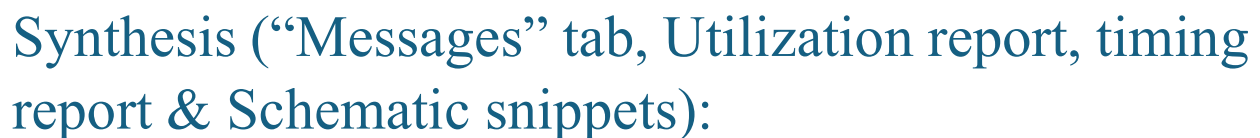
General Messages (3 infos)

- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.

Elaborated Design (22 warnings, 18 infos)

General Messages (22 warnings, 18 infos)

- [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
- [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)



Tcl Console Messages Log Reports Design Runs

Warning (43) Info (41) Status (21) Show All

- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- Synthesis (43 warnings, 32 infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
 - [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
 - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)
 - [Synth 8-6155] done synthesizing module 'sel_reg' (1#1) [sel_reg.v:1] (6 more like this)
 - [Synth 8-3331] design sel_reg has unconnected port clk (38 more like this)
 - [Device 21-403] Loading part xc7a200tffg1156-3

Tcl Console Messages Log Reports Design Runs Utilization x Timing						
Hierarchy						
Hierarchy Summary						
▼ Slice Logic						
▼ Slice LUTs (<1%)						
LUT as Logic (<1%)						
▼ Slice Registers (<1%)						
Register as Flip Flop (<1%)						
Memory						
▼ DSP						
▼ DSPs (<1%)						
DSP48E1 only						
▼ IO and GT Specific						
▼ Bonded IOB (65%)						
IOB Master Pads						
▼ Clocking						
BUFGCTRL (3%)						
Specific Feature						
Primitives						
Black Boxes						
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
▼ DSP48A1	229	158	1	327	1	
_A1REG (sel_reg_pa...	0	18	0	0	0	
_B1REG (sel_reg_pa...	0	18	0	0	0	
_CARRYOUTREG (sel...	0	1	0	0	0	
_CREG (sel_reg_par...	0	48	0	0	0	
_DREG (sel_reg_par...	0	18	0	0	0	
_MREG (sel_reg_par...	0	0	1	0	0	
_OPMODEREG (sel_f...	228	7	0	0	0	
_PREG (sel_reg_paf...	0	48	0	0	0	

Tcl ConsoleMessagesLogReportsDesign RunsUtilizationTiming x

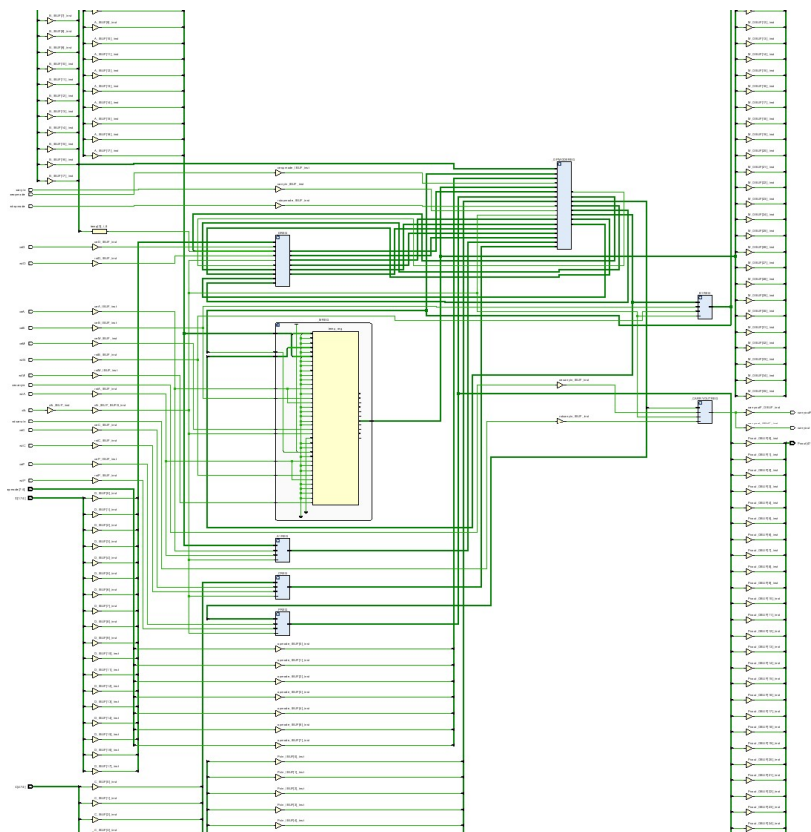
Q

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (329)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.168 ns	Worst Hold Slack (WHS): 0.339 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 86	Total Number of Endpoints: 86	Total Number of Endpoints: 160

All user specified timing constraints are met.



Implementation (“Messages” tab, Utilization report, timing report & device snippets):

Tcl Console Messages x Log Reports Design Runs Power DRC Methodology Timing

Warning (45) Info (226) Status (461) Show All

- Vivado Commands (3 infos)
 - General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'
 - Synthesis (43 warnings, 32 infos)
 - [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
 - [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
 - [Synth 8-6157] synthesizing module 'DSP48A1' [DSP48A1.v:1] (6 more like this)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization x

Hierarchy

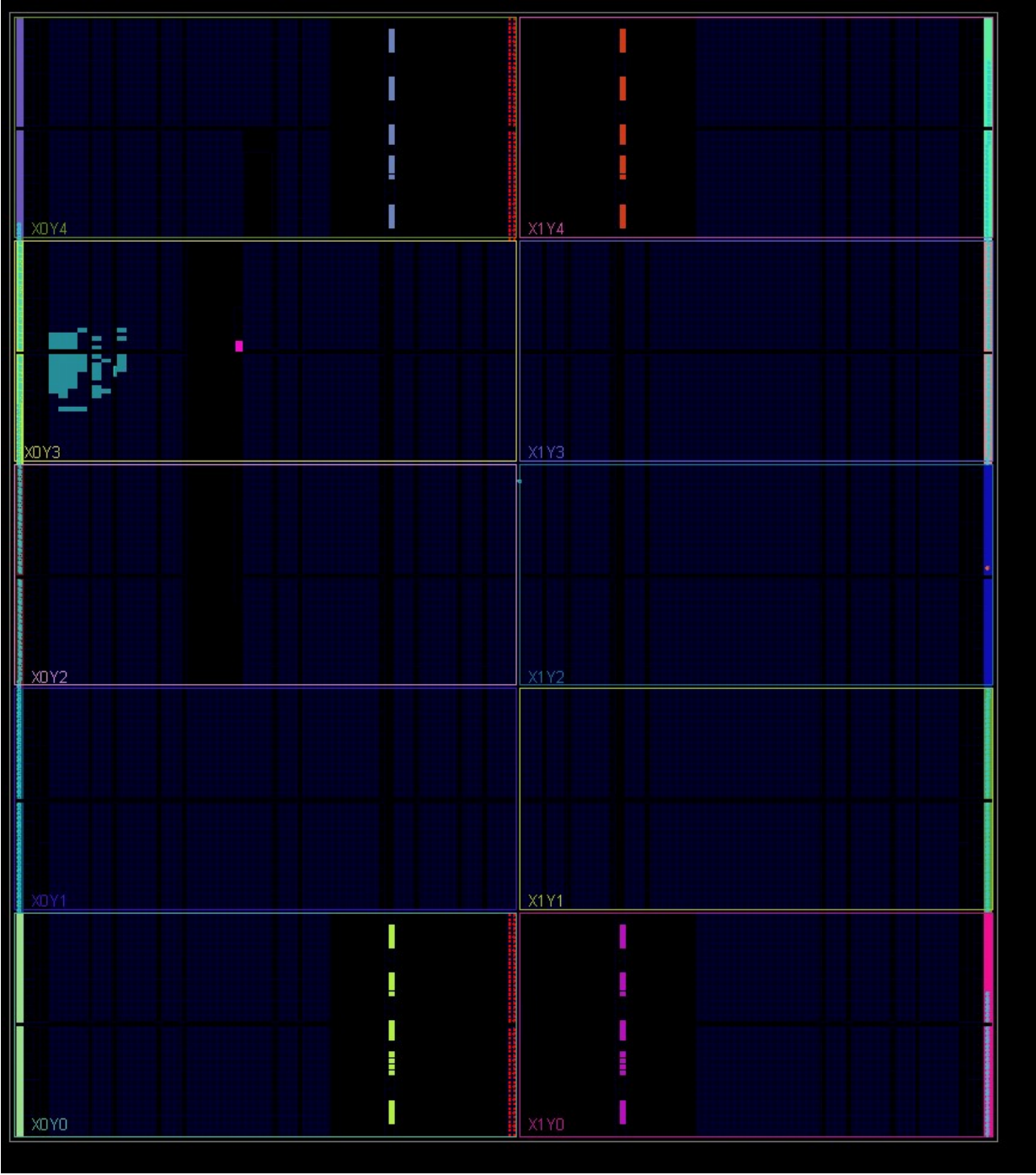
Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (3345 0)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	228	177	103	228	51	1	327	1
_A1REG(sel_reg_pa...	0	18	5	0	0	0	0	0
_B1REG(sel_reg_pa...	0	36	15	0	0	0	0	0
_CARRYOUTREG(sel...	0	2	2	0	0	0	0	0
_CREG(sel_reg_par...	0	48	17	0	0	0	0	0
_DREG(sel_reg_par...	0	18	9	0	0	0	0	0
_MREG(sel_reg_par...	0	0	0	0	0	1	0	0
_OPMODEREG(sel_r...	228	7	70	228	0	0	0	0
_PREG(sel_reg_par...	0	48	12	0	0	0	0	0

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x Utilization

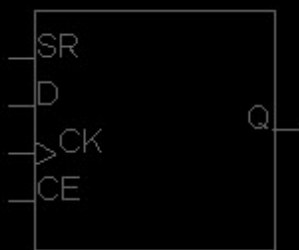
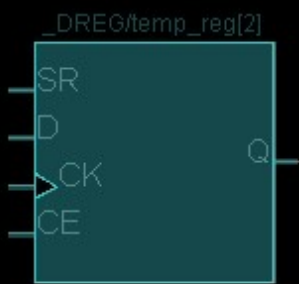
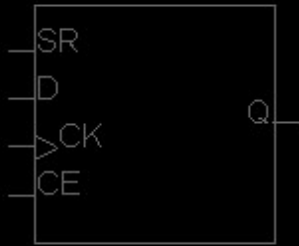
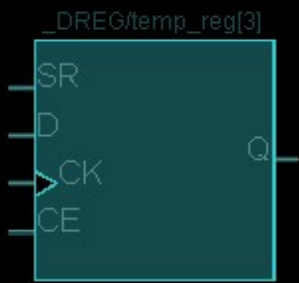
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.136 ns	Worst Hold Slack (WHS): 0.435 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 105	Total Number of Endpoints: 105	Total Number of Endpoints: 179

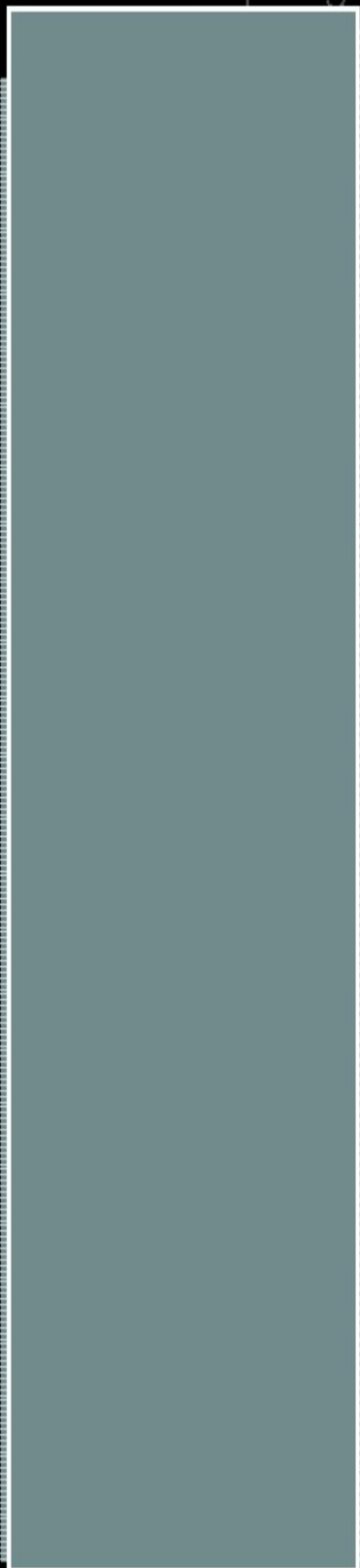
All user specified timing constraints are met.







MREG/temp_reg



MREG/temp_reg

