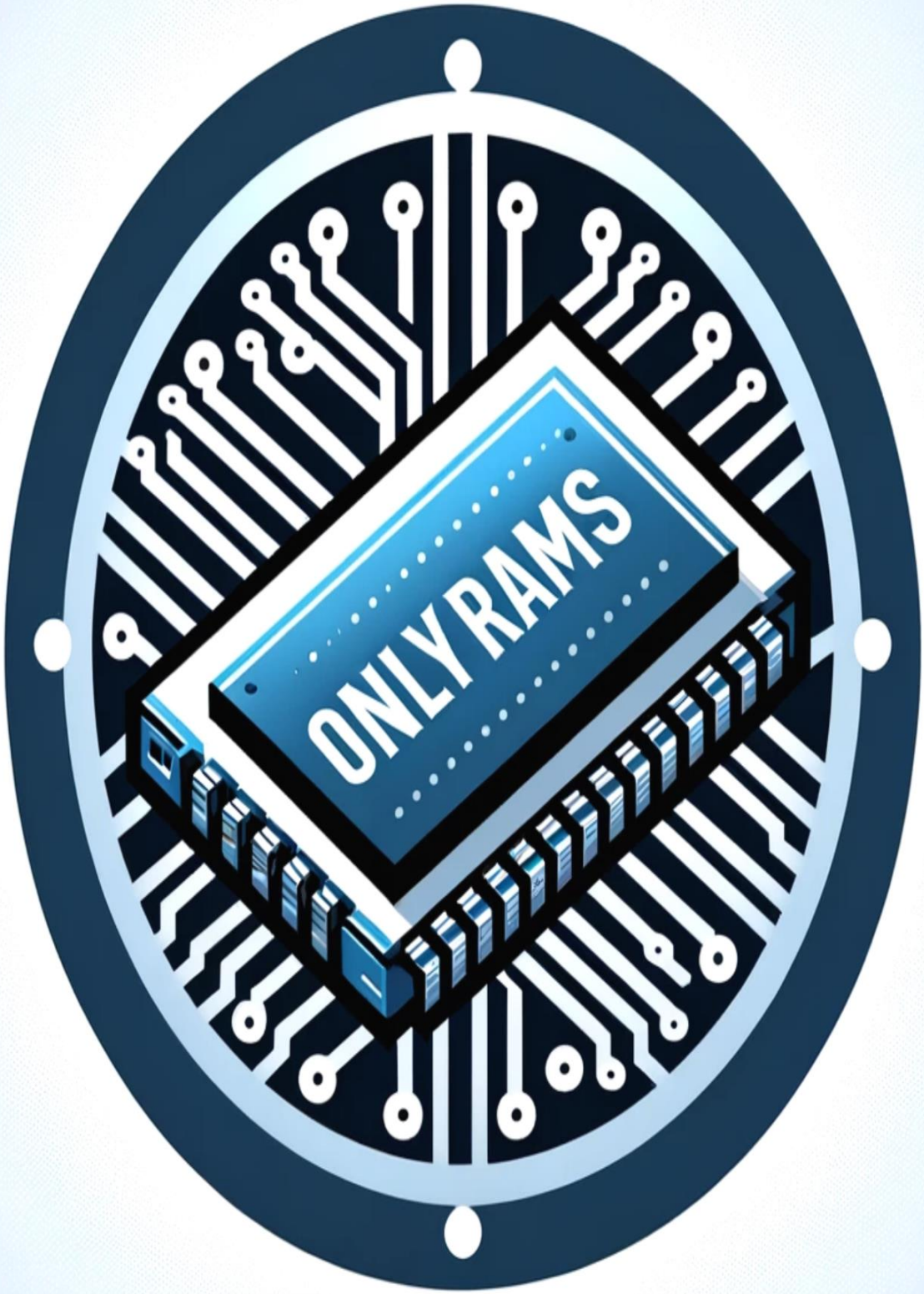
ONLYRAMS

Final Project

SPI slave with single port RAM

ONLY RAMS

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First: RTL design

Single port Ram RTL code:

E: > Digital Design course > project_2 > codes > Single_Port_Async_RAM.v

```v
module Single_Port_Async_RAM (din,clk,rst_n,rx_valid,dout,tx_valid);

parameter MEM_DEPTH = 256;
parameter ADDR_SIZE = 8;

input [9:0] din;
input clk, rx_valid, rst_n; //active low synchronous

//Vivado may not be accepting the asynchronous control signals and may not map them directly on the FPGA board as
//FSM or RAM. If you experience this during implementation, then change the reset to be synchronized with the clock.
//so  used the active low synch rst
output reg [7:0] dout;
output reg tx_valid;

reg [7:0] RAM [MEM_DEPTH - 1 : 0];

// Two Address for write and read respectively
reg [ADDR_SIZE - 1 : 0] Wr_Addr, Rd_Addr;
```

```v

// read/write-----> address
always @(posedge clk) begin
    if (~rst_n) begin
        dout <= 0;
        tx_valid <= 0;
        Wr_Addr <= 0;
        Rd_Addr <= 0;
    end
    else begin
        //to "Read Data" tx_valid must be -> 1 in order to read data from the SPI slave
        tx_valid <= (din[9] & din[8] & rx_valid)? 1 : 0;
        //rx_valid -> 1 , the din[7:0] is accepted
        if (rx_valid) begin
            case (din[9:8])
                2'b00 : Wr_Addr <= din[7:0];      // Write Address
                2'b01 : RAM[Wr_Addr] <= din[7:0]; // Write Data
                2'b10 : Rd_Addr <= din[7:0];      // Read Address
                2'b11 : dout <= RAM[Rd_Addr];     // Read Data
            endcase
        end
    end
end
endmodule
```

SPI slave RTL code:

E: > Digital Design course > project_2 > codes > SPI_Slave_Interface.v

```
1  module SPI_Slave_Interface (MOSI,MISO,SS_n,clk,rst_n,rx_data,rx_valid,tx_data,tx_valid);
2
3  parameter IDLE = 3'b000;
4  parameter CHK_CMD = 3'b001;
5  parameter WRITE = 3'b010;
6  parameter READ_ADD = 3'b011;
7  parameter READ_DATA = 3'b100;
8
9  //FSM Encoding Method ----->GRAY
10
11 (* fsm_encoding = "gray" *)
12
13 // Input Declaration
14 input MOSI, SS_n, clk, rst_n, tx_valid; //Active Low SYNC rst
15 input [7:0] tx_data;
16
17 output reg MISO, rx_valid;
18 output reg [9:0] rx_data;
19
20 //ensure that Read Address Comes 1st and Read Data Comes 2nd
21 reg rd_addr_recieved; //high ---> READ SIGNAL IS RECEIVED
22
23 reg [2:0] cs, ns;
24 reg[3:0] counter;
25
```

```
26
27 // State Memory Logic
28 always @(posedge clk) begin
29     if (~rst_n)
30         cs <= IDLE;
31     else
32         cs <= ns;
33 end
34
```

```
35  // Next State Logic
36 always @(*) begin
37     case (cs)
38         IDLE :
39             begin
40                 if (SS_n)
41                     ns = IDLE;
42                 else
43                     ns = CHK_CMD;
44             end
```

```
45          CHK_CMD :
46              begin
47                  if (SS_n)
48                      ns = IDLE;
49                  else if (~MOSI)
50                      ns = WRITE;
51                  else if (~rd_addr_recieved)
52                      ns = READ_ADD;
53                  else
54                      ns = READ_DATA;
55              end
56          WRITE :
57              begin
58                  if (SS_n)
59                      ns = IDLE;
60                  else
61                      ns = WRITE;
62              end
63          READ_ADD :
64              begin
65                  if (SS_n)
66                      ns = IDLE;
67                  else
68                      ns = READ_ADD;
69              end
```

```
69              end
70          READ_DATA :
71              begin
72                  if (SS_n)
73                      ns = IDLE;
74                  else
75                      ns = READ_DATA;
76              end
77          default : ns = IDLE;
78      endcase
79  end
80
```

```
80  //output logic
81  always @(posedge clk) begin
82      if (~rst_n) begin
83          rx_data <= 0;
84          rx_valid <= 0;
85          rd_addr_recieved <= 0;
86          MISO <= 0;
87          counter <= 0;
88      end
```

```
    else begin
        case (cs)
            IDLE :
                begin
                    counter <= 0;
                    rx_valid <= 0;
                    MISO <= 0;
                end
            CHK_CMD :
                begin
                    counter <= 0;
                    rx_valid <= 0;
                end
            WRITE :
                begin
                    if (counter <= 9) begin
                        rx_data <= {rx_data[8:0],MOSI};
                        rx_valid <= 0;
                        counter <= counter + 1;
                    end
                    if (counter >= 9) begin
                        rx_valid <= 1;
                    end
                end
```

```
            READ_ADD :
                begin
                    if (counter <= 9) begin
                        rx_data <= {rx_data[8:0],MOSI};
                        rx_valid <= 0;
                        rd_addr_recieved <= 1;
                        counter <= counter + 1;
                    end
                    if (counter >= 9)
                        rx_valid <= 1;
                end
            READ_DATA :
                begin
                    if(tx_valid && counter >= 3) begin
                        MISO <= tx_data[counter - 3];
                        counter <= counter - 1;
                    end
                    else
                    if(counter <= 9) begin
                        rx_data <= {rx_data[8:0],MOSI}; // recieved bits are MSB TO LSB
                        rx_valid <= 0;
                        counter <= counter + 1;
                    end
                    if(counter >= 9) begin
                        rx_valid <= 1;
                        rd_addr_recieved <= 0;
                    end
                end
        endcase
    end
end
endmodule
```

SPI Wrapper RTL code (TOP module):

E: > Digital Design course > project_2 > codes > SPI_Wrapper.v

```
1  module SPI_Wrapper (MOSI,MISO,SS_n,clk,rst_n);
2
3  parameter MEM_DEPTH = 256;
4  parameter ADDR_SIZE = 8;
5
6  input MOSI, SS_n, clk, rst_n;
7  // SS_n == 0 then, master begin Communication
8  // SS_n == 1 then, master end Communication
9  output MISO;
10
11 wire [9:0] rx_data_din;
12 wire rx_valid;
13 wire [7:0] tx_data_dout;
14 wire tx_valid;
15
16 SPI_Slave_Interface SPI_Slave_inst (MOSI,MISO,SS_n,clk,rst_n,rx_data_din,rx_valid,tx_data_dout,tx_valid);
17
18 Single_Port_Async_RAM #(MEM_DEPTH,ADDR_SIZE) RAM_inst (rx_data_din,clk,rst_n,rx_valid,tx_data_dout,tx_valid);
19
20 endmodule
```

mem.text:

//It is a 254 rows text of randomized numbers which will be used in the testbench

E: > Digital Design course > project_2 > codes > mem.txt

```
1  7B
2  E9
3  CA
4  B0
5  39
6  8E
7  13
8  C7
9  63
```

Second: Testbench

//Testbench scenario:

```
//TESTBENCH PLAN
//=========================================
//testbench will go as follow:
//=========================================
//rst check
//normal test for RAM read operation --> working on the FSM diagram
//normal test for RAM write operation -->  working on the FSM diagram
//test on write address separately---> followed by write data test (self checking)
//test on read address separately---> followed by read data test    (self checking)
//the verification engineer is acting as the master in giving values (self checking)
```

//tb module:

E: > Digital Design course > project_2 > codes > SPI_Master_tb.v

```
module SPI_Master_tb ();

parameter MEM_DEPTH = 256 ;
parameter ADDR_SIZE = 8 ;
reg clk , rst_n , MOSI , SS_n;
wire MISO;

SPI_Wrapper #(MEM_DEPTH,ADDR_SIZE) DUT (MOSI,MISO,SS_n,clk,rst_n);

// Clock Generation
initial begin
    clk = 0;
    forever
        #5 clk = ~clk; // then negedge sequence will be 0, 10, 20, .... SO,CLK Period = 10
end

reg [7:0] wr_add, rd_add;
reg [7:0] wr_data, rd_data;

```

//RESET check:

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```
31  // Signal to Check MOSI Sequence in Read Operation
32  reg read_sequence;
33
34
35  initial begin
36
37      $readmemh ("mem.txt",DUT.RAM_inst.RAM);
38
39      $display("Test Reset Operation");
40      rst_n = 0;
41      {wr_add,rd_add,wr_data,rd_data} = 4'b0000;
42      repeat(5) begin
43          MOSI = $random;
44          SS_n = $random;
45          @(negedge clk);
46      end
47      rst_n = 1;
```

//normal read operation of RAM:

```
48
49      read_sequence = 1; // Initially Ensure That The Read Sequence is Correct
50
51      $display("Test Normal RAM Read Operation");
52      repeat(4) begin
53          SS_n = 0; // Start Communication
54          MOSI = $random;
55          @(negedge clk);
56          MOSI = 1; // Read Operation
57          read_sequence = ~read_sequence;
58
59          @(negedge clk); // din[9] = 1'b1
60          @(negedge clk); // din[9:8] = 2'b11
61          MOSI = read_sequence;
62          repeat(10) begin
63              @(negedge clk);
64              MOSI = $random;
65          end
66          if (~read_sequence)
67              SS_n = 1; // End Communication
68          else begin
69              repeat(8) @(negedge clk);
70          end
71          SS_n = 1;
72          repeat(3) @(negedge clk);
73      end
74
```

//normal write operation of RAM

```
76      $display("Test Normal RAM Write Operation");
77      // Second Test Write Operation
78      repeat(4) begin
79          SS_n = 0;
80          MOSI = $random;
81          @(negedge clk);
82          MOSI = 0; // Write Operation
83          @(negedge clk); // din[9] = 1'b0;
84          @(negedge clk); // din[9:8] = 2'b00;
85          MOSI = $random;
86          repeat(10) begin // Data to be Written
87              @(negedge clk);
88              MOSI = $random;
89          end
90          SS_n = 1;
91          repeat(3) @(negedge clk);
92      end
```

//write address operation test:

```
94      //testing for each operation separatly
95      $display("Write Address Operation");
96      SS_n = 0;
97      @(negedge clk);
98      MOSI = 0;
99      repeat(3) @(negedge clk);
100
101     repeat (8) begin
102         MOSI = $random;
103         wr_add = {wr_add[6:0],MOSI};
104         @(negedge clk);
105     end
106     SS_n = 1;
107     @(negedge clk);
108     // Check for Write Address Value
109     if (DUT.RAM_inst.Wr_Addr == wr_add)
110         $display("Write Address is Done Correctly");
111     else begin
112         $display("Error in Write Address");
113         $stop;
114     end
115     @(negedge clk);
116
```

//write data operation test:

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```
    $display("Write Data Operation");
    SS_n = 0;
    @(negedge clk);

    MOSI = 0;
    repeat(2) @(negedge clk);
    MOSI = 1;
    @(negedge clk);

    repeat(8) begin
        MOSI = $random;
        wr_data = {wr_data[6:0],MOSI};
        @(negedge clk);
    end
    SS_n = 1;
    @(negedge clk);
    // Check for Write Data Value
    if (DUT.RAM_inst.RAM[DUT.RAM_inst.Wr_Addr] == wr_data)
        $display("Write Data is Done Correctly");
    else begin
        $display("Error in Write Data");
        $stop;
    end
    @(negedge clk);
```

//read address operation test:

```

    $display("Read Address Operation");
    SS_n = 0;
    @(negedge clk);
    MOSI = 1;
    repeat(2) @(negedge clk);
    MOSI = 0;
    @(negedge clk);

    repeat(8) begin
        MOSI = $random;
        rd_add = {rd_add[6:0],MOSI};
        @(negedge clk);
    end
    SS_n = 1;
    @(negedge clk);
    // Check for Read Address
    if (DUT.RAM_inst.Rd_Addr == rd_add)
        $display("Read Address is Done Correctly");
    else begin
        $display("Error in Read Address");
        $stop;
    end
    @(negedge clk);
```

//read data operation test:

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```
    $display("Read Data Operation");
    SS_n = 0;
    @(negedge clk);
    MOSI = 1;
    repeat(3) @(negedge clk);

    repeat(8) begin
        MOSI = $random; //--------------->dummy values
        @(negedge clk);
    end
    @(negedge clk);

    repeat(8) begin
        @(negedge clk);
        rd_data = {rd_data[6:0],MISO};
    end
    SS_n = 1;
    @(negedge clk);
    // Check for Read Addresss
    if (DUT.RAM_inst.RAM[DUT.RAM_inst.Rd_Addr] == rd_data)
        $display("Read Data is Done Correctly");
    else begin
        $display("Error in Read Data");
        $stop;
    end
    repeat(2) @(negedge clk);

    $stop;
end
```

//monitoring

```

initial
$monitor("MOSI = %b, MISO = %b, SS_n = %b, clk = %b, rst_n = %b, rx_data = %d, rx_valid = %b, tx_data = %d, tx_valid = %b, TIME=  %t",
        MOSI,MISO,SS_n,clk,rst_n,DUT.rx_data_din,DUT.rx_valid,DUT.tx_data_dout,DUT.tx_valid, $time);

endmodule
```

Third: DO file

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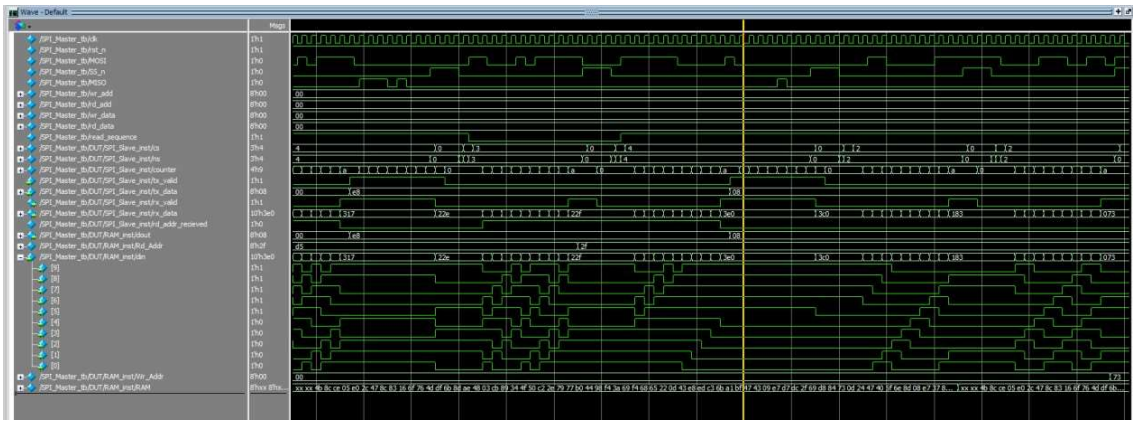
E: > Digital Design course > project_2 > codes > spi.do.txt

```
vlib work
vlog SPI_Slave_Interface.v Single_Port_Async_RAM.v SPI_Wrapper.v SPI_Master_tb.v
vsim -voptargs=+acc work.SPI_Master_tb
add wave *
add wave -position insertpoint  \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/cs \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/ns \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/counter \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/tx_valid \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/tx_data \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/rx_valid \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/rx_data \
sim:/SPI_Master_tb/DUT/SPI_Slave_inst/rd_addr_recieved \
sim:/SPI_Master_tb/DUT/RAM_inst/dout \
sim:/SPI_Master_tb/DUT/RAM_inst/Rd_Addr \
sim:/SPI_Master_tb/DUT/RAM_inst/din \
sim:/SPI_Master_tb/DUT/RAM_inst/Wr_Addr \
sim:/SPI_Master_tb/DUT/RAM_inst/RAM
run -all
```

Fourth: Questa snippets



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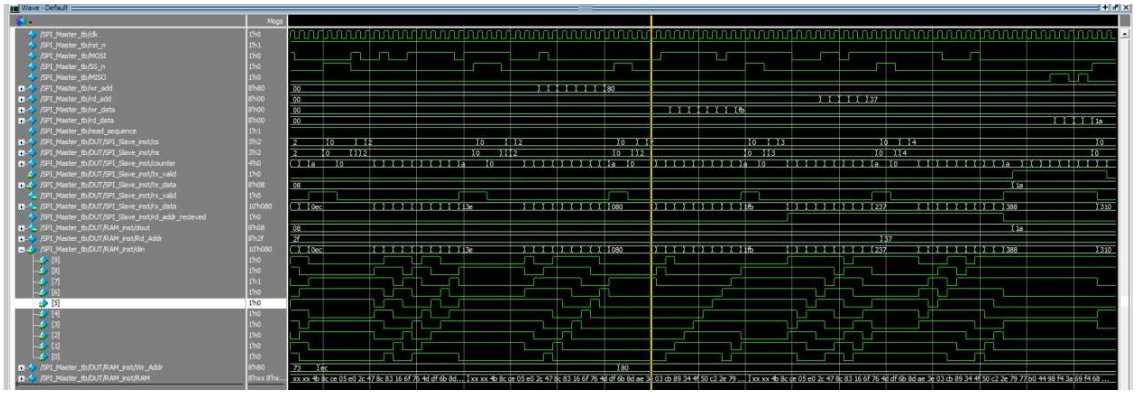

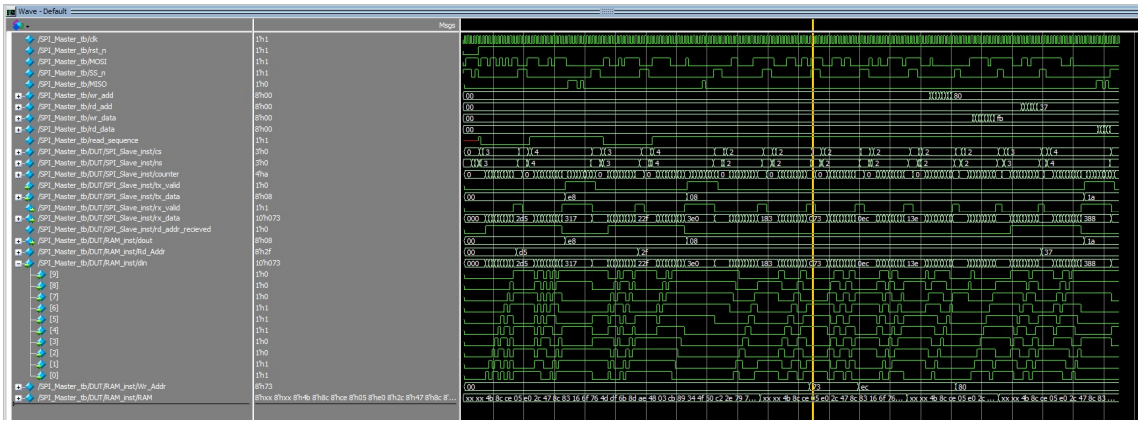

```
# Test Reset Operation
# MOSI = 0, MISO = x, SS_n = 1, clk = 0, rst_n = 0, rx_data =    x, rx_valid = x, tx_data =   x, tx_valid = x, TIME=                0
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                5
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               10
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               15
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               20
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               25
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               30
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               35
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               40
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 0, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               45
```

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```
# Test Normal RAM Read Operation
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                50
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                55
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                60
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                65
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    0, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                70
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    1, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                75
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    1, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                80
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    2, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                85
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    2, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                90
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    5, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=                95
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    5, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               100
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   11, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               105
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   11, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               110
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   22, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               115
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   22, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               120
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   45, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               125
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   45, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               130
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   90, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               135
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   90, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               140
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  181, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               145
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  181, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               150
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  362, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               155
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  362, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               160
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               165
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               170
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               175
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               180
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               185
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               190
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               195
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               200
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               205
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               210
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               215
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               220
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               225
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  725, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               230
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  427, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               235
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  427, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               240
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  855, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               245
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  855, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               250
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  686, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               255
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  686, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               260
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  348, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               265
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  348, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               270
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  696, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               275
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  696, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               280
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  369, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               285
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  369, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               290
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  738, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               295
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  738, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               300
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  453, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               305
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  453, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               310
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  907, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               315
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  907, rx_valid = 0, tx_data =   0, tx_valid = 0, TIME=               320
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               325
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data =   0, tx_valid = 0, TIME=               330
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=               335
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=               340
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Only RAMS

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# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  345
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  350
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  355
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  360
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  365
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  370
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  375
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  380
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  385
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  390
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  395
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  400
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  405
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  410
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  415
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  791, rx_valid = 1, tx_data = 232, tx_valid = 1, TIME=  420
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 1, TIME=  425
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 1, TIME=  430
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  435
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  440
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  445
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  450
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  455
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  460
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  465
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  558, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  470
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   93, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  475
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   93, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  480
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  186, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  485
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  186, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  490
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  372, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  495
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  372, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  500
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  744, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  505
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  744, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  510
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  465, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  515
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  465, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  520
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  930, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  525
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  930, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  530
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  837, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  535
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  837, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  540
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  651, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  545
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  651, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  550
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  279, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  555
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  279, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  560
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  565
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  570
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  575
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  580
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  585
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  590
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  595
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  600
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  605
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  610
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  615
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  620
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  625
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  559, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  630
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   95, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  635
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# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   95, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  640
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  191, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  645
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  191, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  650
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  383, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  655
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  383, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  660
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  767, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  665
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  767, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  670
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  511, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  675
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  511, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  680
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1022, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  685
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1022, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  690
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1020, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  695
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1020, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  700
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1016, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  705
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1016, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  710
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1008, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  715
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1008, rx_valid = 0, tx_data = 232, tx_valid = 0, TIME=  720
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  725
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data = 232, tx_valid = 0, TIME=  730
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  735
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  740
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  745
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  750
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  755
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  760
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  765
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  770
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  775
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  780
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  785
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  790
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  795
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  800
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  805
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  810
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  815
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  992, rx_valid = 1, tx_data =   8, tx_valid = 1, TIME=  820
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 1, TIME=  825
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 1, TIME=  830
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=  835
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=  840
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=  845
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# Test Normal RAM Write Operation
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                850
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                855
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                860
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                865
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  960, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                870
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  896, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                875
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  896, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                880
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  769, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                885
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  769, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                890
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  515, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                895
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  515, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                900
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    6, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                905
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    6, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                910
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   12, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                915
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   12, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                920
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   24, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                925
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   24, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                930
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   48, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                935
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   48, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                940
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   96, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                945
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   96, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                950
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  193, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                955
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  193, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                960
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                965
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                970
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                975
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                980
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                985
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                990
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                995
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1000
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1005
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1010
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1015
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1020
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1025
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  387, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1030
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  774, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1035
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  774, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1040
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  524, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1045
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  524, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1050
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   24, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1055
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   24, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1060
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   49, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1065
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   49, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1070
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   99, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1075
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   99, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1080
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  199, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1085
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  199, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1090
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  398, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1095
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  398, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1100
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  796, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1105
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  796, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1110
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  569, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1115
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  569, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1120
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1125
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1130
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1135
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1140
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1145
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1150
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1155
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1160
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1165
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1170
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1175
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1180
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1185
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  115, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1190
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  230, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1195
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  230, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1200
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  460, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1205
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  460, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1210
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  921, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1215
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  921, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1220
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  819, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1225
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  819, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1230
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  615, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1235
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  615, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1240
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  206, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1245
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  206, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1250
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  413, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1255
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  413, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1260
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  827, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1265
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  827, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1270
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  630, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1275
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  630, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1280
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1285
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1290
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1295
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1300
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1305
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1310
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1315
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1320
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1325
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1330
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1335
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1340
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1345
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  236, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1350
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  472, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1355
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  472, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1360
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  945, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1365
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  945, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1370
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  866, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1375
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  866, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1380
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  708, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1385
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  708, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1390
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  393, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1395
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  393, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1400
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  787, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1405
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  787, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1410
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  551, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1415
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  551, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1420
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   79, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1425
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   79, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1430
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  159, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1435
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  159, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=               1440
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=               1445
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Only RAMS

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# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1445
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1450
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1455
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1460
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1465
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1470
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1475
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1480
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1485
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# Write Address Operation
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1490
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1495
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1500
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1505
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  318, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1510
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  636, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1515
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  636, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1520
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  248, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1525
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  248, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1530
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  497, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1535
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  497, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1540
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  994, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1545
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  994, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1550
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  964, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1555
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  964, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1560
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1565
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1570
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1575
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1580
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  544, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1585
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  544, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1590
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   64, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1595
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   64, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1600
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  128, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1605
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  128, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1610
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  128, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1615
# Write Address is Done Correctly
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  128, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1620
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1625
```

```
# Write Data Operation
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1630
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1635
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1640
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1645
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  128, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1650
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  256, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1655
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  256, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1660
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  513, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1665
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  513, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1670
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    3, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1675
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    3, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1680
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =    7, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1685
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =    7, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1690
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   15, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1695
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   15, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1700
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   31, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1705
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   31, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1710
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =   63, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1715
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =   63, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1720
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  126, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1725
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  126, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1730
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  253, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1735
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  253, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1740
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  507, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1745
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  507, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1750
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  507, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1755
# Write Data is Done Correctly
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  507, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1760
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1765
```

```
# Read Address Operation
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1770
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1775
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1780
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1785
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  507, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1790
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1015, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1795
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1015, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1800
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1006, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1805
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1006, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1810
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  988, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1815
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  988, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1820
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  952, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1825
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  952, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1830
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  881, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1835
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  881, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1840
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  739, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1845
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  739, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1850
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  454, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1855
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  454, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1860
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  909, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1865
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  909, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1870
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  795, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1875
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  795, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1880
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  567, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1885
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  567, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1890
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  567, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1895
# Read Address is Done Correctly
# MOSI = 1, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  567, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=              1900
# MOSI = 1, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=              1905
```

Only RAMS

```
# Read Data Operation
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1910
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1915
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1920
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1925
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  567, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1930
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  111, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1935
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  111, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1940
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  223, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1945
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  223, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1950
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  447, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1955
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  447, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1960
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  894, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1965
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  894, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1970
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  764, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1975
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  764, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1980
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  504, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1985
# MOSI = 1, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  504, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1990
# MOSI = 1, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data = 1009, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                1995
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data = 1009, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                2000
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  994, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                2005
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  994, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                2010
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  964, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                2015
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  964, rx_valid = 0, tx_data =   8, tx_valid = 0, TIME=                2020
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                2025
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =   8, tx_valid = 0, TIME=                2030
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2035
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2040
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2045
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2050
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2055
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2060
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2065
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2070
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2075
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2080
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2085
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2090
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2095
# MOSI = 0, MISO = 0, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2100
# MOSI = 0, MISO = 1, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2105
# MOSI = 0, MISO = 1, SS_n = 0, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2110
# MOSI = 0, MISO = 0, SS_n = 0, clk = 1, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2115
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  904, rx_valid = 1, tx_data =  26, tx_valid = 1, TIME=                2120
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =  26, tx_valid = 1, TIME=                2125
# Read Data is Done Correctly
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =  26, tx_valid = 1, TIME=                2130
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =  26, tx_valid = 0, TIME=                2135
# MOSI = 0, MISO = 0, SS_n = 1, clk = 0, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =  26, tx_valid = 0, TIME=                2140
# MOSI = 0, MISO = 0, SS_n = 1, clk = 1, rst_n = 1, rx_data =  784, rx_valid = 0, tx_data =  26, tx_valid = 0, TIME=                2145
# ** Note: $stop    : SPI_Master_tb.v(197)
#    Time: 2150 ns  Iteration: 1  Instance: /SPI_Master_tb
```

Fifth: Constraints file

E: > Digital Design course > project_2 > codes > basys_master.xdc

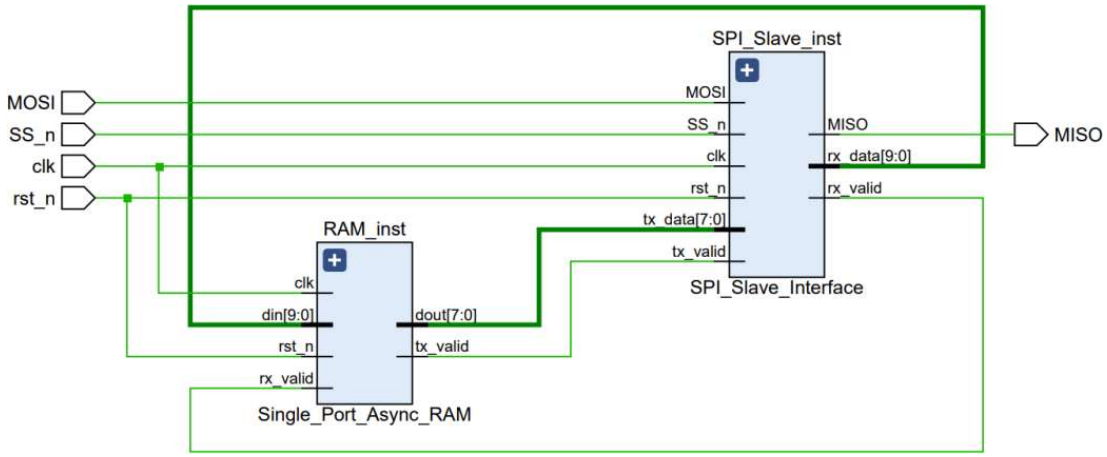
```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
set_property -dict {PACKAGE_PIN W5 IOSTANDARD LVCMOS33} [get_ports clk]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk]

## Switches
set_property -dict {PACKAGE_PIN V17 IOSTANDARD LVCMOS33} [get_ports rst_n]
set_property -dict {PACKAGE_PIN V16 IOSTANDARD LVCMOS33} [get_ports SS_n]
set_property -dict {PACKAGE_PIN W16 IOSTANDARD LVCMOS33} [get_ports MOSI]

## LEDs
set_property -dict {PACKAGE_PIN U16 IOSTANDARD LVCMOS33} [get_ports MISO]

## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

Only RAMS

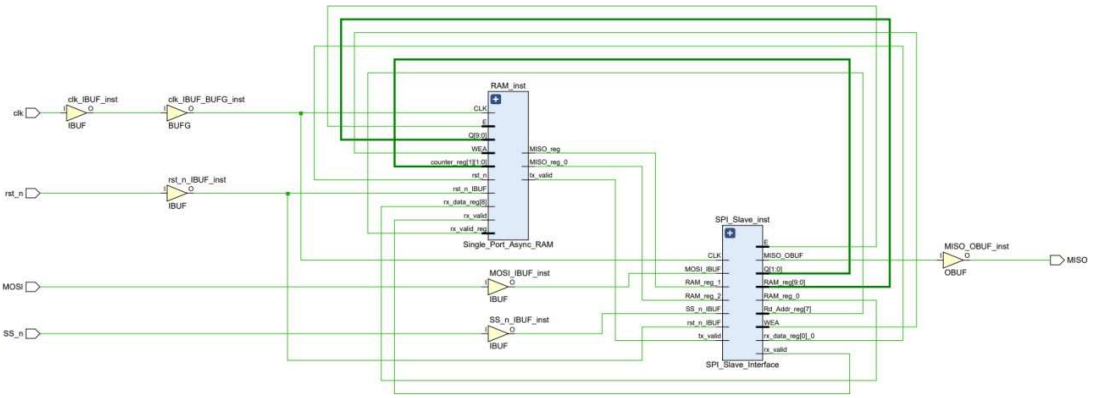
//Three FSM encoding (Gray, One hot, Seq)

Sixth: Gray encoding

Schematic after elaboration:

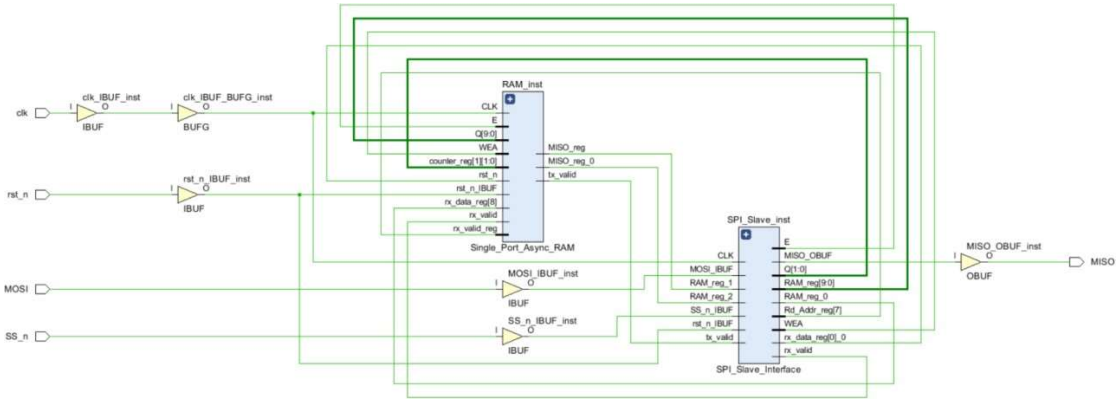


Schematic after synthesis:

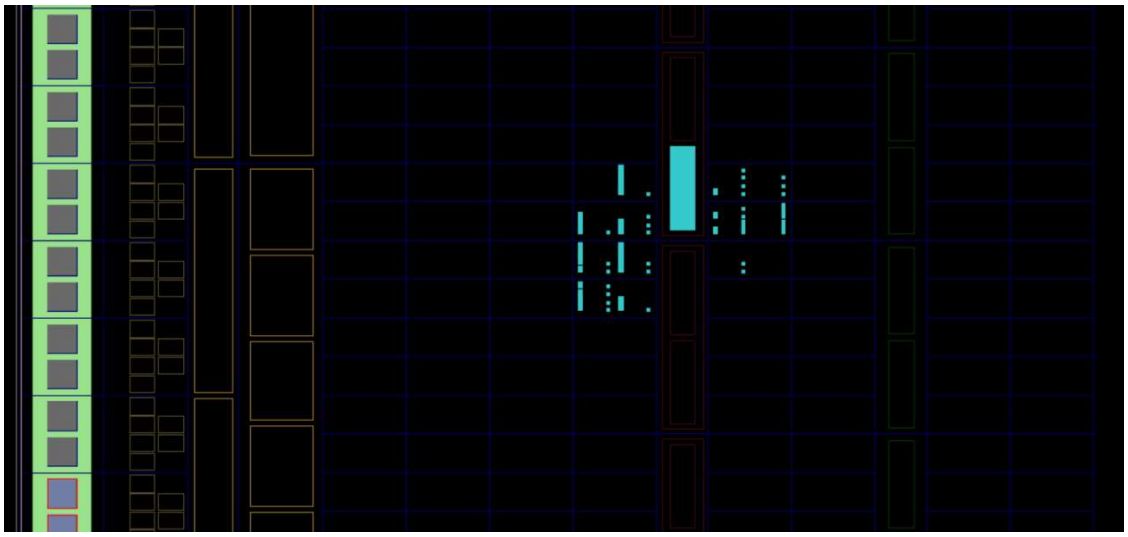


Only RAMS

Schematic after Implementation:



Device after Implementation:



Messages tab:

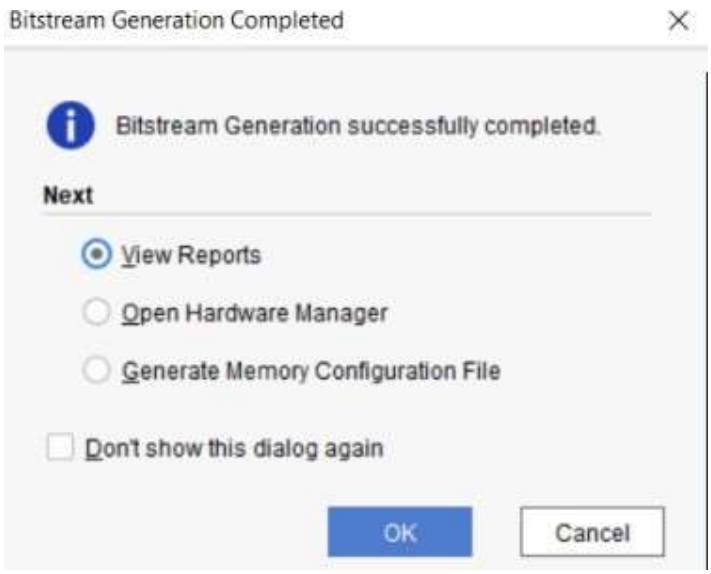
Only RAMS

Utilization:

Summary

Resource	Utilization	Available	Utilization %
LUT	26	20800	0.13
FF	37	41600	0.09
BRAM	0.50	50	1.00
IO	5	106	4.72

Bitstream:



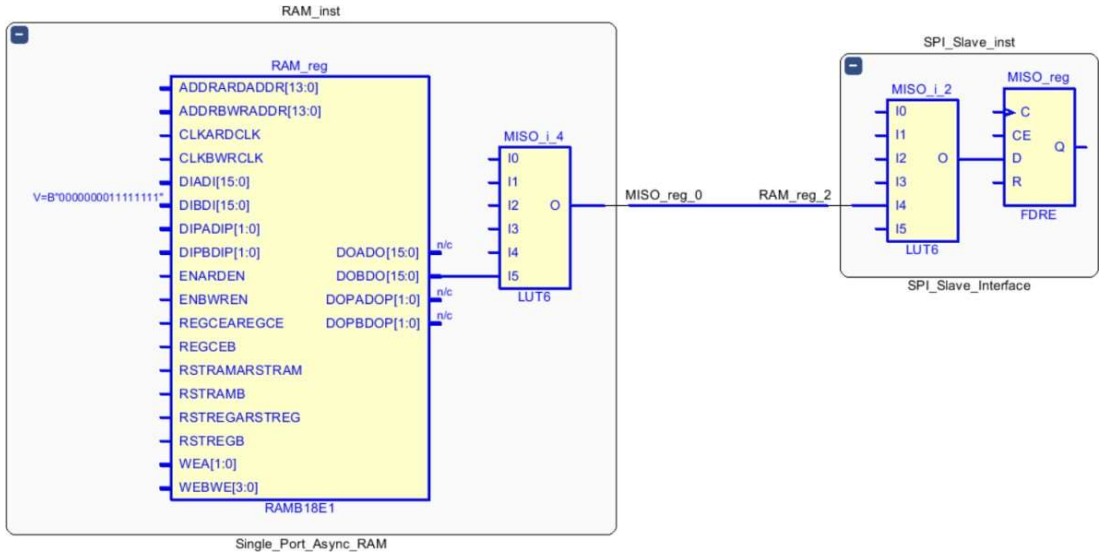
Only RAMS

Timing summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.490 ns	Worst Hold Slack (WHS):	0.077 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	111	Total Number of Endpoints:	111	Total Number of Endpoints:	50

Critical path:

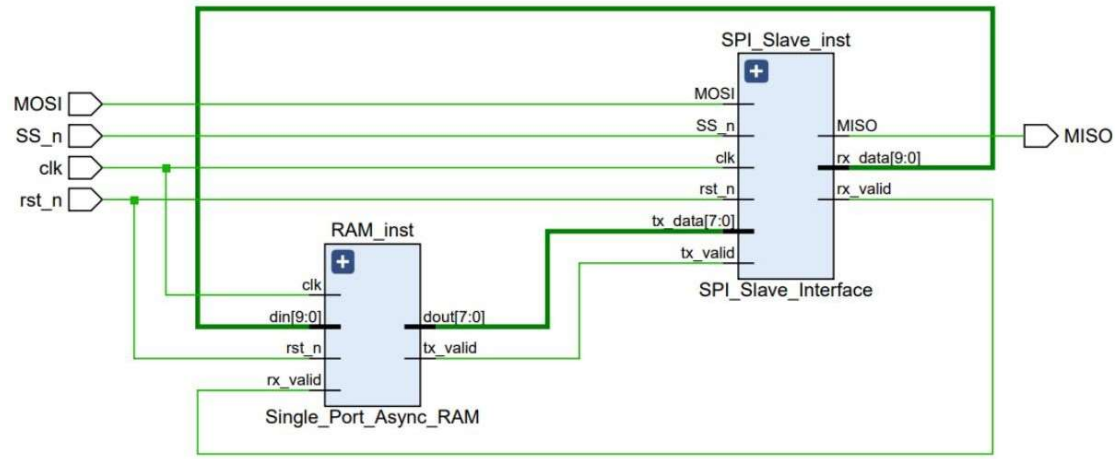


FSM encoding:

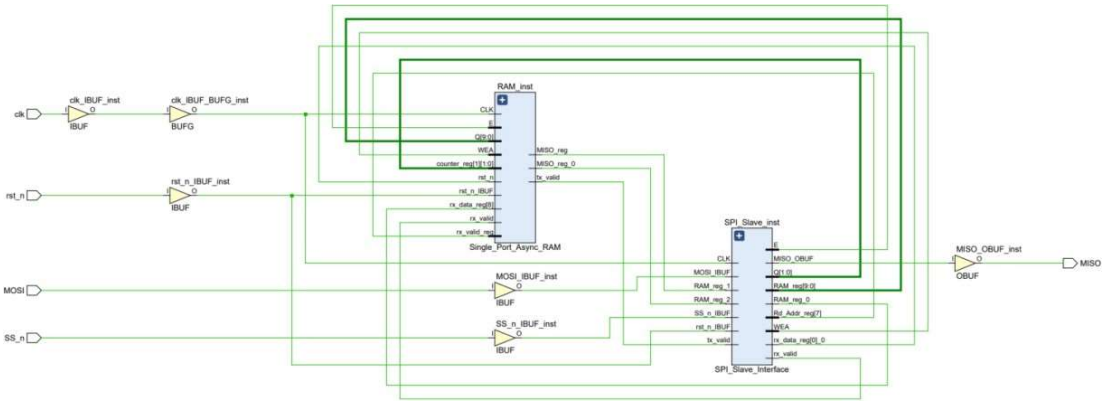
State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

Seventh: One Hot encoding

Schematic after elaboration:

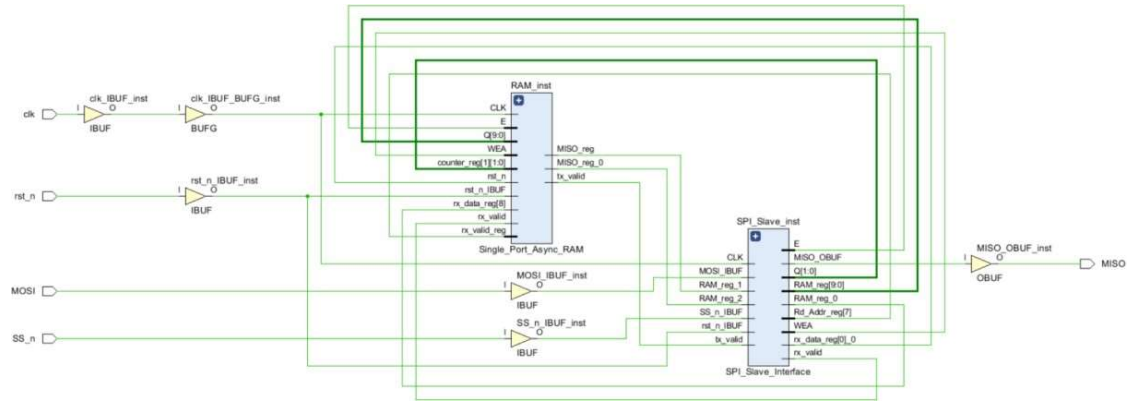


Schematic after Synthesis:

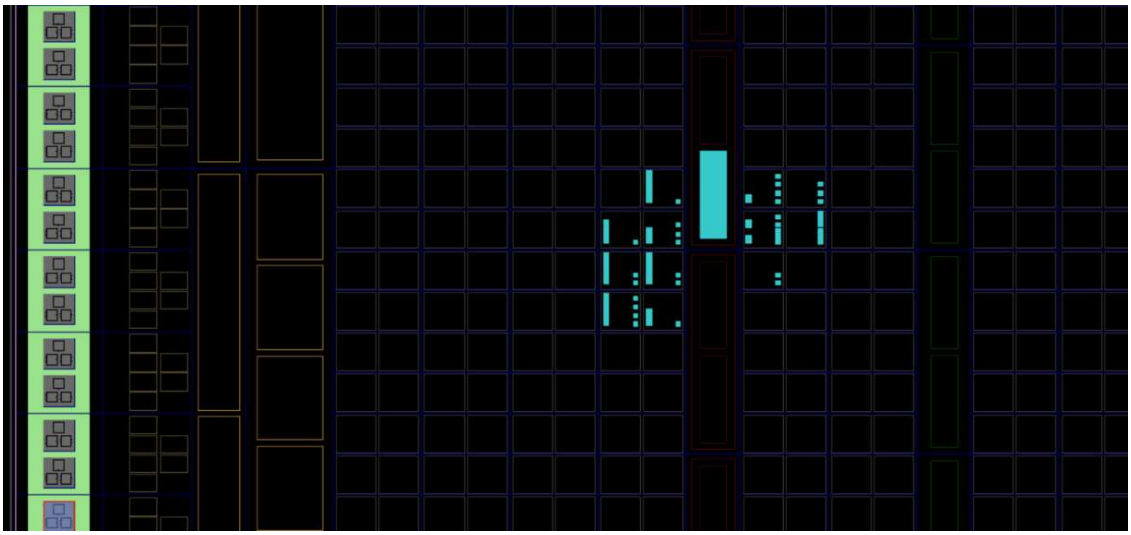


Only RAMS

Schematic after Implementation:



Device after Implementation:



Messages tab:

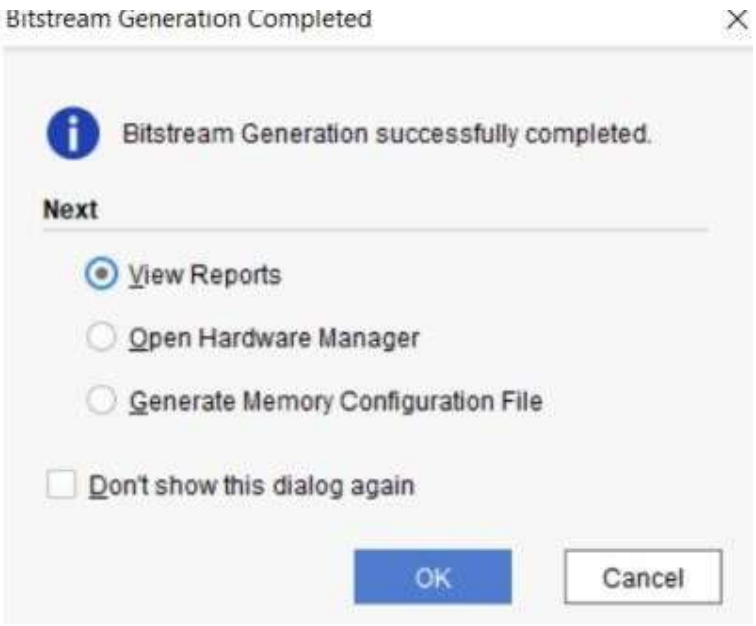
Only RAMS

Utilization:

Summary

Resource	Utilization	Available	Utilization %
LUT	26	20800	0.13
FF	37	41600	0.09
BRAM	0.50	50	1.00
IO	5	106	4.72

Bitstream:



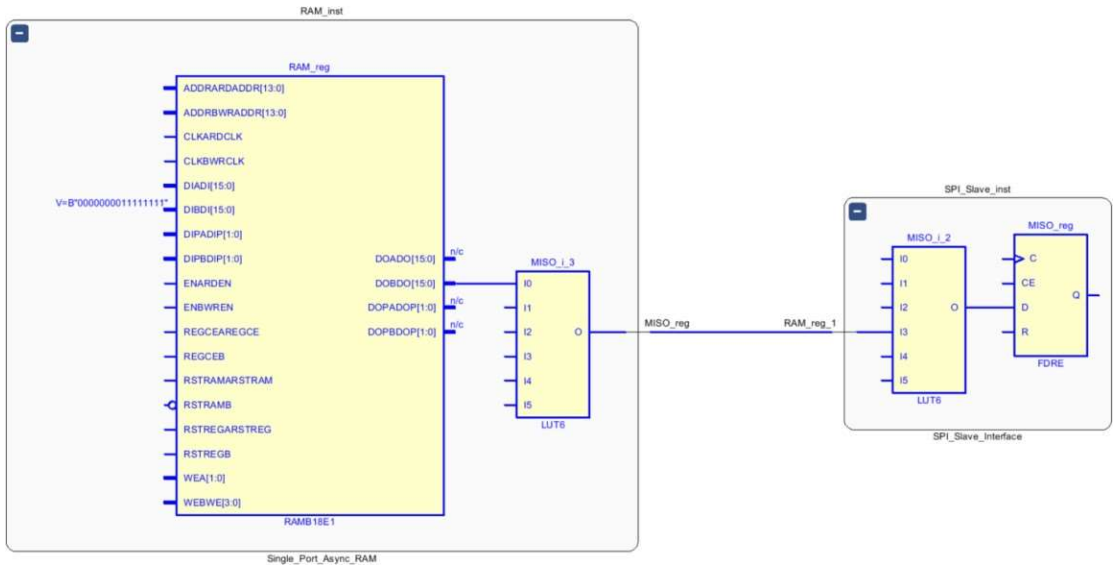
Only RAMS

Timing Summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.352 ns	Worst Hold Slack (WHS):	0.073 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	113	Total Number of Endpoints:	113	Total Number of Endpoints:	52

Critical Path:

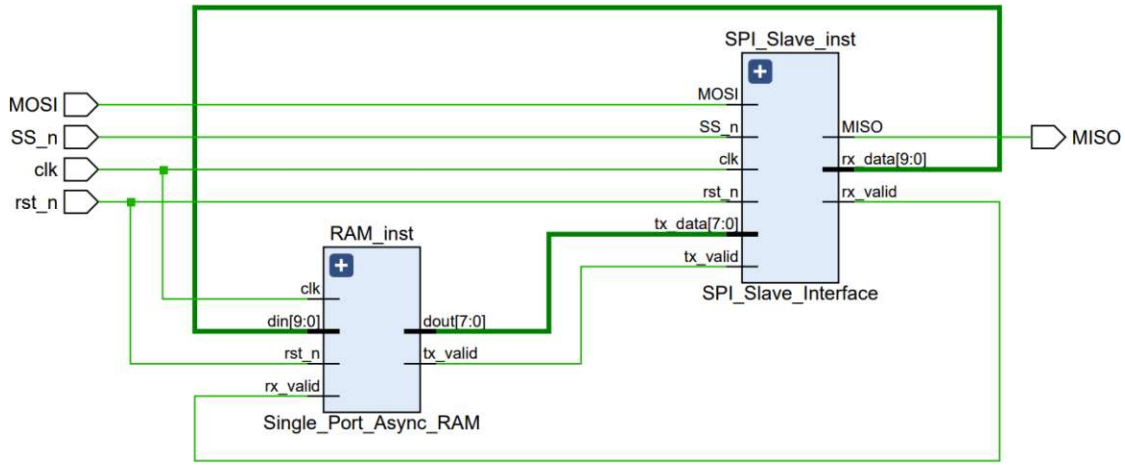


FSM encoding:

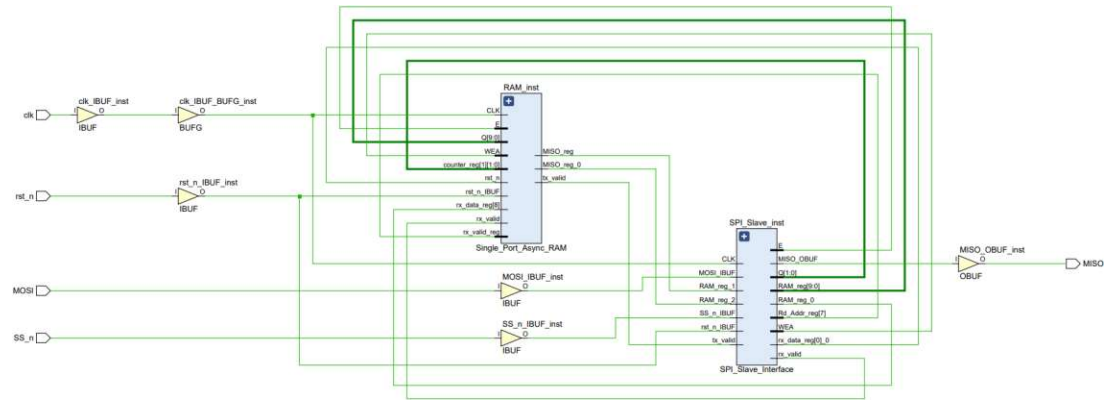
State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

Eighth: SEQ encoding

Schematic after elaboration:

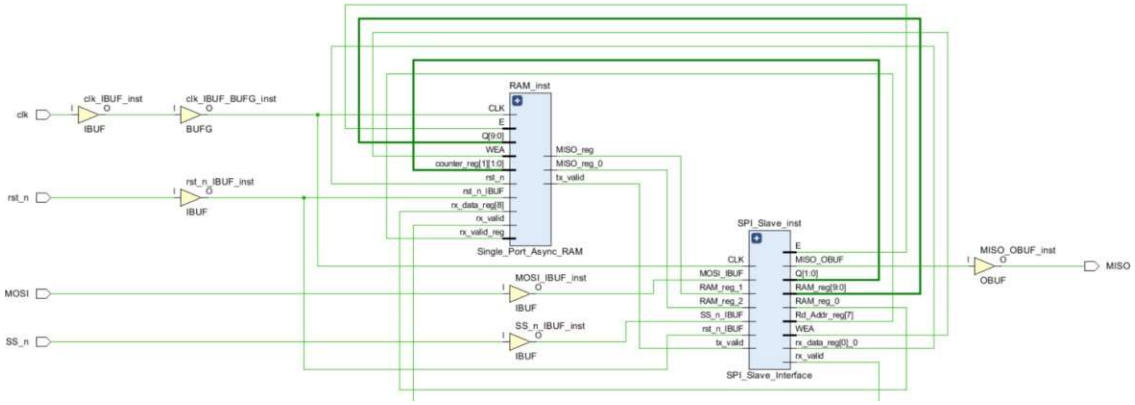


Schematic after Synthesis:

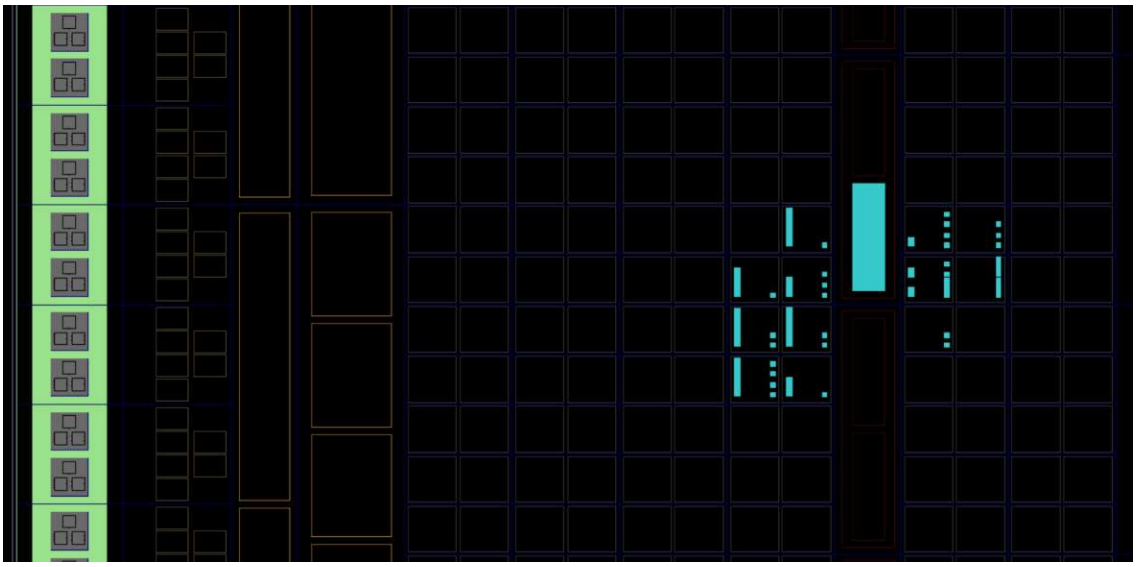


Only RAMS

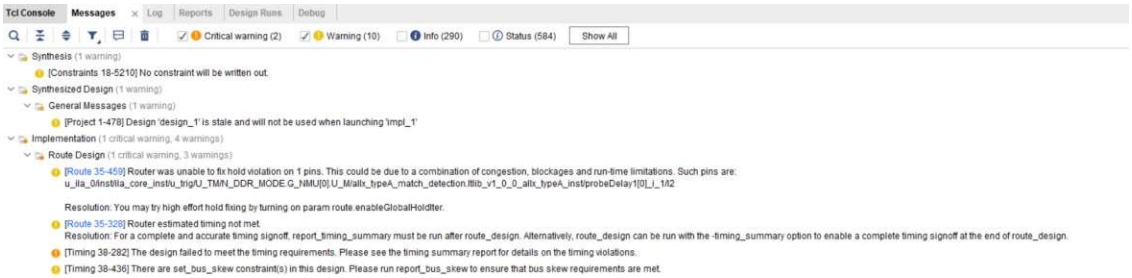
Schematic after Implementation:



Device after Implementation:



Messages tab:



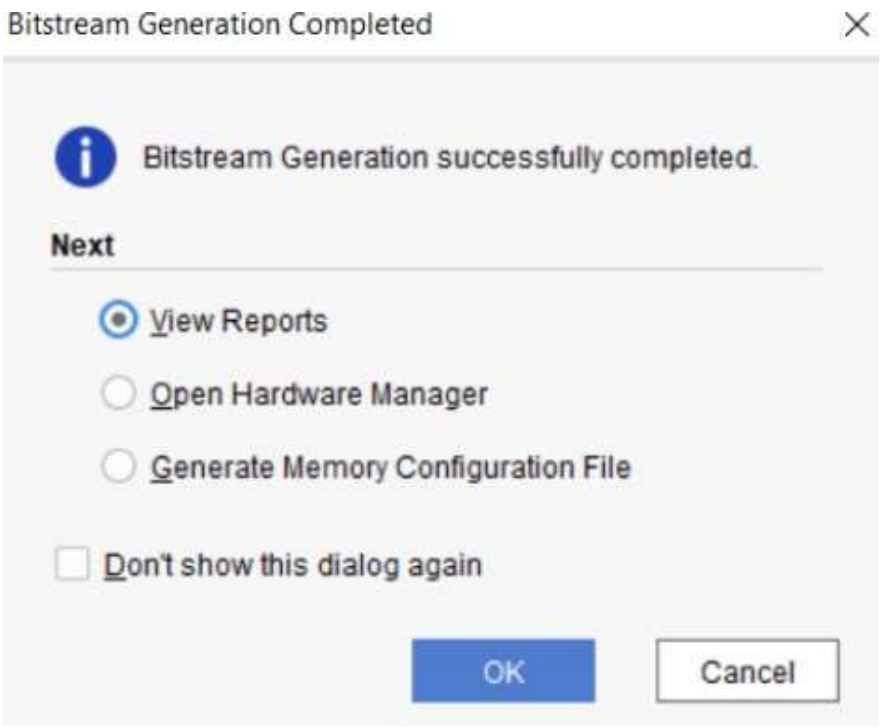
Only RAMS

Utilization:

Summary

Resource	Utilization	Available	Utilization %
LUT	26	20800	0.13
FF	37	41600	0.09
BRAM	0.50	50	1.00
IO	5	106	4.72

Bitstream:



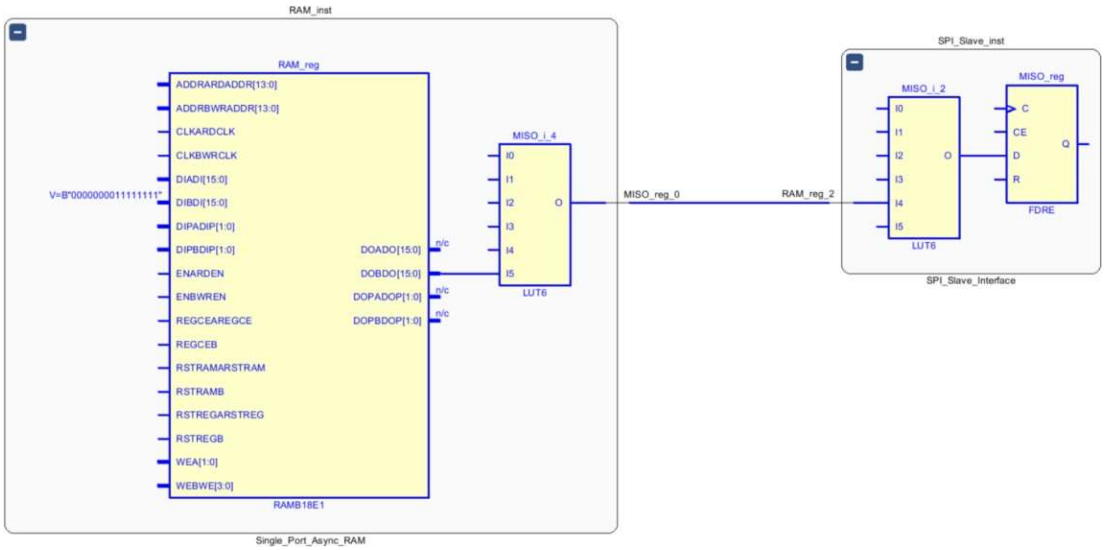
Only RAMS

Timing Summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.895 ns	Worst Hold Slack (WHS):	0.067 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	111	Total Number of Endpoints:	111	Total Number of Endpoints:	50

Critical path:



FSM encoding:

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

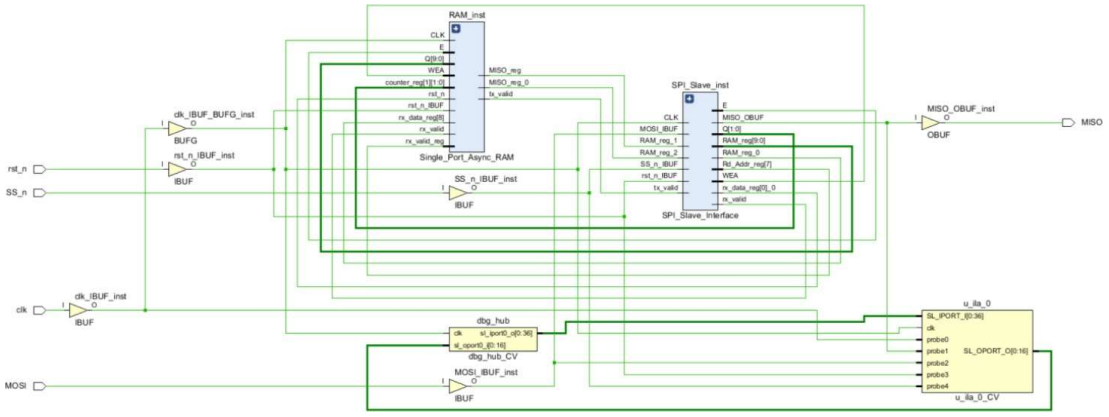
Ninth: best encoding

//Specs wise → it is required to operate at the highest frequency, then it is obvious that the //GRAY encoding is relatively the best as it has the highest setup slack time = 5.490 ns, which //was shown in the GRAY FSM encoding timing summary.

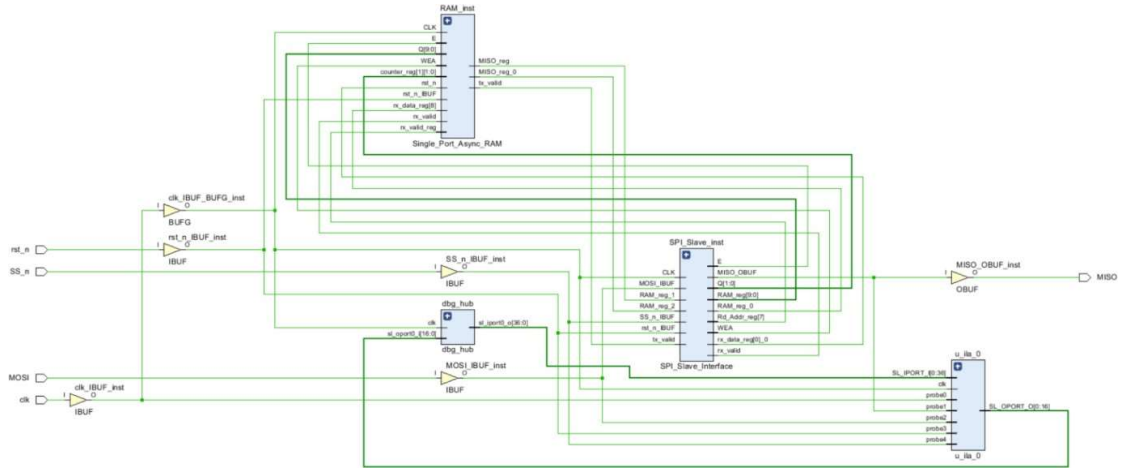
//Then, Gray encoding is chosen.

//Debug core is added in the following schematics.

Synthesis Schematic:



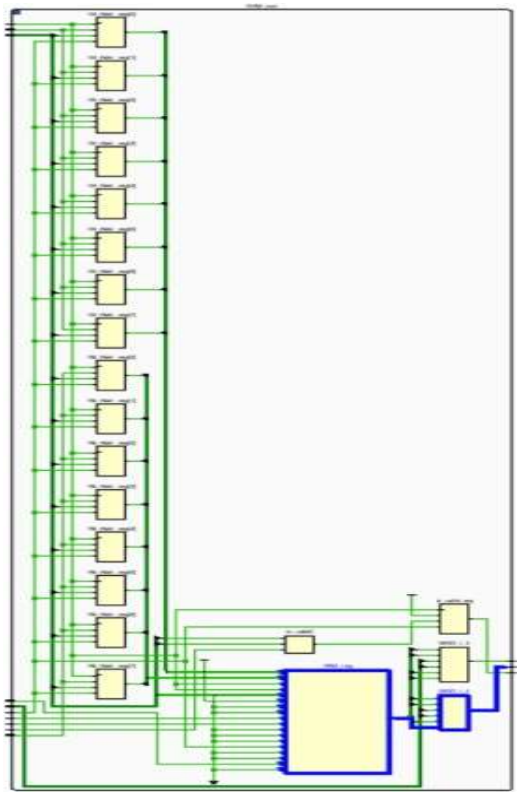
Implementation Schematic:

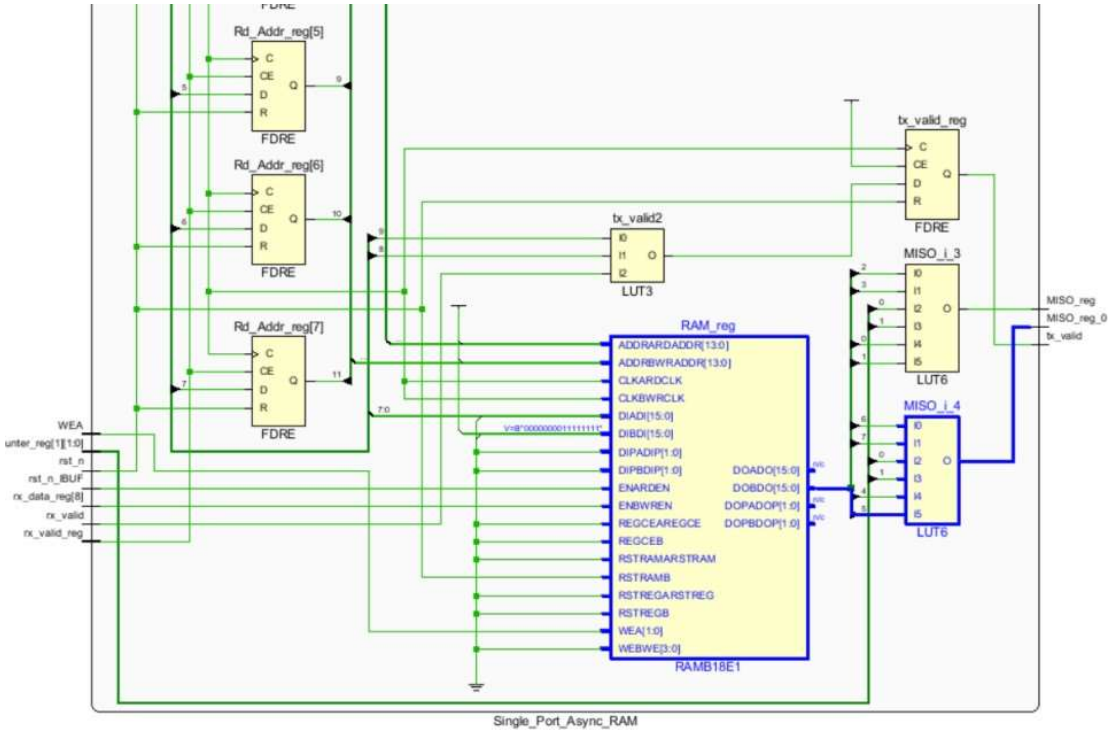


Only RAMS

Tenth: Critical path

RAM:





Only RAMS

SPI: