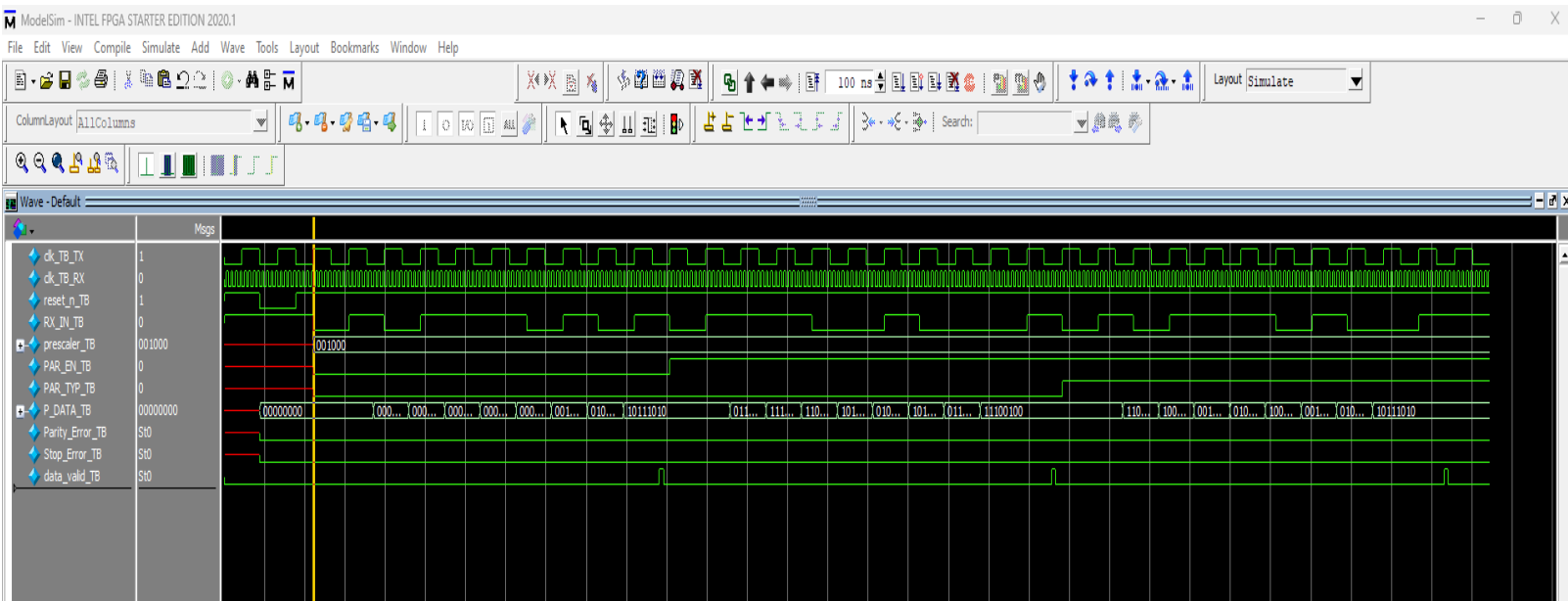


UART_RX

Case1: Prescale by 8:

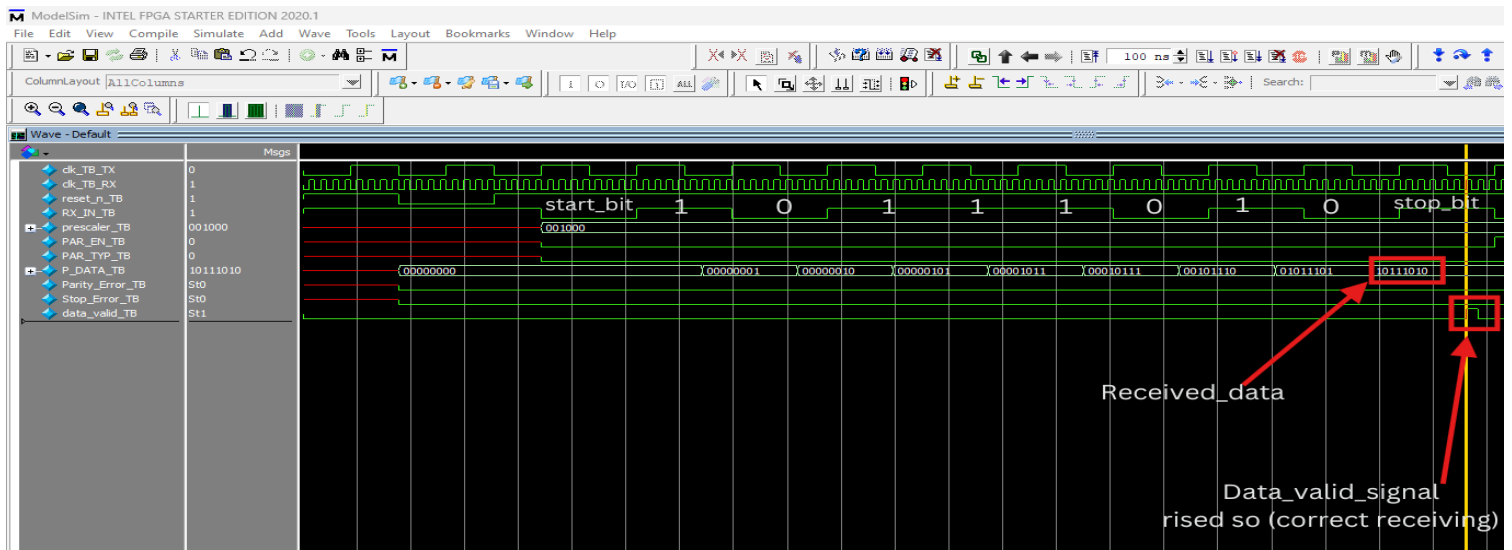
1. Waveform of 3 Consequent Frames:



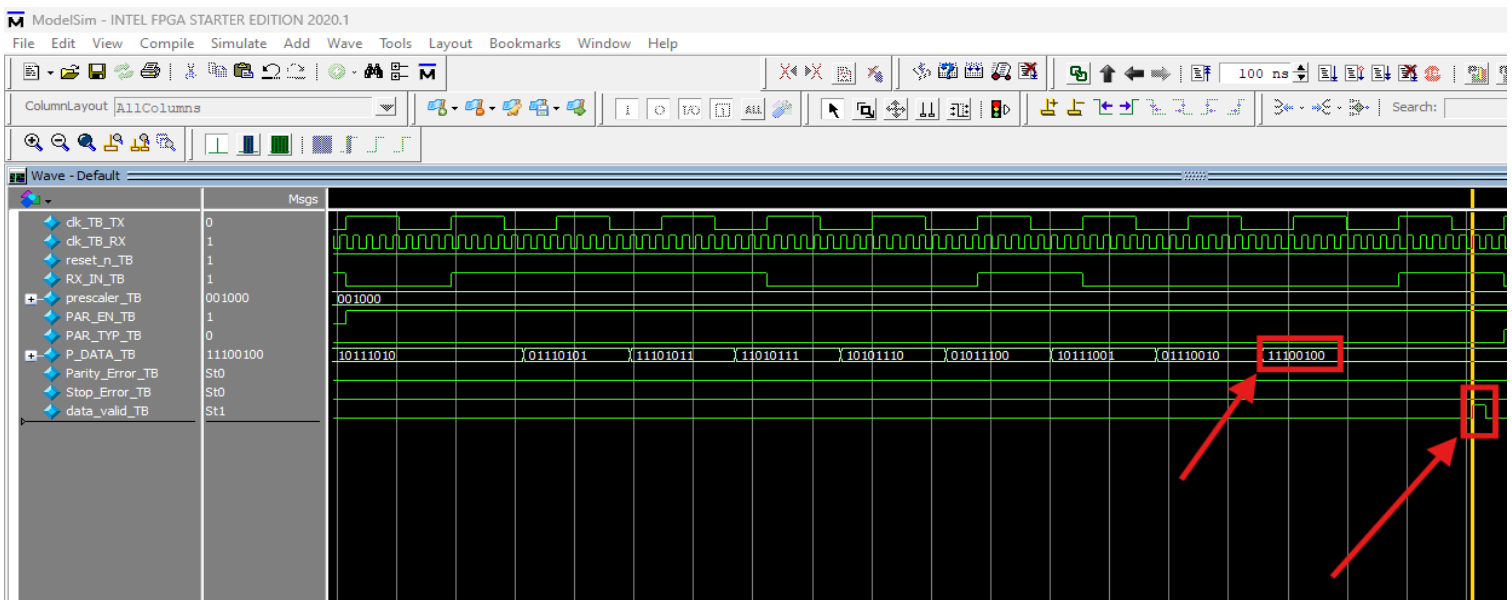
2. Log Window:

```
VSIM 13> run -all
*****CASE 1 CHECK IS PASSED*****
*****Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 111000 us*****
*****CASE 2 CHECK IS PASSED*****
*****Data are correctly sent and detected ----> P_DATA = 11100100 ----> Time = 208000 us*****
*****CASE 3 CHECK IS PASSED*****
*****Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 297000 us*****
** Note: $stop : E:/Verilog/Quartus/UART_RX/UART_RX_TB.v(107)
Time: 314530 ns Iteration: 0 Instance: /UART_RX_TB
Break in Module UART_RX_TB at E:/Verilog/Quartus/UART_RX/UART_RX_TB.v line 107
VSIM 14>
```

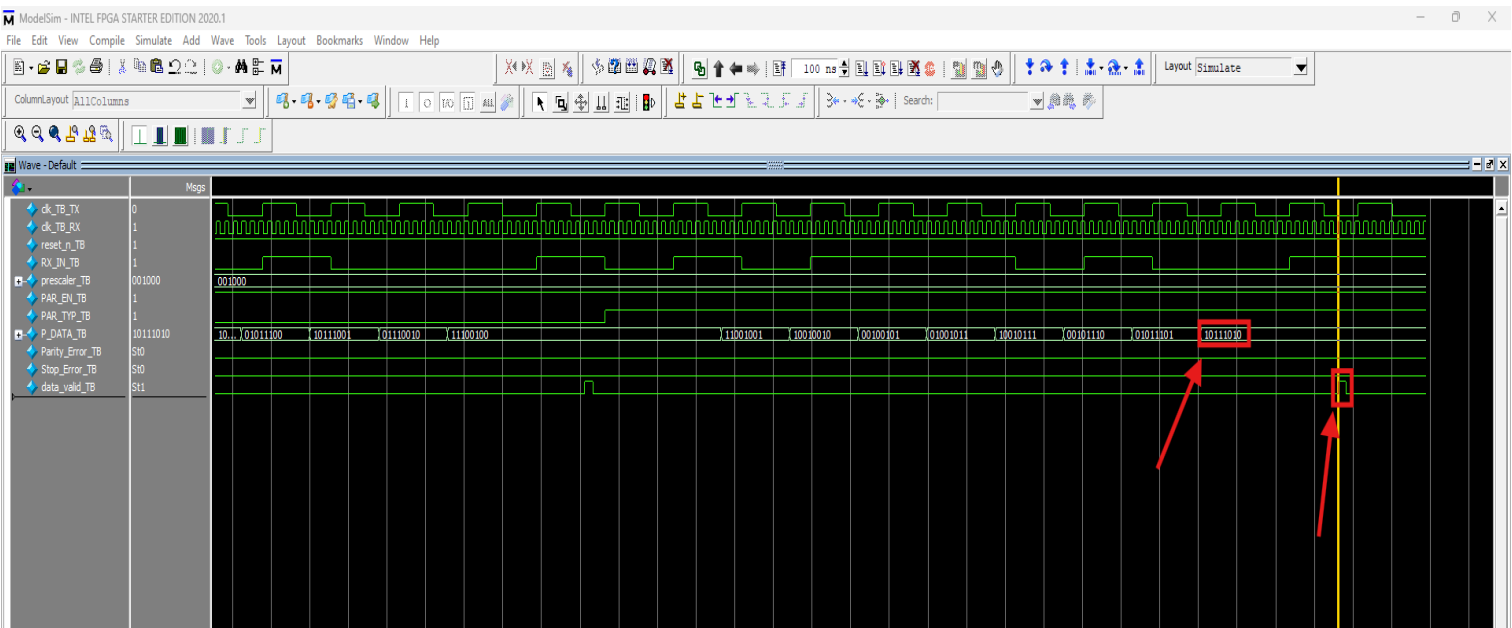
First Frame:



Second Frame:

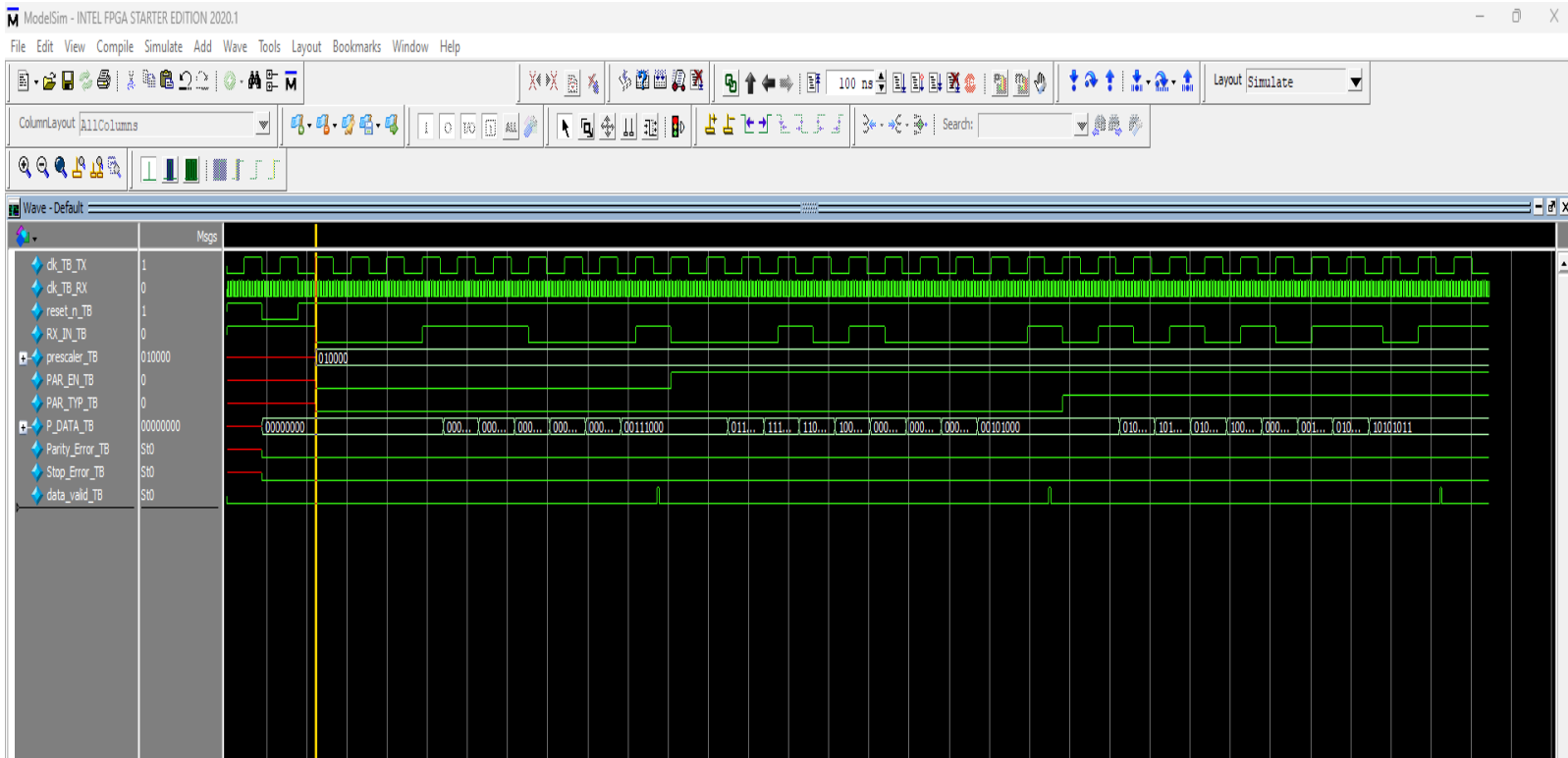


Third Frame:



Case2: Prescale by 16:

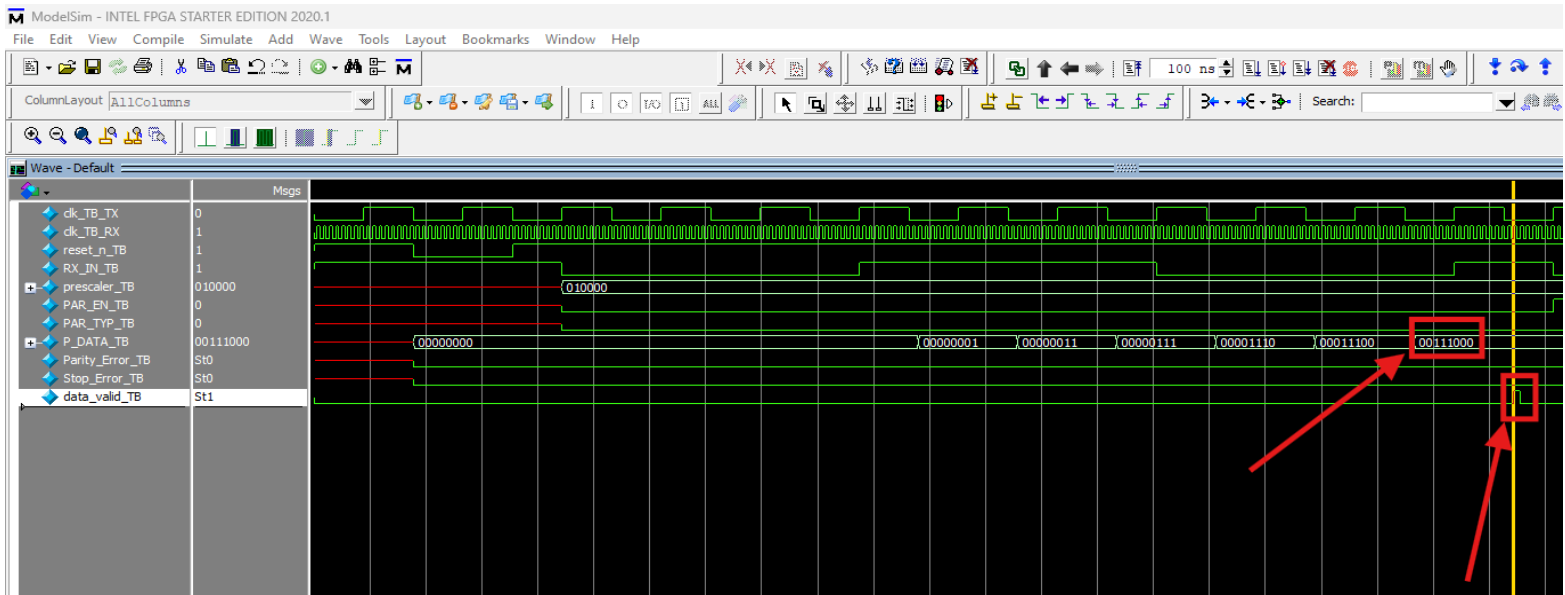
1. Waveform of 3 Consequent Frames:



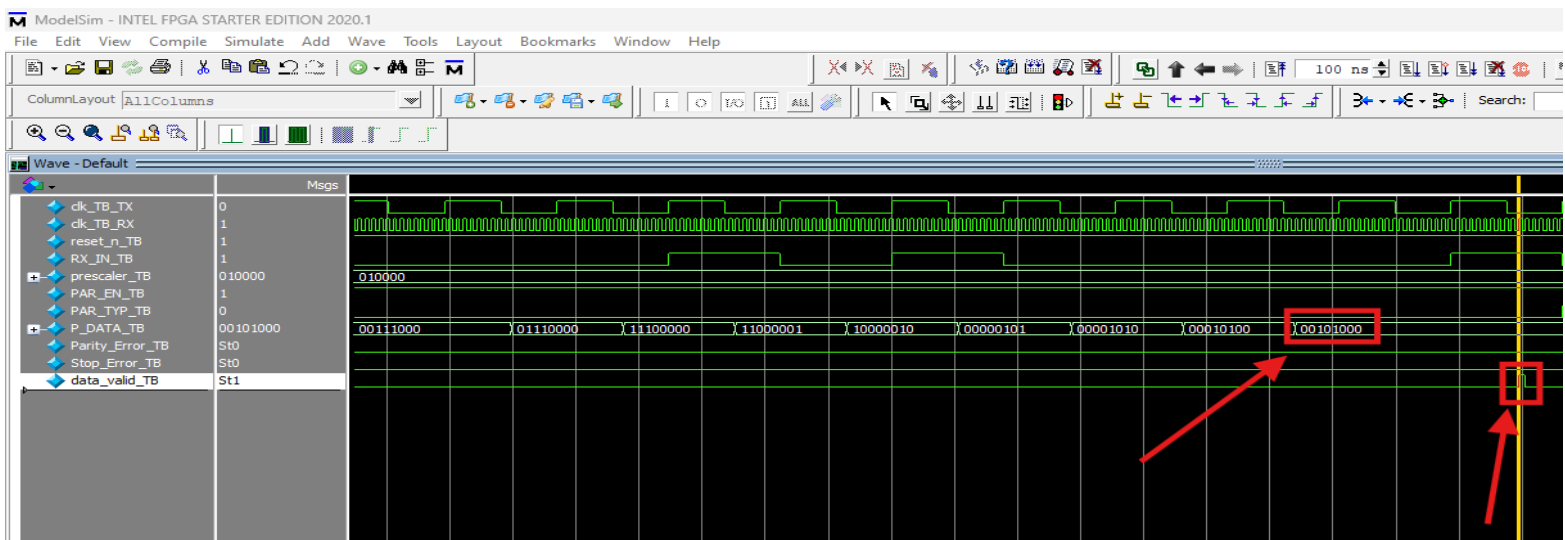
2. Log Window:

```
VSIM 13> run -all
*****
*****#CASE 1 CHECK IS PASSED*****
*****#Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 111000 us*****
*****
*****
*****#CASE 2 CHECK IS PASSED*****
*****#Data are correctly sent and detected ----> P_DATA = 11100100 ----> Time = 208000 us*****
*****
*****
*****#CASE 3 CHECK IS PASSED*****
*****#Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 297000 us*****
*****
*****
** Note: $stop : E:/Verilog/Quartus/UART_RX/UART_RX_TB.v(107)
Time: 314530 ns Iteration: 0 Instance: /UART_RX_TB
# Break in Module UART_RX_TB at E:/Verilog/Quartus/UART_RX/UART_RX_TB.v line 107
VSIM 14>
```

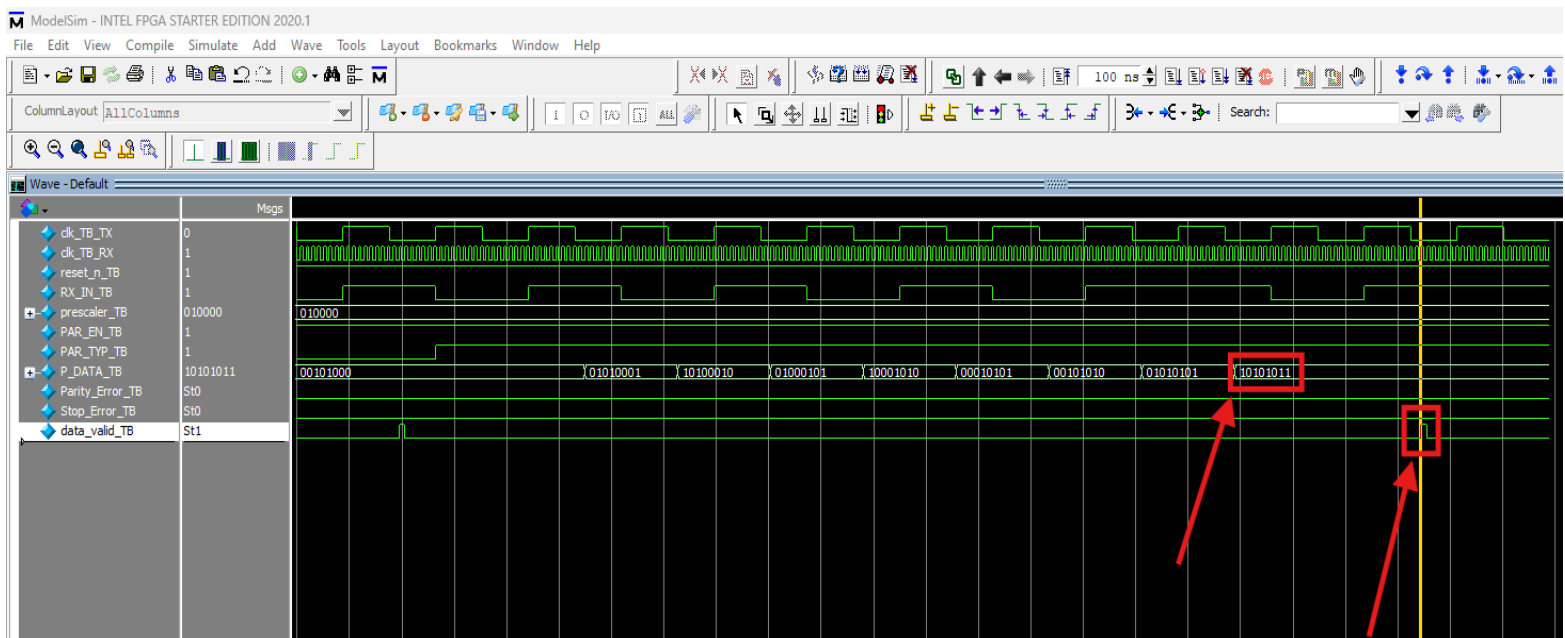
First Frame:



Second Frame

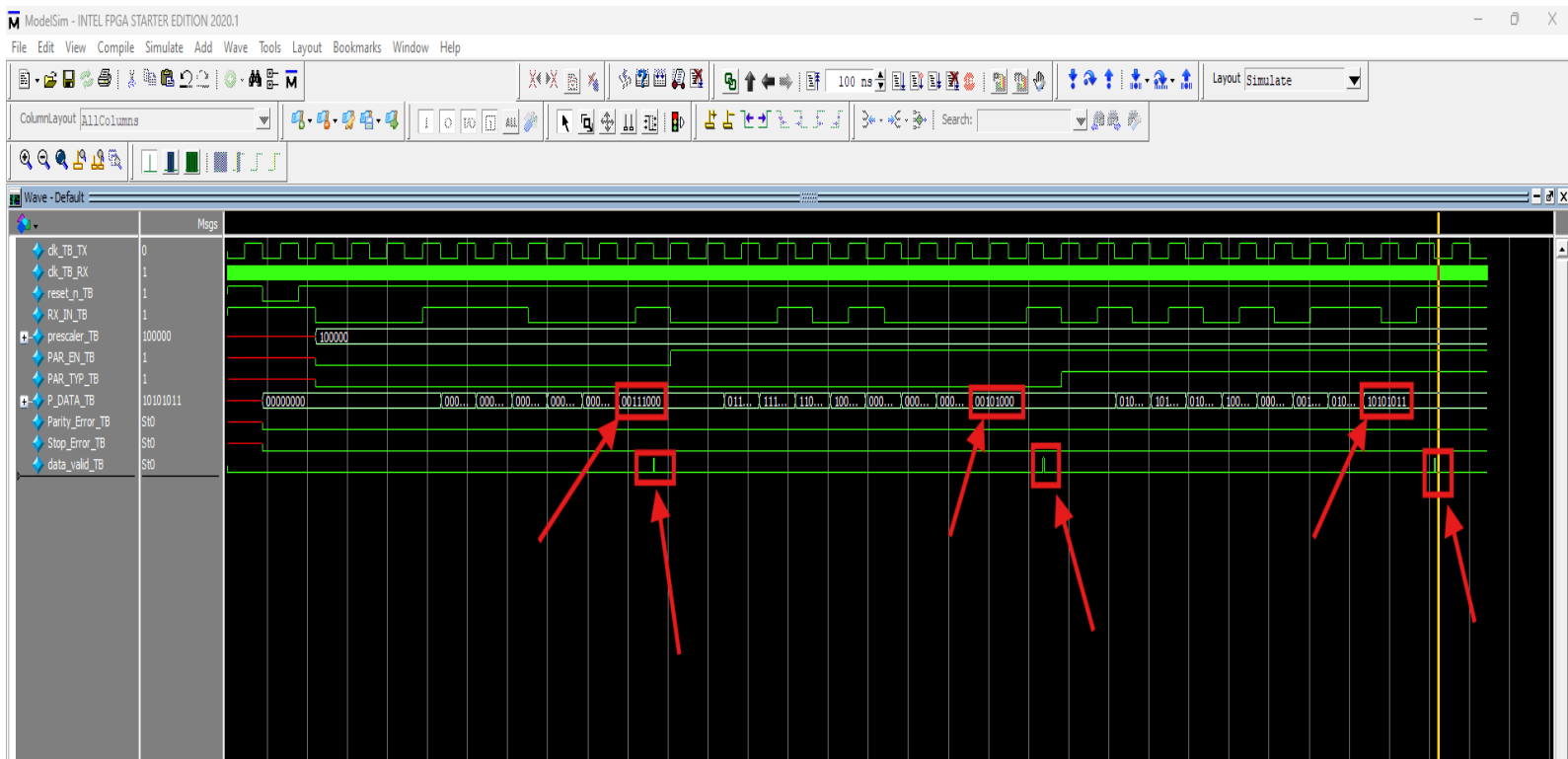


Third Frame:



Case3: Prescale by 32:

1. Waveform of 3 Consequent Frames:



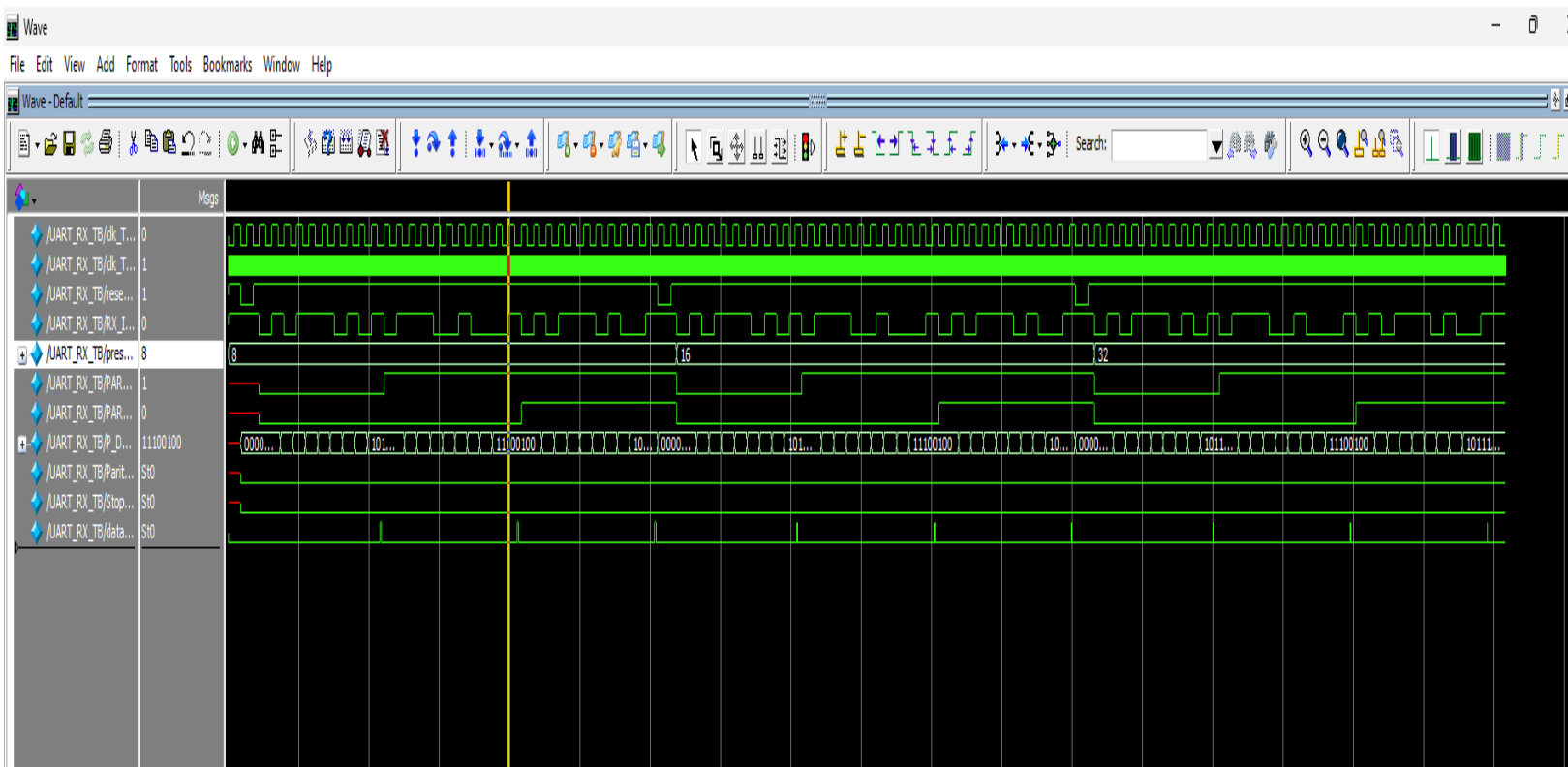
2. Log Window:

```
VSIM 13> run -all
*****
*****CASE 1 CHECK IS PASSED*****
*****#Data are correctly sent and detected -----> P_DATA = 10111010 -----> Time = 111000 us*****
*****
*****CASE 2 CHECK IS PASSED*****
*****#Data are correctly sent and detected -----> P_DATA = 11100100 -----> Time = 208000 us*****
*****
*****CASE 3 CHECK IS PASSED*****
*****#Data are correctly sent and detected -----> P_DATA = 10111010 -----> Time = 297000 us*****
*****
** Note: $stop : E:/Verilog/Quartus/UART_RX/UART_RX_TB.v(107)
Time: 314530 ns Iteration: 0 Instance: /UART_RX_TB
# Break in Module UART_RX_TB at E:/Verilog/Quartus/UART_RX/UART_RX_TB.v line 107
VSIM 14>
```

- The functionality of the UART_RX doesn't change with the value of the prescale, it just only determined when the bits will be sampled (i.e. prescale = 8 → the bits will be sampled at the third, fourth and fifth edge of the clock).

All Cases in One Waveform:

1. Waveform:



2. Log Window:

```
# Loading work.StopCheck
add wave -position insertpoint sim:/UART_RX_TB/*
vSIM 3> run -all
#####
#
#####
#
#####PRESCALE BY 8#####
#
#####
#
#####
#
#####
#
#####CASE 1 CHECK IS PASSED#####
#
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 111000 us#####
#
#####
#
#####
#
#####CASE 2 CHECK IS PASSED#####
#
#####Data are correctly sent and detected ----> P_DATA = 11100100 ----> Time = 208000 us#####
#
#####
#
#####
#
#####CASE 3 CHECK IS PASSED#####
#
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 297000 us#####
#
#####
#
#####
#
#####
```

```
#####PRESCALE BY 16#####
#####
#####
#####
#####
#####CASE 1 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 408000 us#####
#####
#####
#####
#####CASE 2 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 11100100 ----> Time = 505000 us#####
#####
#####
#####
#####CASE 3 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 594000 us#####
#####
#####
#####
#####PRESCALE BY 32#####
#####
#####
#####
#####CASE 1 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 704000 us#####
#####
#####
#####
#####CASE 2 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 11100100 ----> Time = 802000 us#####
#####
#####
#####
#####CASE 3 CHECK IS PASSED#####
#####Data are correctly sent and detected ----> P_DATA = 10111010 ----> Time = 890000 us#####
#####
#####
#####
#####
** Note: $stop : C:/Users/muhmd/OneDrive/Desktop/UART_RX_Mohamed Dawod/RTL&TB/UART_RX_TB.v(266)
Time: 908150 ns Iteration: 0 Instance: /UART_RX_TB
# Break in Module UART_RX_TB at C:/Users/muhmd/OneDrive/Desktop/UART_RX_Mohamed Dawod/RTL&TB/UART_RX_TB.v line 266
```