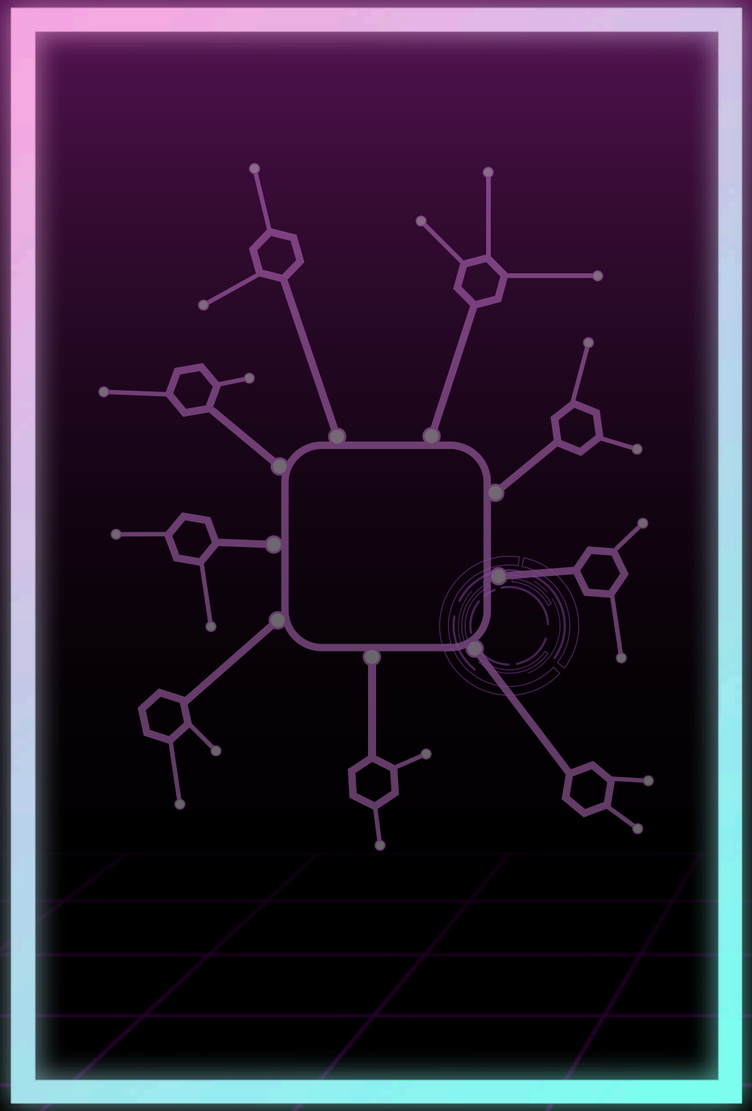
TEAM 13

Mohamed Dawod

Nour Hussien

Mariam

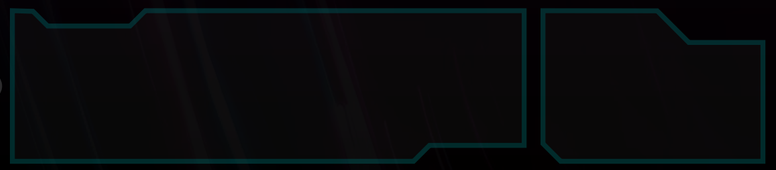


SINGLE CYCLE RISC-V

IMPLEMENTATION

01

OVERVIEW



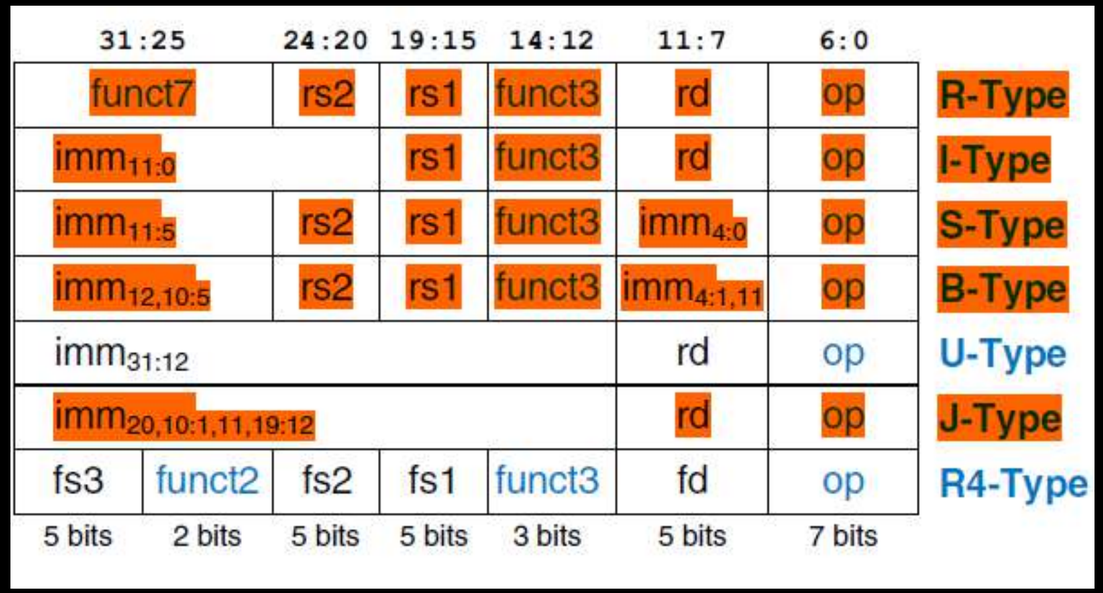
- Design and implement a single-cycle RISC-V processor using Verilog.
- Integrate the processor with the cache system.

AGENDA

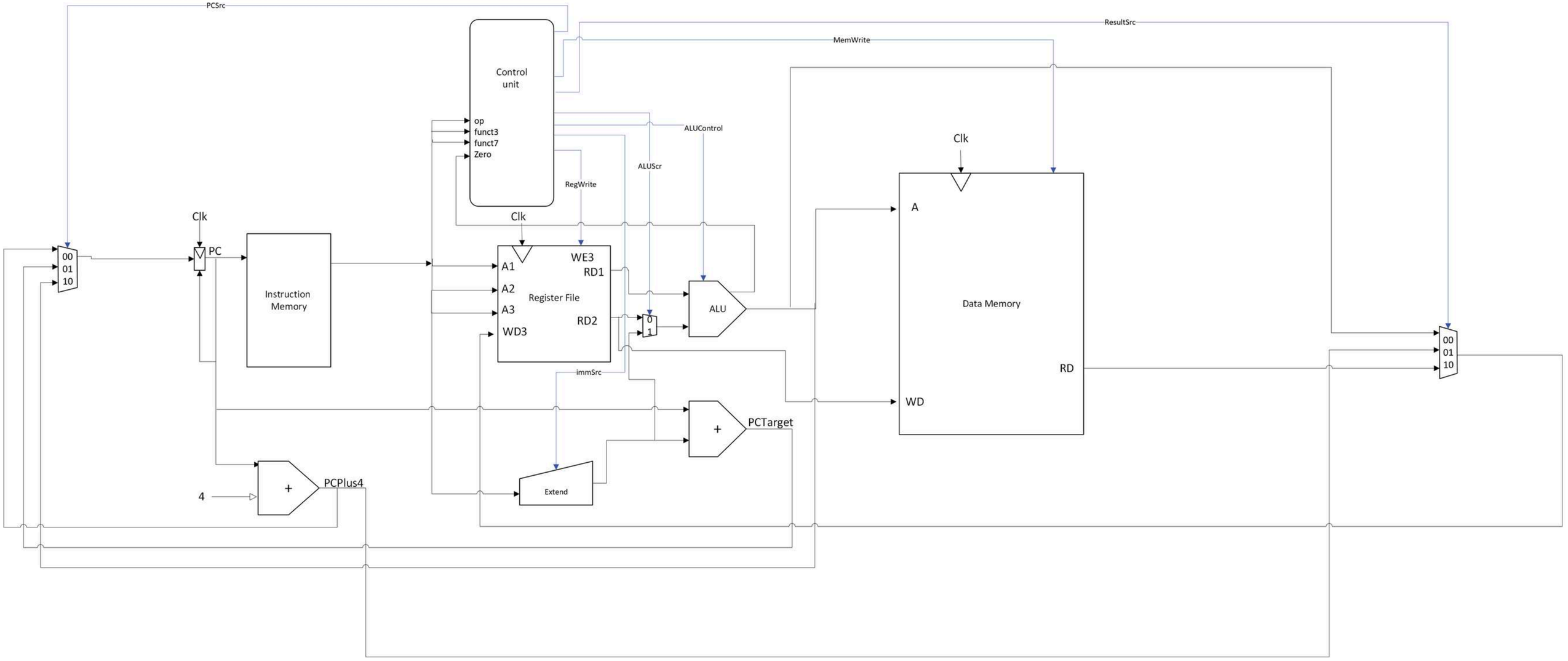
- Supported Instructions.
- Design Architecture.
- Simulation Results.
- Integration With Caching System.
- Future Work.

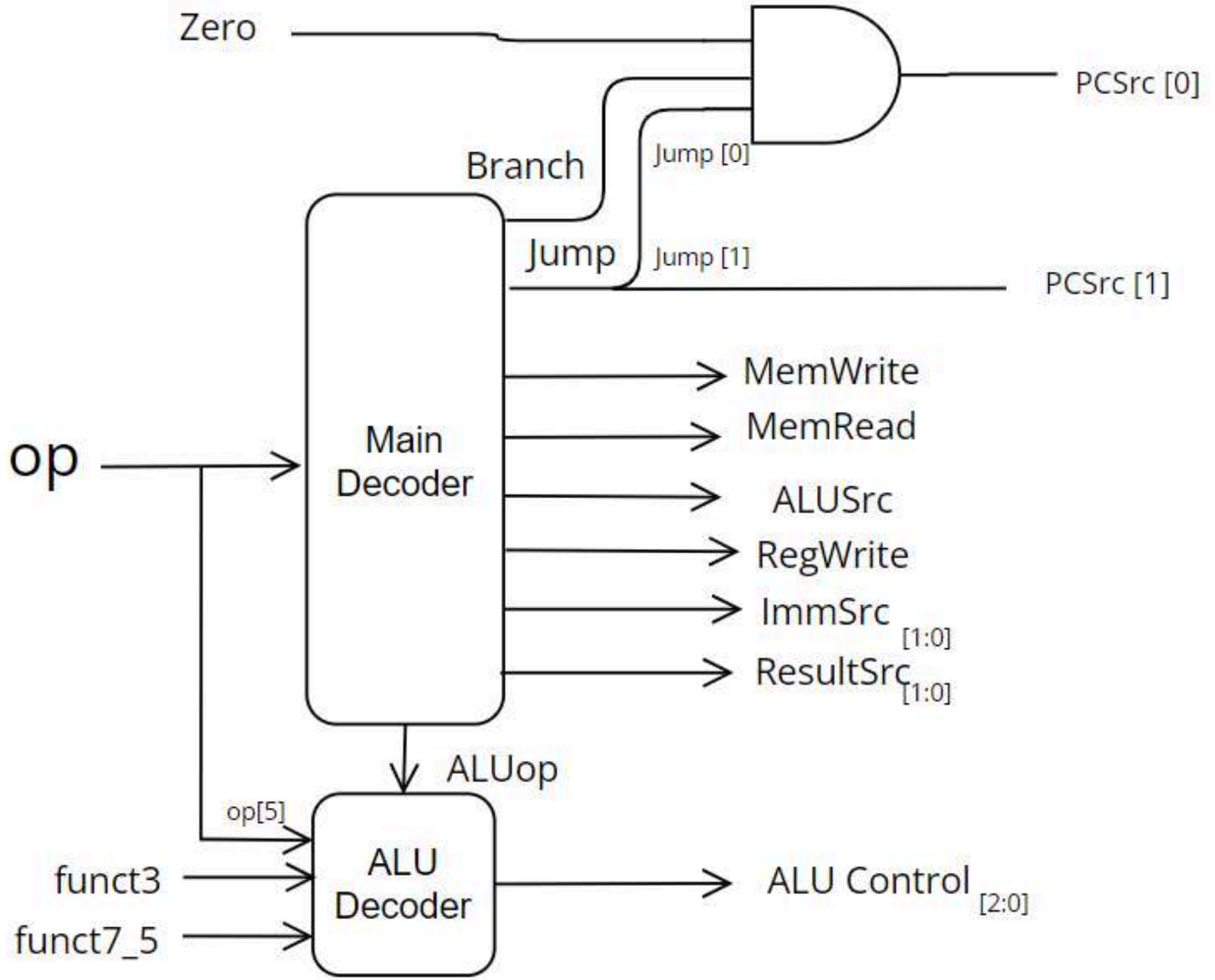
Supported Instructions

R-TYPE	ADD, SUB, AND, OR
I-TYPE	ADDI, ADI, ORI, LW, JALR
B-TYPE	BEQ, BNE
J-TYPE	JAL
S-TYPE	SW



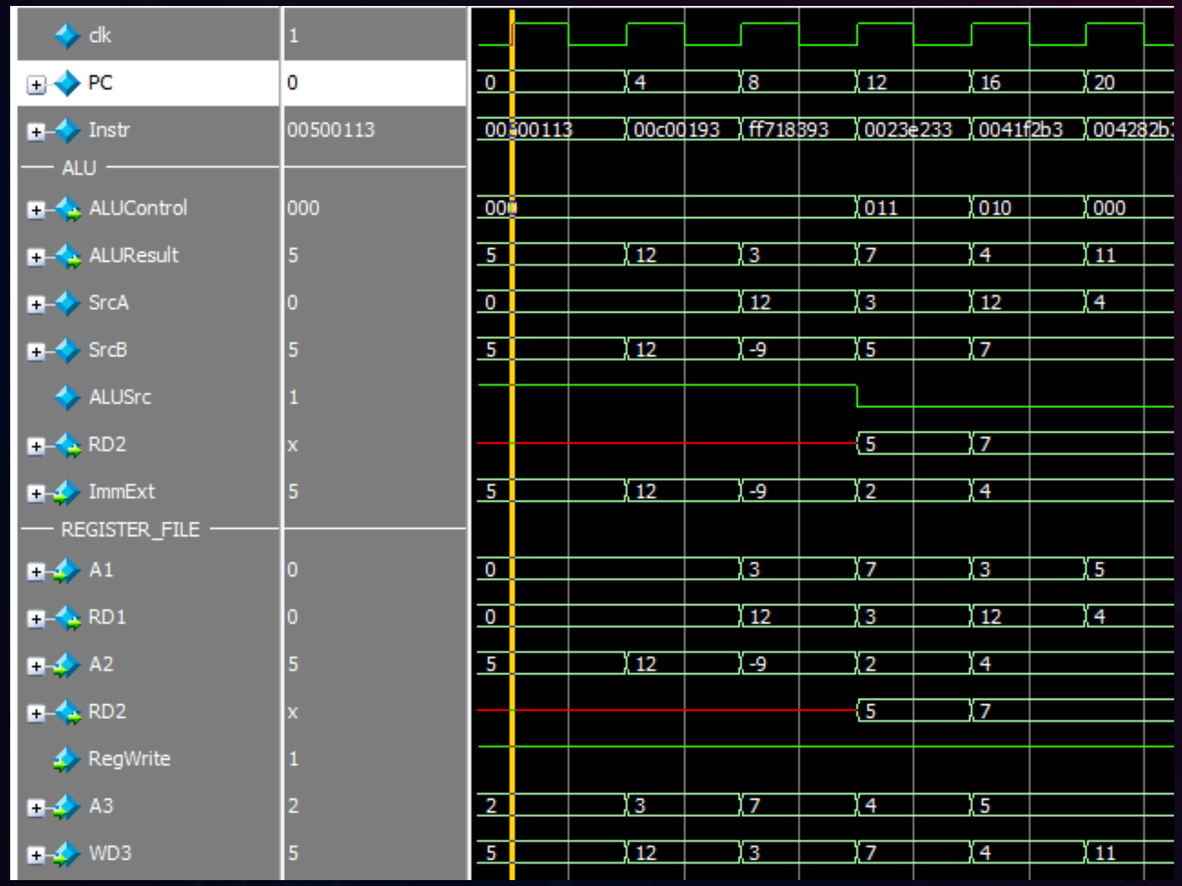
Design Architecture


PCSrc
ResultSrc
MemWrite
Control unit
op
funct3
funct7
Zero
ALUControl
ALUScr
RegWrite
Clk
Clk
Clk
00
01
10
PC
Instruction Memory
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
0
1
ALU
A
Data Memory
RD
WD
immSrc
+
PCTarget
+
PCPlus4
4
Extend
00
01
10


Zero
PCSrc [0]
Branch
Jump [0]
Jump
Jump [1]
PCSrc [1]
MemWrite
MemRead
op
Main
Decoder
ALUSrc
RegWrite
ImmSrc [1:0]
ResultSrc [1:0]
ALUop
op[5]
funct3
ALU
Decoder
ALU Control [2:0]
funct7_5

Simulation Results

SIM RESULTS



1 - ADDI X2 X0 5

X2 = 5

2 - ADDI X3 X0 12

X3 = 12

3 - ADDI X7 X3 -9

X7 = 3

4 - OR X4 X7 X2

X4 = 7

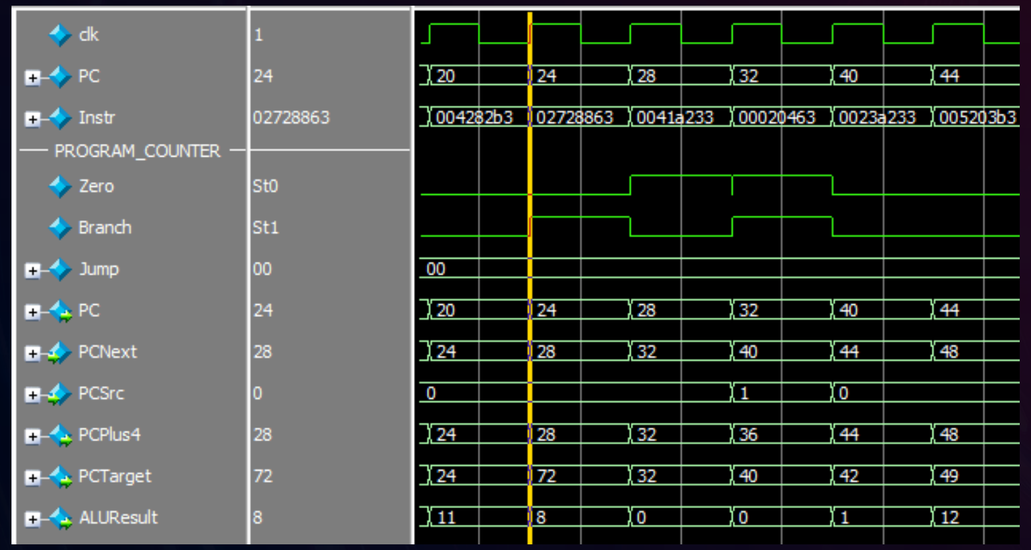
5 - AND X5 X3 X4

X5 = 4

6 - ADD X5 X5 X4

X5 = 11

SIM RESULTS



1 - BEQ X5 X7 48

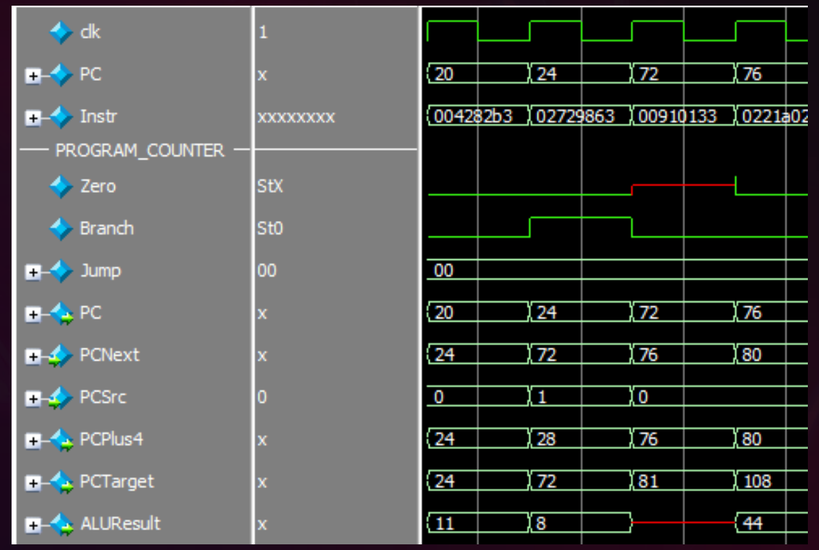
NOT TAKEN

2 - SLT X4 X3 X4

X4 = 0

3 - BEQ X4 X0 8

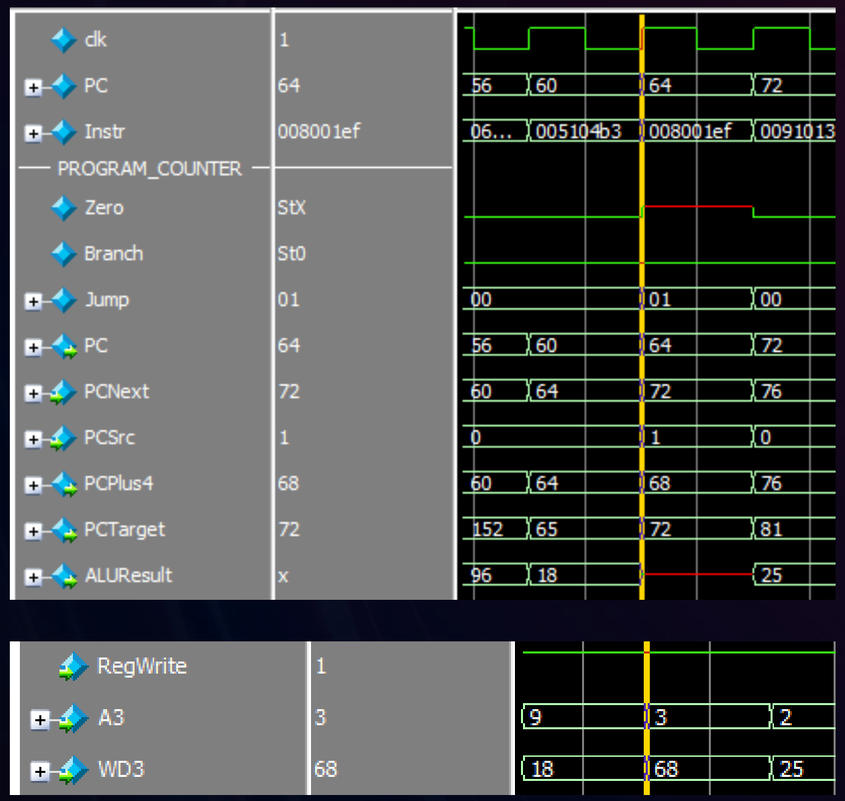
TAKEN



1 - BNQ X5 X7 48

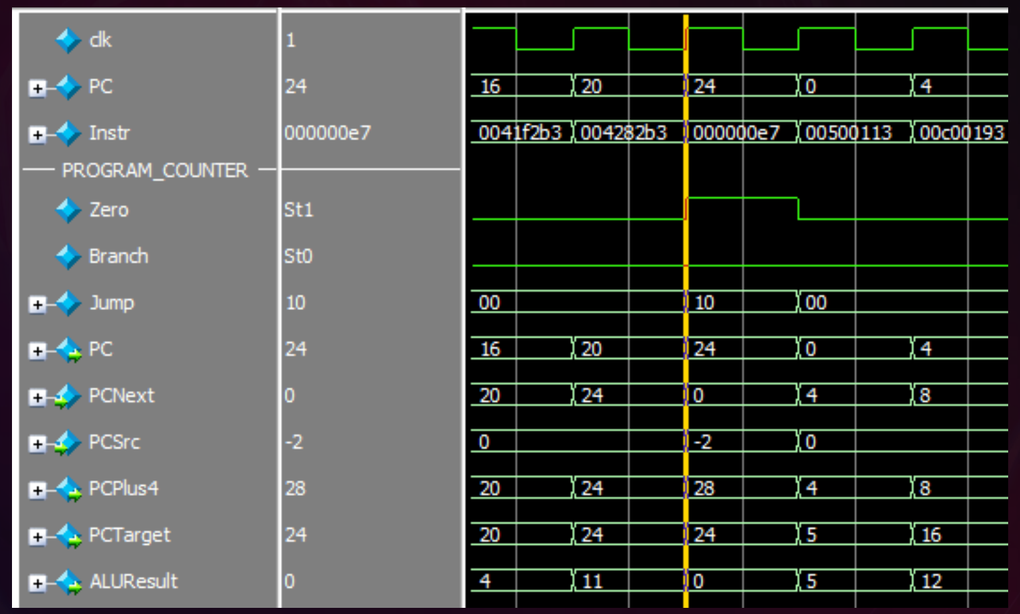
TAKEN

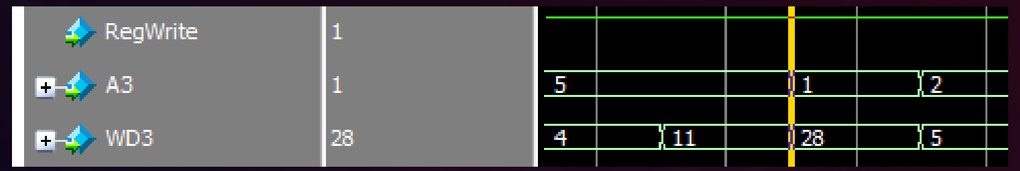
SIM RESULTS



JAL X3 8

X3 = 68

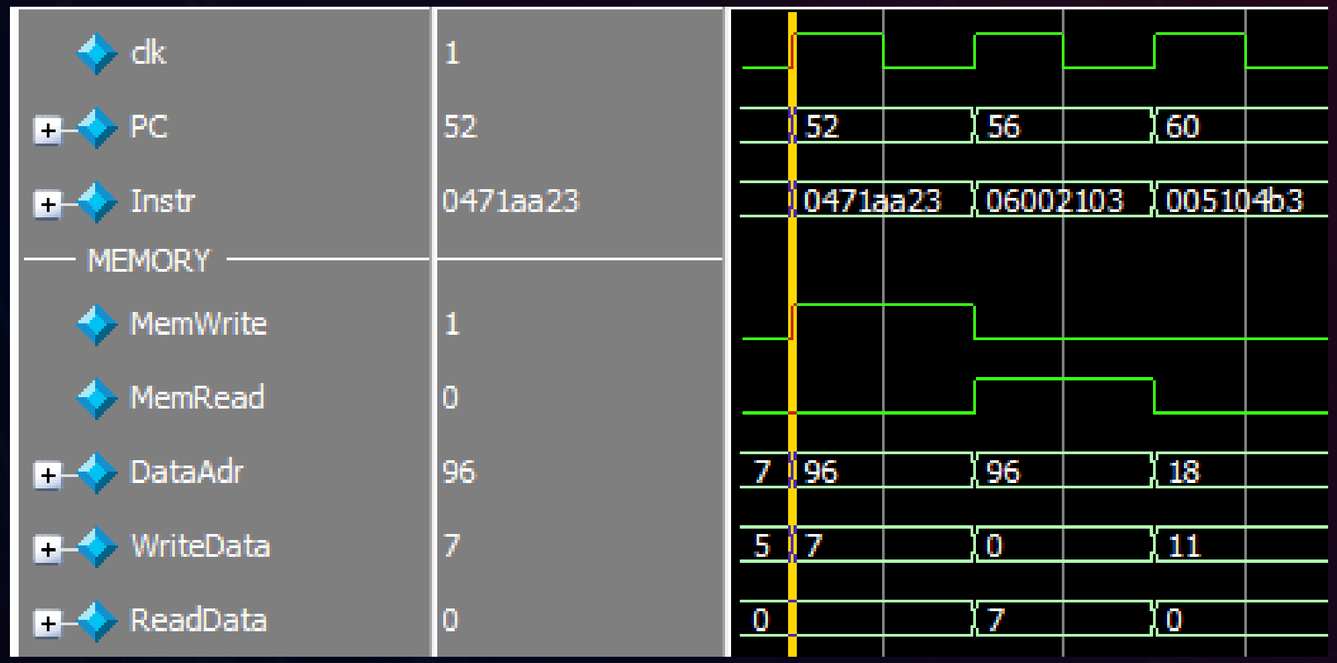




JALR X1 X0 0

X1 = 28

SIM RESULTS



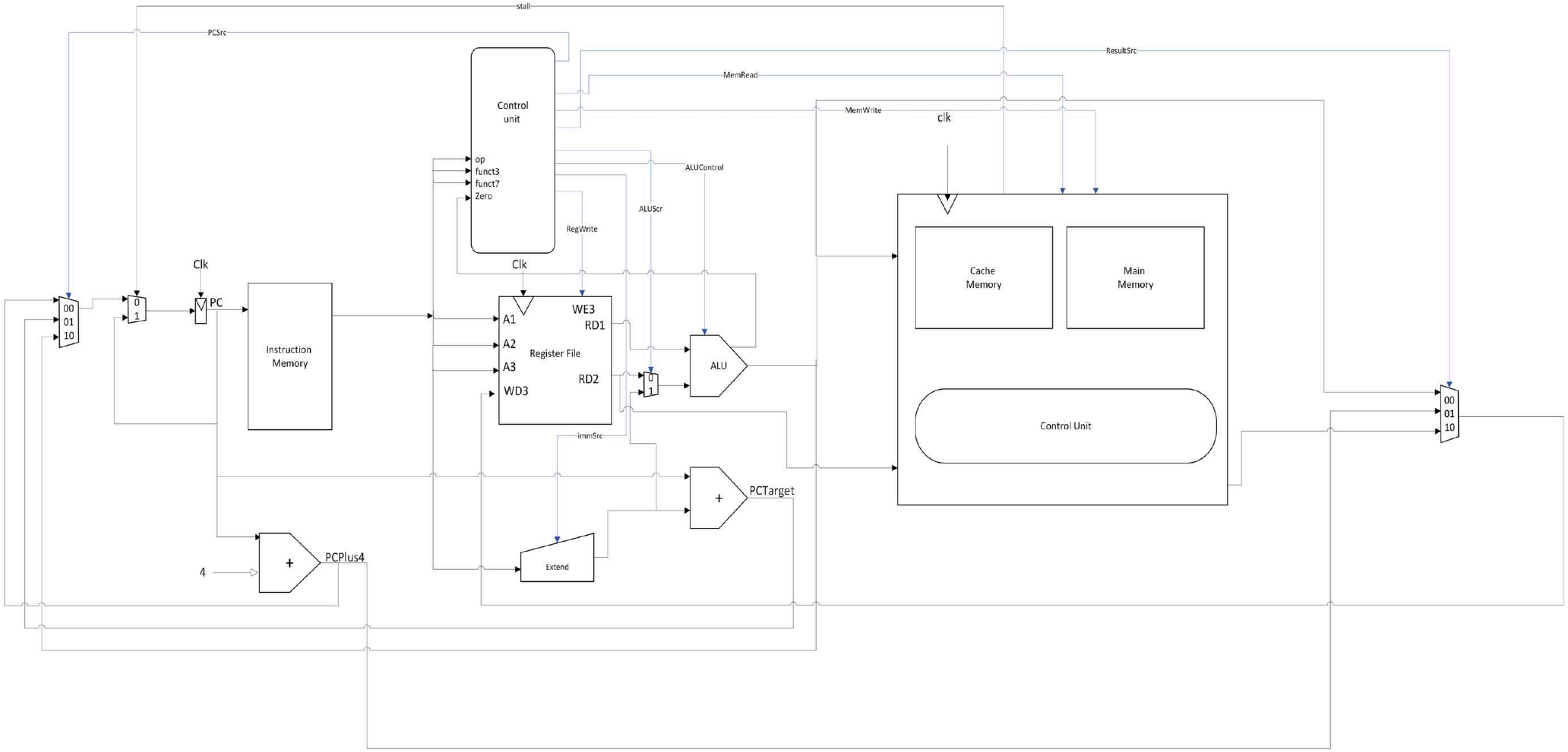
SW X7 84(X3)

X7 = 7 , X3 = 12

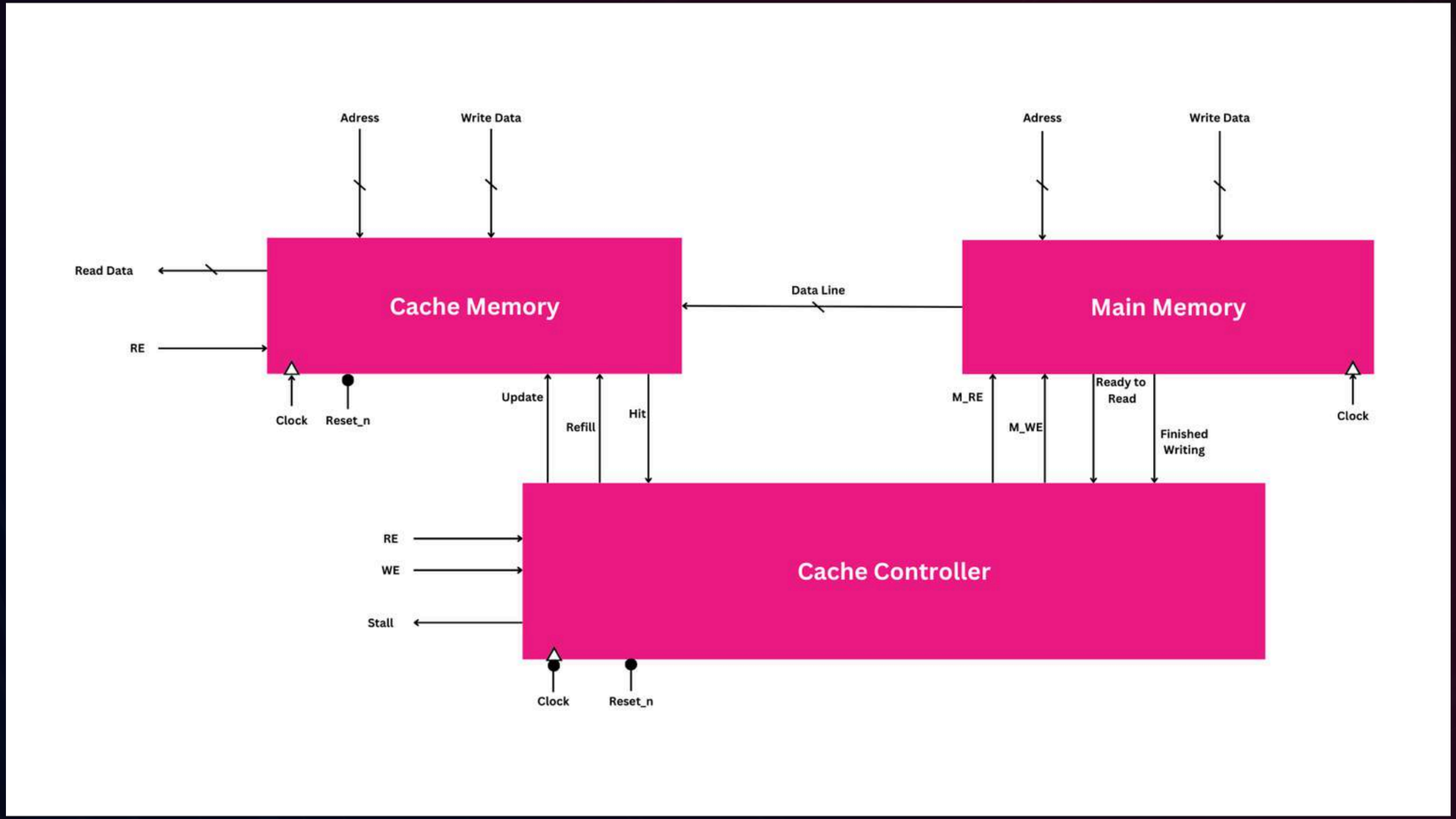
LW X2 96(X0)

X2 = 7

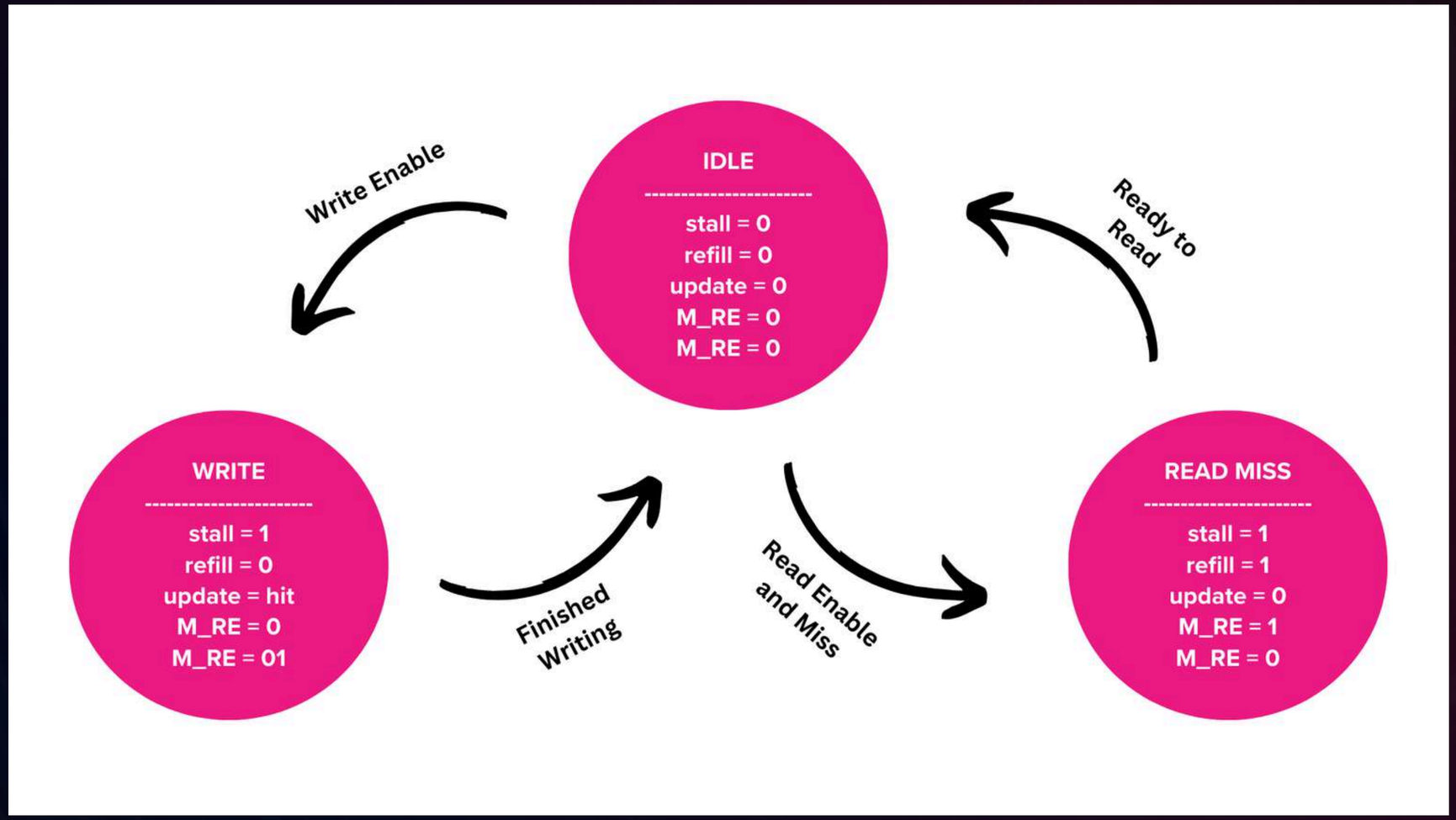
INTEGRATION WITH CACHING SYSTEM


stall
PCSrc
ResultSrc
MemRead
Control unit
op
funct3
funct7
Zero
MemWrite
clk
ALUControl
ALUScr
RegWrite
Clk
Clk
00
01
10
0
1
PC
Instruction Memory
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
ALU
0
1
immSrc
Cache Memory
Main Memory
Control Unit
00
01
10
+
PCTarget
4
+
PCPlus4
Extend

BLOCK DIAGRAM



STATE DIAGRAM



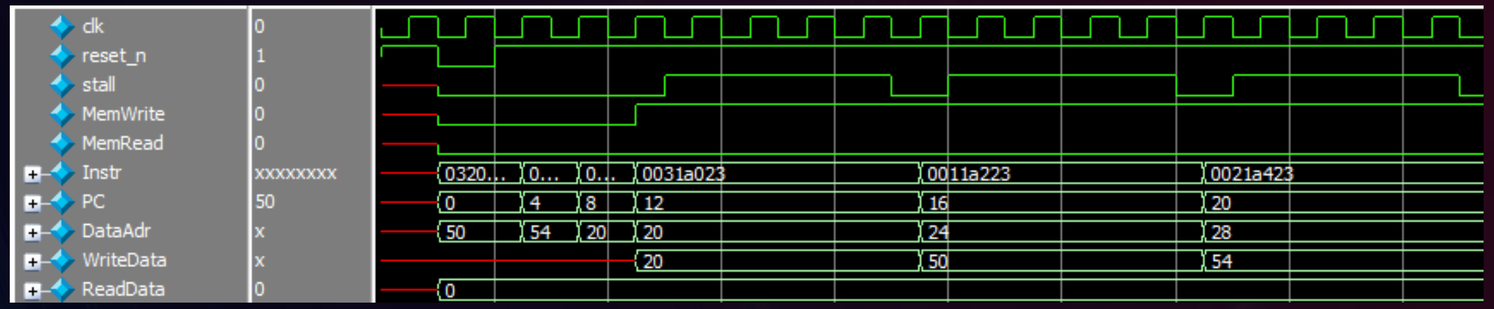
SIM RESULTS

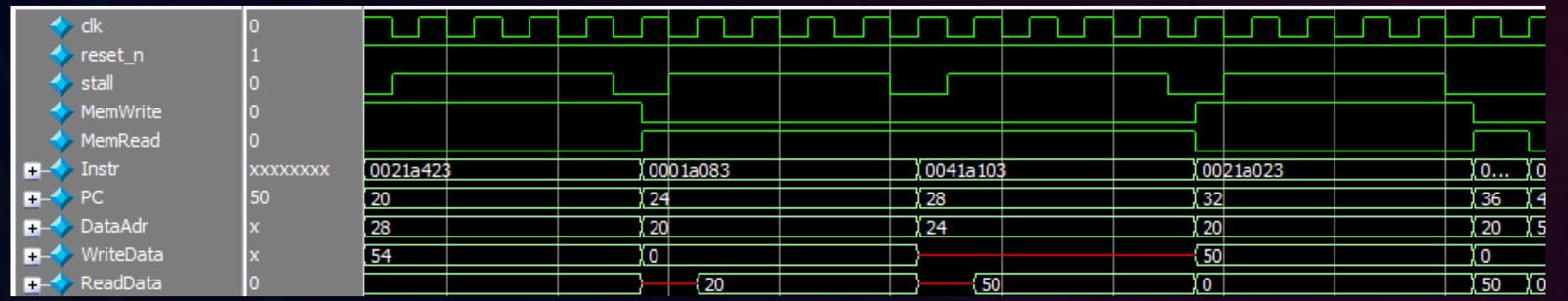
1-ADDI X1, X0, 50
2-ADDI X2, X0, 54
3-ADDI X3, X0, 20

4-SW X3, 0(X3)
5-SW X1, 4(X3)
6-SW X2, 8(X3)

7-LW X1, 0(X3)
8-LW X2, 4(X3)

9-SW X2, 0(X3)
10-LW X1, 0(X3)



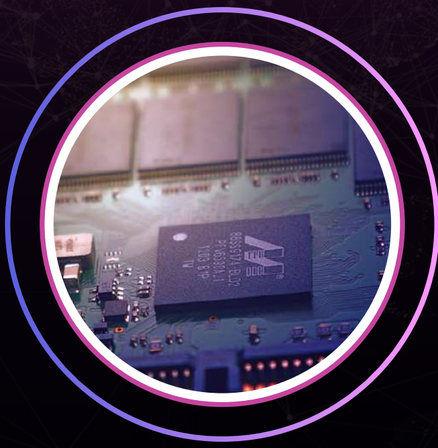


Future Work

FUTURE WORK

Specific Instructions

High Performance Memory system



Final Chip Product

QUESTIONS?

IT IS NOT THE END.
IT IS THE BEGINNING.