

Electronic Circuits

design and Simulation

Report 2

Design and Implementation of 32-bit RISC Processor using modelsim

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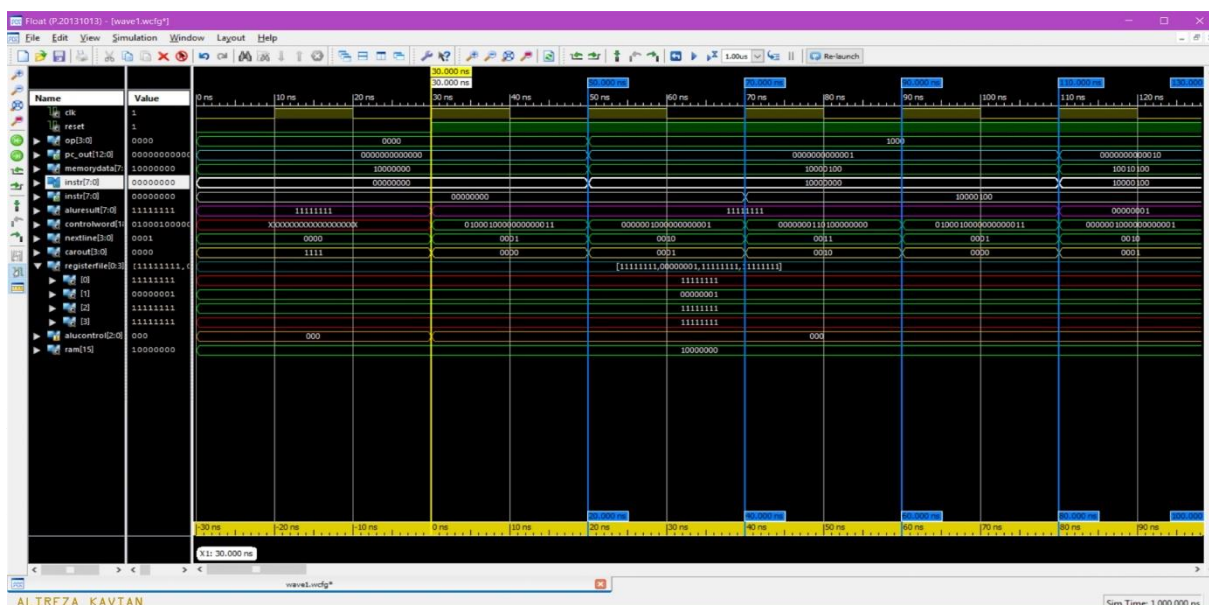


Objective:

This RISC or Reduced Instruction Set Computer is a design philosophy that has become mainstream in Scientific and engineering applications. The main objective of this paper is to design and implement of 32-bit RISC (Reduced Instruction Set Computer) processor using a modelsim tool. The design will help to improve the speed of processor and to give the higher performance of the processor. The most important feature of the RISC processor is that this processor is very simple and supports load/store architecture. The important components of this processor include the Arithmetic Logic Unit, Shifter, Rotator, and Control unit.

Introduction:

VHDL, or Very High-Speed Integrated Circuit Hardware Description Language, is integral to digital design and electronic systems, offering a structured approach to model hardware behavior. It enables designers to create detailed system models for simulation before hardware implementation, aiding in issue identification, performance optimization, and error reduction. VHDL supports the verification process through test benches and test vectors, crucial for detecting and correcting errors early in the design phase. Additionally, it is commonly used with synthesis tools to convert high-level descriptions into hardware-compatible forms. VHDL's modular design approach fosters reusability, collaboration, and the development of large systems by breaking them into manageable modules. As an IEEE standard (IEEE 1076), VHDL ensures consistency and interoperability across different tools and platforms. Its significance extends to education and research, serving as a fundamental language for teaching digital design and enabling the exploration of new methodologies. In summary, VHDL is indispensable in the digital design lifecycle, playing a pivotal role in conceptualization, simulation, and verification for engineers in the field of electronic design.





Conclusion:

A 32-bit RISC processor with 16 instruction set has been designed. Every instruction is executed in one clock cycles with 5-stage pipelining. The design is verified through exhaustive simulations. The processor achieves higher performance, lower area and lower power dissipation. This processor can be used as a systolic core to perform mathematical computations like solving polynomial and differential equations. Apart from this it can be used in portable gaming kits.

Appendix:

https://github.com/MohamedFadl2344/Risc_CPU_32bit.git



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