Expeiment .2

And Gate

InternalArcitecure

Truth table

input a	input b	output
0	0	0
0	1	0
1	0	0
1	1	1

Truth table verification

OR Gate

InternalArcitecure

Truth table

input a	input b	output
0	0	0
0	1	1
1	0	1
1	1	1

Truth table verification

NAND Gate

InternalArcitecure

Truth table

INPUT	INPUT	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

Truth table verification

NOR Gate

InternalArcitecure

7402 Quad 2-input NOR Gates

Truth table

input a	input b	output
0	0	1
0	1	0
1	0	0
1	1	0

Truth table verification

NOT Gate

InternalArcitecure

Truth table

INPUT	OUTPUT
0	1
1	0

Truth table verification

XOR Gate

InternalArcitecure

Truth table

INPUT	OUTPUT	output
0	0	0
1	0	1
0	1	1
1	1	0

Truth table verification

Implementing INV using NOR gate :

We connect the 2 input so they receive the same value and from the truth table of NOR, when we enter 2 zeros the output is 1 , and when we enter 2 ones the output is 0 so we can use it as an inverter

INPUT	OUTPUT
0	1

Implementing an OR gate using NANG gate and two INV : Bonus

INPUT	OUTPUT	output
0	0	0
1	0	1
0	1	1
1	1	1

Implementing an AND gate using NOR gate and two INV : Bonus

INPUT	OUTPUT	output
0	0	0
1	0	0
0	1	0
1	1	1

Expeiment .3

PROCESURE (1)

Truth Table of

Binary To Gray Code converter

A	B	C	D	G1	G2	G3	G4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

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Schematic Capture
Device Libraries
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7486
LOGICPROBE (BIG)
LOGICSTATE
[74LS86]
[7486]
U1:A
U1:B
U1:C
74LS86
2 Message(s)
ANIMATING: 00:06:10.850000 (CPU load 0%)

Template System Help
Base Design
U1:A
U1:B
U1:C
74LS86

Schematic Capture
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LOGICPROBE (BIG)
LOGICSTATE
[74LS86]
[7486]
U1:A
U1:B
U1:C
74LS86
2 Message(s)
ANIMATING: 00:01:10.350000 (CPU load 0%)

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LOGICSTATE
[74LS86]
[7486]
U1:A
U1:B
U1:C
74LS86
2 Message(s)
ANIMATING: 00:01:32.750000 (CPU load 0%)

2) 5-BIT BINARY TO GRAY

A	B	C	D	E	a	b	c	d	e
0	1	0	1	1	0	1	1	1	0
1	1	0	0	1	1	0	1	0	1

PROCESURE (3)-A

CIRCUIT IMPLEMENTS THE TABLE

Truth Table

A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

This circuit is a 2-input 4-output decoder

Decoder that has a set of two or more bits will be defined as having an n-bit code, and therefore it will be possible to represent 2n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its n outputs to logic"1".

If a binary decoder receives n inputs (usually grouped as a single binary or Boolean number) it activates one and only one of its 2n outputs based on that input with all other outputs deactivated.

QUESTION 4 THE CIRCUIT WILL BE ATTACHED TO THE FILE

7-segment .pdsprj

7-segment display truth table

A	B	C	D	a	b	c	d	e	f	g	sympol
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	1	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	0	1	1	1	1	0	1	1	9

7-segment - Proteus 8 Professional - Schematic Capture

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Base Design

Schematic Capture

DEVICES

7SEG-COM-AN-GRN
7SEG-COM-CAT-GRN
9C04021A3300FLHF3
74LS47
LOGICSTATE
MINRES330R

No Messages

Root sheet 1

-4900.0

+2400.0

Questions:

ANSWER (1)-A CIRCUIT CONVERTS GRAY TO BINARY :

ANSWER(2)-WE CONVERT IT TO ACTIVE LOW BY CONNECTING INVERTERS TO THE OUTPUTS OF THE AND GATES AT THE END

ANSWER(3) – TO VERIFY THAT THE COMMON ANODE IS DIFFERENT FROM COMMON CATHODE WE SEE IN THE FIGURE (common cathode is connected to ground and all leds are connected to the VCC terminal and used reverse decoder in it)

Answer(4):

We connect inputs of the display with 330 ohm resistors because the display bears up to limited value of voltage if volt exceeds that it will be burnt .