Term Project

Design, Simulation, and Implementation of a Multistage BJT Audio Amplifier with Volume Control

In this project, you will design, simulate, and implement a multistage BJT audio amplifier with volume control. The block diagram is shown in Figure 1. The sound source is your smart phone ("**Frequency Generator**" Android Application). The audio signal is amplified by the first stage (a CE preamplifier). The second stage is a buffer (common collector / emitter follower). The third and last stage is a class AB power amplifier to drive the speaker.

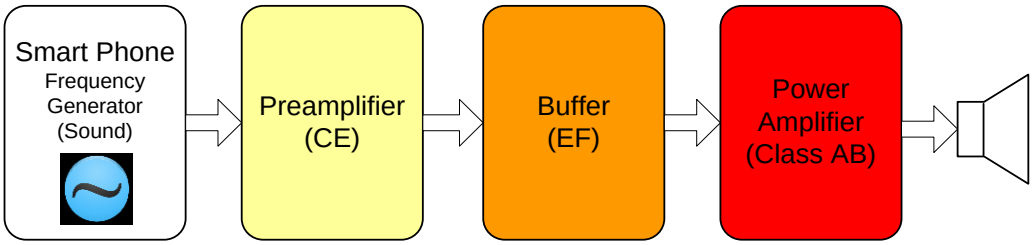

Figure 1 System block diagram.

Design Procedure and Technical Insights

The schematic of the amplifier drawn in Multisim is shown in Figure 2. In this section, we will explain the different components of the system, **starting from the speaker and going backward**. **Note that for all the values given/computed a deviation of about 10% is usually acceptable. Also note that the you do not have to exactly follow the design procedure explained below. You can make changes, BUT you must explain and justify them very well.**

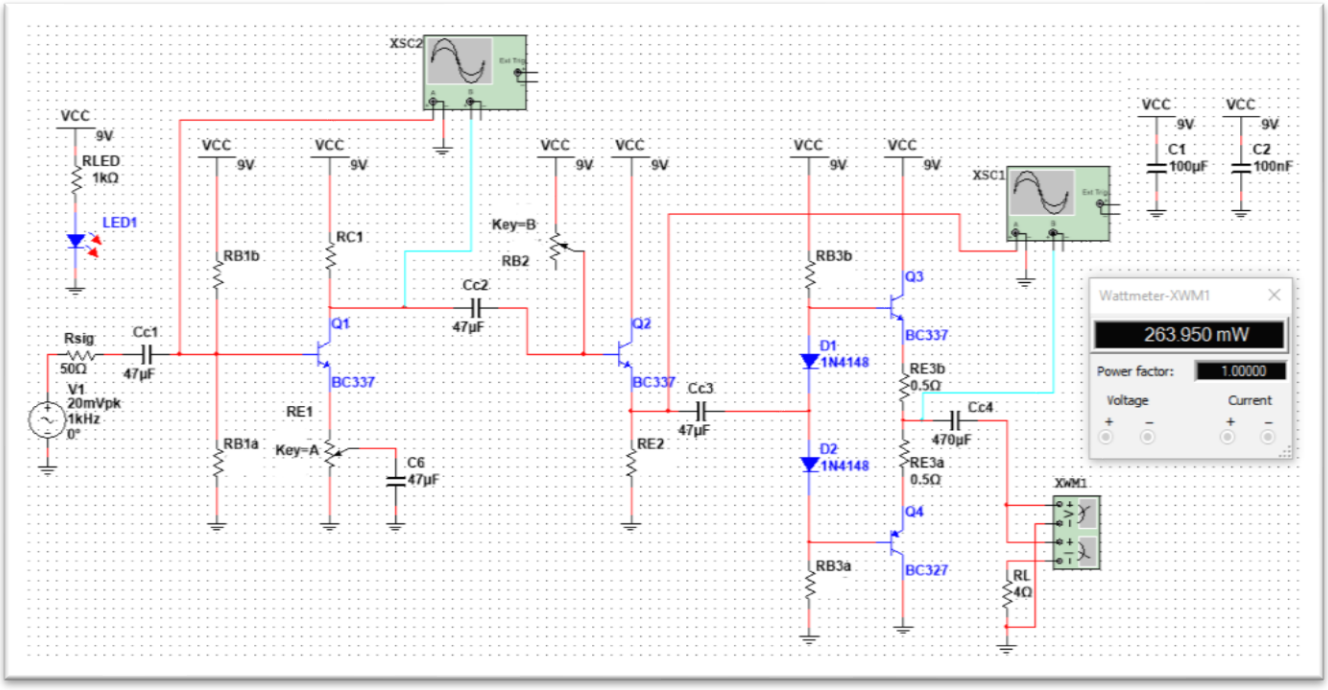

Figure 2 Amplifier schematic in Multisim. The resistor values are not shown because you have to do the design by yourself!

1. The Speaker (R_L)

- The recommended speaker is a 4Ω 0.5W speaker. An 8Ω 0.25W speaker will also work, but the sound will be weaker.
- We want to deliver about 3Vpk-pk at the speaker → $V_{pk} \approx 1.5V$.
- This means that the power delivered to the speaker is $\approx \frac{V_{pk}^2}{2R_L} \approx 280mW \approx 25dBm$ → quite good for a class project! The sound you will hear will be nicely loud!
- The max current going into the speaker is $I_{pk} \approx \frac{V_{pk}}{R_L} \approx 375mA$ → this is a large current! But it is necessary to give the clearly audible sound we are looking for.
- In Multisim, connect a wattmeter across the speaker as shown in Figure 2. The wattmeter will display the power delivered to the speaker.
- A DC voltage directly connected to a speaker may damage it. That's why we connect the speaker to the amplifier via a **large** coupling capacitor C_{C4}.

2. The Class AB Power Amplifier (Stage III: Q3 and Q4)

- As you have just seen, the speaker needs a lot of current (power) to give audible sound.
- The amplifier that delivers "high power" to the load is called a power amplifier (PA).
- A simple ordinary amplifier cannot do this job in an efficient way.
- A very popular power amplifier for audio applications is the push-pull class AB power amplifier, which is the one used in Figure 2.
- You can think of the class AB PA as two EF amplifiers (NPN + PNP). The NPN is conducting when the input signal is positive (e.g., positive half cycle of a sine wave), and the PNP is conducting when the input signal is negative (e.g., negative half cycle of a sine wave). That's why it is called push-pull PA.
- You can find more details about class AB PA at this link: http://www.electronics-tutorials.ws/amplifier/class-ab-amplifier.html
- The small 0.5Ω resistors are used to limit the current and prevent the overheating of the transistors.
- Design the resistors $RB3a$ and $RB3b$ such that the current flowing through the bias branch is $\approx \frac{I_{pk}}{20}$ (get I_{pk} from the previous subsection). In the class we usually used $\approx \frac{I_C}{10}$, but the current in the PA is already very high, so we reduced the bias branch current by a factor of 2 to be $\approx \frac{I_C}{20}$. Also higher current in the bias branch means smaller resistance and more loading on Stage II. Note that a $\pm 10\%$ deviation in the resistor values is usually acceptable.
- You can get V_{BEon} of the diodes from their datasheets.
- Calculate the input resistance of this stage $R_{in3} \approx RB3a//RB3b//\beta R_L \approx RB3a//RB3b$.

3. The CC (EF) Buffer (Stage II: Q2)

- If we connect the PA directly to the preamplifier, it will cause loading effect that drastically reduces the gain. That's why we place a buffer stage in between.
- Plot the DC load line and the AC load line of the buffer stage. Prove that the max allowable signal amplitude at the buffer output is approximately given by

$$V_{pk} \approx I_{CQ2}(R_{E2}//R_{in3}) \approx V_{E2}\frac{R_{in3}}{R_{E2}+R_{in3}}$$

- Since the amplitude of the PA is 1.5V, we would like to take some margin and design the buffer to support an amplitude of 2V.
- We will select a bit large V_{E2} to allow for a bit large R_{E2} (large R_{E2} reduces loading on previous stage). Let's design the bias point such that the voltage at the emitter $V_{E2} \approx 6V$. Thus, you can now simply calculate R_{E2} from the previous equation.
- You can now calculate the bias current I_C and gain of this stage.
- Get the value of β from the transistor datasheet. You will find it written in the datasheet as DC current gain or h_{FE}. Note that it depends on the bias current.

- Select R_{B2} to satisfy the required bias point ($V_{E2} \approx 6V$). Note that R_{B2} will be sensitive to β. Since β is not stable, it is better to implement R_{B2} as a potentiometer and adjust it till you get $V_{E2} \approx 6V$.
- Calculate the input resistance of this stage (R_{in2}).

4. The CE Preamplifier (Stage I: Q1)

- Stage II and stage III provide large current gain.
- The purpose of stage I is to provide voltage gain.
- Remember that power gain = voltage gain x current gain.
- This stage is a simple CE amplifier with a bypass capacitor.
- The volume control is implemented as follows: The bypass capacitor is connected to a potentiometer (R_{E1}). Thus, we can introduce some degeneration to reduce the gain. Note that as we change the volume the bias point will remain unchanged.
- In class we studied the (1/3 + 1/3 + 1/3 rule). However, in this circuit we would like to give more priority to the voltage gain and signal swing. Thus, we will design the bias such that the voltage at the emitter $V_{E1} \approx 1V$.
- We will use a bias current $I_C = 2$mA. This bias current will ensure that the loading effect of R_{in2} is small. Note that a higher bias current dictates smaller R_C (i.e., smaller R_{out}) but also smaller r_π (i.e., smaller R_{in}). We don't have to worry a lot about R_{in} of this stage as we will show in the next subsection.
- Let's select the voltage at the collector to be $V_{C1} \approx 4V$. This is a 2V deviation from our (1/3 + 1/3 + 1/3 rule) in order to allow higher gain and higher signal swing.
- Calculate the values of R_{C1} and R_{E1}.
- Calculate the **max and min voltage gain (that corresponds to max and min volume)**, i.e., without degeneration and with full degeneration.
- Design the resistors $RB1a$ and $RB1b$ such that the current flowing through the bias branch is $\approx \frac{I_{CQ}}{10}$ and $V_{E1} \approx 1V$. Actually, a current $\approx \frac{I_{CQ}}{5}$ may be a better choice here because I_{CQ} is already small and R_{in1} is not critical.
- Note that the resistive divider output (the resistors ratio) this time is a bit important, so you should implement R_{B1} as potentiometer and adjust it till you get the required bias point ($V_{E1} \approx 1V$).
- You will notice that the output signal is a bit distorted (the positive half cycle is smaller than the negative half cycle). The reason is not the AC load line this time. The reason is that the gain depends on g_{m1}, which depends on I_{C1}, which depends on the output voltage! Simply, at the positive half cycle, V_{RC1} is smaller; thus, the gain is smaller. Better linearity can be achieved by using degeneration where the gain is approximately $-\frac{R_C}{R_E}$ which is independent of the bias point. However, this gain will be small and we will have to use two gain stages.
- Calculate the input resistance of this stage (R_{in1}).

5. The Signal Source (Your Smart Phone)

- You will test the amplifier using this app on your smart phone to generate sine wave (single tone) of different frequencies: https://play.google.com/store/apps/details?id=com.seventeenchoices.frequencygenerator&hl=en
- Your smart phone can generate a signal of variable amplitude (controlled via the smart phone volume control) with relatively small output resistance. The amplitude typically range from 2mV to 200mV and the output resistance is typically few tens of Ohms.
- In Multisim, we will model the smart phone as a 20mVpk signal source with 50Ω output resistance and 1kHz frequency as shown in Figure 2. You can try to vary the amplitude and adjust the volume using R_{E1}.
- Since the output resistance is relatively small, the loading effect due to R_{in1} is negligible.

- The DC voltage may damage the smart phone sound source; thus, we must use a coupling capacitor C_{C1}.

6. The Power Supply

- You will use a 9V supply.
- The quality (cleanliness and stability) of the power supply greatly affects the sound quality.
- Note that there are decoupling capacitors connected to the supply in Figure 2. These capacitors filter out any noise or spikes.
- You cannot use a simple 9V battery because the current consumption is a bit high, so the battery will be depleted in a very short time.
- You need a power supply that can provide up to 500mA of current.
- A good option is to use a power supply like the one found in desktop computer cases.
- You can also use a good charger or a good voltage adapter. But in this case, it is better to generate 12V from the adapter, then use a positive voltage regulator like LM3809 to generate a clean 9V supply. Add decoupling capacitors. Check how to connect the circuit on the internet.
- You can also create your own power supply as in the Bonus Project that will be offered by your TAs!
    - **WARNING! ELECTRIC SHOCK HAZARD: If you design your own power supply, you will be dealing with the mains electricity (220V and HIGH CURRENT). This can be VERY DANGEROUS. You must be VERY CAUTIOUS.**
    - If you want to do your own power supply, you will find this link helpful: http://www.learnabout-electronics.org/PSU/psu10.php

7. The LED (LED1)

- The LED shown in Figure 2 is a nice way to show that your power supply is ON.

8. Capacitive coupling

- C_{C1} and C_{C4} are necessary as mentioned before because we use a single supply (they can be removed in a complex dual supply system).
- In this project, we also use coupling capacitors between the amplifier stages. This simplifies the design process because we can adjust the DC bias of each stage independently.
- Commercial audio amplifiers usually use direct coupling between stages as it provides better sound quality.

9. The Microphone (This part is optional. It will give you 3 bonus points.)

- The input signal you used is coming from a smart phone. If you modify the amplifier to accept additional input from a microphone, you will receive 3 bonus points. The sound generated by the speaker must be loud and clear.
- Dynamic mic is a bit expensive. Its output signal is similar to the smart phone output signal. It does not need any powering. It also has relatively low output impedance. It can be connected directly to the preamplifier.
- Condenser (electret) mic is cheaper and easier to find. It has relatively high output impedance (few $k\Omega$). Also it must be powered by connecting it to V_{CC} via a bias resistance. Check the mic datasheet for details.
- The condenser mic signal is also very weak (few mV). Thus, you will need additional amplification stage. The additional stage can be similar to the CE first stage shown in Figure 2, but try to get higher input impedance to avoid loading.

10. Other Useful Hints

- You can find electronic components datasheets and prices at this link: http://ram-e-shop.com
- For Q1 and Q2 you can use any common transistor like 2N3904 NPN BJT transistor.
- For Q3 and Q4 you need a transistor that can handle higher current like the one used in Figure 2.

- When debugging your circuit, start with your supply, then the bias point of every stage.
- You can test the signal amplitude using your DMM AC measurement. The DMM is originally designed to measure low frequencies (50-60Hz). But usually it can also measure frequencies of few kHz with a small error. Note that the DMM measures the rms signal. $V_{pk} = \sqrt{2} \times V_{rms}$.

Deliverables

You will deliver a detailed report and a working prototype. Read this section carefully.

1. The Report

The report should contain the following:

1) Detailed design procedure including how you determined all component values. **Answer all the questions in the "Design Procedure" part.** Clearly calculate the gain of every stage and the overall gain of the amplifier.
2) Simulation results using Multisim. Report the following:
    a. The schematic with Wattmeter snapshot showing > 250mW of power as in Figure 2.
    b. Oscilloscope snapshots clearly showing the input signal and the output signal of every stage. Use white background. The signals should be clean sine waves without significant distortion. The final output should be larger than 2.5Vpk-pk.
    c. Measure the gain of every stage from the simulation.
3) Compare the gain you got from simulations with that of hand calculations in a table.
4) A clear photograph of your implemented prototype.
5) Simulate and measure the frequency bandwidth of the amplifier
    a. First, in Multisim, record the power in the load at 1kHz frequency. This is the mid band power: Po. Decrease the frequency till the power is 0.5 Po. This is the lower cutoff frequency. Increase the frequency above 1kHz till the power is again 0.5 Po. This is the higher cutoff frequency. These min and max frequencies define the bandwidth of your amplifier.
    b. Second, in the implemented circuit, set the Android app frequency to 1kHz and record the RMS output voltage at the load using a DMM. This is the midband output: Vo. Decrease the frequency till the output is Vo/sqrt(2). This is the lower cutoff frequency. Increase the frequency above 1kHz again till the output is Vo/sqrt(2). This is the higher cutoff frequency. These min and max frequencies define the bandwidth of your amplifier.
    c. Third, compare simulation and measurement.
6) A table showing the contribution of each member in the group.
7) **Feedback and comments from your side on the project (what you liked about the project and what can be improved in the future).**

2. The Circuit

- When you deliver the circuit to the TA it MUST BE working. There will be no time for debugging.
- **Bring a printed hard copy of your report.**
- You can implement the circuit on a bread board.
- If you do it on a PCB you will get 2 bonus points.
- Bring your own power supply to test the circuit.
- Please note that we will just check your implemented circuit. We will not take it from you. If it is on a PCB you can keep it till you show it to your children inshaAllah ☺

Instructions and Deadlines

- **This is a group project. Each group can be 6 to 10 students. Each group must have a leader.**
- **In Canvas, each group leader should go to "People" tab and add himself and his group members to an empty group.**
- **Students of the same group must be of the same gender (mixed groups are not allowed).**
- **If your group is less than 6 then you must find group-less students and ask them to join your group. If you can't meet because the extra member lives far away, he may handle a standalone part of the project (ex: simulation or the bonus project).**
- **Use camscanner on Android to take professional scan of your analysis and insert it in your report. You don't have to rewrite it on MS Word.**
- **If you buy electronic components from "west el-balad", please be very cautious as you may run into problems if you are found carrying electronic components at security check points (especially in the underground). They may not understand that you are an electrical engineering student.**
- **Deadline for delivering the project report ONLINE on Canvas (single pdf < 2MB): Tue July-2nd 10:59 PM.**
- **Delivering the circuit to TAs and project discussion: Wed and Thu July-3rd and 4th (exact time for each group will be announced later.**