AMBA APB Vivado Report

Created By:

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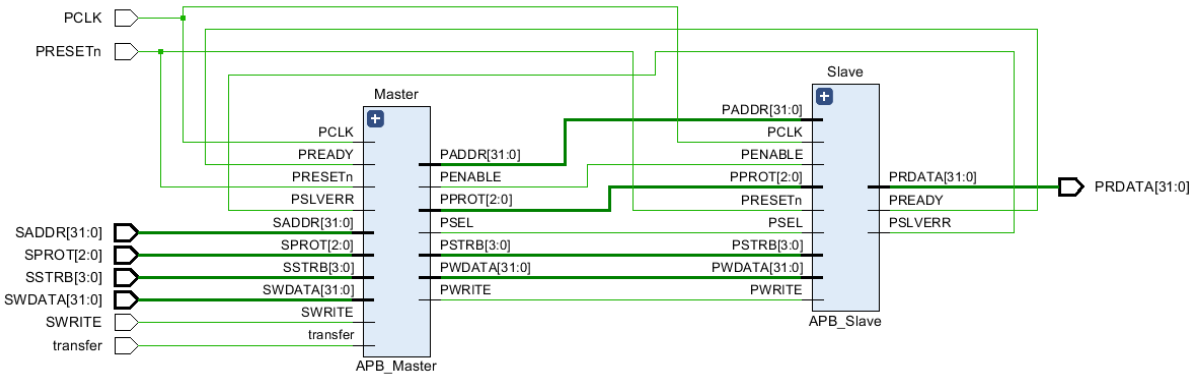
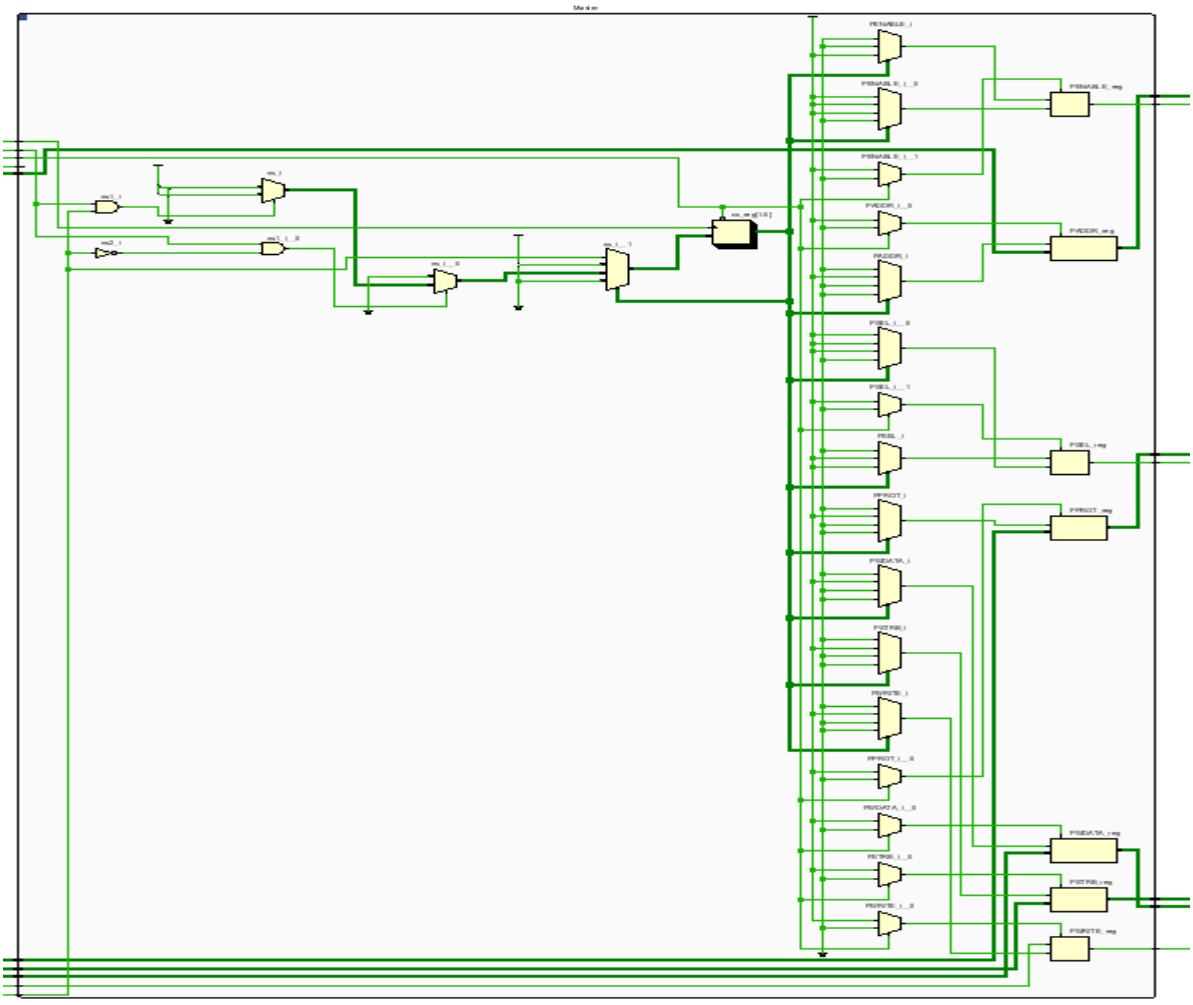
Vivado:

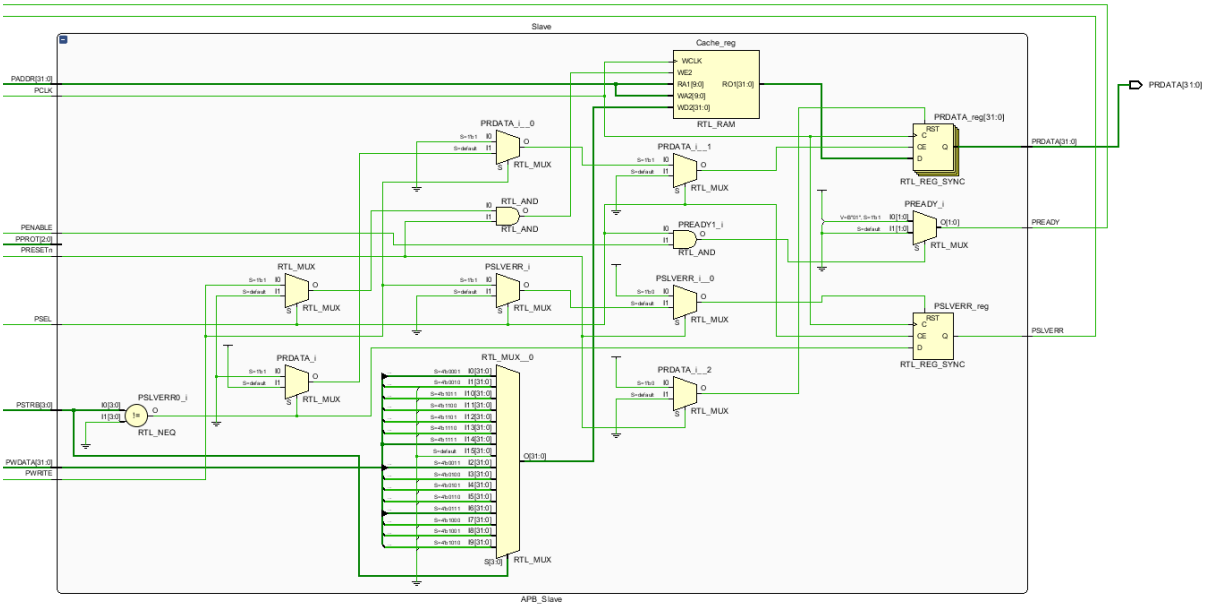
- Elaboration:
  - System:



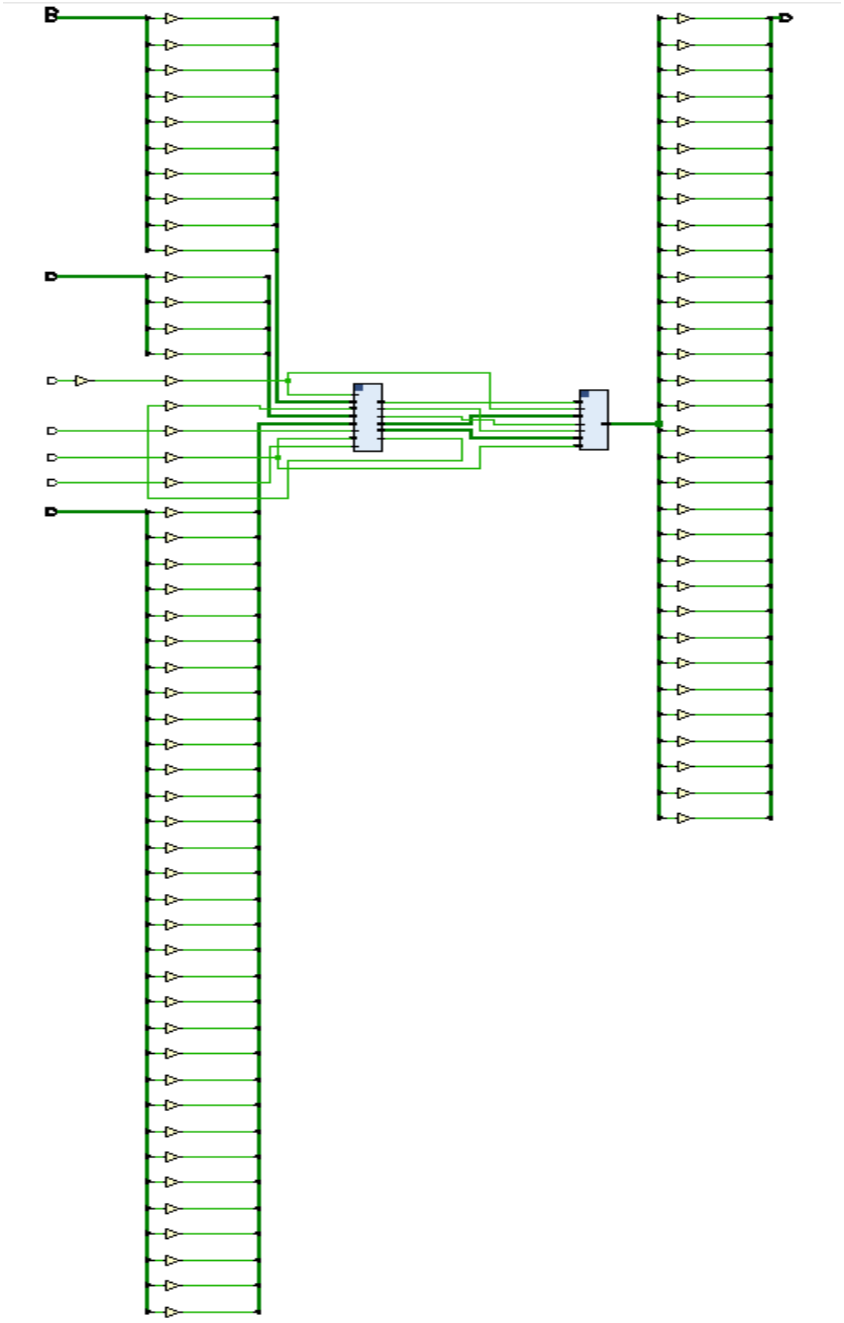
  - Master:



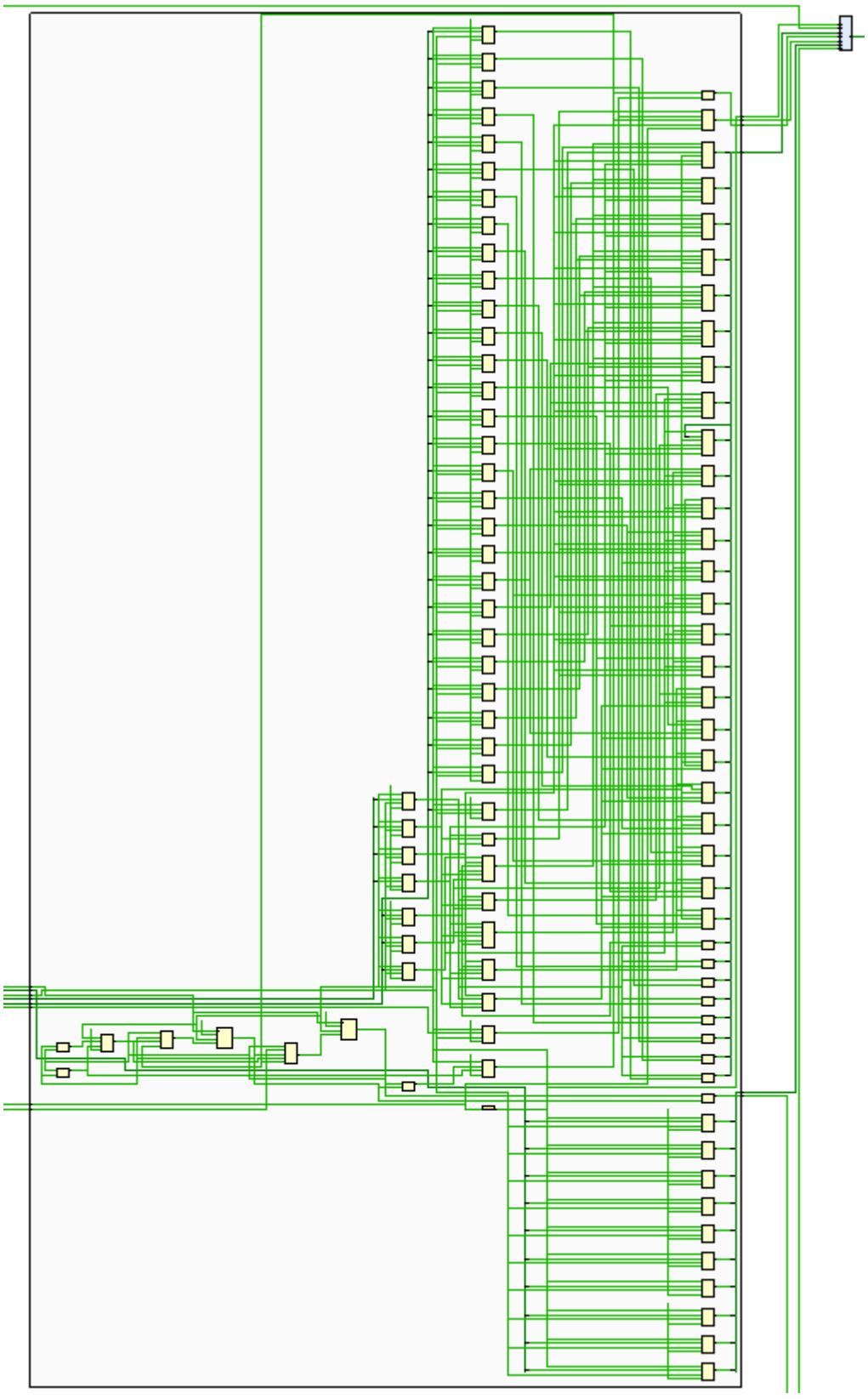
- Slave:


Slave
PADDR[31:0]
PCLK
PENABLE
PPROT[2:0]
PRESETn
PSEL
PSTRB[3:0]
PWDATA[31:0]
PWRITE
Cache_reg
WCLK
WE2
RA1[9:0]
RO1[31:0]
WA2[9:0]
WD2[31:0]
RTL_RAM
PRDATA_i__0
PRDATA_i__1
PRDATA_i__2
PRDATA_i
RTL_MUX
RTL_AND
PREADY1_i
PSLVERR_i
PSLVERR_i__0
RTL_MUX__0
PSLVERR0_i
RTL_NEQ
PRDATA_reg[31:0]
PSLVERR_reg
RTL_REG_SYNC
PREADY_i
PRDATA[31:0]
PREADY
PSLVERR
APB_Slave

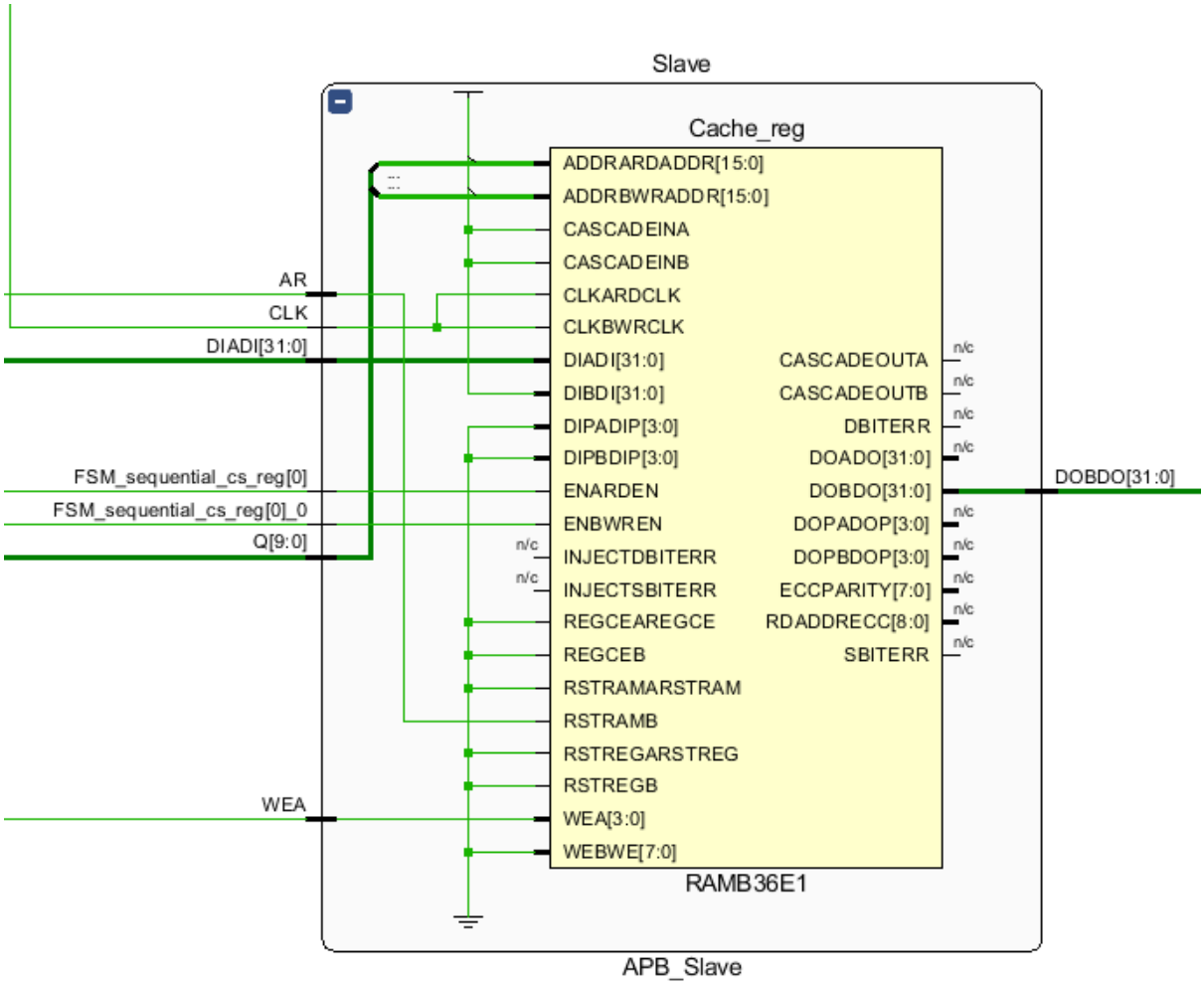
- **Synthesis:**
  - **Seq:**
    - Schematic:
      - System:



- Master:



- Slave:

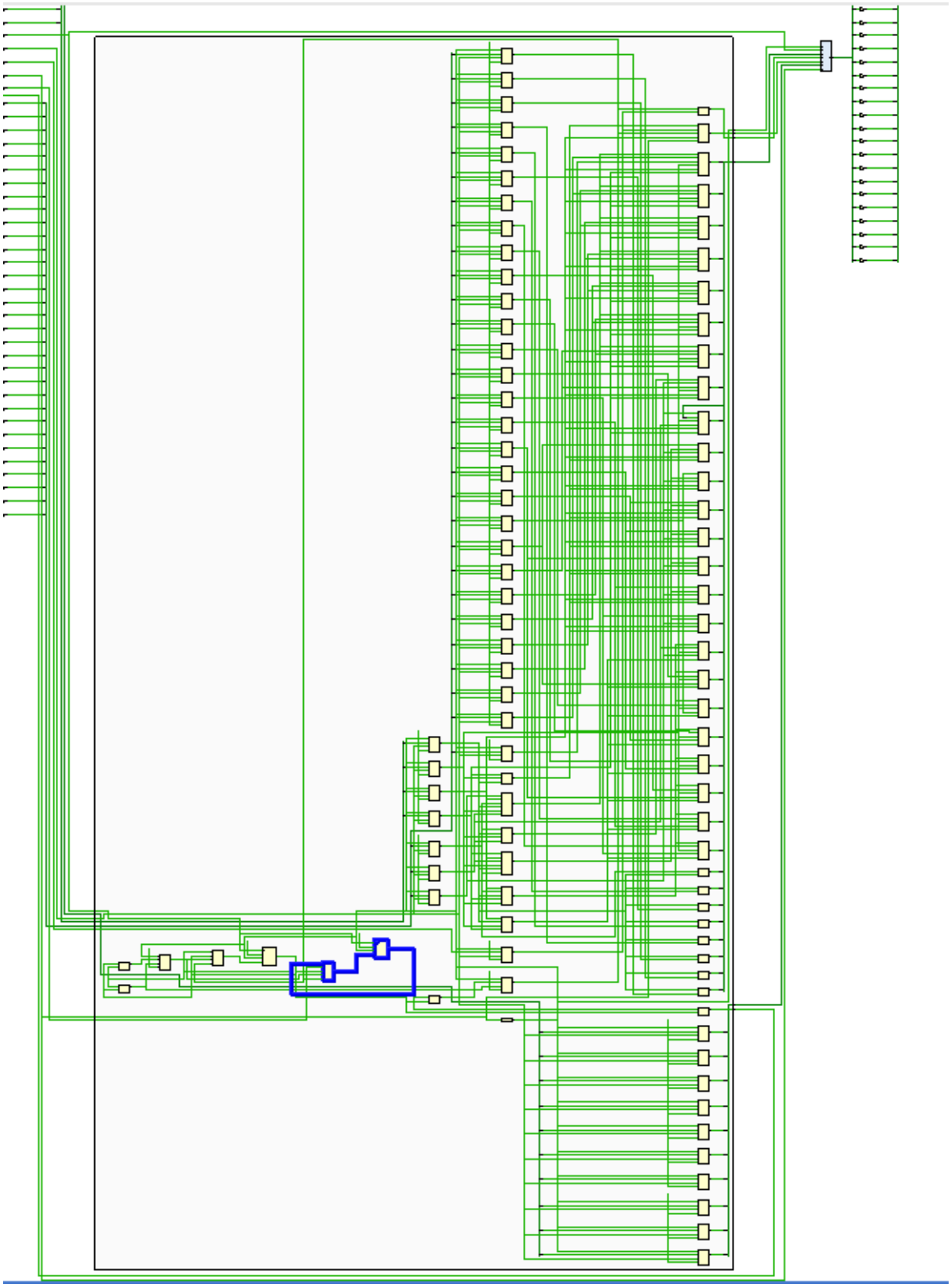


- Encoding Report:

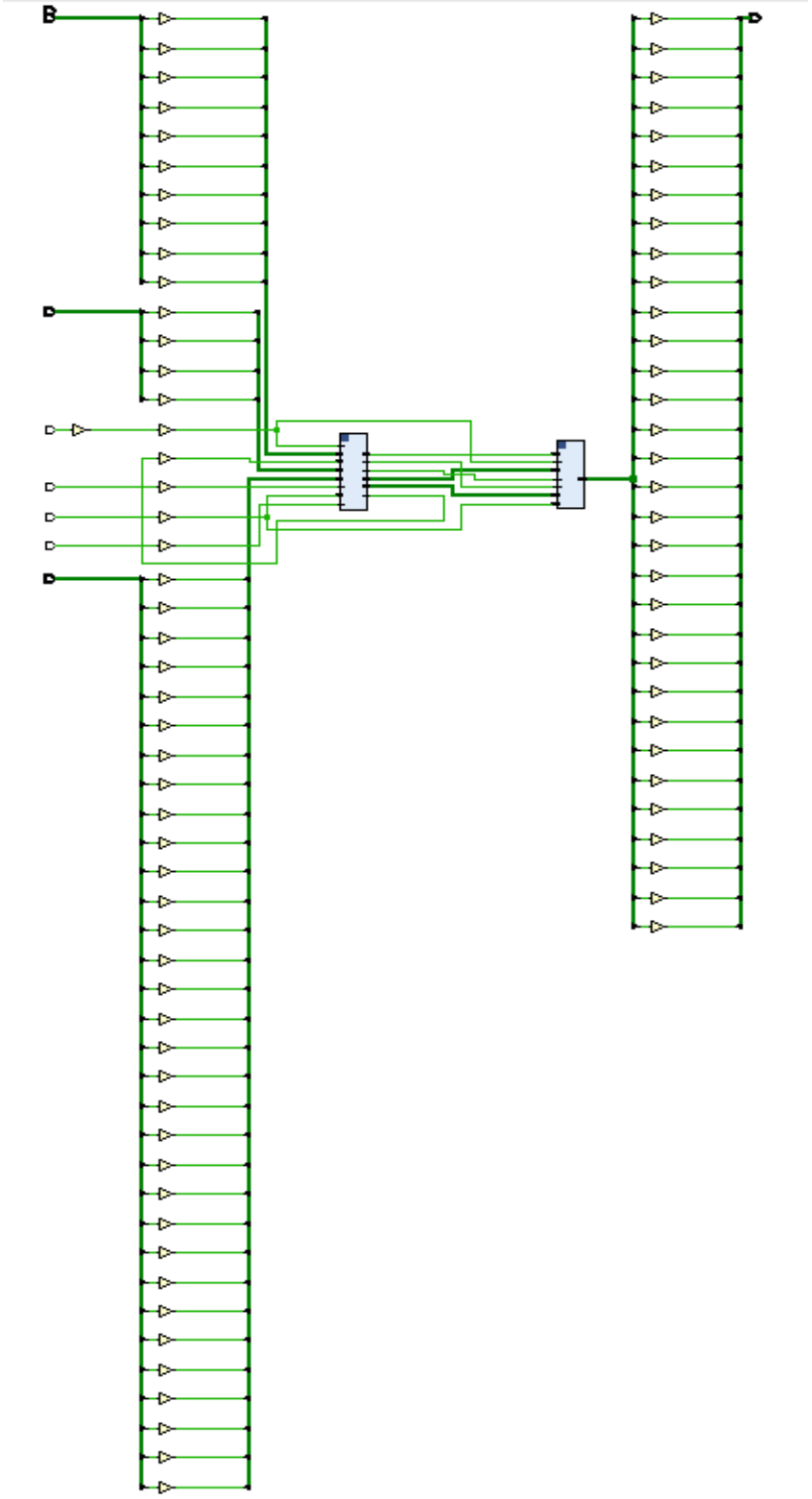
State	New Encoding	Previous Encoding
IDLE	00	00
SETUP	01	01
ACCESS	10	10

- Timing Summary on 10 ns clock period:

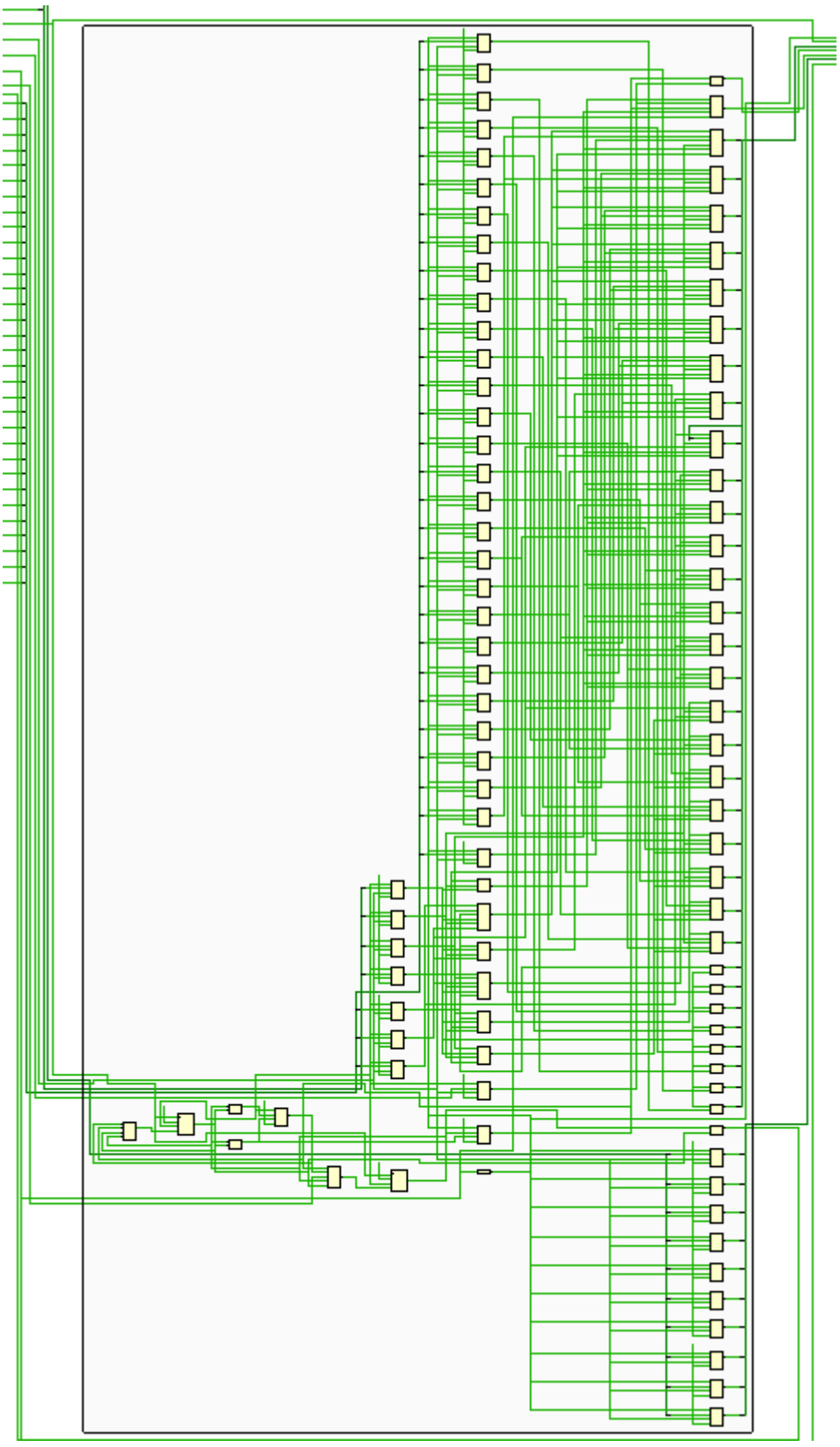
- Critical Path:



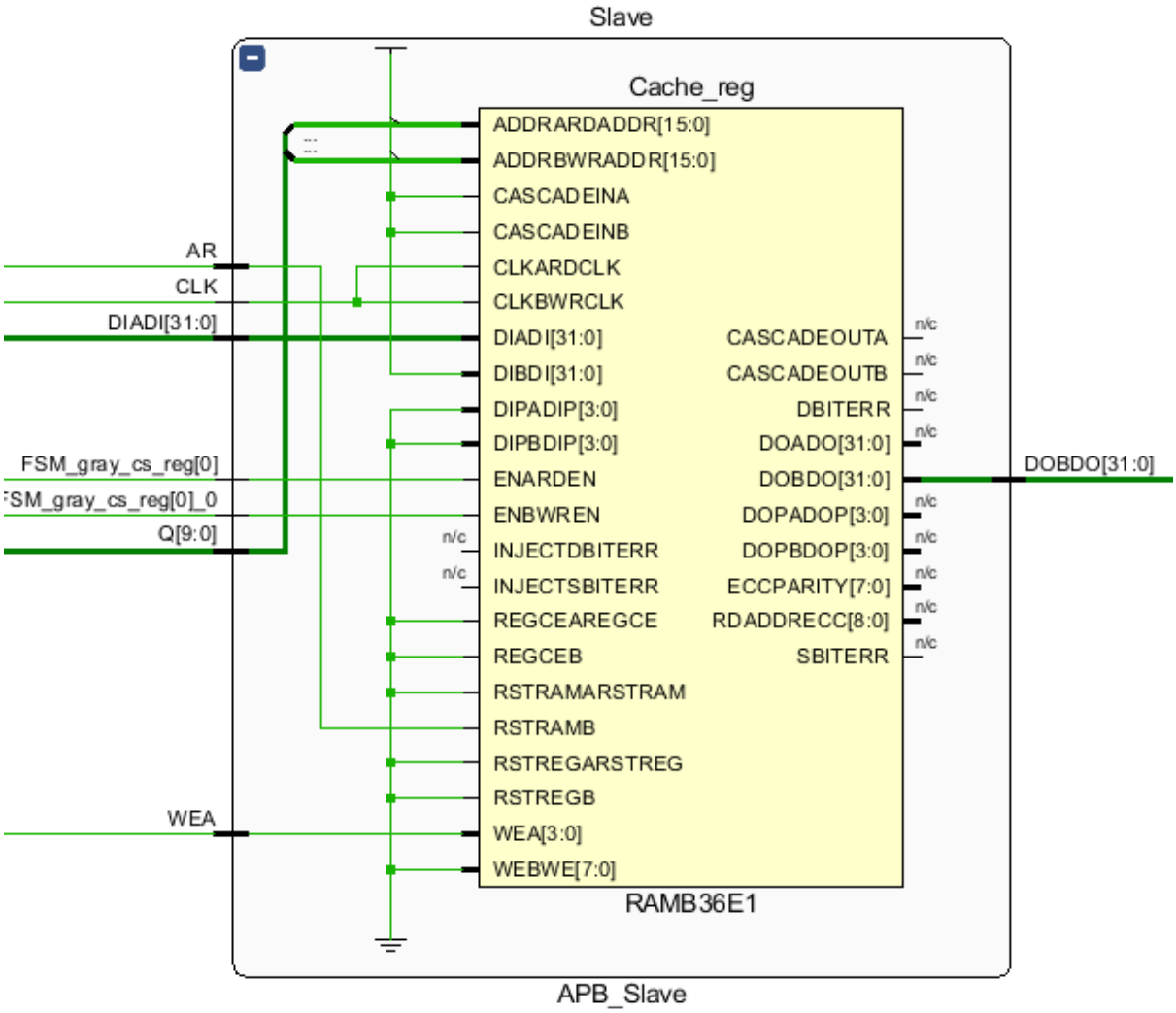
- **Gray:**
  - Schematic:
    - System:



- Master:



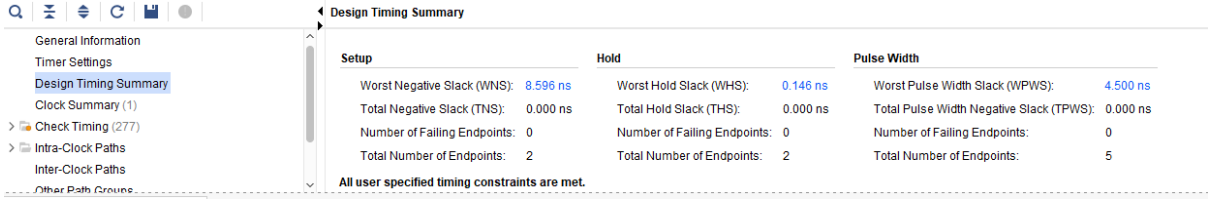
- Slave:



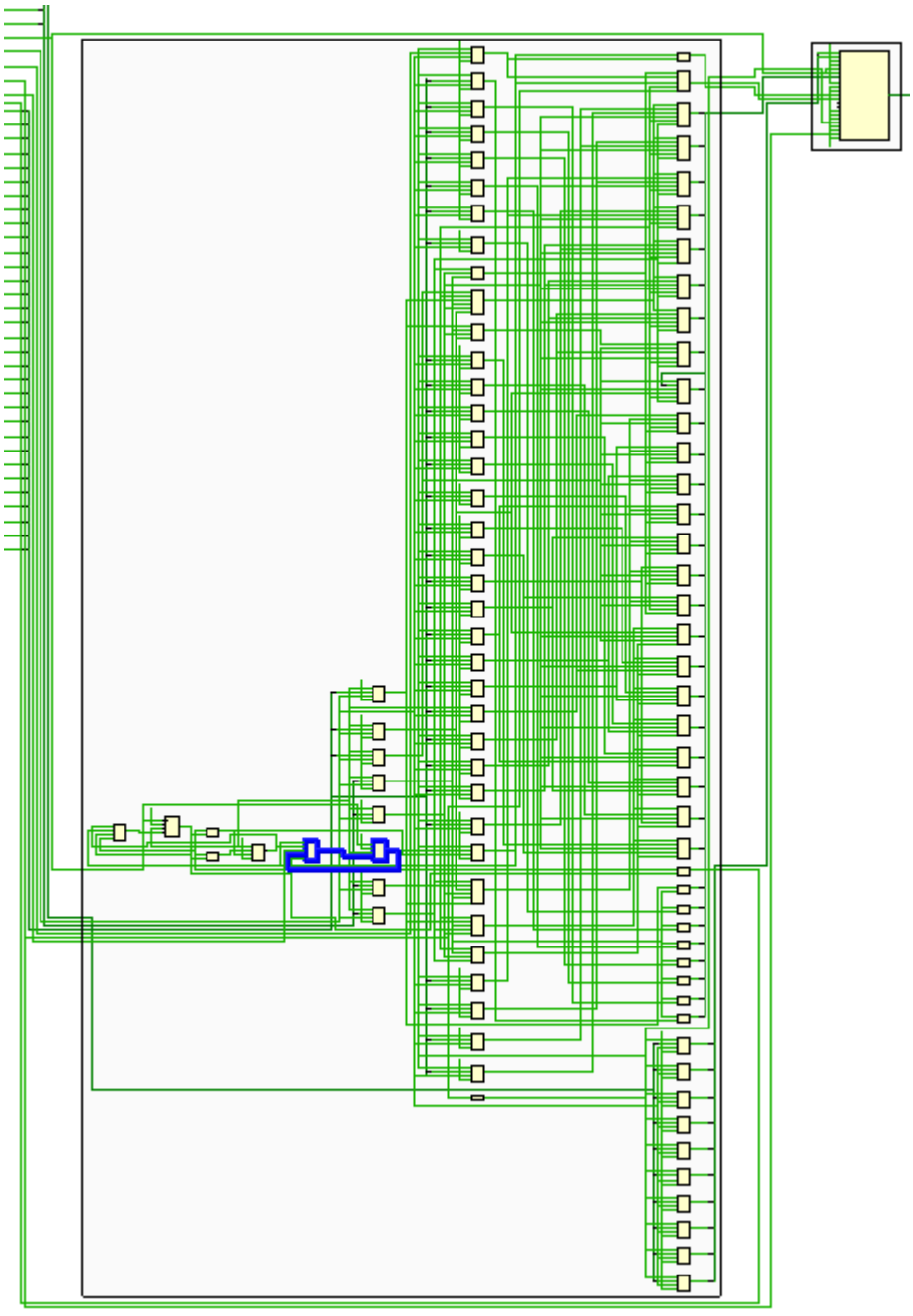
- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	00	00
SETUP	01	01
ACCESS	11	10

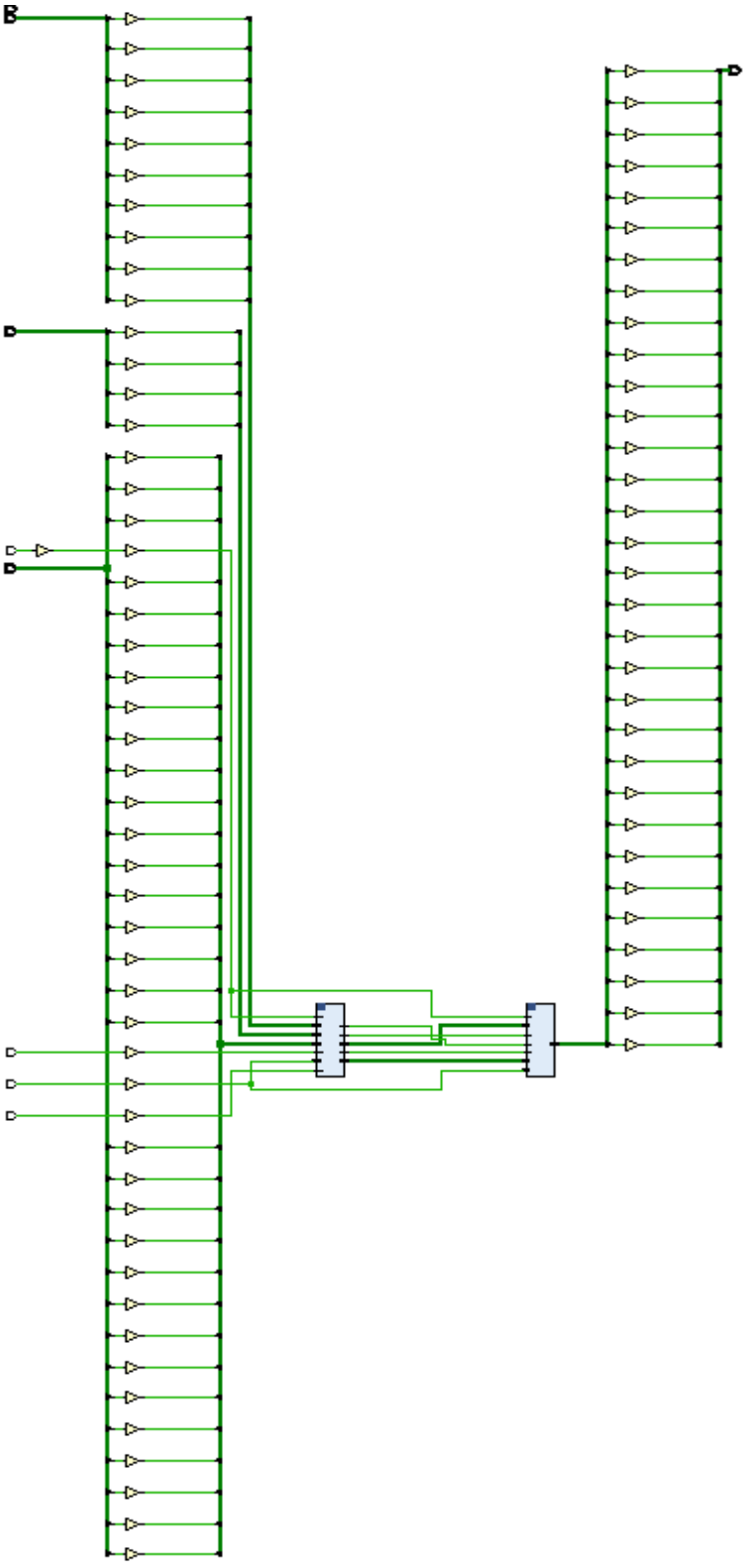
- Timing Summary on 10 ns clock period:



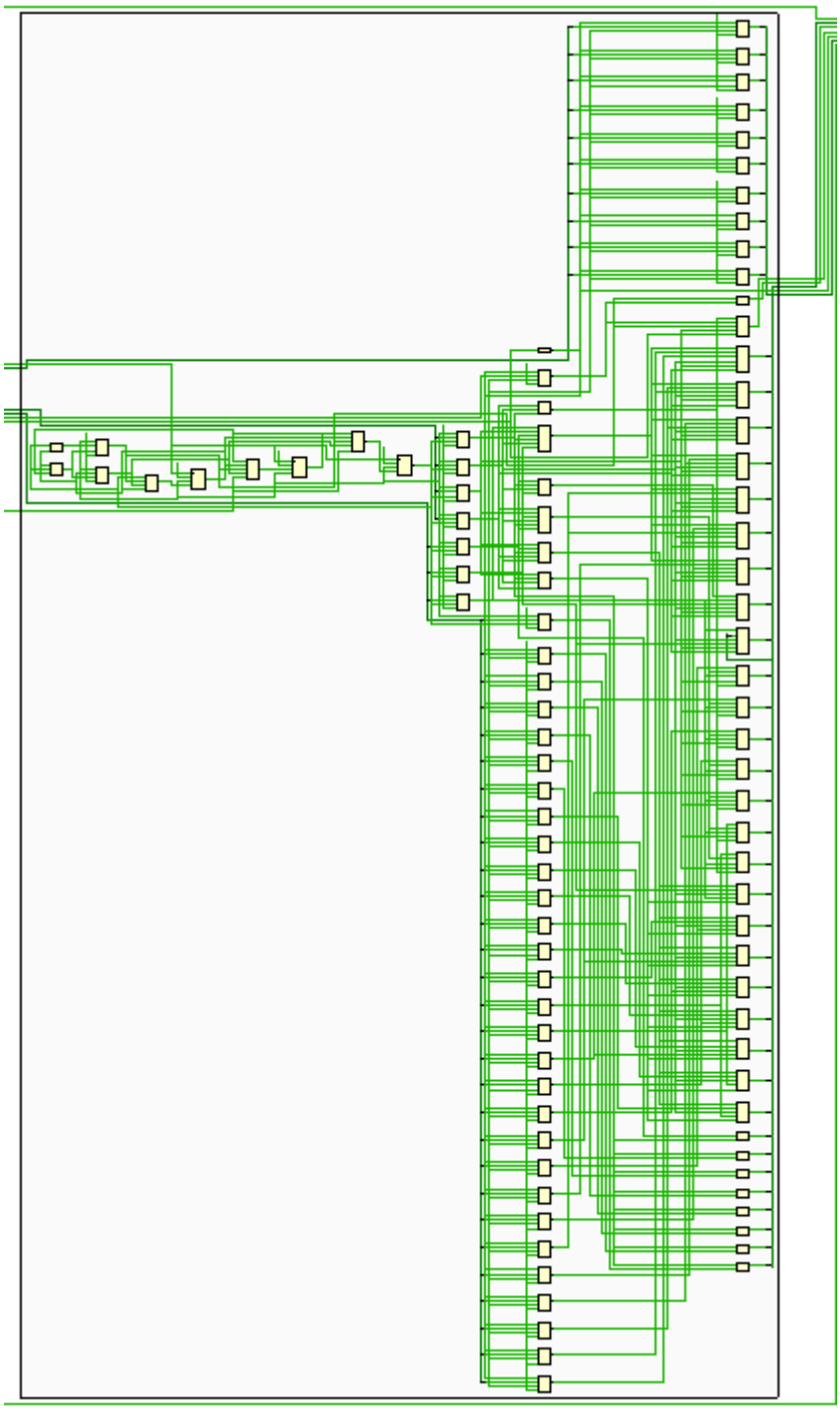
- Critical Path:



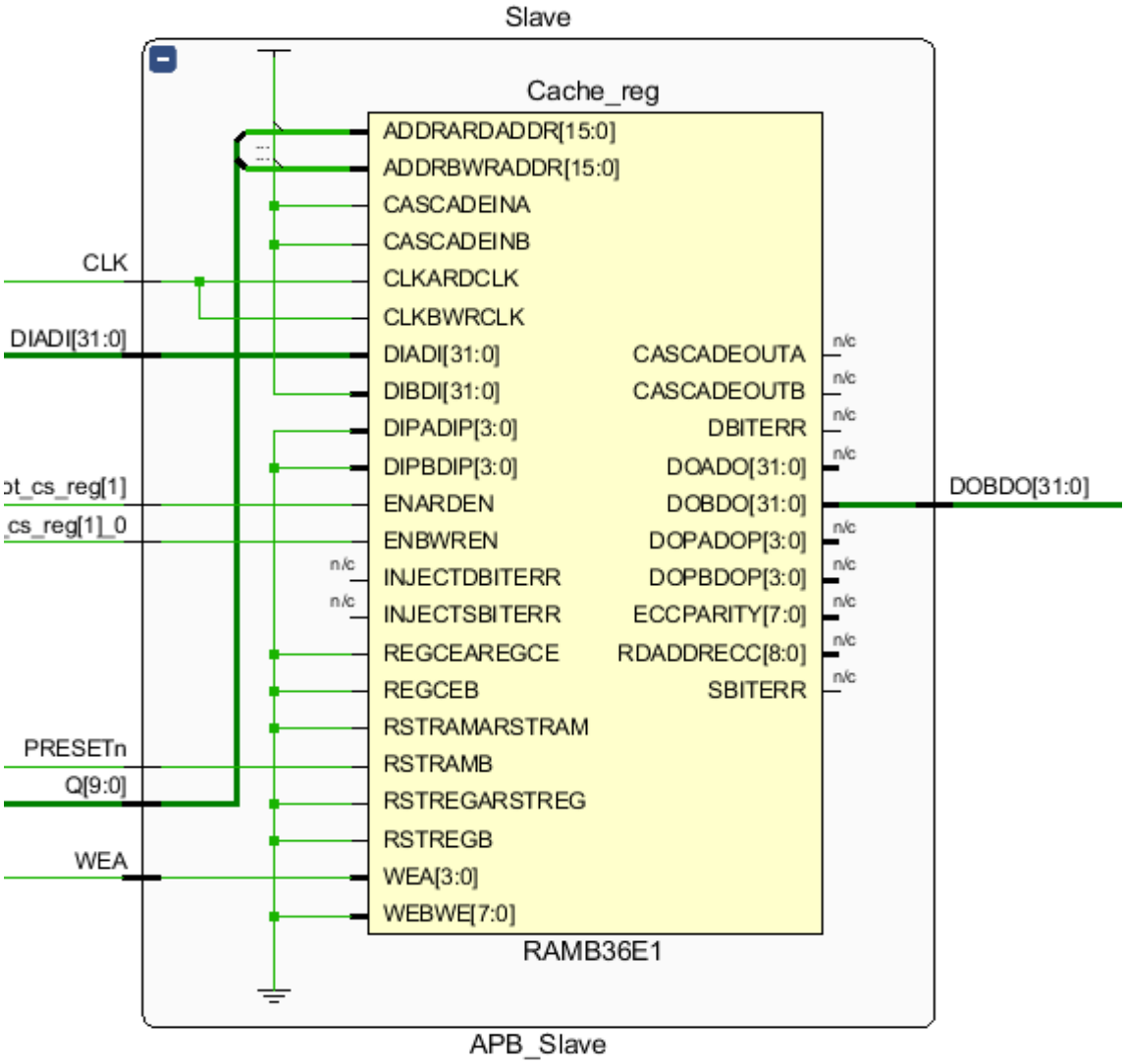
- **One_Hot:**
  - Schematic:
    - System:



- Master:



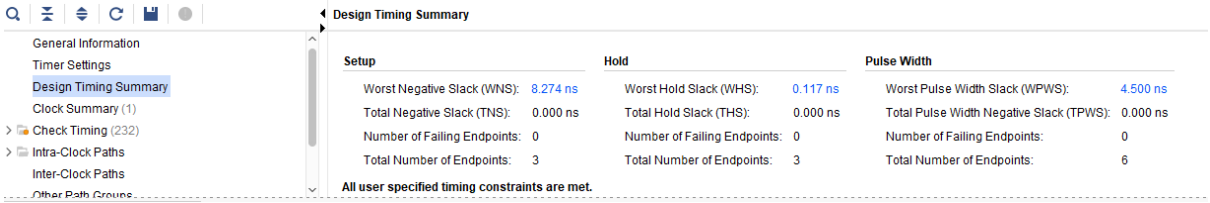
- Slave:



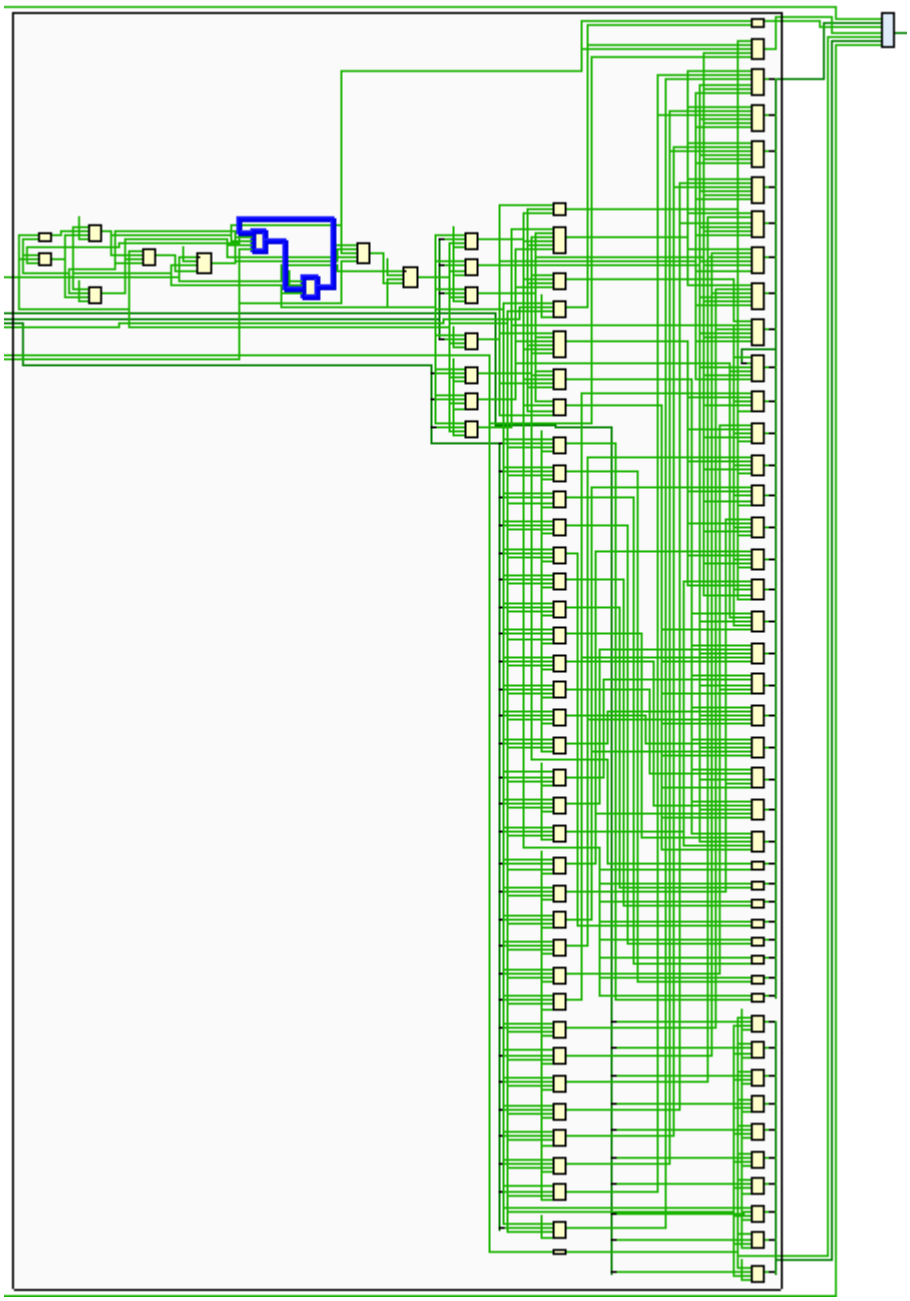
- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	001	00
SETUP	010	01
ACCESS	100	10

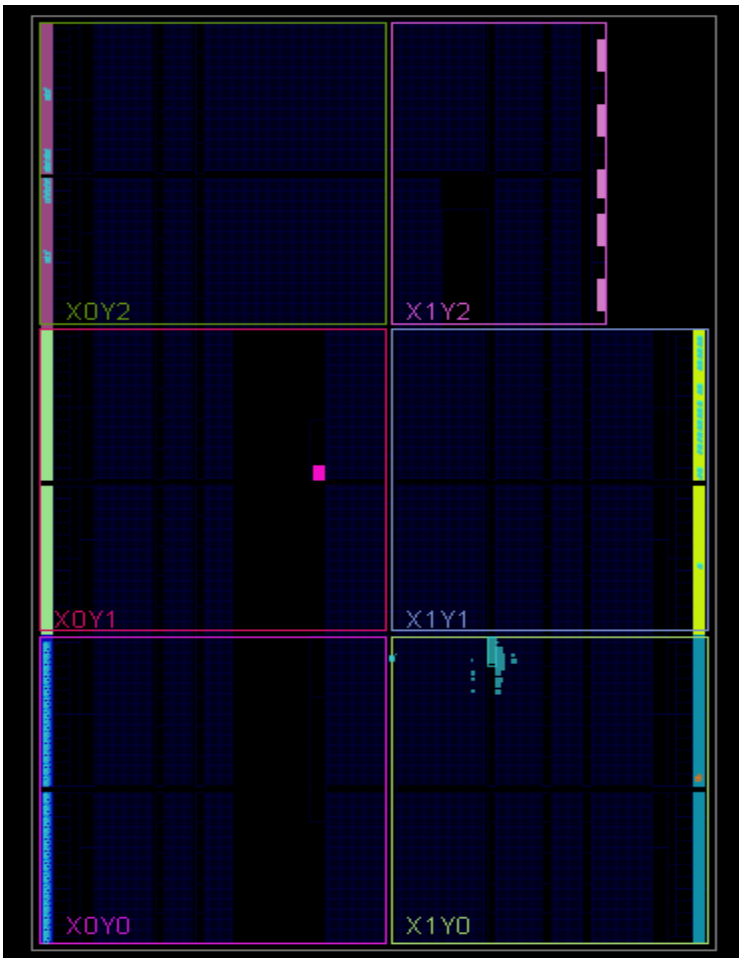
- Timing Summary on 10 ns clock period:



- Critical Path:



- # Implementation:
  - ## Seq:
    - ### Schematic:

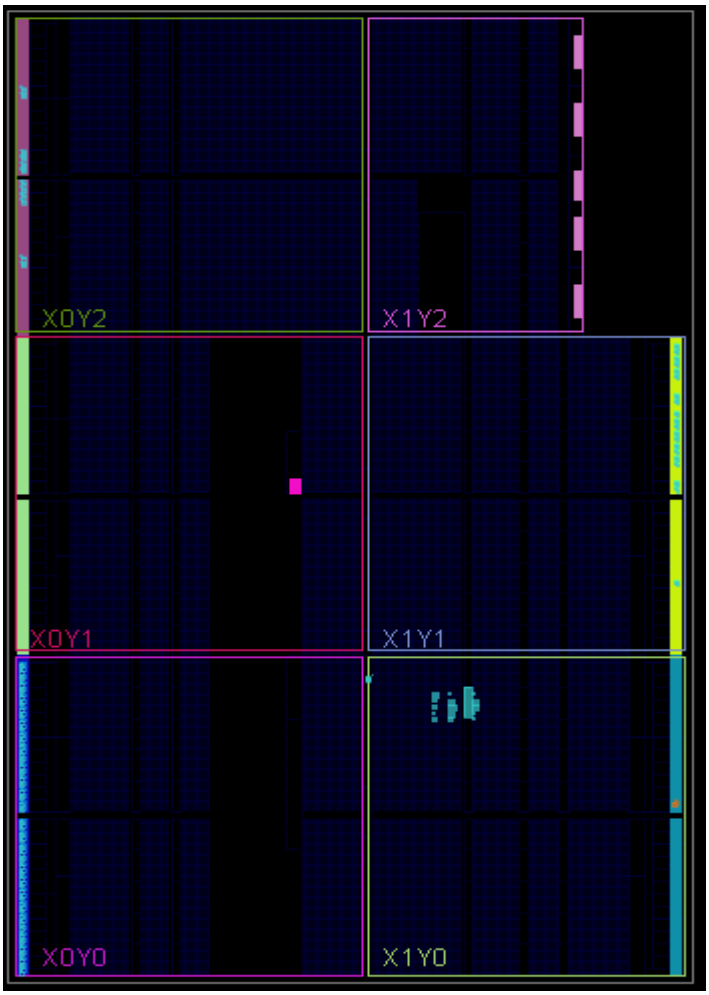


    - ### Timing on 10 ns clock period:

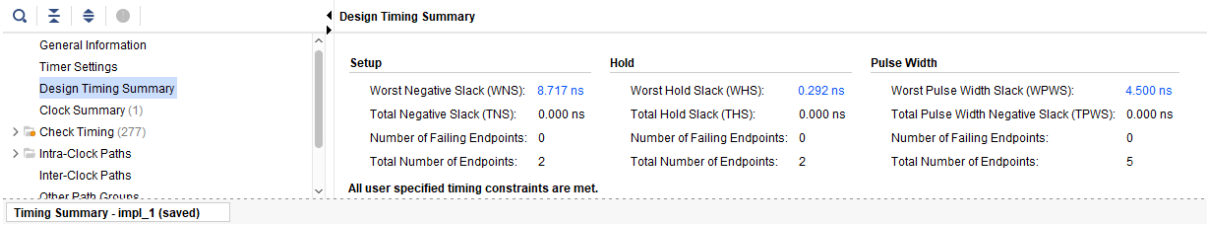
    - ### Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N APB_Wrapper	44	51	22	44	4	1	82	2
Master (APB_Master)	44	51	22	44	4	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0

- **Gray:**
  - Schematic:



  - Timing on 10 ns clock period:



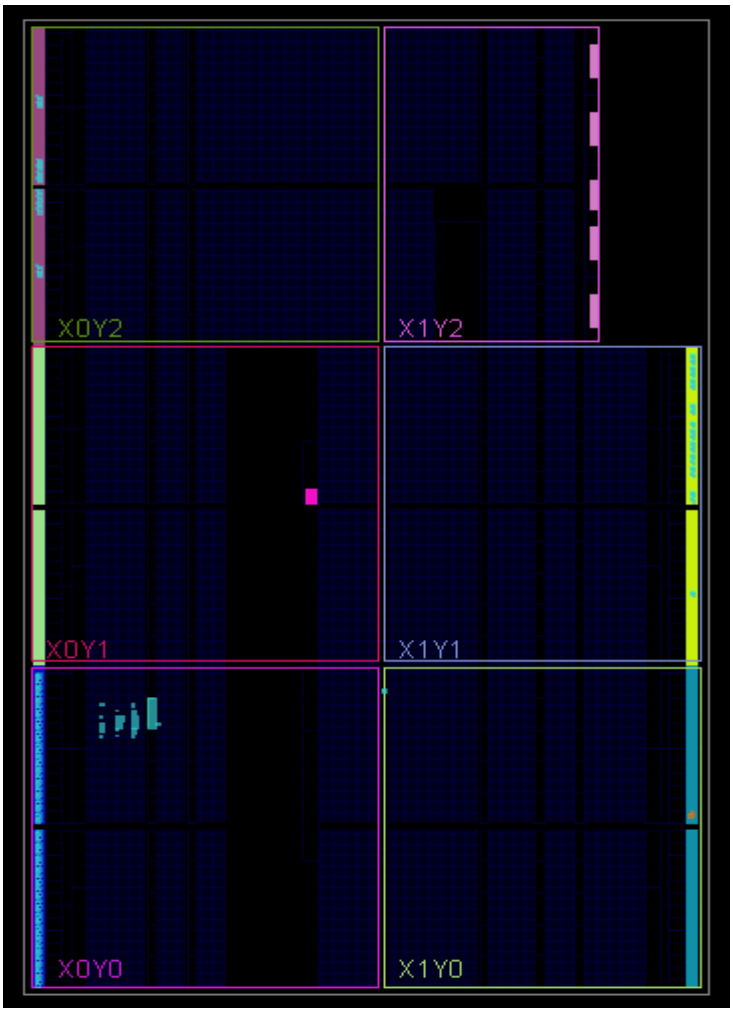
  - Utilization:

Hierarchy

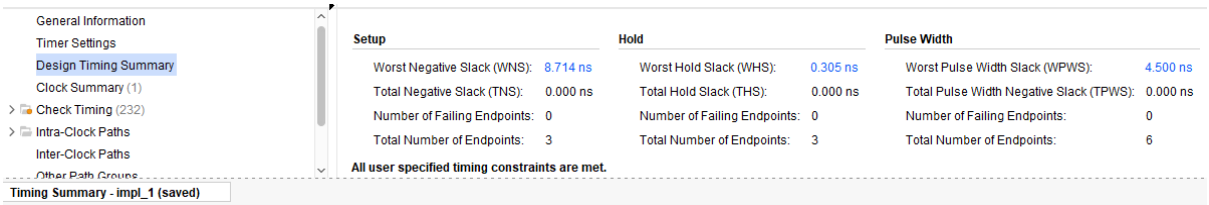
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N APB_Wrapper	42	51	26	42	2	1	82	2
Master (APB_Master)	42	51	26	42	2	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0

One_Hot:

Schematic:



Timing on 10 ns clock period:



Utilization:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
APB_Wrapper	44	52	26	44	3	1	82	1
Master (APB_Master)	44	52	26	44	3	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0

From results we found that the best encoding is seq.