

# AMBA APB Vivado Report

**Created By:**

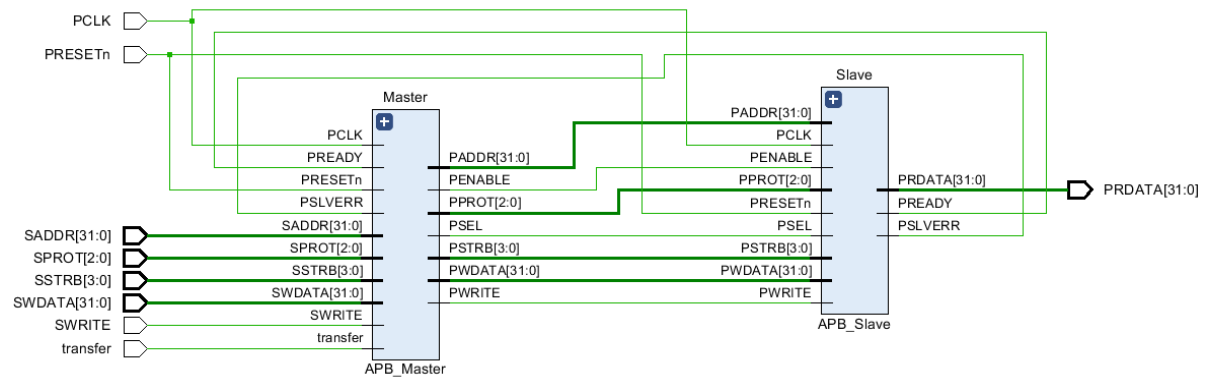
**Mohamed Ahmed Mohamed Hussein**

**25/8/2024**

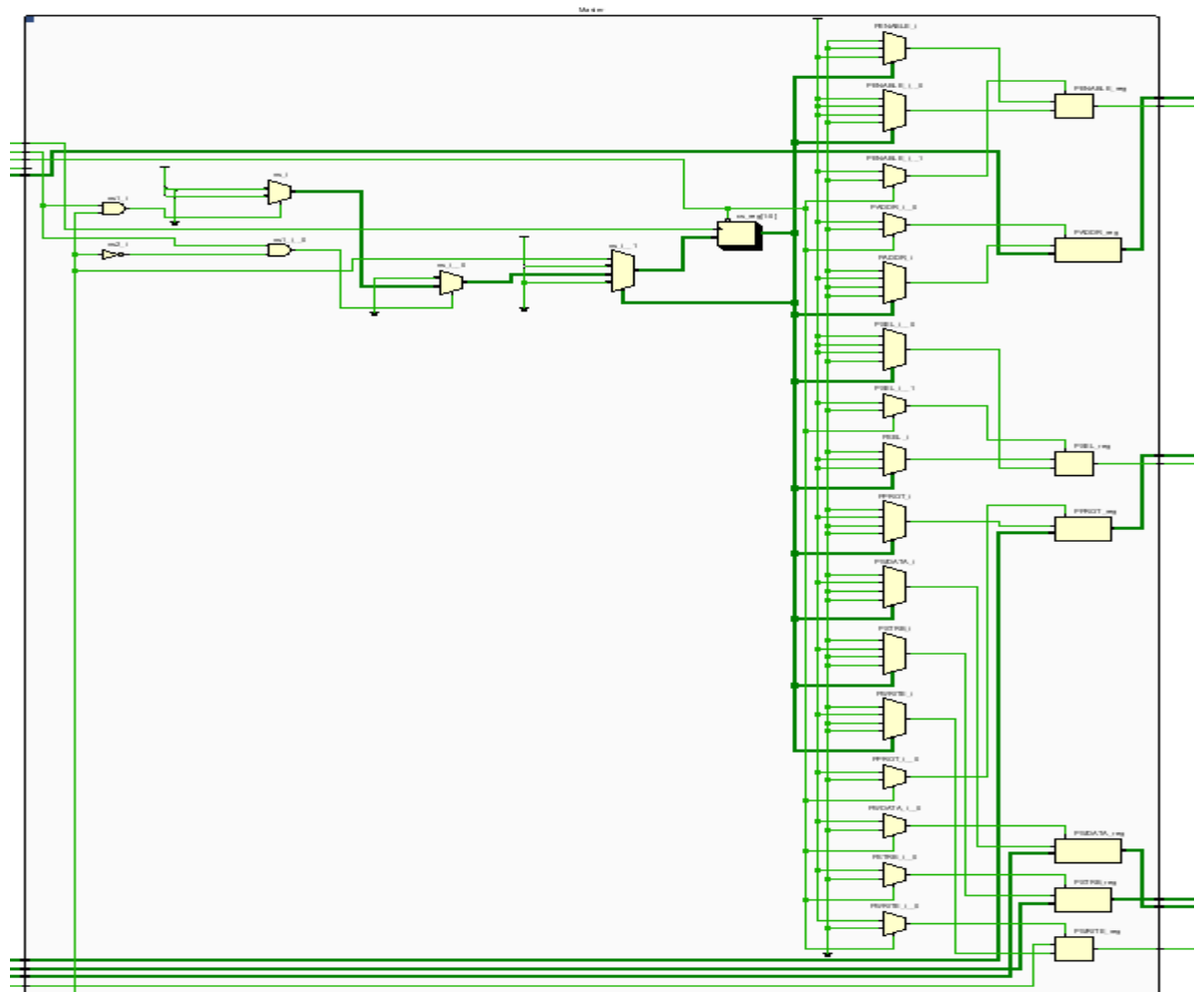
# Vivado:

- Elaboration:

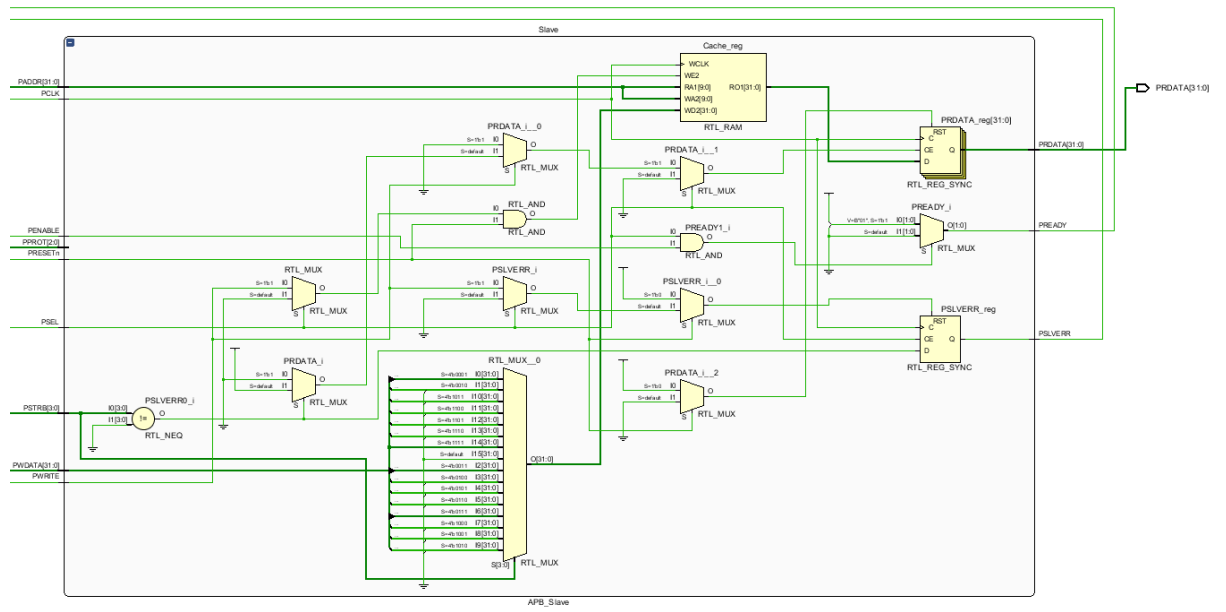
- System:



- Master:



## ■ Slave:

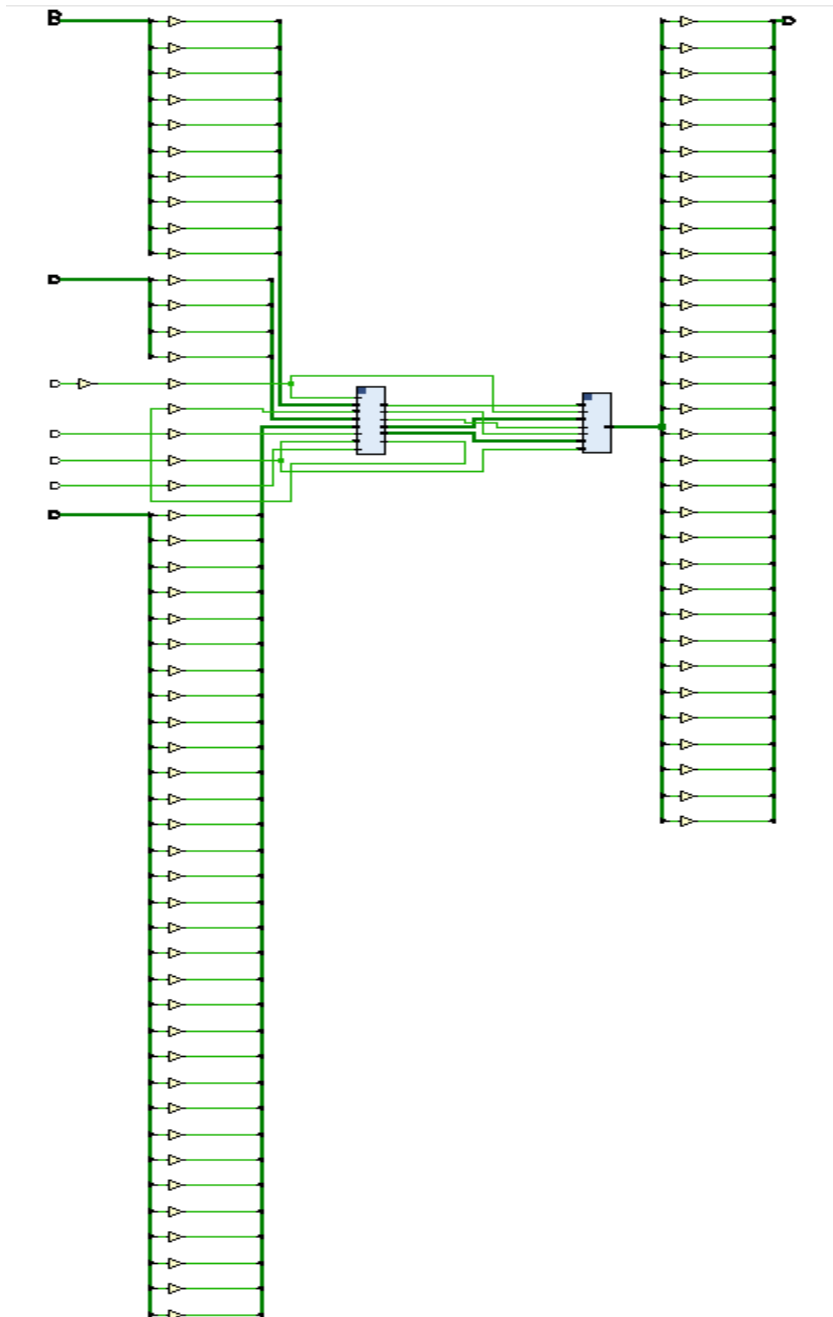


- **Synthesis:**

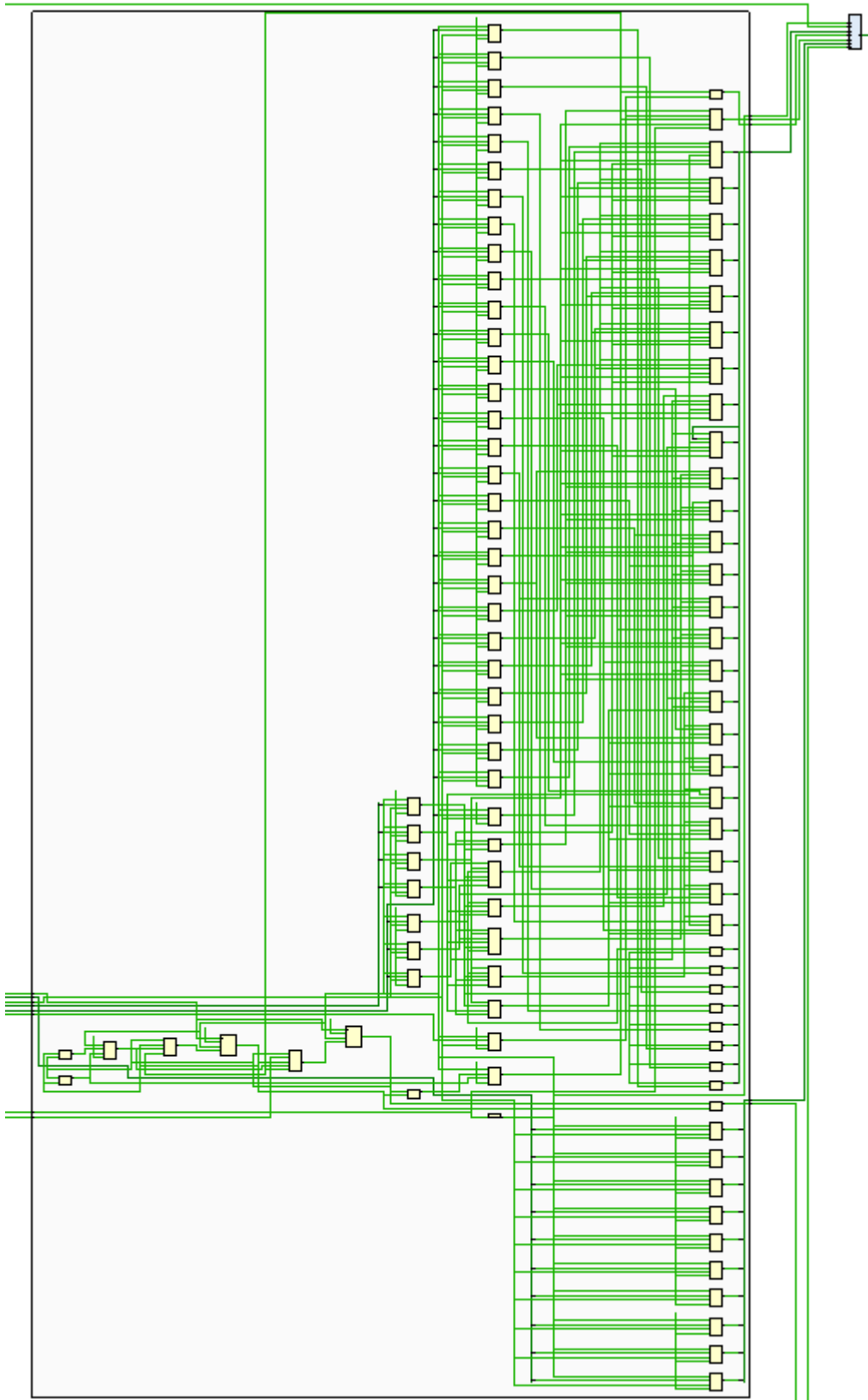
- **Seq:**

- Schematic:

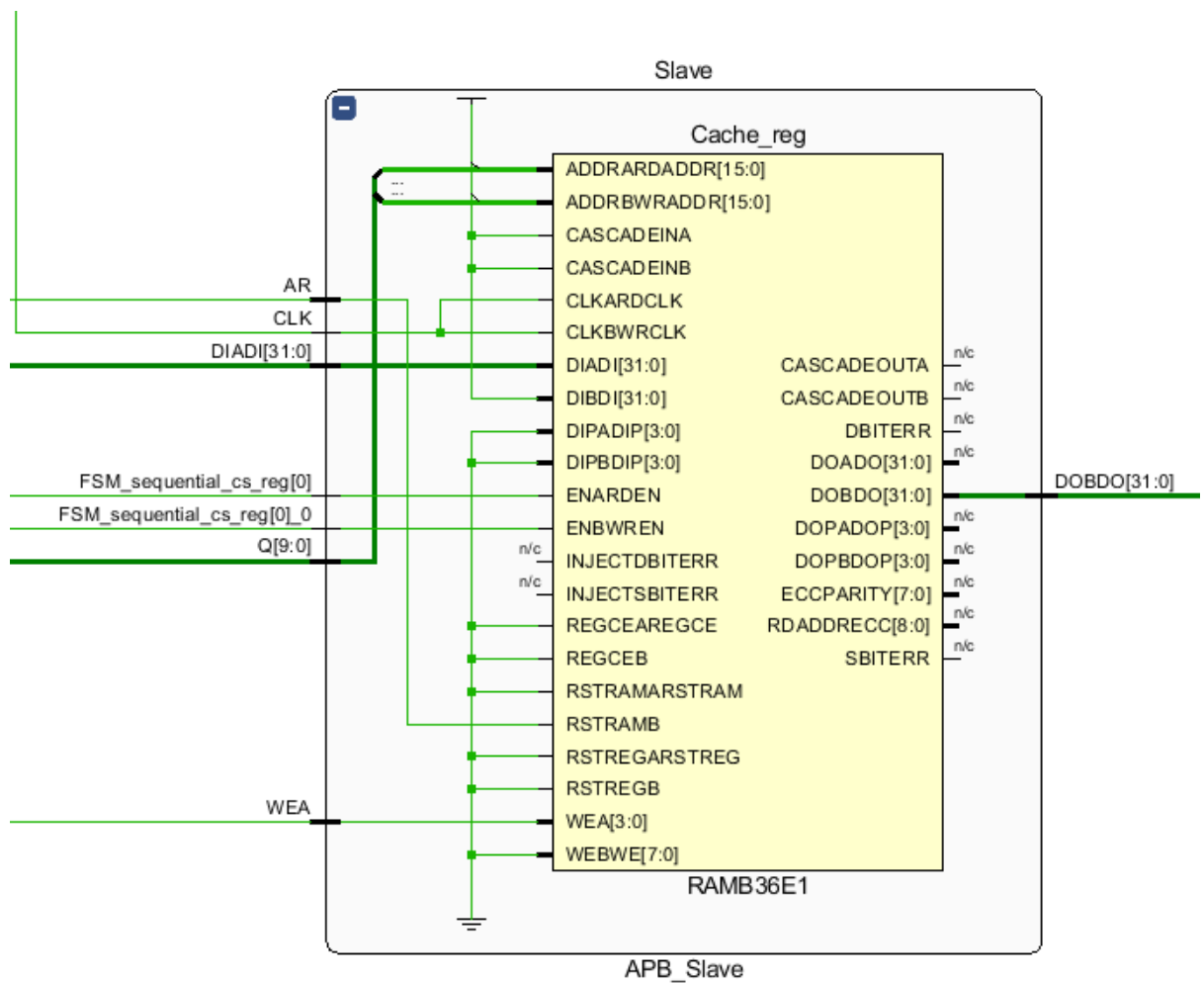
- System:



- Master:



- Slave:



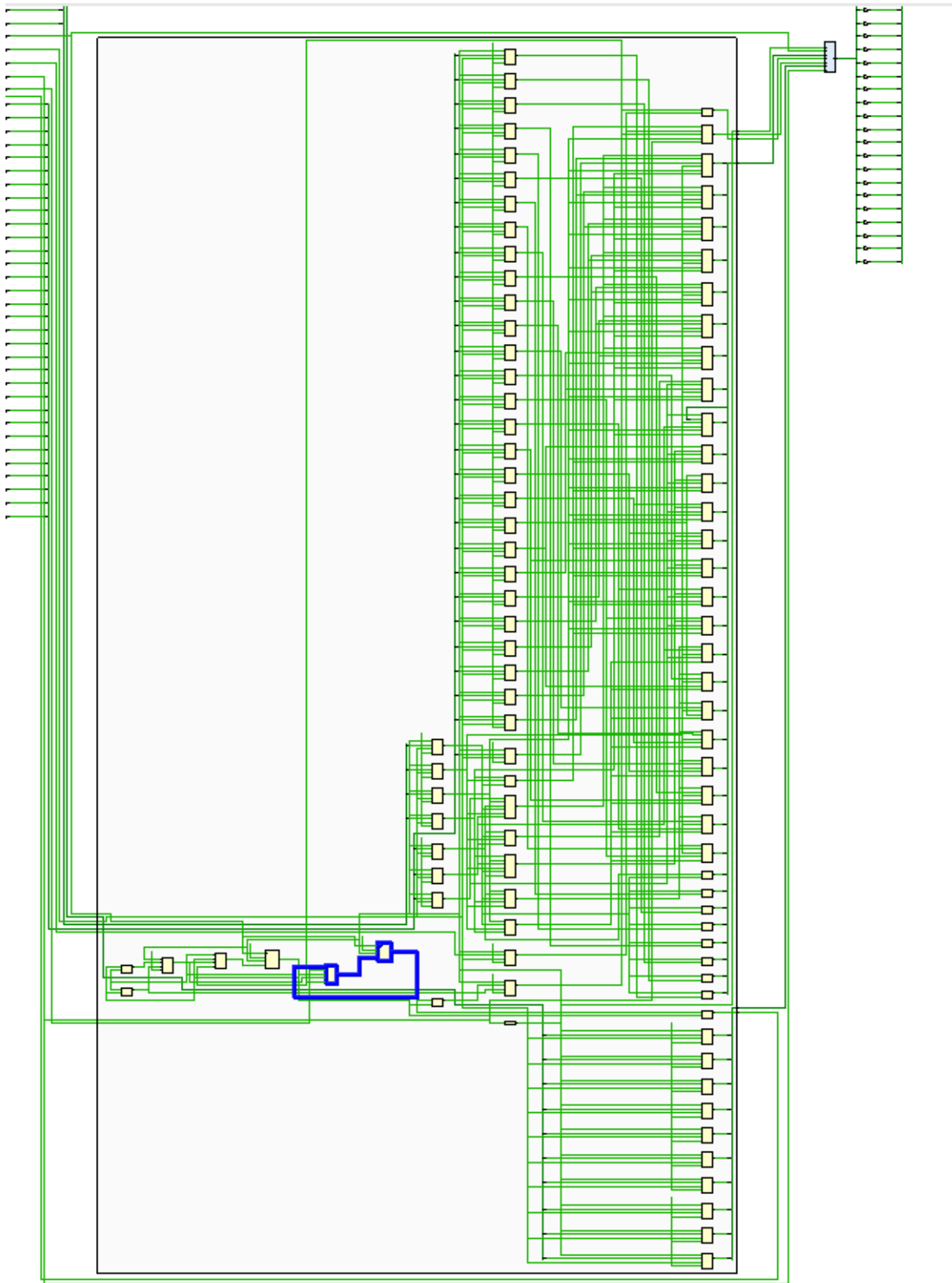
- Encoding Report:

State	New Encoding	Previous Encoding
IDLE	00	00
SETUP	01	01
ACCESS	10	10

- Timing Summary on 10 ns clock period:

General Information			
Timer Settings			
<b>Design Timing Summary</b>			
Clock Summary (1)			
➤ Check Timing (277)			
➤ Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
Timing Summary - timing_seq			

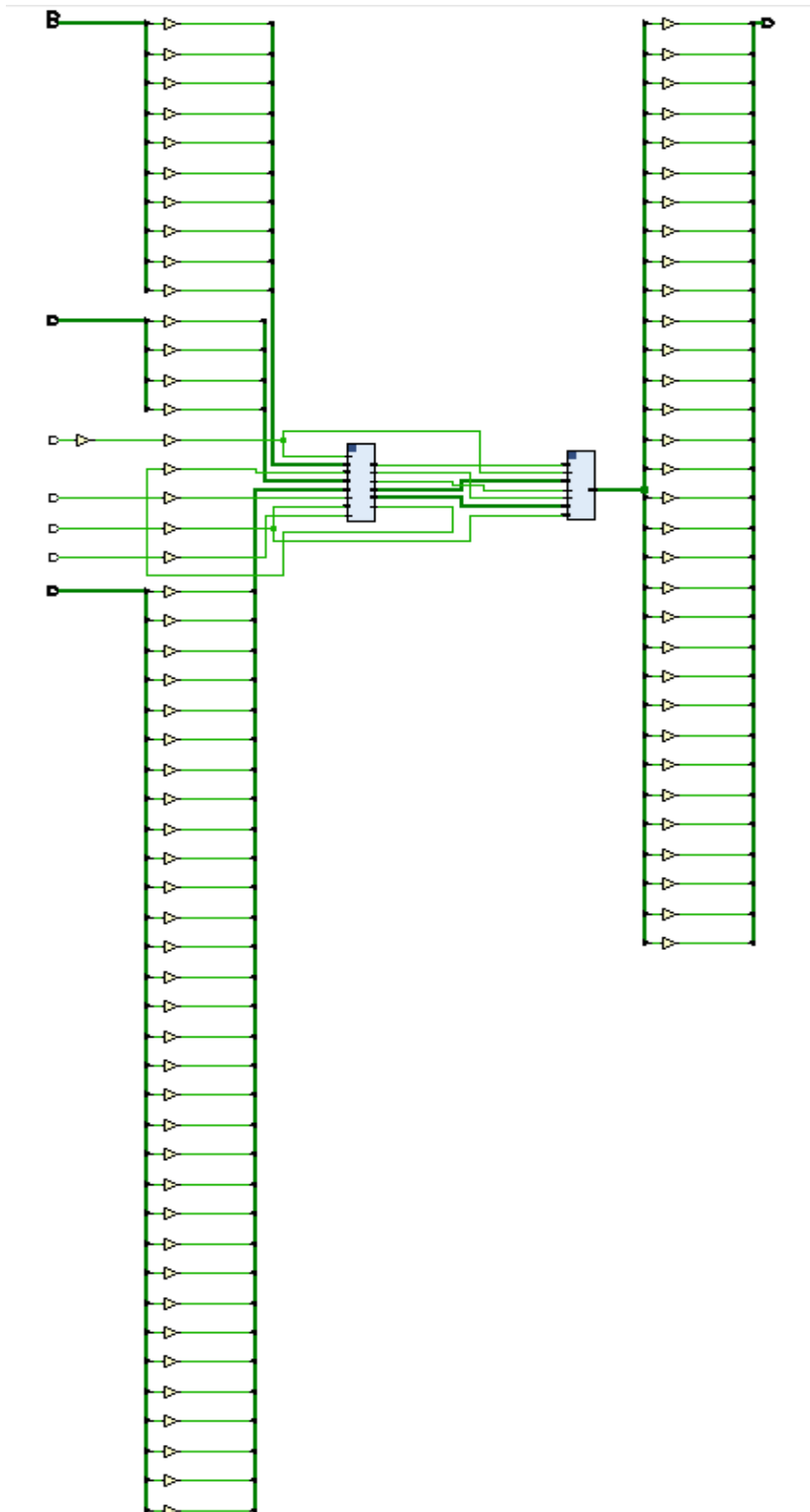
■ Critical Path:



- **Gray:**

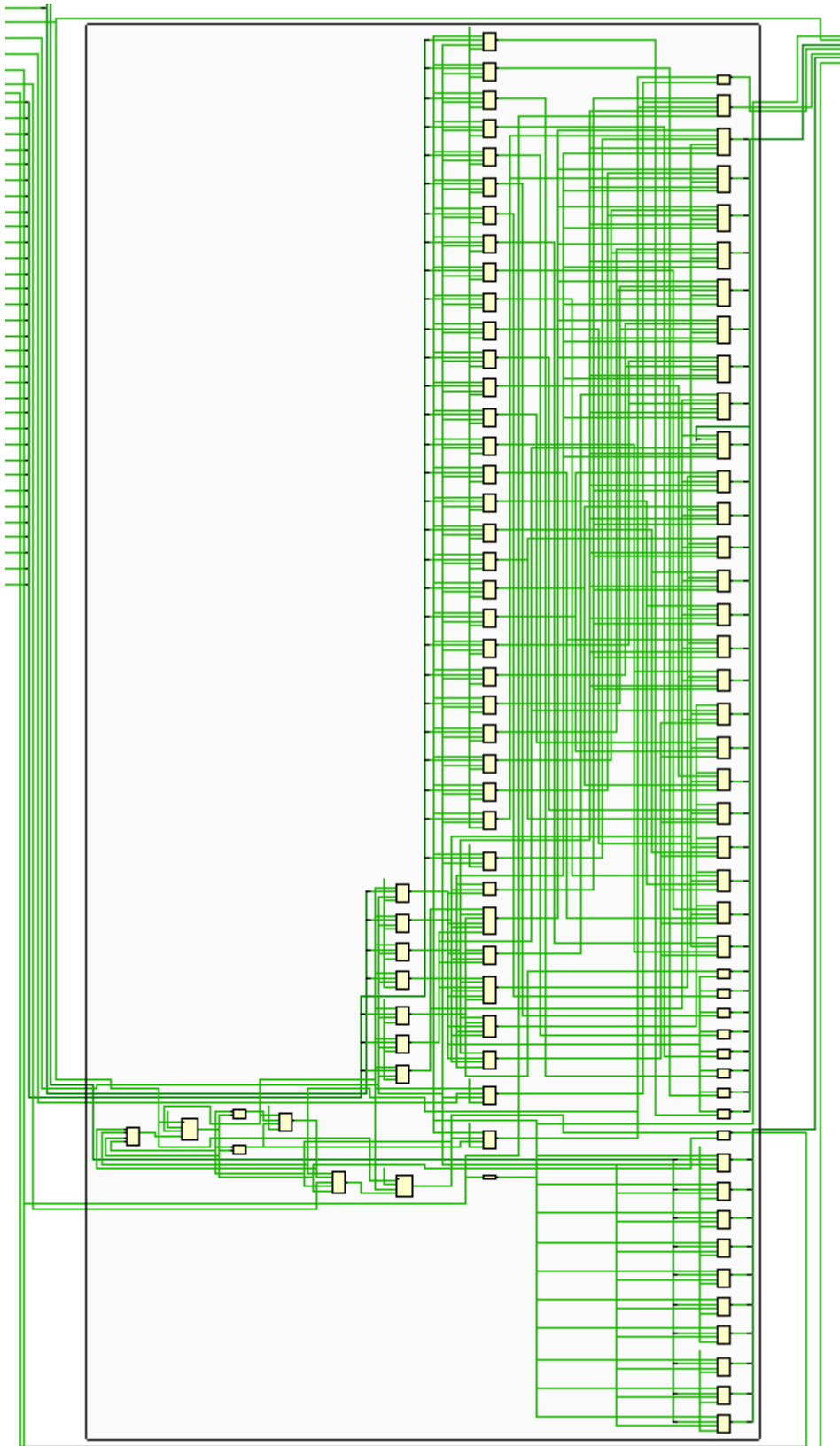
- Schematic:

- System:

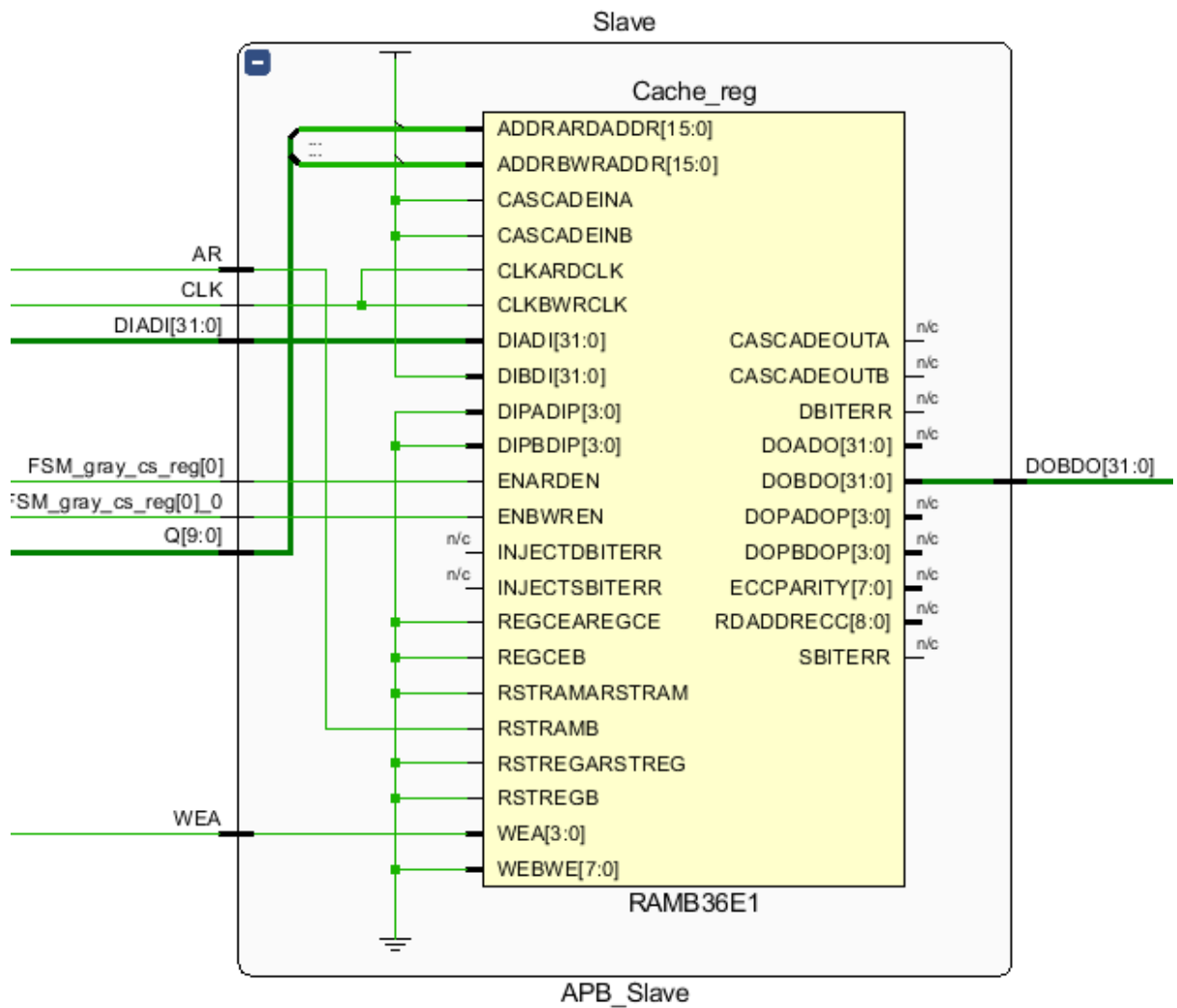




- Master:



• Slave:



■ Encoding Report:

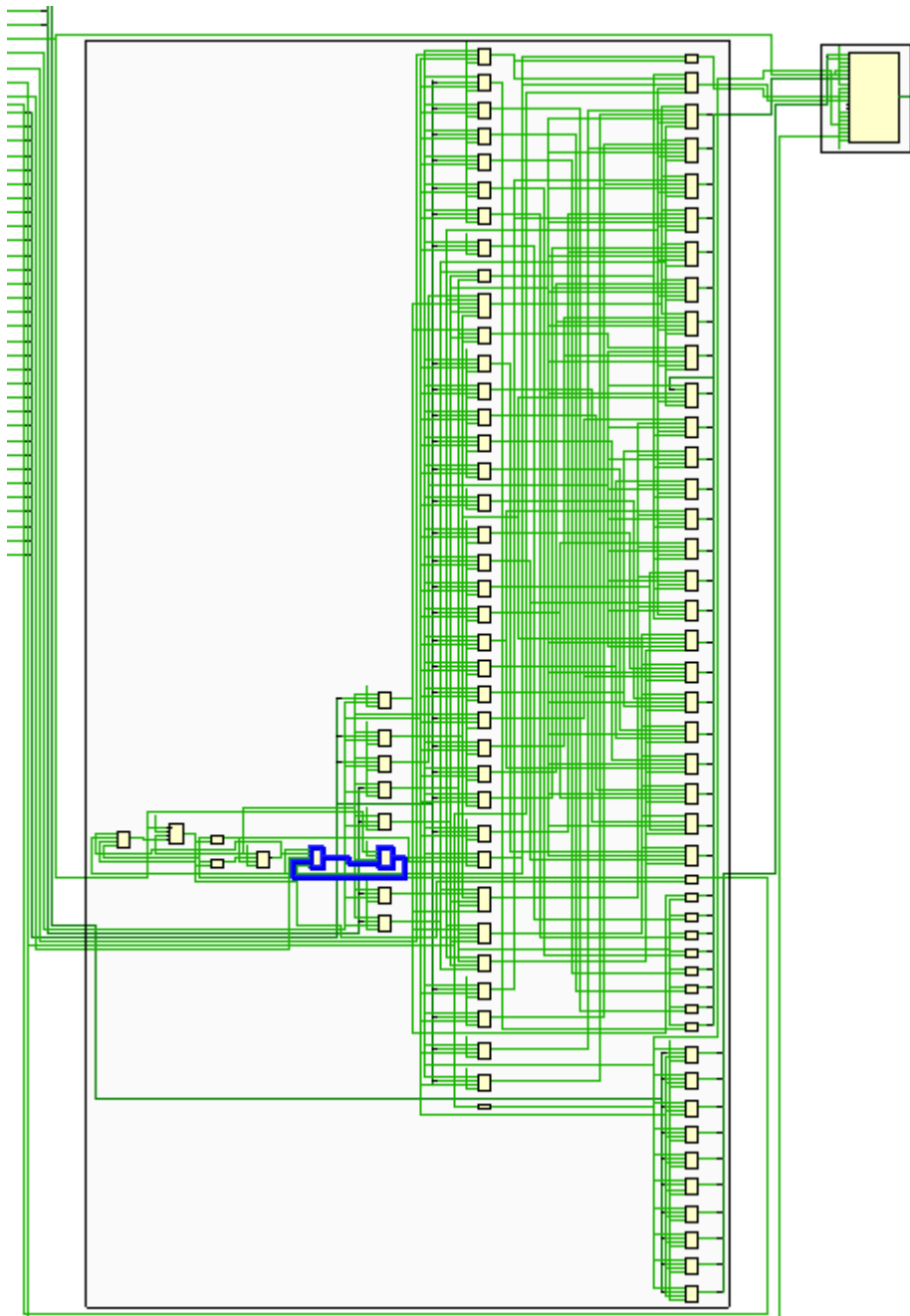
State	New Encoding	Previous Encoding
IDLE	00	00
SETUP	01	01
ACCESS	11	10

■ Timing Summary on 10 ns clock period:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.596 ns	Worst Hold Slack (WHS): 0.146 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 2	Total Number of Endpoints: 2	Total Number of Endpoints: 5

All user specified timing constraints are met.

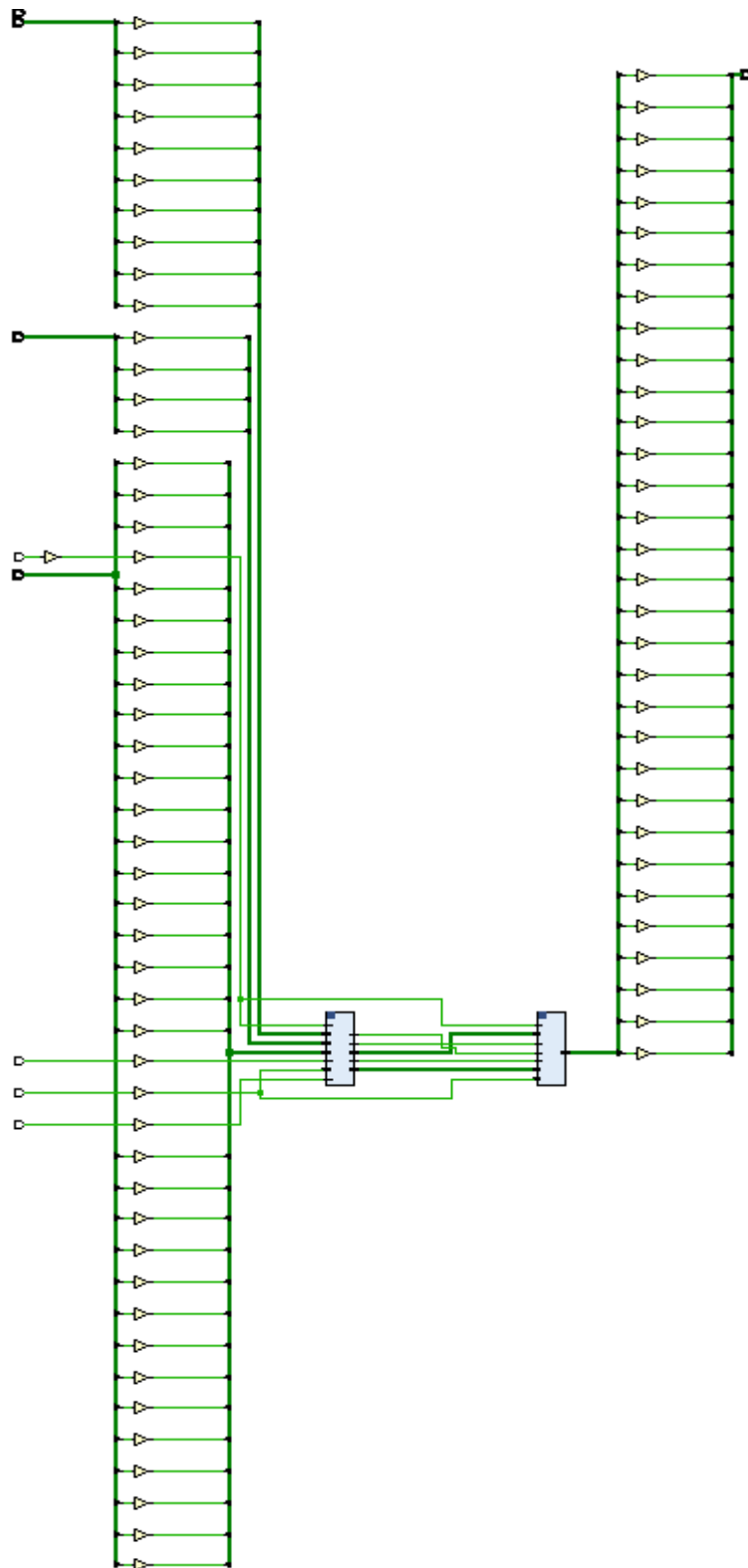
■ Critical Path:



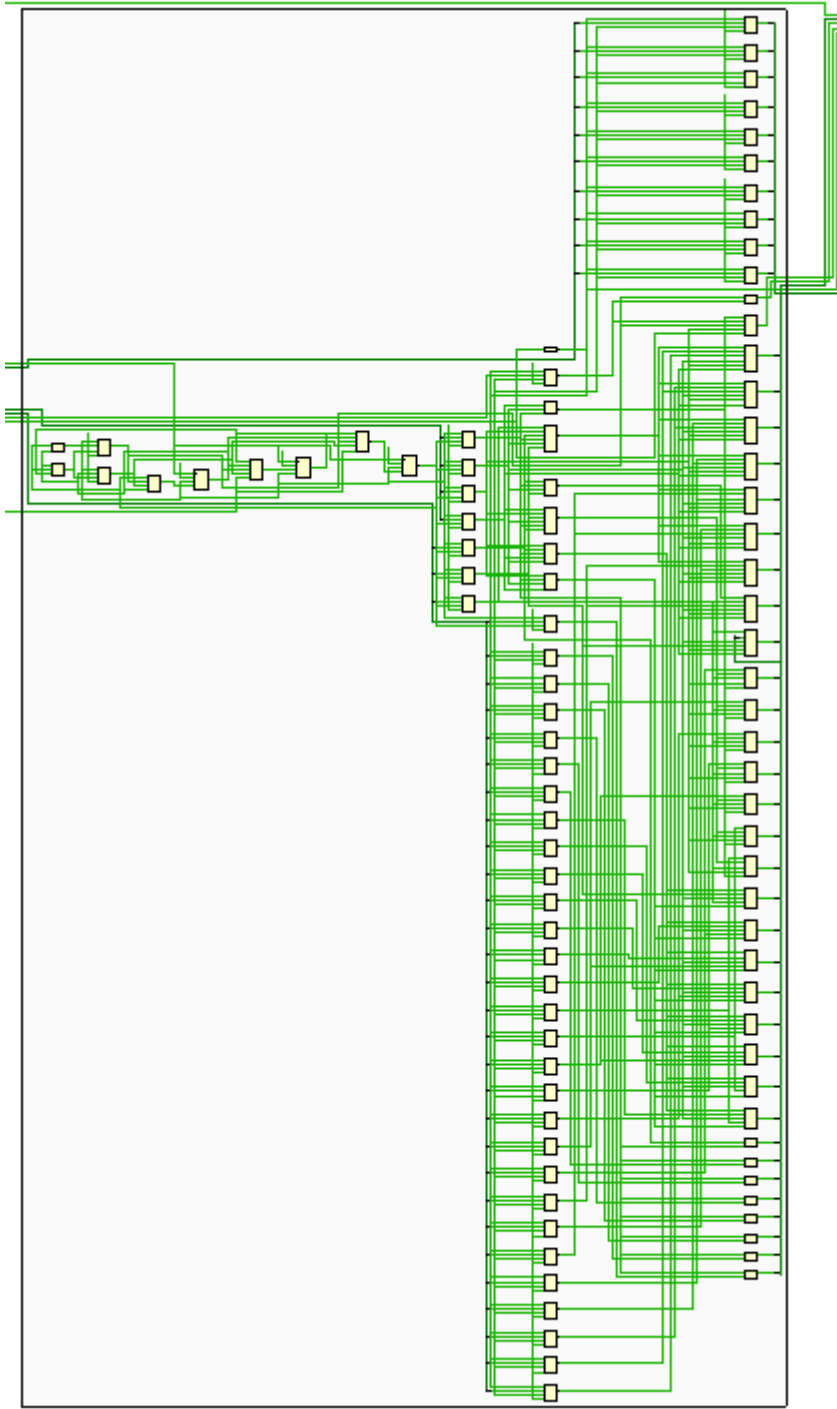
- **One\_Hot:**

- Schematic:

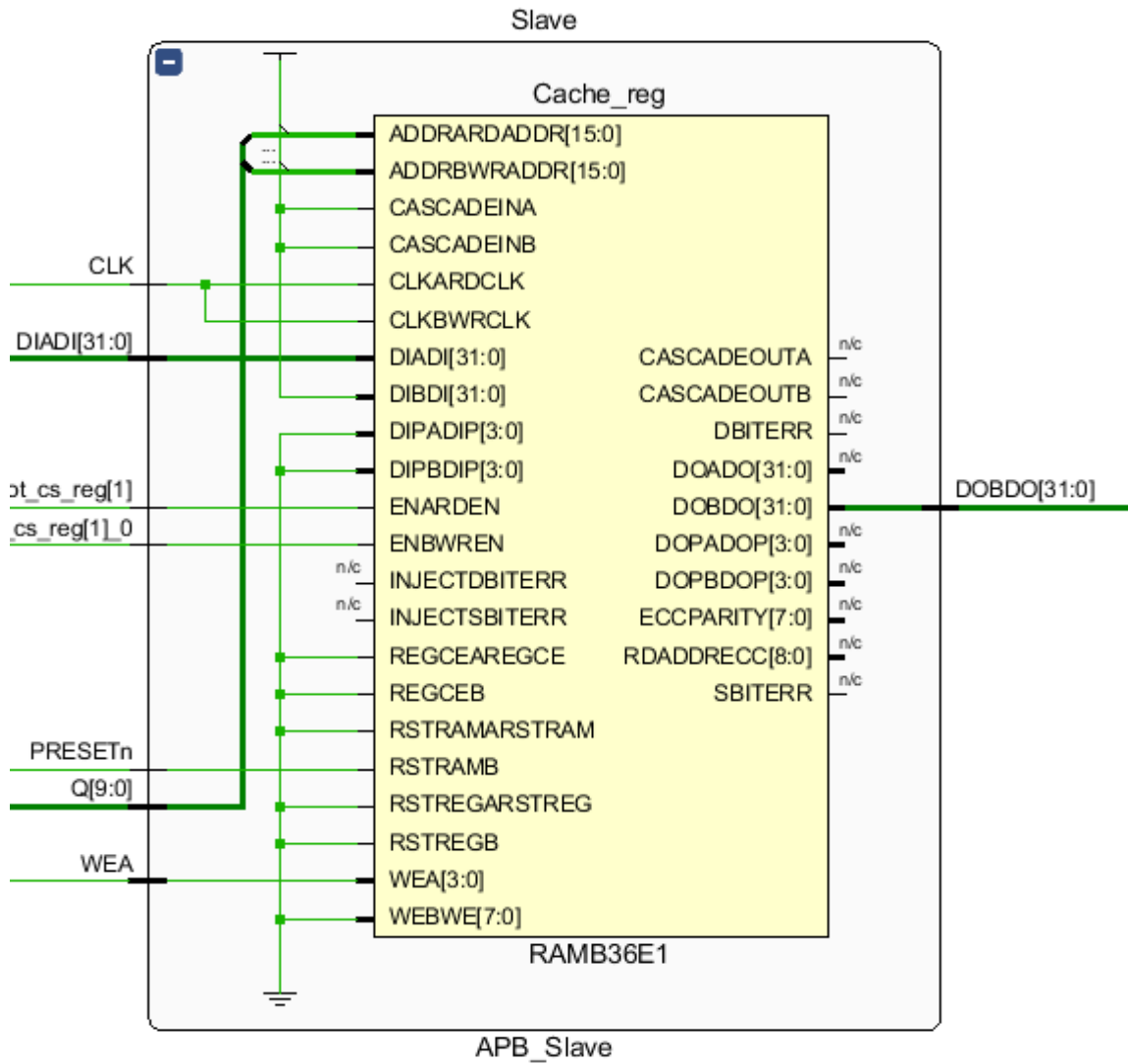
- System:



- Master:



- Slave:



- Encoding Report:

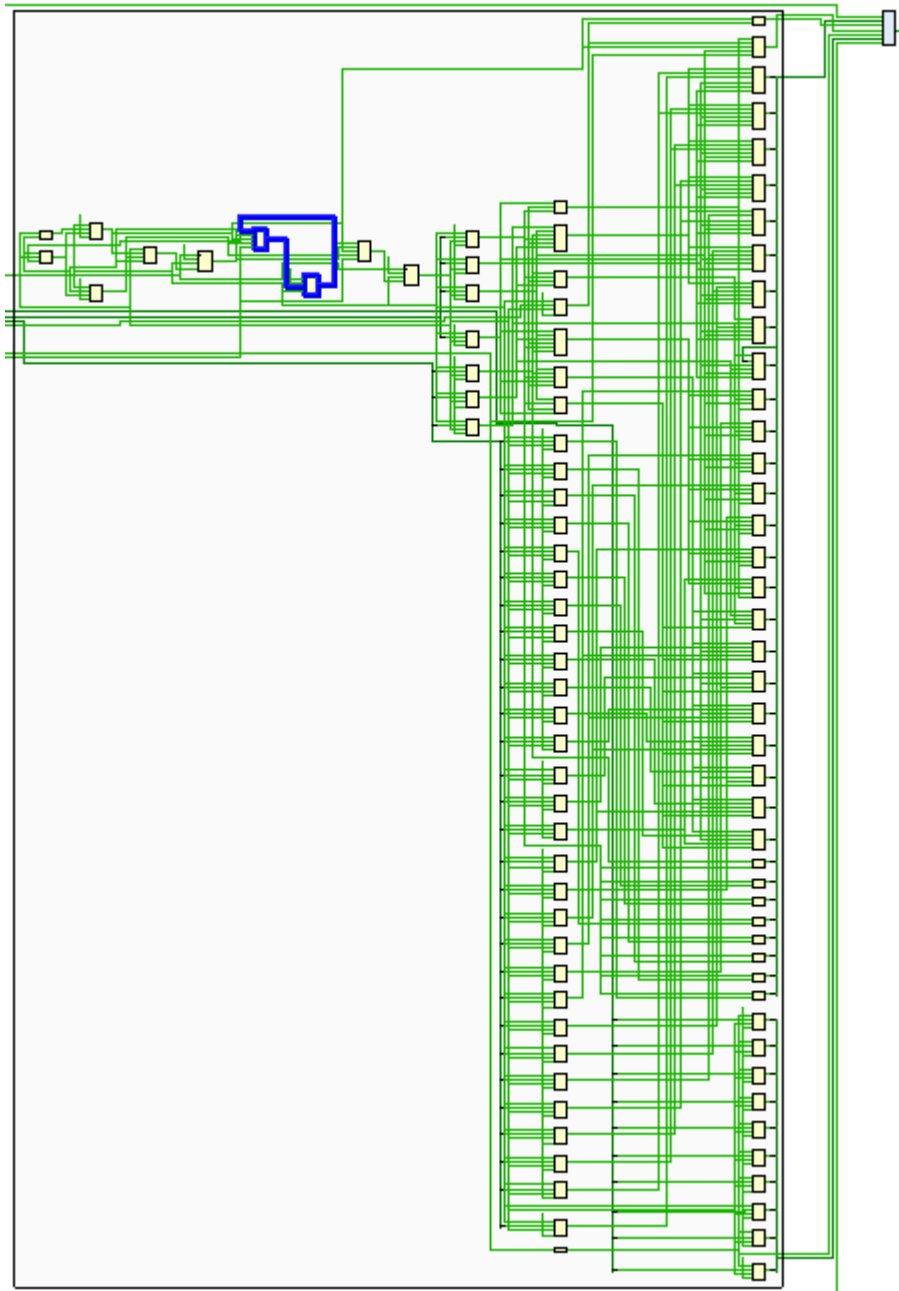
State	New Encoding	Previous Encoding
IDLE	001	00
SETUP	010	01
ACCESS	100	10

- Timing Summary on 10 ns clock period:

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 8.274 ns	Worst Hold Slack (WHS): 0.117 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 3	Total Number of Endpoints: 3	Total Number of Endpoints: 6

All user specified timing constraints are met.

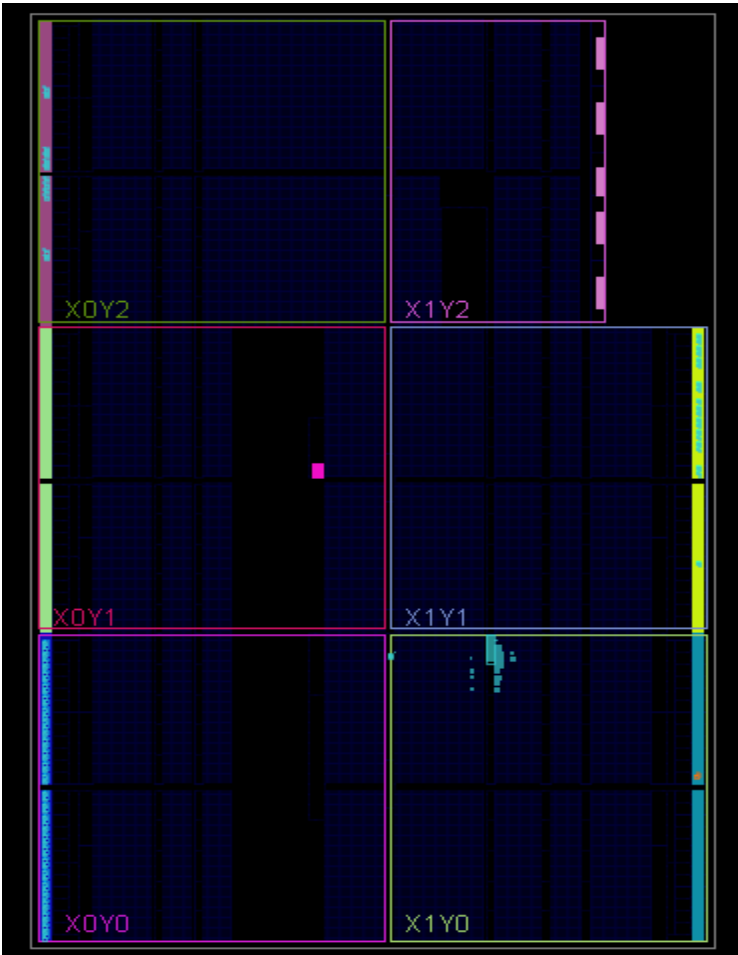
■ Critical Path:



- **Implementation:**

- **Seq:**

- **Schematic:**



- **Timing on 10 ns clock period:**

Design Timing Summary			
Setup		Hold	Pulse Width
Worst Negative Slack (WNS): 8.720 ns		Worst Hold Slack (WHS): 0.249 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns		Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0		Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 2		Total Number of Endpoints: 2	Total Number of Endpoints: 5
All user specified timing constraints are met.			

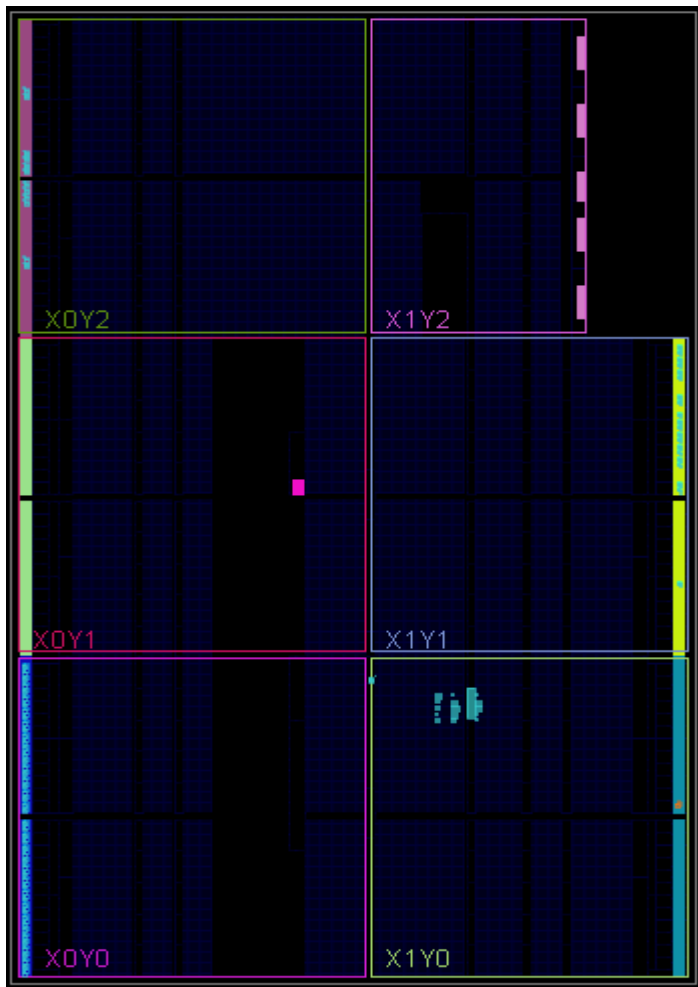
- **Utilization:**

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
APB_Wrapper	44	51	22	44	4	1	82	2
Master (APB_Master)	44	51	22	44	4	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0



## ○ Gray:

### ■ Schematic:



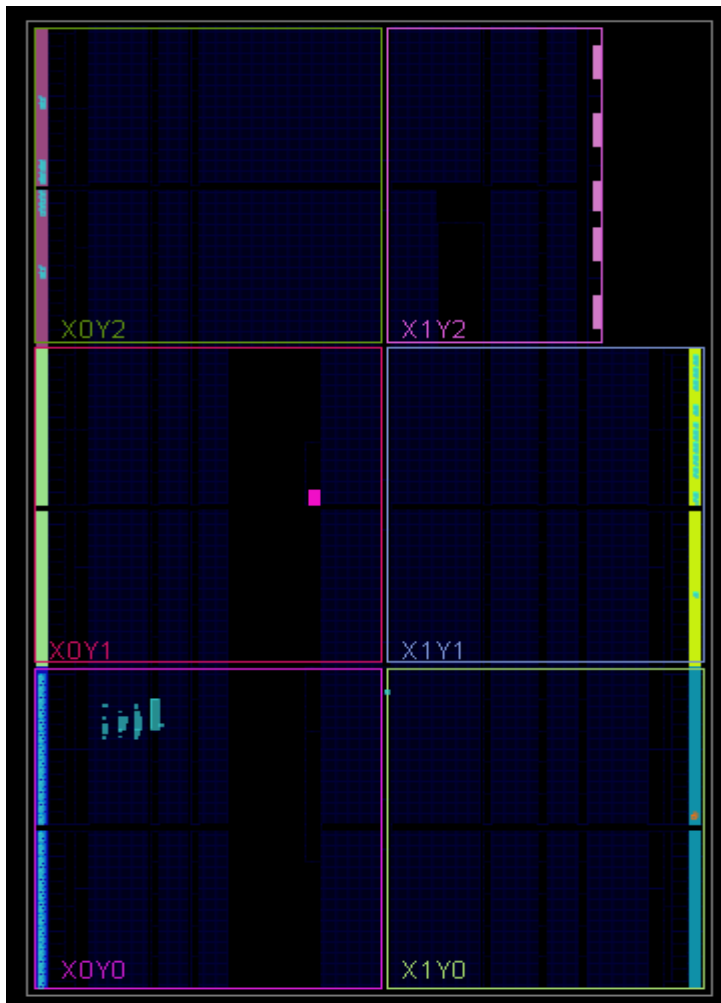
### ■ Timing on 10 ns clock period:

Design Timing Summary			
General Information			
Timer Settings			
Design Timing Summary			
Clock Summary (1)			
Check Timing (277)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
Timing Summary - Impl_1 (saved)			
Setup			
Worst Negative Slack (WNS):	8.717 ns	Worst Hold Slack (WHS):	0.292 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	2	Total Number of Endpoints:	2
Hold			
Pulse Width			
Worst Pulse Width Slack (WPWS):	4.500 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	5	Total Number of Endpoints:	5
All user specified timing constraints are met.			

### ■ Utilization:

Hierarchy								
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
APB_Wrapper	42	51	26	42	2	1	82	2
Master (APB_Master)	42	51	26	42	2	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0

- One\_Hot:
  - Schematic:



- Timing on 10 ns clock period:

General Information	Setup	Hold	Pulse Width
Timer Settings	Worst Negative Slack (WNS): 8.714 ns	Worst Hold Slack (WHS): 0.305 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (1)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
> Check Timing (232)	Total Number of Endpoints: 3	Total Number of Endpoints: 3	Total Number of Endpoints: 6
> Intra-Clock Paths	All user specified timing constraints are met.		
Inter-Clock Paths			
Other Path Groups			
Timing Summary - impl_1 (saved)			

- Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
APB_Wrapper	44	52	26	44	3	1	82	1
Master (APB_Master)	44	52	26	44	3	0	0	0
Slave (APB_Slave)	0	0	0	0	0	1	0	0

**From results we found that the best encoding is**  
**seq.**