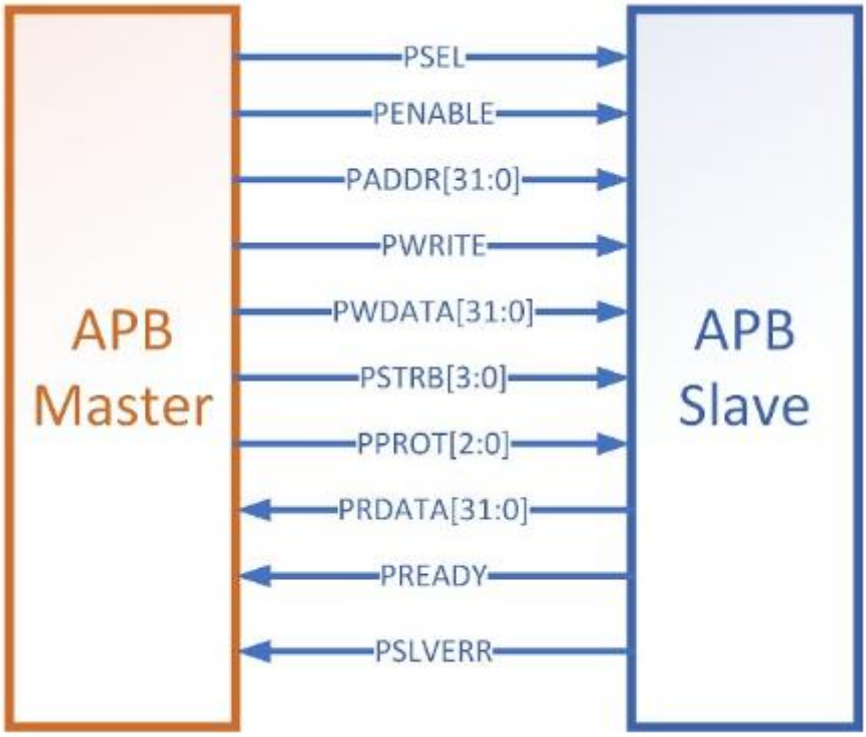
# AMBA APB Protocol

# (APB4)




## Created By:

**Mohamed Ahmed Mohamed Hussein** **25/8/2024**

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# Introduction to AMBA APB Protocol:

The AMBA (Advanced Microcontroller Bus Architecture) APB (Advanced Peripheral Bus) protocol is a low-complexity, low-power interface used in modern System-on-Chip (SoC) designs. As part of the AMBA family of protocols, the APB is specifically optimized for communication with peripherals that do not demand the high performance or complexity of buses like AHB (Advanced High-performance Bus) or AXI (Advanced eXtensible Interface).

# Importance of the AMBA APB Protocol:

The AMBA APB protocol is integral to efficient system design in embedded systems and microcontroller architectures due to its simplicity and power efficiency. By providing a straightforward, non-pipelined communication method, APB allows designers to connect and manage various low-speed peripherals such as timers, UARTs, GPIOs, and more without the overhead associated with more complex bus protocols.

One of the key advantages of the APB protocol is its ability to minimize power consumption, which is critical in battery-operated devices and applications where power efficiency is a priority. The protocol's non-pipelined nature and single-clock edge operation simplify timing requirements, making it easier to integrate with other system components.

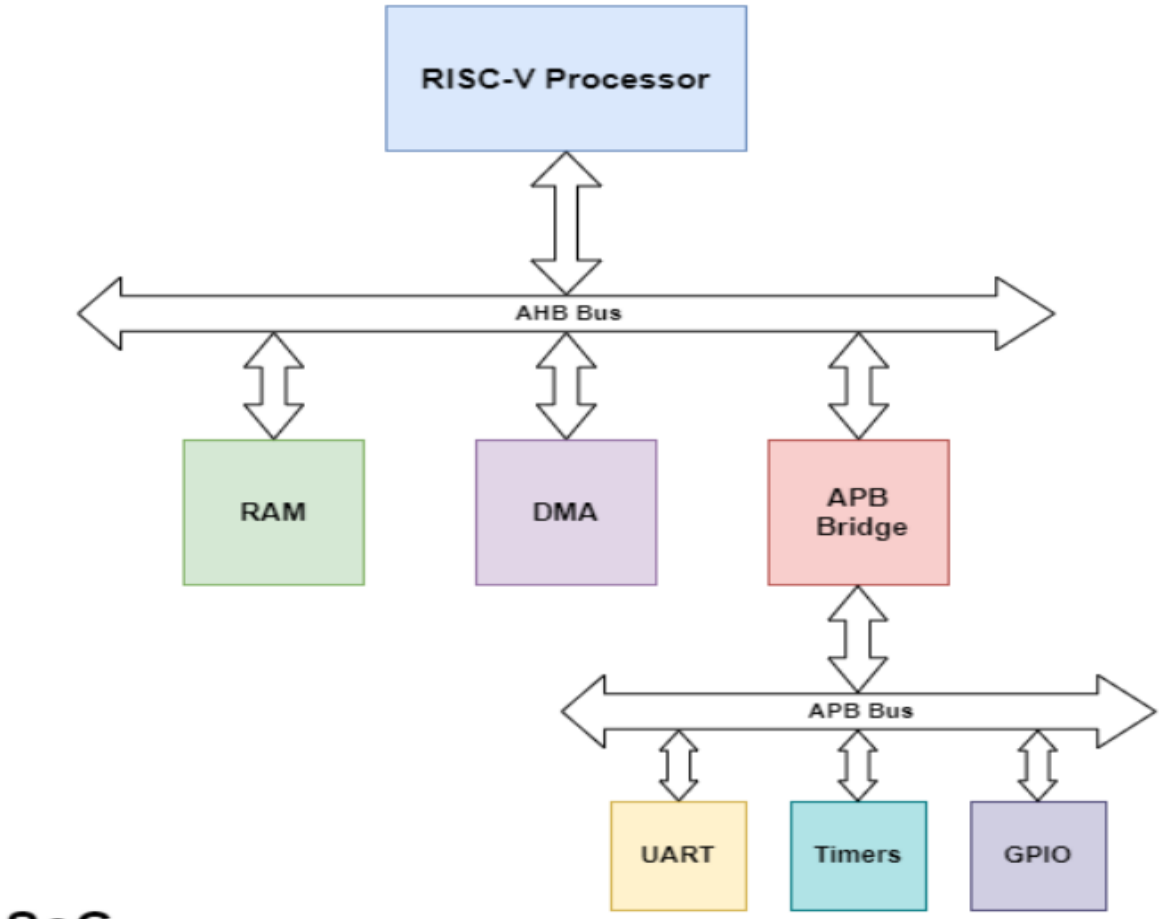
# Applications of the AMBA APB Protocol:

The AMBA APB protocol is widely used in various applications within SoCs, particularly in areas where simplicity and low power are essential. Common applications include:

- **Peripheral Connectivity:** APB is ideal for connecting low-speed peripherals like GPIO controllers, UARTs, and timers to the main processor. These peripherals typically do not require high-speed data transfers, making APB a perfect fit.
- **Configuration Registers:** Many SoCs use APB for accessing configuration registers that control various aspects of the chip's operation. The low-bandwidth nature of these operations suits the APB's characteristics.
- **Power Management Modules:** APB is often used in power management and clock control modules within SoCs. Its low power consumption aligns with the requirements of these subsystems, ensuring efficient operation.
- **Debug and Control Interfaces**: APB is also used for debug interfaces, control interfaces, and other low-speed data paths within an SoC. Its simplicity makes it easy to implement and integrate into complex designs.

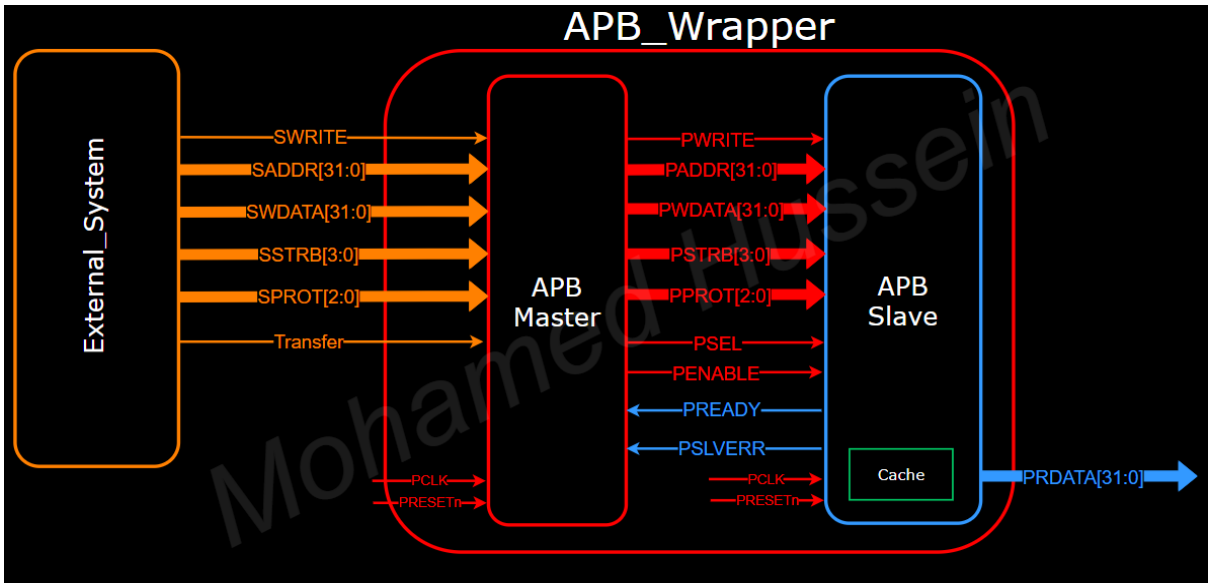
By providing a low-complexity, low-power bus interface, the AMBA APB protocol plays a crucial role in the efficient design and operation of modern embedded systems and SoCs. Its widespread adoption and applicability in various peripheral communication scenarios underscore its importance in the industry.

# SoC Application using AMBA protocols:




SoC

# Design Architecture:

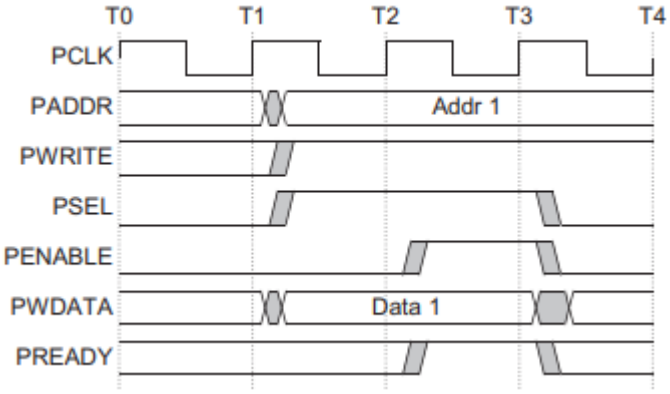


# Explanation of Signals:

- **PCLK:** The clock signal that times all transfers on the APB. The rising edge of PCLK triggers the transfer of data between the APB bridge and peripheral devices.
- **PRESETn:** A reset signal that is active LOW. It resets the entire APB system, including the peripheral devices connected to the bus.
- **PADDR:** The address bus driven by the APB bridge, which selects the register or memory location within the peripheral that will be accessed during a read or write operation.
- **PPROT:** The protection type signal that indicates the security level of the transaction. It can specify if the transaction is a normal or privileged access, and whether it is secure or non-secure.
- **PSELx:** A select signal generated by the APB bridge to each peripheral. It indicates which slave device is selected for communication and if a data transfer is required.
- **PENABLE:** The enable signal that indicates the second and subsequent cycles of an APB transfer. It differentiates between the setup phase and the access phase of the transfer.
- **PWRITE:** The direction signal that determines if the current operation is a write (HIGH) or read (LOW) operation.
- **PWDATA:** The data bus that carries the write data from the APB bridge to the peripheral. It is only valid when PWRITE is HIGH.
- **PSTRB:** The write strobe signal that indicates which byte lanes are active during a write transfer. Each strobe corresponds to a byte in the write data bus.
    - **More details:**

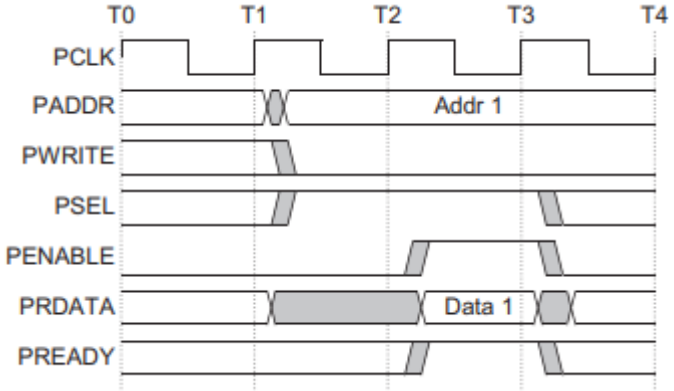
      The **PSTRB** signal, or write strobe, is used during a write transfer to indicate which byte lanes of the write data bus contain valid data. Each bit in PSTRB corresponds to one byte in the write data bus. For example, in a 32-bit data bus, PSTRB[3] controls bits [31:24], PSTRB[2] controls bits [23:16], and so on
- **PREADY:** A signal driven by the peripheral to indicate that it is ready to complete the transfer. It is used to extend the transfer if the peripheral is not ready.
- **PRDATA:** The read data bus driven by the peripheral during a read operation when PWRITE is LOW.
- **PSLVERR:** This signal indicates if there was an error during the transfer. It is not mandatory for peripherals to support this signal.

# Write Transfers:



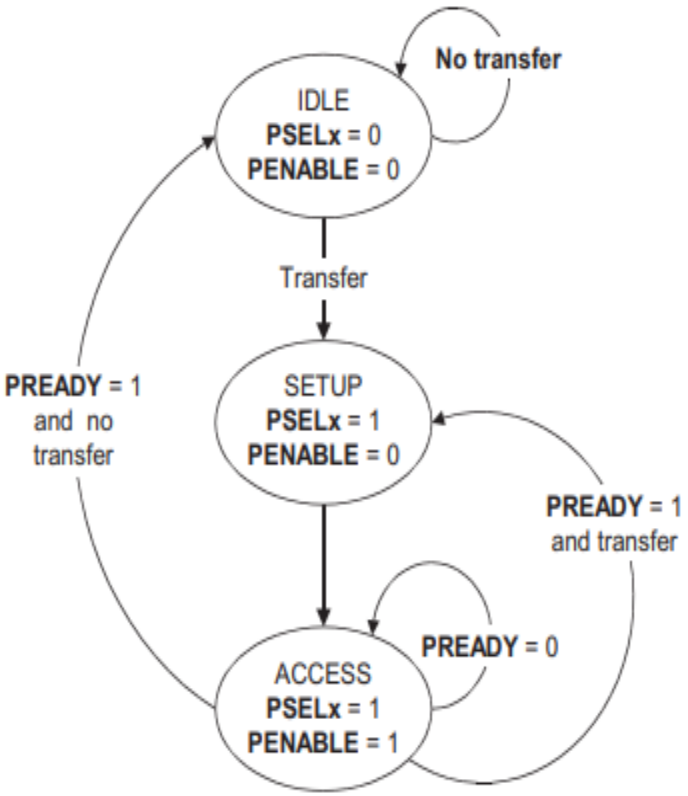

- **T1 (Setup Phase):** The write transfer begins with the address (PADDR), write data (PWDATA), the write signal (PWRITE), and the select signal (PSEL) being registered at the rising edge of PCLK. This phase is called the Setup phase.
- **T2 (Access Phase):** The enable signal (PENABLE) and the ready signal (PREADY) are registered at the next rising edge of PCLK. When PENABLE is asserted, the Access phase begins, and the slave prepares to complete the transfer.
- **T3 (Completion):** The transfer completes when PREADY is asserted by the slave, indicating that the data has been successfully written. The address, write data, and control signals remain valid until the end of the transfer.

# Read Transfers:




- **T1 (Setup Phase):** The read transfer begins with the setup of the address (PADDR), write signal (PWRITE = LOW), select signal (PSEL), and enable signal (PENABLE = LOW). This is the Setup phase.
- **T2 (Access Phase):** The enable signal (PENABLE) is asserted, marking the start of the Access phase. The peripheral must provide the read data (PRDATA) before the end of this phase.
- **T3 (Completion):** The transfer completes when the ready signal (PREADY) is asserted by the slave, indicating that the data is available for the master to read

# FSM Explanation:




The APB protocol FSM has the following states:

1. **IDLE:** This is the default state of the bus. When no transfers are required, the bus remains in the IDLE state.
2. **SETUP:** When a transfer is initiated, the bus moves into the SETUP state where the select signal (PSELx) is asserted. This state only lasts for one clock cycle and prepares the bus for the Access phase.
3. **ACCESS:** In this state, the enable signal (PENABLE) is asserted. The address, write, select, and write data signals remain stable during the transition from the SETUP to the ACCESS state. If the ready signal (PREADY) is asserted by the slave, the bus moves back to the IDLE state if no further transfers are required or to the SETUP state if another transfer is needed. If PREADY is held LOW by the slave, the bus remains in the ACCESS state until the transfer can be completed

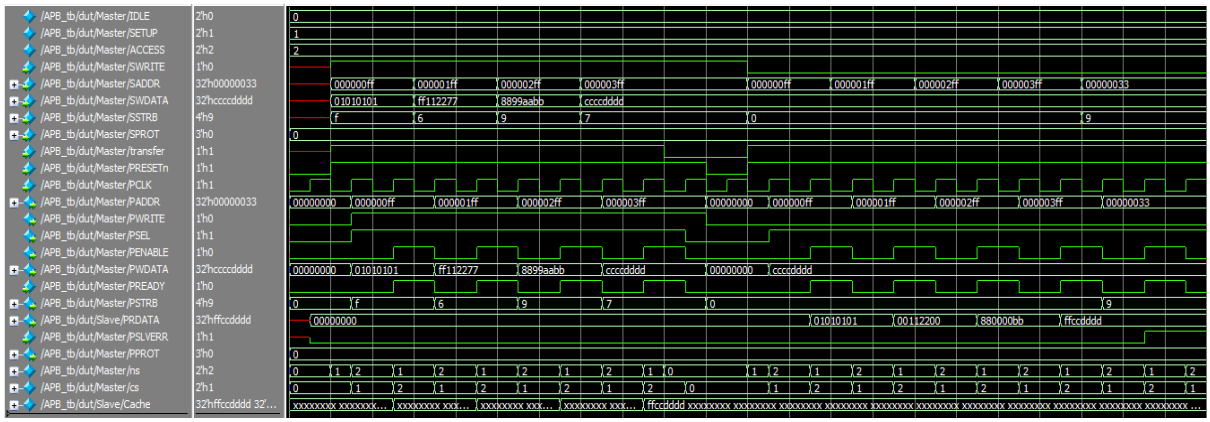
# Verifying Functionality:

In the test bench we are pretending to be the external system and we are sending the address, write data and the transfer signal to the APB master and then the master will the commands to the APB slave.

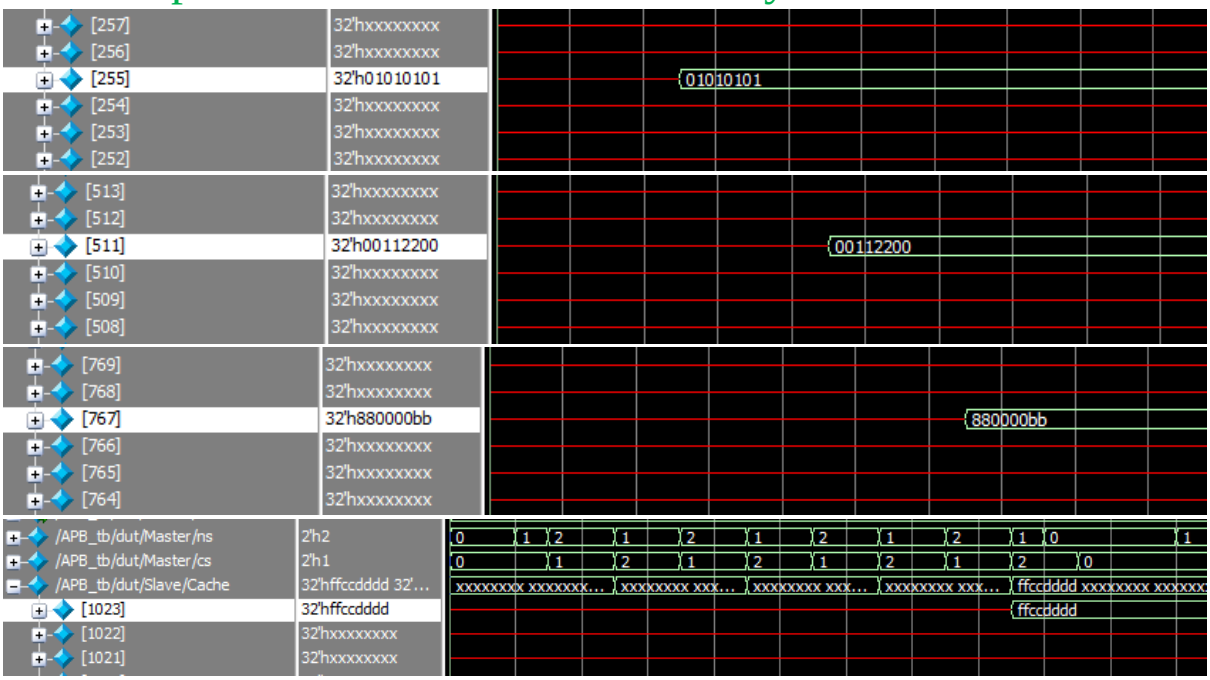
- **Scenario:**
  - **Writing**: We will write random data in several addresses and each address will have a different data to be written and also each address will have a different write strobe signal to verify its functionality.
  - **Reading**: After writing process comes the reading process in which we will read from the same addresses we wrote data into, and at the end there is a test to verify slave error signal functionality, so we are expecting the following:
    - PSEL, PENABLE signals are low in IDLE state
    - PSEL is high and PENABLE is low in SETUP state and SETUP state is only entered for one clock cycle
    - PSEL, PENABLE signals are high in ACCESS state
    - PREADY signal when high it lasts for one clock cycle and then turns back low
    - Note that the above specs can be verified through the **whole snippet** and the **comparison** in the next pages
    - The data values in each writing process to be written in cache memory in its specified address and the data will be written by their format specified by the PSTRB signal
    - The values written in memory will show in the PRDATA signal
    - Finally, the SLVERR signal will be high at the end due to our scenario

**Note:** we will see each one of the above observations in order in the **snippets** section

- **Snippets:**
  - Snapshot of whole wave form:

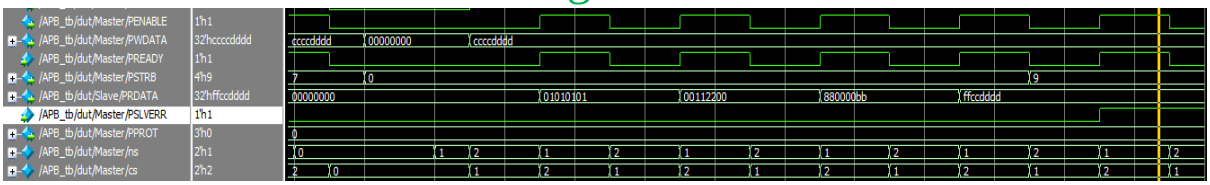



  - Snapshot of data written in memory in order:




    - Note that the values written in memory are different from the input values due to write strobe signal and last element stored has sign extension
  - Snapshot of the values written in memory showing up in **PRDATA** signal in order:

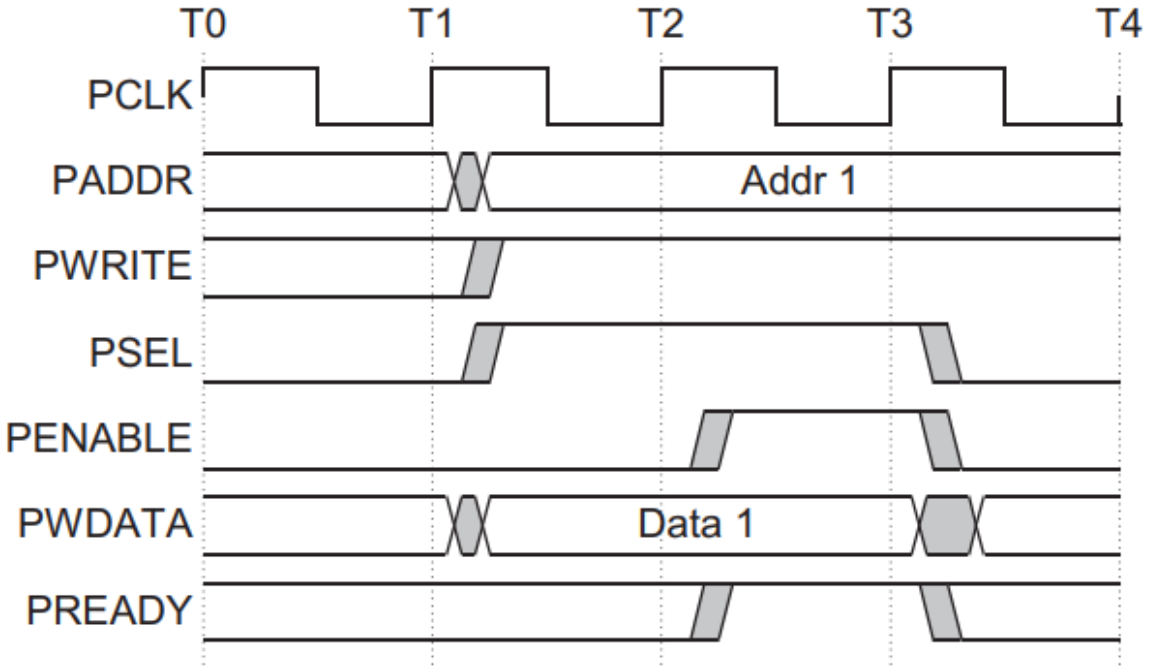
- Snapshot of **PSLVERR** high as **PSTRB** signal has some value while reading:




# • Comparison:

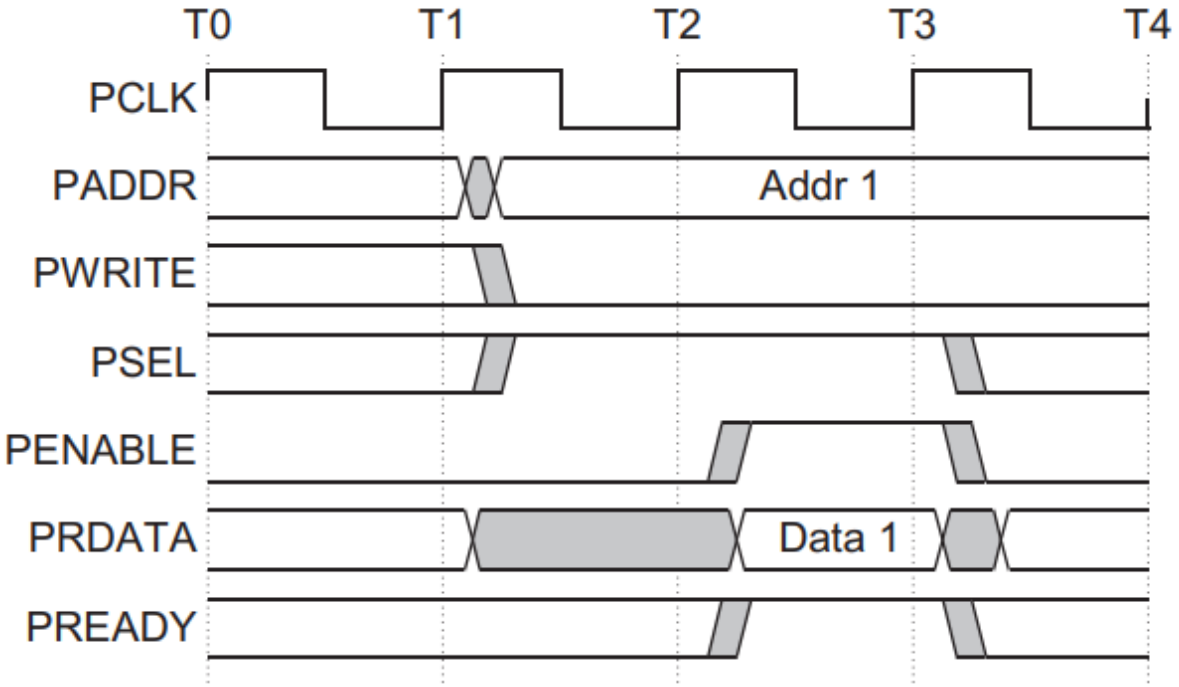
## ○ Writing Process:

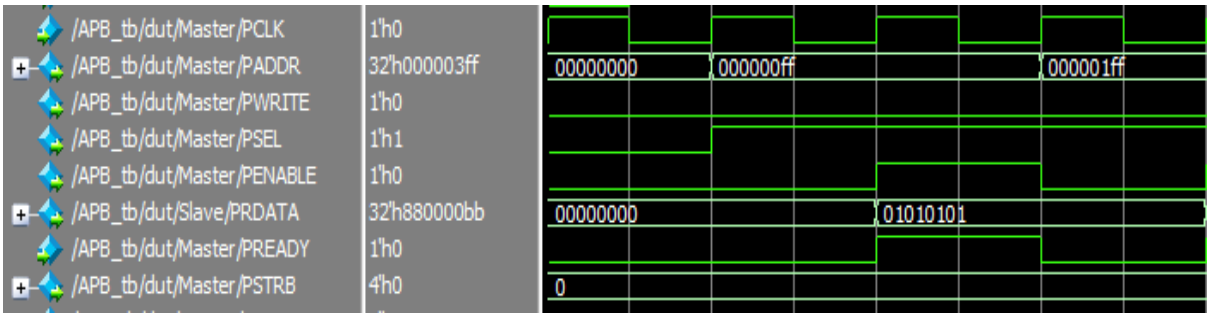
Comparing between the APB documentation wave form and my design wave form in writing process




- ## Reading Process:

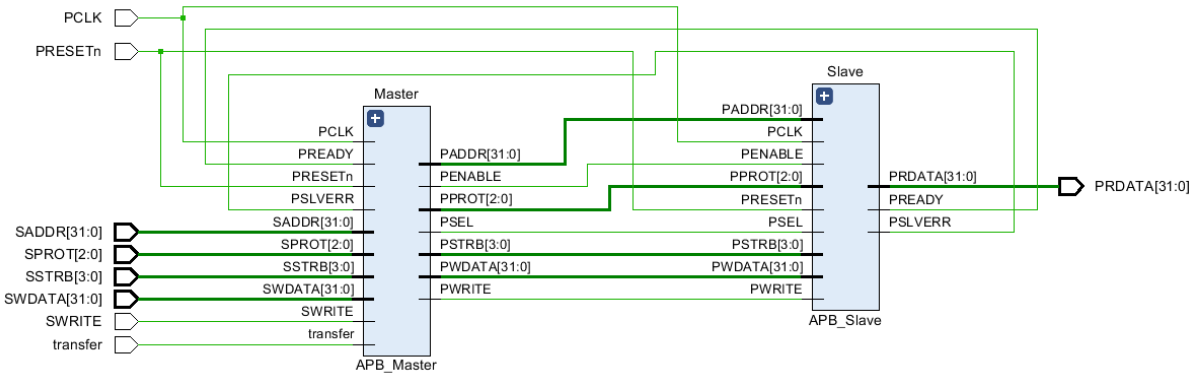
  Comparing between the APB documentation wave form and my design wave form in reading process



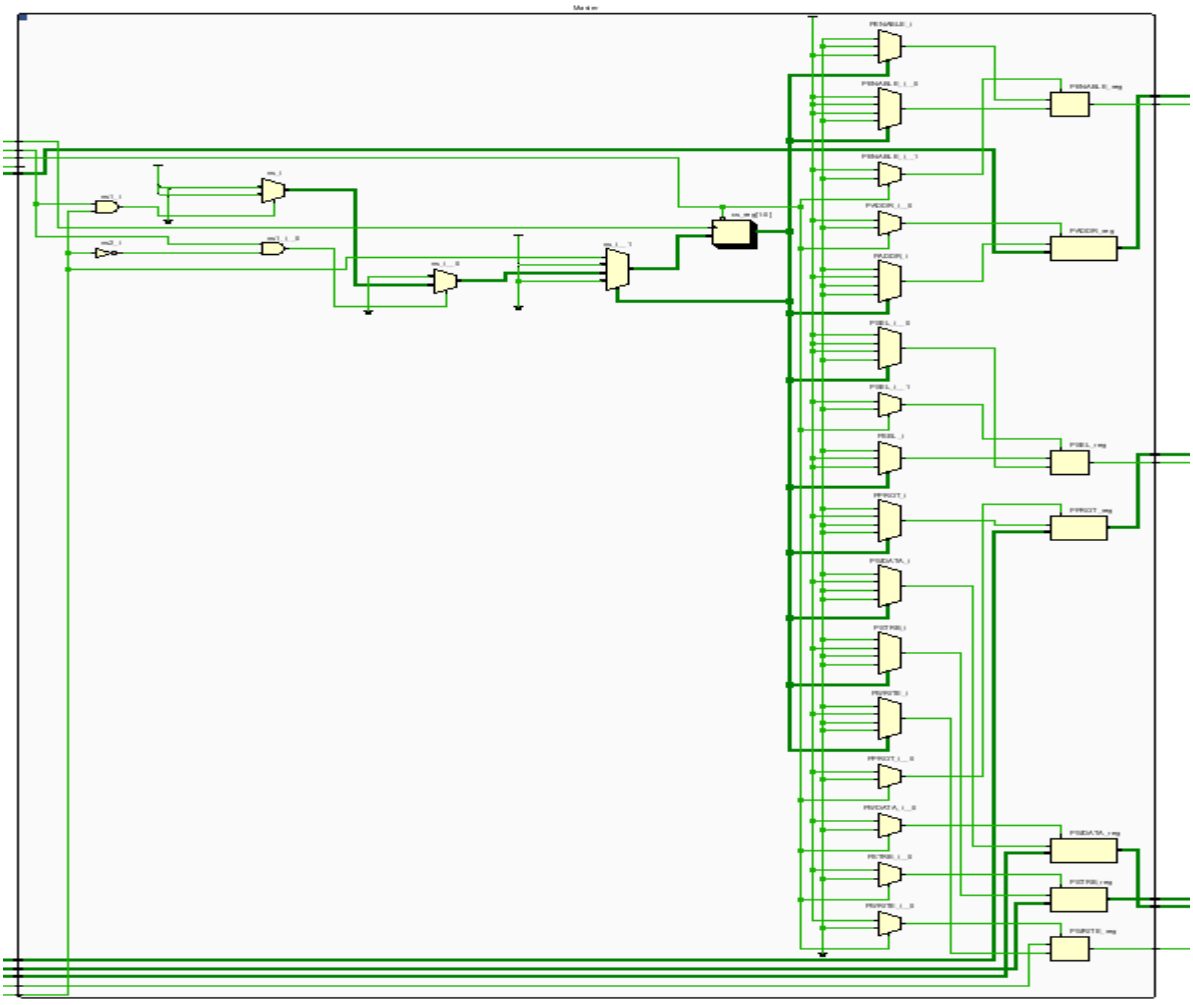



# Vivado:

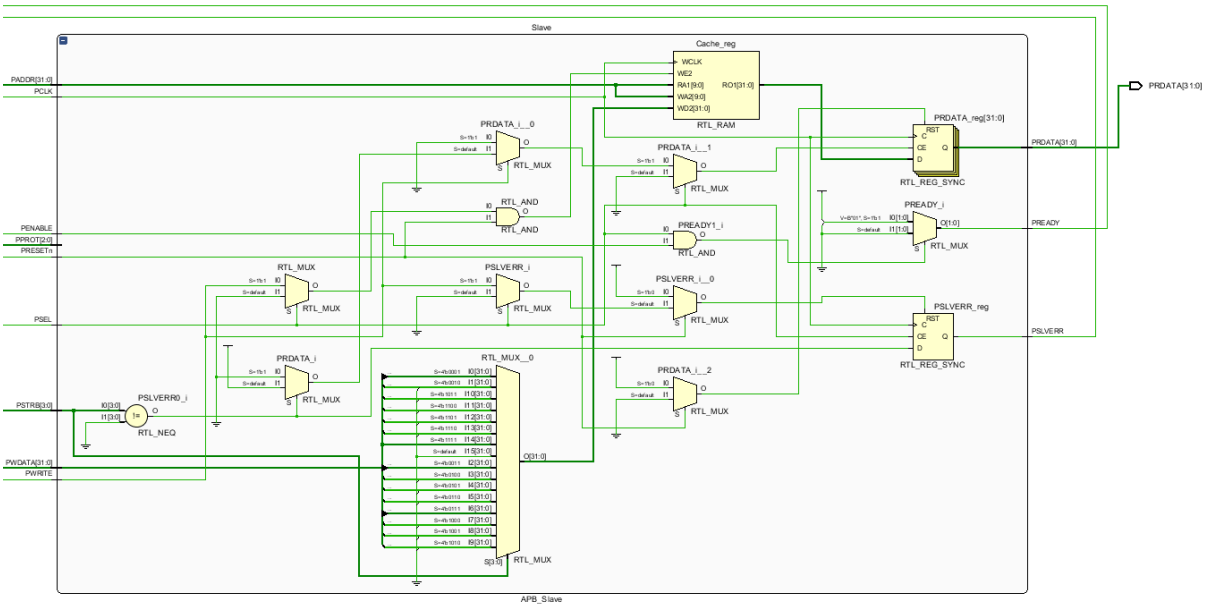
- Elaboration:
  - System:



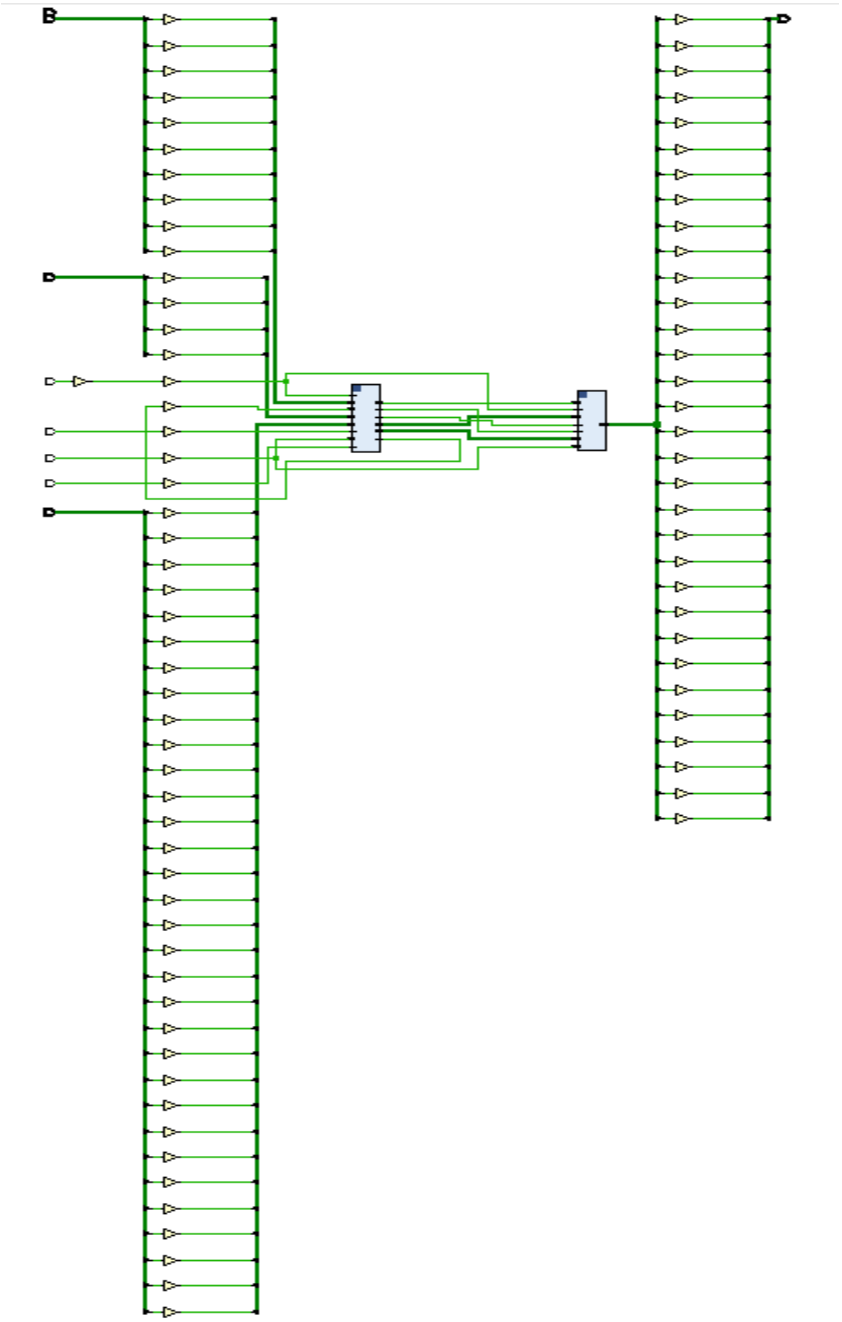

  - Master:



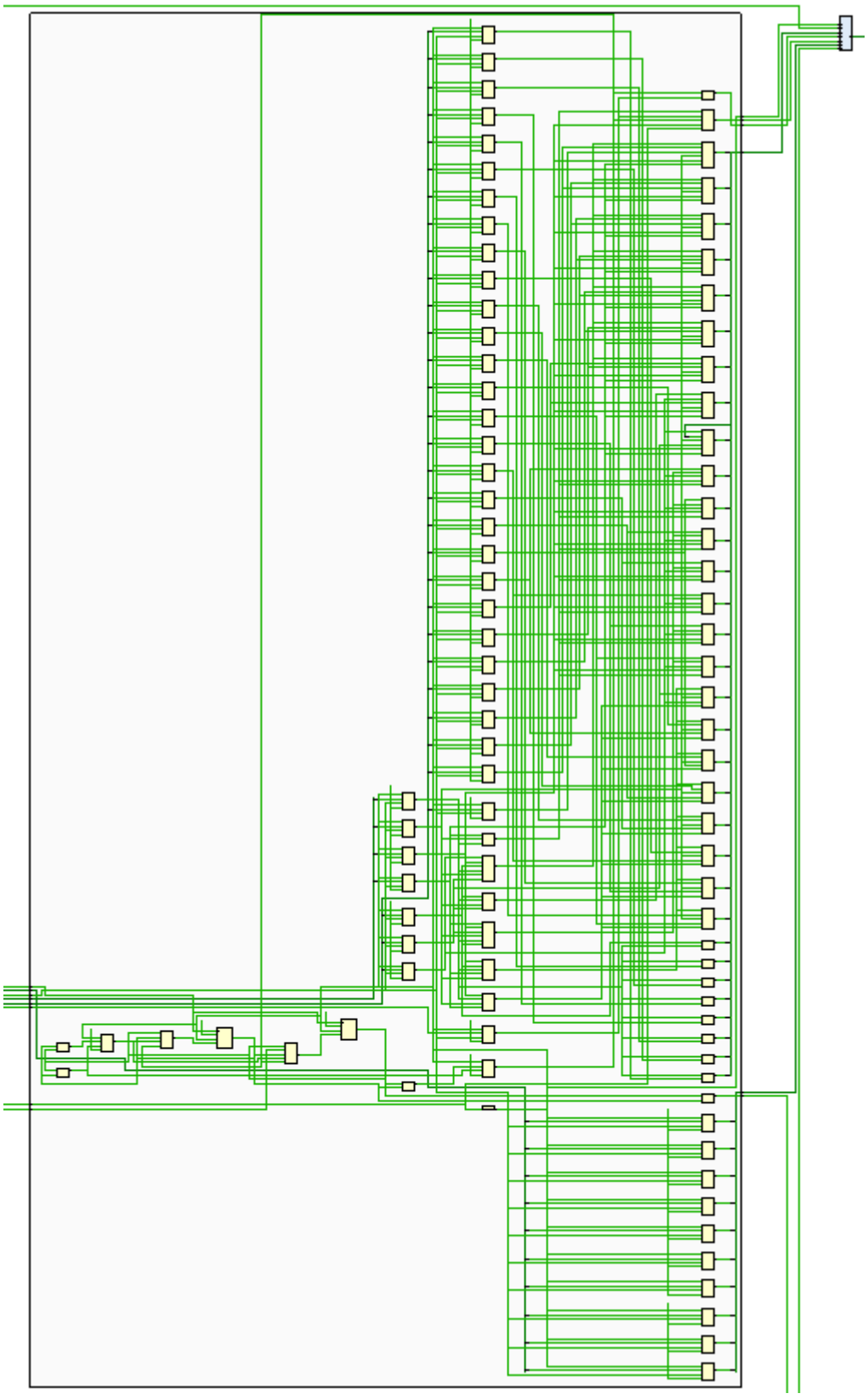
- Slave:


Slave
Cache_reg
WCLK
WE2
RA1[9:0]
RO1[31:0]
WA2[9:0]
WD2[31:0]
RTL_RAM
PADDR[31:0]
PCLK
PENABLE
PPROT[2:0]
PRESETn
PSEL
PSTRB[3:0]
PWDATA[31:0]
PWRITE
PRDATA_i__0
PRDATA_i__1
PRDATA_i
PRDATA_i__2
RTL_MUX
RTL_AND
PREADY1_i
PSLVERR_i
PSLVERR_i__0
PSLVERR0_i
RTL_NEQ
RTL_MUX__0
PRDATA_reg[31:0]
RTL_REG_SYNC
PREADY_i
PSLVERR_reg
PRDATA[31:0]
PREADY
PSLVERR
APB_Slave

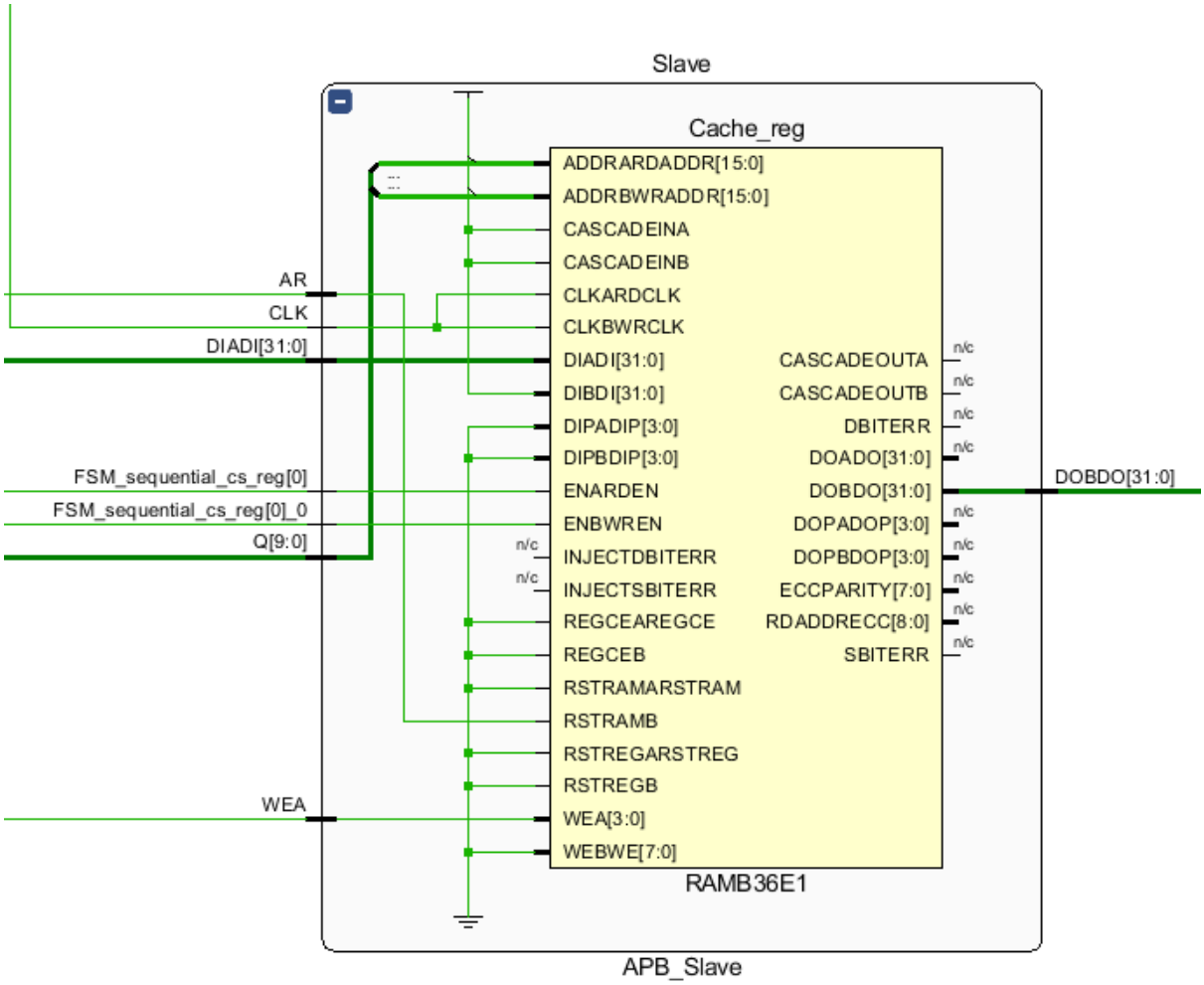
- **Synthesis:**
  - **Seq:**
    - Schematic:
      - System:



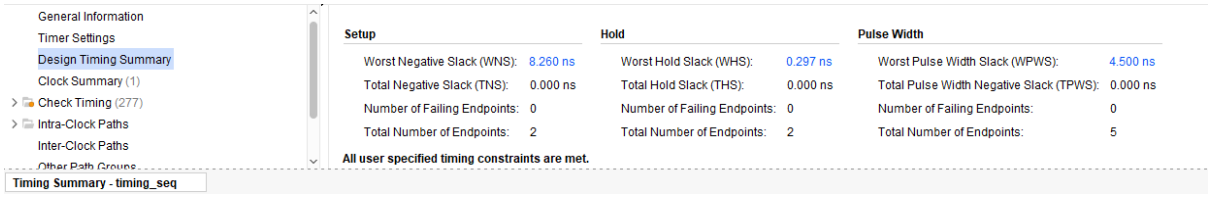
- Master:



- Slave:

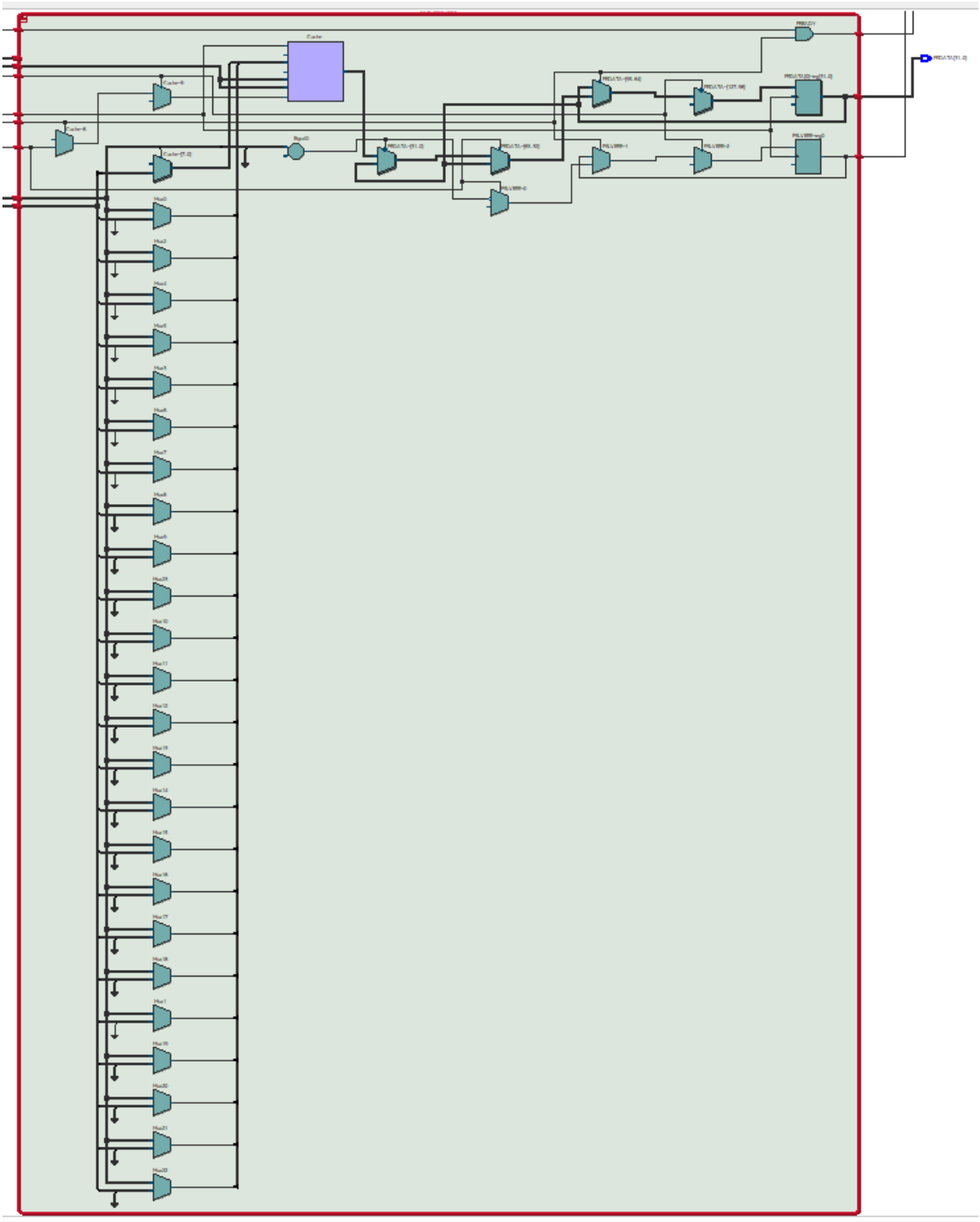



- Timing Summary on 10 ns clock period:



# Quartus:

- Schematic:



- Timing (10ns Period):
  - **Clock**

<<Filter>>

| | Clock Name | Type | Period | Frequency | Rise | Fall | Duty Cycle | Divide by |
|---|---|---|---|---|---|---|---|---|
| 1 | PCLK | Base | 10.000 | 100.0 MHz | 0.000 | 5.000 | | |

  - **Fmax**

| | Fmax | Restricted Fmax | Clock Name | Note |
|---|---|---|---|---|
| 1 | 108.92 MHz | 108.92 MHz | PCLK | |

  - **Hold**

<<Filter>>

| | Clock | Slack | End Point TNS |
|---|---|---|---|
| 1 | PCLK | 0.326 | 0.000 |

  - **Setup**

| | Clock | Slack | End Point TNS |
|---|---|---|---|
| 1 | PCLK | 0.819 | 0.000 |

  - **Slack**

<<Filter>>

| | Clock | Slack | End Point TNS |
|---|---|---|---|
| 1 | PCLK | 4.578 | 0.000 |

# References:

[AMBA APB Protocol Specification]