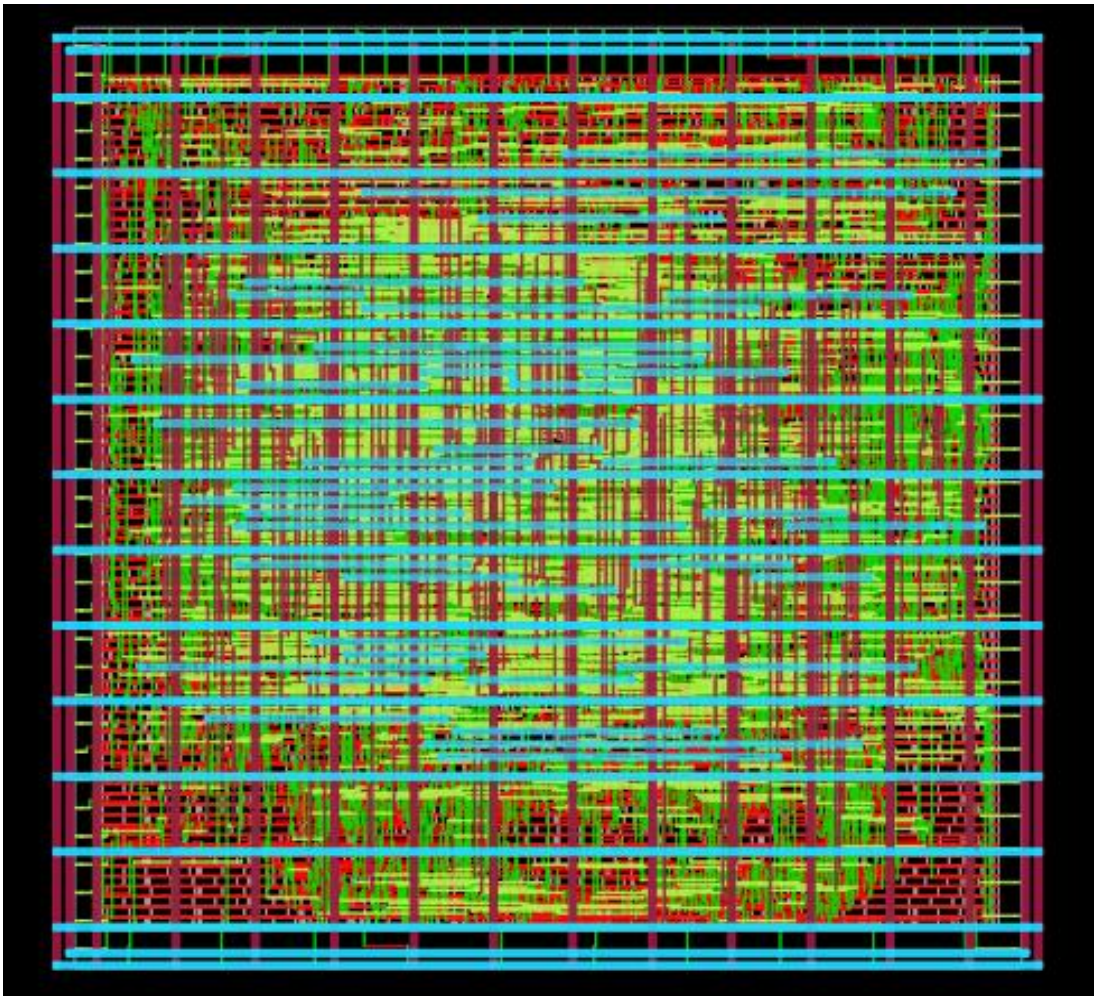
Backend Implementation of Wishbone QSPI Flash Controller using OpenROAD & OpenLANE



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Presented to: **ICpedia PnR team**

Introduction

Project Goals:

- Implement the **RTL-to-GDSII** flow for the wbqspiflash.
- Achieve the **maximum operating frequency** possible under relaxed area constraints.
- Reduce the **die area to the minimum possible** without violating timing or DRC rules.
- Validate the final design by comparing **GDS** and **LEF** views, verifying pin metal layers, and checking that LEF dimensions match the floorplan report.

How to achieve these goals?

- We are going to implement the complete **RTL-to-GDSII flow** for the wbqspiflash design using the **OpenLane physical design toolchain**.
- We will first focus on **timing optimization** by achieving the **maximum operating frequency under relaxed area constraints.**
- After that, we will keep the frequency constant and work on **minimizing the die area** as much as possible without violating timing or DRC rules.
- We will **customize the physical design aspects** by:
    - Arranging the input and output pins according to the required specifications (inputs on East/West and outputs on North/South).
    - Modifying the **power delivery network (PDN)** to include straps on all metal layers (Met1–Met5).
- We will tune **placement, CTS, and routing configurations** to close timing and reduce area while analyzing trade-offs.
- We will also experiment with the DRT_OPT_ITERS parameter to evaluate the effect on **DRC count versus runtime trade-offs**.
- Using **KLayout**, we will validate:
    - The differences between **GDS and LEF** files.
    - Which layers correspond to **Met2 and Met3** for pin creation.
    - That the **LEF dimensions** match our floorplan configurations.
- Finally, **we will document all steps**, configuration changes, screenshots, and results in a report, including tables comparing different trials for frequency, area, timing (WNS/TNS), and DRC count.

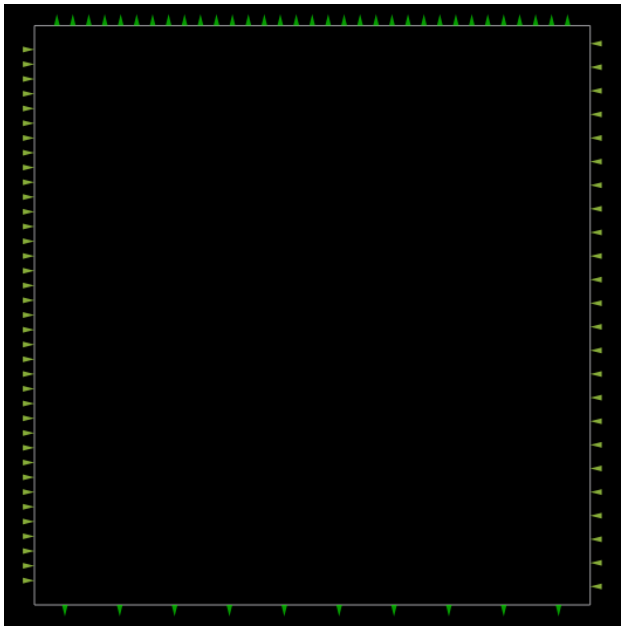
Floor planning and Power planning

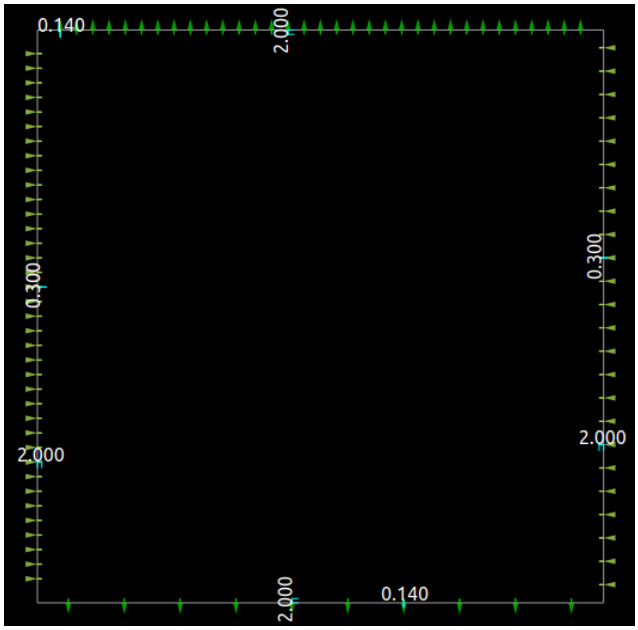
1. Floorplan (Pins order)

Required:

- Input pins “Yellow” are in East and West of the IP.
- Output pins “Green” are in North and South of the IP.
- i_wb_data[*] is to be in WEST only / o_wb_data[*] is to be in North only.
- The thickness of the vertical and horizontal pins is to be 1x default width
- The length of the pins is to be 2um.

Implemented:





- For pins order check pin_order.cfg & for thickness and length of the pins check config.tcl
- We see that the length of all pins is 2um as required, also the thickness for the vertical pins is 0,14 um by default and 0.3 um for horizontal pins by default

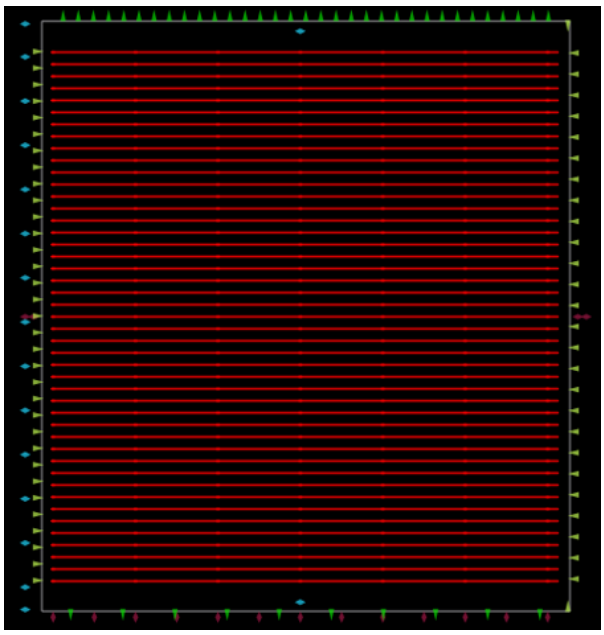
2. Power Plan

Required:

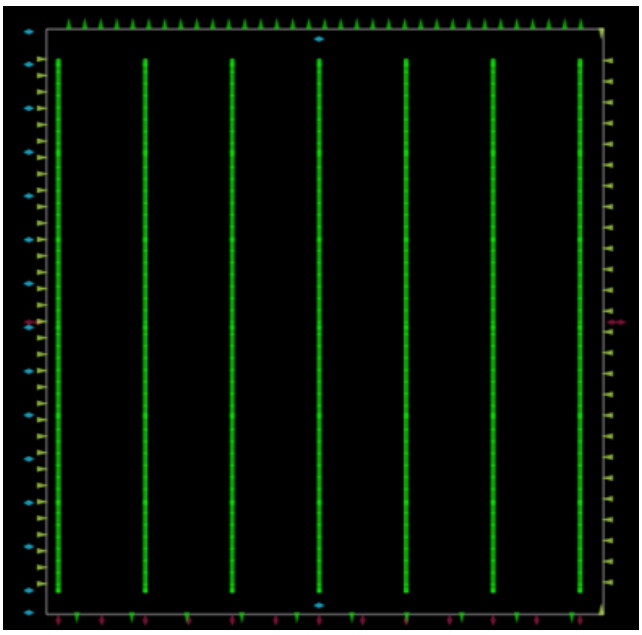
Edit the power structure in order to have straps in all metals (met1 to met5).

- **Implemented:**

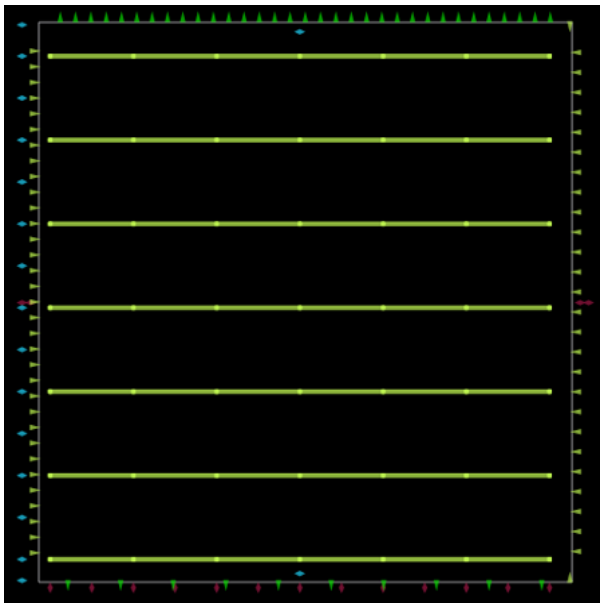
Metal 1:



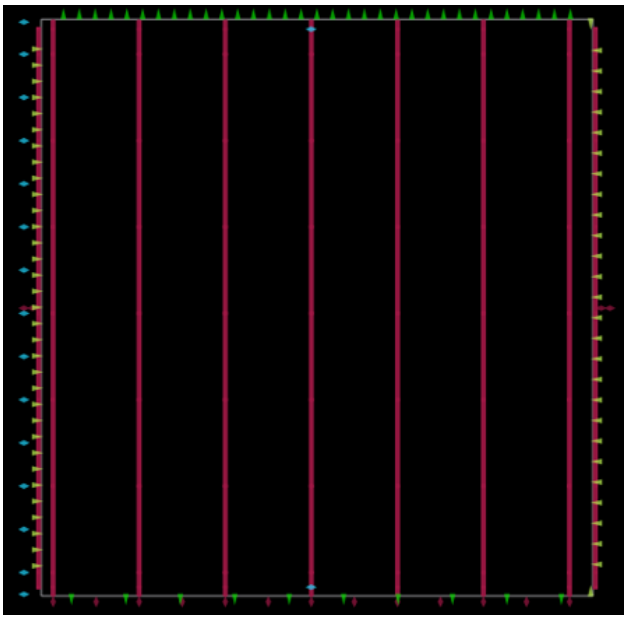
Metal 2:



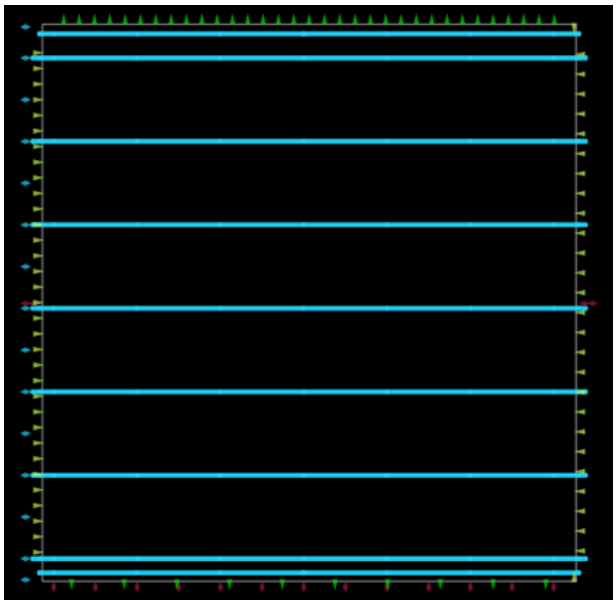
Metal 3:



Metal 4:

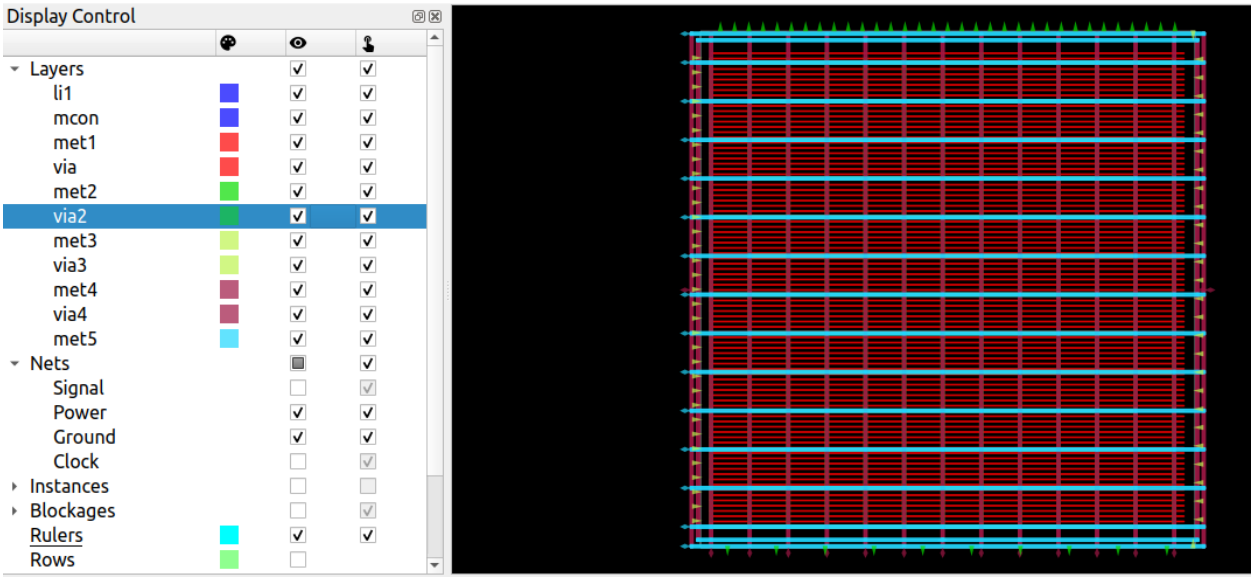


Metal 5:



Hint: You may check floorplan in [sky130A_sky130_fd_sc_hd_config.tcl] to get the PDN configs

Whole PDN:



Note: Metal snapshots are for power only; I'm not including ground.

PDN Implementation Details

- **Metal Orientation:**
  - **M1:** Horizontal (local power rails)
  - **M2:** Vertical (connects M1 to upper layers)
  - **M3:** Horizontal (intermediate straps)

- **M4:** Vertical (VGND global strap)
- **M5:** Horizontal (VPWR global strap)

- **Reasoning:**
  - Alternating directions (H-V-H-V-H) reduces routing interference and improves power distribution.
  - **VPWR** and **VGND** use **higher metals (M5, M4)** for lower resistance, higher current capacity, and reduced IR drop.
  - Lower metals (M1–M3) connect standard cells to the global power grid efficiently.

Placement and CTS

Required:

compare results of two different configurations, Mention the variables you have changed.

Case 1:

- **Configurations:**

sky130A_sky130_fd_sc_hd_config.tcl - /home/opentools/OpenLane/designs/wbqspiflash/

File Edit Search Preferences Shell Macro Windows

orplan.tcl | synthesis.tcl | routing.tcl | placement.tcl | config.tcl | sky130A_sky130_fd_sc_ | cts.tcl

```
# SCL Configs
set ::env(CLOCK_PERIOD) "20"
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(FP_CORE_UTIL) 40
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]
#set ::env(PL_TARGET_DENSITY) 0.50

# Synth defaults
set ::env(SYNTH_BIN) yosys
set ::env(SYNTH_SCRIPT) $::env(SCRIPTS_DIR)/yosys/synth.tcl
set ::env(SYNTH_NO_FLAT) 0
set ::env(SYNTH_CLOCK_UNCERTAINITY) 0.10
set ::env(SYNTH_CLOCK_TRANSITION) 0.10
set ::env(SYNTH_TIMING_DERATE) 0.05
set ::env(SYNTH_CAP_LOAD) 5
set ::env(SYNTH_SHARE_RESOURCES) 1
set ::env(SYNTH_BUFFERING) 1
set ::env(SYNTH_SIZING) 1
set ::env(SYNTH_MAX_FANOUT) 30
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(SYNTH_ADDER_TYPE) "YOSYS"
set ::env(CLOCK_BUFFER_FANOUT) 16
set ::env(SYNTH_READ_BLACKBOX_LIB) 0
set ::env(SYNTH_TOP_LEVEL) 0
set ::env(SYNTH_FLAT_TOP) 0
set ::env(IO_PCT) 0.2

# floorplan
set ::env(FP_SIZING) relative
set ::env(FP_PDN_VOFFSET) 0
set ::env(FP_PDN_VPITCH) 40
set ::env(FP_PDN_HOFFSET) 0
set ::env(FP_PDN_HPITCH) 40
set ::env(FP_PDN_AUTO_ADJUST) 1

#placement (all other values are set to default)
set ::env(PL_TARGET_DENSITY) 0.45
set ::env(PL_ROUTABILITY_DRIVEN) 1
set ::env(PL_TIME_DRIVEN) 1

# cts (all other values are set to default)
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 200
set ::env(CTS_TOLERANCE) 100
set ::env(CTS_SINK_CLUSTERING_SIZE) 25
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 50
```

Changed:

```
PP_CORE_UTIL: 40
PL_TARGET_DENSITY: 0.5
PL_ROUTABILITY_DRIVEN: 1
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 50
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
```

- **Results in Reports:**

1. Timing after CTS (slacks):

Open | 13-cts_rsz_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/wbqspiflash/runs/Case1/reports/cts

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 13.36
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.32
```

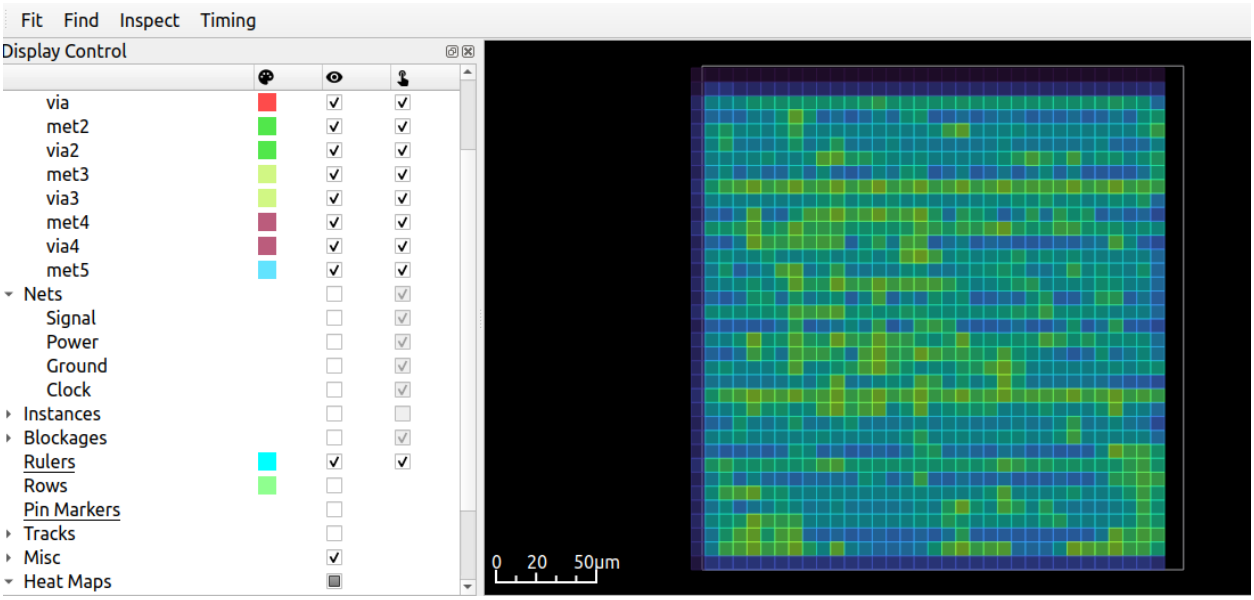
2. Timing after Signoff:

Open | 29-rcx_mca_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/w...spiflash/runs/Case1/reports/signoff

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 10.08
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.16
```

3. Congestion map:



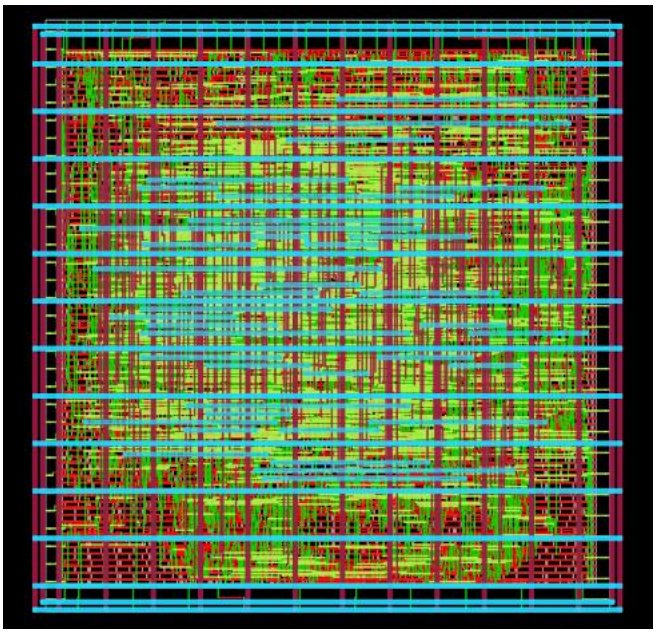
4. Area after signoff:

Open | 28-rcx_sta.area.rpt
/home/opentools/OpenLane/designs/wbqspiflash/runs/Case1/reports/signoff | Save

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt | 28-rcx_sta.area.rpt

```
1
2 ---------------------------------------------------------------------------
3 report_design_area
4 ---------------------------------------------------------------------------
5 Design area 49895 u^2 97% utilization.
```

5. Whole map:



Case 2:

- **Configurations:**

sky130A_sky130_fd_sc_hd_config.tcl - /home/opentools/OpenLane/designs/wbqspiflash/

File Edit Search Preferences Shell Macro Windows

porplan.tcl | synthesis.tcl | routing.tcl | placement.tcl | config.tcl | sky130A_sky130_fd_sc_ | cts.tcl | README.md

```
# SCL Configs
set ::env(CLOCK_PERIOD) "20"
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(FP_CORE_UTIL) 55
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]
#set ::env(PL_TARGET_DENSITY) 0.50

# Synth defaults
set ::env(SYNTH_BIN) yosys
set ::env(SYNTH_SCRIPT) $::env(SCRIPTS_DIR)/yosys/synth.tcl
set ::env(SYNTH_NO_FLAT) 0
set ::env(SYNTH_CLOCK_UNCERTAINITY) 0.10
set ::env(SYNTH_CLOCK_TRANSITION) 0.10
set ::env(SYNTH_TIMING_DERATE) 0.05
set ::env(SYNTH_CAP_LOAD) 5
set ::env(SYNTH_SHARE_RESOURCES) 1
set ::env(SYNTH_BUFFERING) 1
set ::env(SYNTH_SIZING) 1
set ::env(SYNTH_MAX_FANOUT) 30
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(SYNTH_ADDER_TYPE) "YOSYS"
set ::env(CLOCK_BUFFER_FANOUT) 16
set ::env(SYNTH_READ_BLACKBOX_LIB) 0
set ::env(SYNTH_TOP_LEVEL) 0
set ::env(SYNTH_FLAT_TOP) 0
set ::env(IO_PCT) 0.2

# floorplan
set ::env(FP_SIZING) relative
set ::env(FP_PDN_VOFFSET) 0
set ::env(FP_PDN_VPITCH) 40
set ::env(FP_PDN_HOFFSET) 0
set ::env(FP_PDN_HPITCH) 40
set ::env(FP_PDN_AUTO_ADJUST) 1

#placement (all other values are set to default)
set ::env(PL_TARGET_DENSITY) 0.65
set ::env(PL_ROUTABILITY_DRIVEN) 0
set ::env(PL_TIME_DRIVEN) 1

# cts (all other values are set to default)
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 100
set ::env(CTS_TOLERANCE) 50
set ::env(CTS_SINK_CLUSTERING_SIZE) 12
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 30
```

Changed:

```
PP_CORE_UTIL: 55
PL_TARGET_DENSITY: 0.65
PL_ROUTABILITY_DRIVEN: 0
CTS_TARGET_SKEW: 100
CTS_TOLERANCE: 50
CTS_SINK_CLUSTERING_SIZE:12
CTS_SINK_CLUSTERING_MAX_DIAMETER:30
```

- **Results in Reports:**

1. Timing after CTS (slacks):

Open — 13-cts_rsz_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/wbqspiflash/runs/Case2/reports/cts

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 12.87
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.33
```

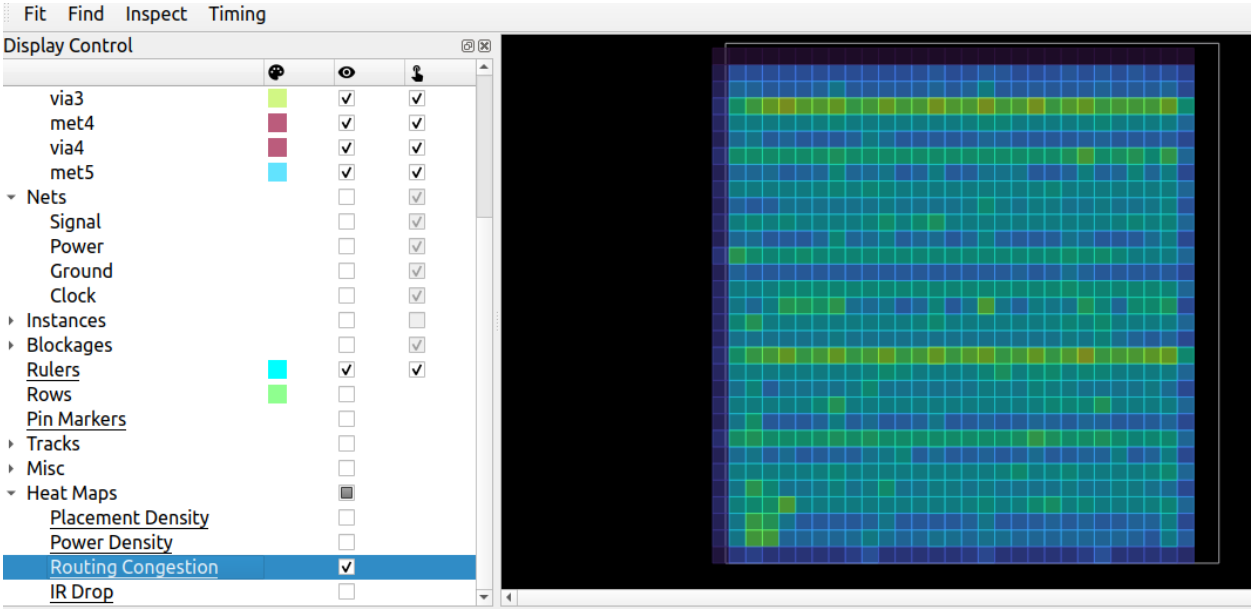
2. Timing after Signoff:

Open — 29-rcx_mca_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/w...spiflash/runs/Case2/reports/signoff

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 8.67
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.17
```

3. Congestion map:



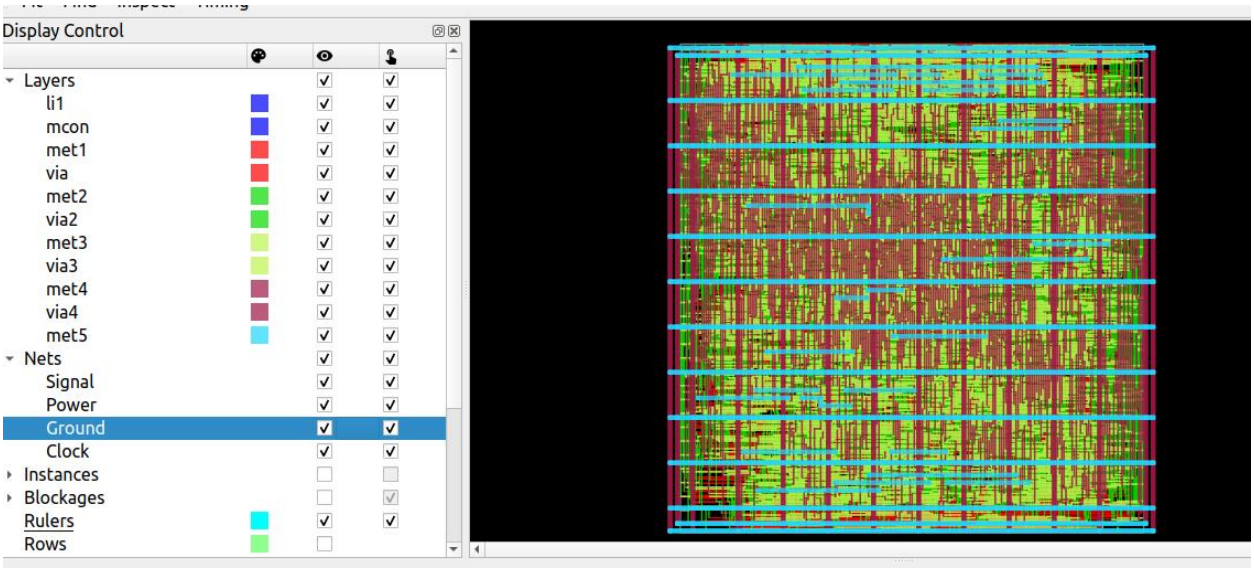
4. Area after signoff:

Open — 28-rcx_sta.area.rpt
/home/opentools/OpenLane/designs/wbqspiflash/runs/Case2/reports/signoff — Save

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | 13-cts_rsz_sta.worst_slack.rpt | 28-rcx_sta.area.rpt

```
1
2 ---------------------------------------------------------------------------
3  report_design_area
4 ---------------------------------------------------------------------------
5 Design area 36344 u^2 97% utilization.
```

5. Whole map:



Comparison:

- **One to one:**

Parameter	Run 1 (Lower Utilization)	Run 2 (Higher Utilization)
Core Utilization	40%	55%
Placement Density	0.45	0.65
CTS Target Skew	200 ps	100 ps
Area	**Larger** (due to lower utilization)	**Smaller** (due to higher utilization)
Congestion	**Higher** (cells spread out → more wire crossings)	**Lower** (tighter clustering → shorter routes)
Slack (Timing)	**Better** (lighter CTS, less insertion delay)	**Worse** (heavier CTS, more buffers, higher latency)

- **Reasoning:**

In the **first run**, routability-driven placement with a **lower target density** resulted in **more evenly spread cells, increasing routing congestion**. However, the looser skew target during CTS produced a lighter clock tree with fewer buffers, lower insertion delay, and therefore **better slack**.

In the **second run**, time-driven placement with a higher target density clustered critical cells, which **reduced apparent congestion in the global routing heatmap**. But the aggressive CTS settings (tight skew, small clustering size) inserted many buffers and increased insertion delay, **which degraded slack**.

DRCs and Run time tradeoff

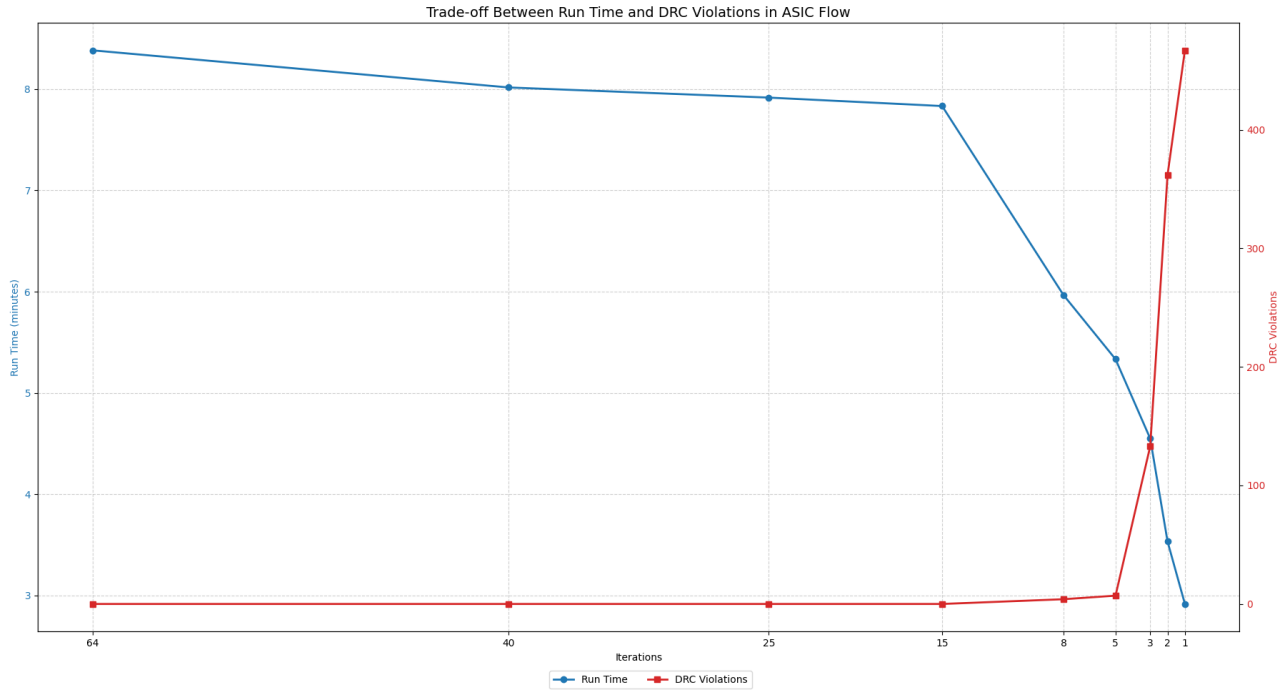
Required:

Change DRT_OPT_ITERS variable in routing configuration and report the tradeoff between reported DRCs and runtime.

Comparison table:

Iterations	Run time	DRCs
64	8min, 23sec	No violations
40	8min, 01sec	No violations
25	7min, 55sec	No violations
15	7min, 50sec	No violations
8	5min, 58sec	4 violations
5	5min, 20sec	7 violations
3	4min, 33sec	133 violations
2	3min, 32sec	362 violations
1	2min, 55sec	467 violations

Graph:



Note: you can run this python script to get the graph, [DRCs vs Run time .py]

Explanation:

- **High Iterations (64, 40, 25):** Tools have enough time to fix design issues, resulting in **zero DRC violations** but **longer runtime**.
- **Moderate Iterations (8, 5):** Runtime improves, but minor violations appear as optimization is incomplete.
- **Very Low Iterations (3, 2, 1):** Drastic drop in runtime, but **hundreds of violations occur** because the flow cannot finish fixing congestion, routing, and spacing errors.
- **Conclusion:** There is a **trade-off between runtime and design quality**. Choosing iterations depends on the required QoR (Quality of Results) and time-to-market constraints.

Frequency and Area

Required:

close timing and DRC with the minimum die area and max frequency possible**. First is to reach max frequency** with relaxed area constraints (hint: initial utilization), **then make frequency constant and focus on area reduction** getting the minimum die area possible.

Trails to get max Frequency

Note: I used default values except for the **max fanout** I changed it to be **30**, this section uses mainly default values in configs, later I will make some combinations in those configuration to get the **max frequency with the min area!**

1. Trail #1 (15 ns)

Open

29-rcx_mca_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/w...lash/runs/15ns_full/reports/signoff

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.area.rpt | 29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.area.rpt

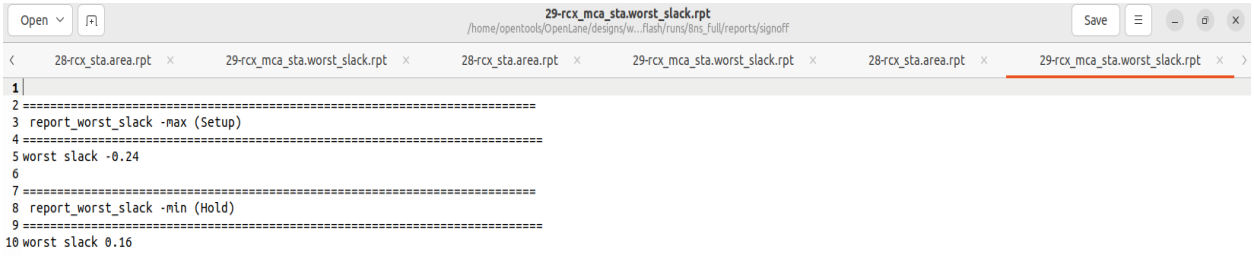
```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 6.13
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.16
```

Flow success

2. Trail #2 (10 ns)

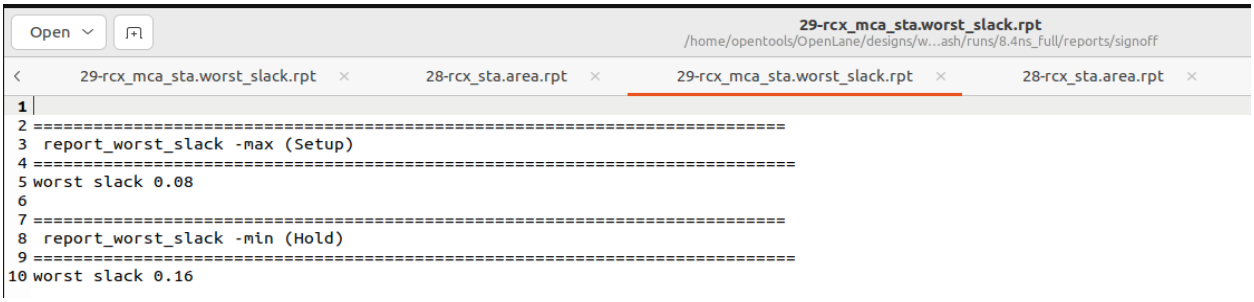
Flow success

3. Trial #3 (8 ns)



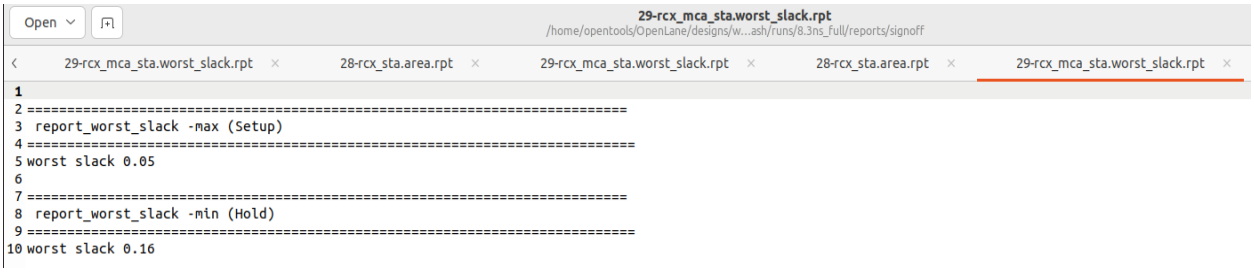
Flow failed in multiple corner analysis for setup after signoff

4. Trial #4 (8.4 ns)



Flow success

5. Trail #5



Flow success

Summary Table:

TRIAL #	Changed Parameter	Frequency	Area	Timing Results (MCA Slacks)		DRCs Count
				Setup	Hold	
1	Period 15 ns	66.67 MHz	**Default**	6.13	0.16	**No violations**
2	Period 10 ns	100 MHz	**Default**	1.69	0.16	**No violations**
3	Period 8 ns	125 MHz	**Default**	**- 0.24** (Violated MCA)	0.16	**No violations**
4	Period 8.4ns	119 MHz	**Default**	0.08	0.16	**No violations**
5	Period 8.3ns	120.5MHz (Highest Freq)	**Default**	**0.05**	0.16	**No violations**

Configurations used:

sky130A_sky130_fd_sc_hd_config.tcl - /home/opentools/OpenLane/designs/wbqspiflash/

File Edit Search Preferences Shell Macro Windows

lacement.tcl | README.md | sky130A_sky130_fd_sc_ | floorplan.tcl | cts.tcl | routing.tcl | synthesis.tcl

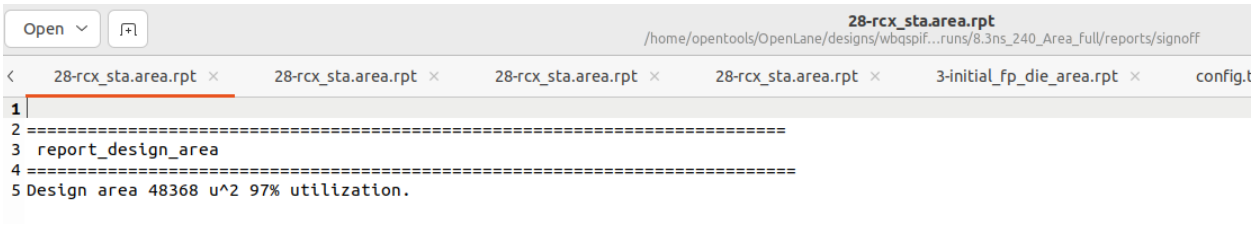
```
# SCL Configs
set ::env(CLOCK_PERIOD) "8.3"
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(FP_CORE_UTIL) 40
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]
#set ::env(PL_TARGET_DENSITY) 0.50

# Synth defaults
set ::env(SYNTH_BIN) yosys
set ::env(SYNTH_SCRIPT) $::env(SCRIPTS_DIR)/yosys/synth.tcl
set ::env(SYNTH_NO_FLAT) 0
set ::env(SYNTH_CLOCK_UNCERTAINITY) 0.10
set ::env(SYNTH_CLOCK_TRANSITION) 0.10
set ::env(SYNTH_TIMING_DERATE) 0.05
set ::env(SYNTH_CAP_LOAD) 5
set ::env(SYNTH_SHARE_RESOURCES) 1
set ::env(SYNTH_BUFFERING) 1
set ::env(SYNTH_SIZING) 1
set ::env(SYNTH_MAX_FANOUT) 30
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(SYNTH_ADDER_TYPE) "YOSYS"
set ::env(CLOCK_BUFFER_FANOUT) 16
set ::env(SYNTH_READ_BLACKBOX_LIB) 0
set ::env(SYNTH_TOP_LEVEL) 0
set ::env(SYNTH_FLAT_TOP) 0
set ::env(IO_PCT) 0.2

# floorplan
set ::env(FP_SIZING) relative
set ::env(FP_PDN_VOFFSET) 0
set ::env(FP_PDN_VPITCH) 40
set ::env(FP_PDN_HOFFSET) 0
set ::env(FP_PDN_HPITCH) 40
set ::env(FP_PDN_AUTO_ADJUST) 1
#set ::env(DIE_AREA) "0.0 0.0 240.0 240.0"

# placement (all other values are set to default)
set ::env(PL_TARGET_DENSITY) 0.45
set ::env(PL_ROUTABILITY_DRIVEN) 1
set ::env(PL_TIME_DRIVEN) 1

# cts (all other values are set to default)
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 200
set ::env(CTS_TOLERANCE) 100
set ::env(CTS_SINK_CLUSTERING_SIZE) 25
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 50

# Routing
set ::env(DRT_OPT_ITERS) 64

```

Trails to get min Area

Note: We will use the **max frequency (120.5MHz)** we got and try different die areas on it till we get the min area for this frequency.

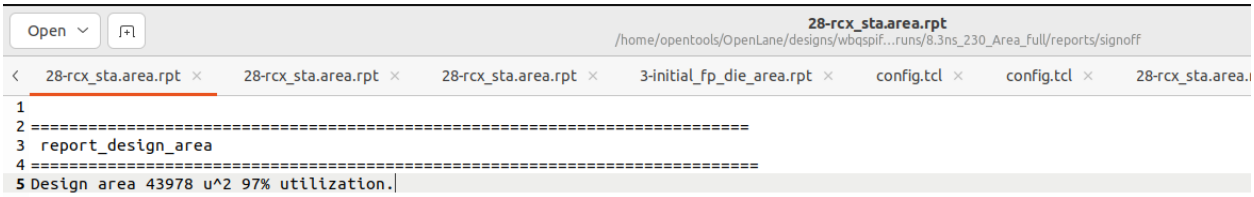
Note: I only have been changing the `DIE_AREA` and `PL_TARGET_DENSITY` in those trails, and I made the `FP_SIZING` to be **absolute** rather than **relative**

1. Trail #1 ("0.0 0.0 240.0 240.0", `DENSITY`: 0.45)



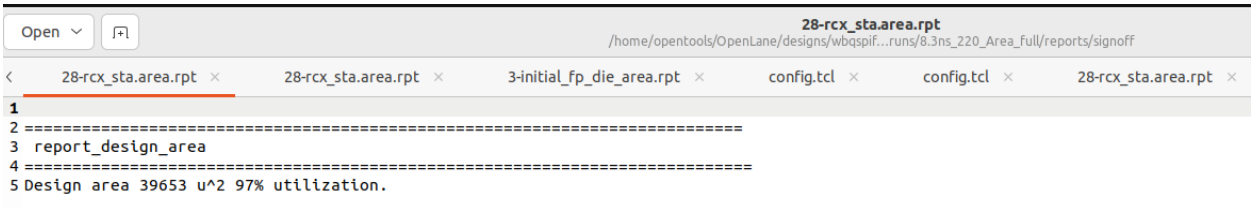
Flow success

2. Trail #2 ("0.0 0.0 230.0 230.0", `DENSITY`: 0.48)



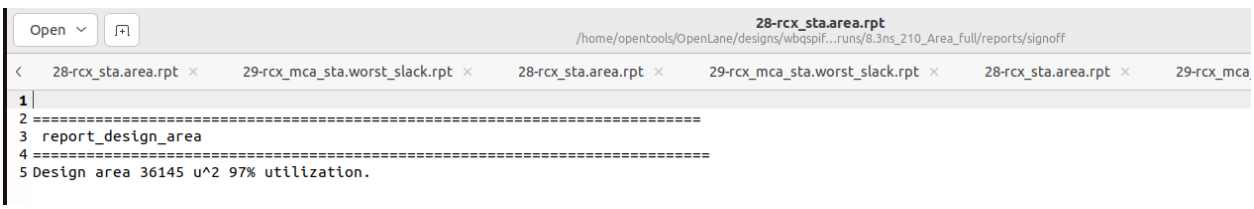
Flow success

3. Trail #3 ("0.0 0.0 220.0 220.0", `DENSITY`: 0.53)



Flow success

4. Trail #4 ("0.0 0.0 210.0 210.0", `DENSITY`: 0.58)



Flow success but violated setup in MCA

Summary Table:

TRIAL #	Changed Parameter	Frequency	Area	DRCs Count & Timing Violations
1	DIE_AREA PL_TARGET_DENSITY: 0.45	120.5MHz	"0.0 0.0 240.0 240.0" Signoff Area: 48368 u^2	**No violations**
2	DIE_AREA PL_TARGET_DENSITY: 0.48	120.5MHz	"0.0 0.0 230.0 230.0" Signoff Area: 43978 u^2	**No violations**
3	DIE_AREA PL_TARGET_DENSITY: 0.53	120.5MHz	"0.0 0.0 220.0 220.0" Signoff Area: 39653 u^2 **(Min AREA)**	**No violations**
4	DIE_AREA PL_TARGET_DENSITY: 0.58	120.5MHz	"0.0 0.0 210.0 210.0" Signoff Area: 36145 u^2	**No DRCs but setup violation (MCA)**

Configurations used:

NEdit "Nirvana Text Editor" Aug 24 03:52

sky130A_sky130_fd_sc_hd_config.tcl - /home/opentools/OpenLane/designs/wbqspiflash/

File Edit Search Preferences Shell Macro Windows

lacement.tcl | README.md | sky130A_sky130_fd_sc_ | floorplan.tcl | cts.tcl | routing.tcl | synthesis.tcl

```
# SCL Configs
set ::env(CLOCK_PERIOD) "8.3"
set ::env(SYNTH_STRATEGY) "AREA 0"
set ::env(FP_CORE_UTIL) 40
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]
#set ::env(PL_TARGET_DENSITY) 0.50

# Synth defaults
set ::env(SYNTH_BIN) yosys
set ::env(SYNTH_SCRIPT) $::env(SCRIPTS_DIR)/yosys/synth.tcl
set ::env(SYNTH_NO_FLAT) 0
set ::env(SYNTH_CLOCK_UNCERTAINITY) 0.10
set ::env(SYNTH_CLOCK_TRANSITION) 0.10
set ::env(SYNTH_TIMING_DERATE) 0.05
set ::env(SYNTH_CAP_LOAD) 5
set ::env(SYNTH_SHARE_RESOURCES) 1
set ::env(SYNTH_BUFFERING) 1
set ::env(SYNTH_SIZING) 1
set ::env(SYNTH_MAX_FANOUT) 30
set ::env(SYNTH_STRATEGY) "DELAY 0"
set ::env(SYNTH_ADDER_TYPE) "YOSYS"
set ::env(CLOCK_BUFFER_FANOUT) 16
set ::env(SYNTH_READ_BLACKBOX_LIB) 0
set ::env(SYNTH_TOP_LEVEL) 0
set ::env(SYNTH_FLAT_TOP) 0
set ::env(IO_PCT) 0.2

# floorplan
set ::env(FP_SIZING) absolute
set ::env(FP_PDN_VOFFSET) 0
set ::env(FP_PDN_VPITCH) 40
set ::env(FP_PDN_HOFFSET) 0
set ::env(FP_PDN_HPITCH) 40
set ::env(FP_PDN_AUTO_ADJUST) 1
set ::env(DIE_AREA) "0.0 0.0 210.0 210.0"


# placement (all other values are set to default)
set ::env(PL_TARGET_DENSITY) 0.58
set ::env(PL_ROUTABILITY_DRIVEN) 1
set ::env(PL_TIME_DRIVEN) 1

# cts (all other values are set to default)
set ::env(CLOCK_TREE_SYNTH) 1
set ::env(CTS_TARGET_SKEW) 200
set ::env(CTS_TOLERANCE) 100
set ::env(CTS_SINK_CLUSTERING_SIZE) 25
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) 50

# Routing
set ::env(DRT_OPT_ITERS) 64

```

Trails to get max Frequency with area threshold

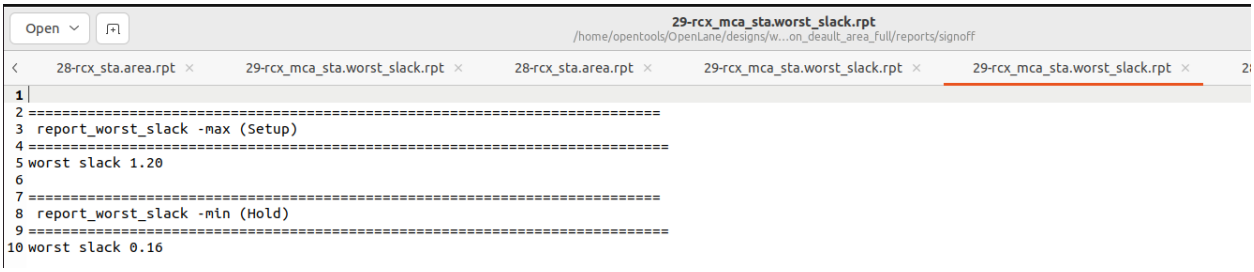
Now we need to get the **max frequency this design can handle**, so we will set an **area threshold** as to get the max frequency while our design area is smaller than this threshold

Let the **area threshold to be 50,000 u^2**, however this is a smaller threshold

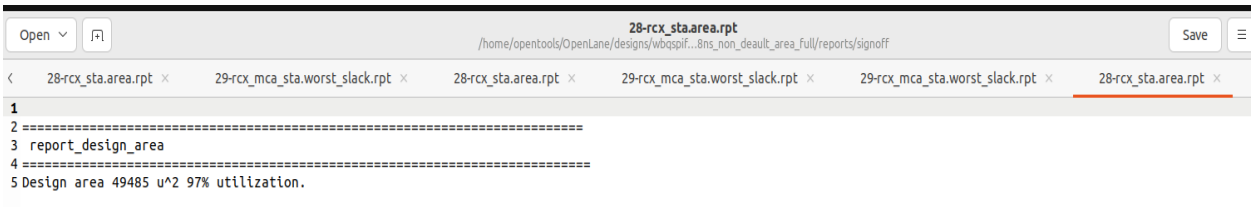
Note: I've been changing the configurations in every run so I will report the configs with with run

1. Trail #1 (8ns)

- **Slacks:**



- **Area:**

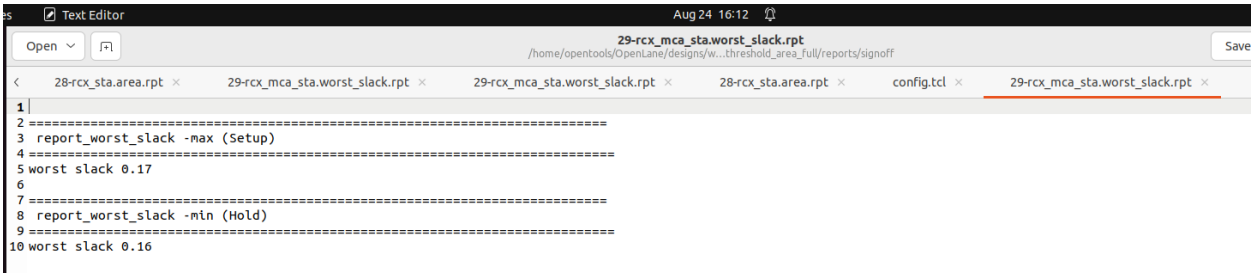


- **Configurations:**

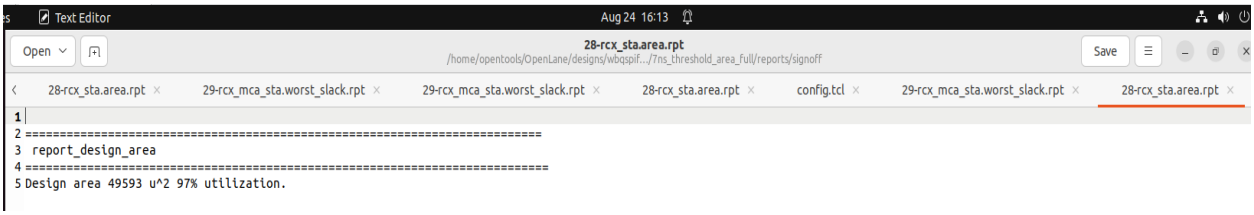
```
CLOCK_PERIOD "8"
PP_CORE_UTIL: 40
SYNTH_STRATEGY "AREA 3"
SYNTH_TIMING_DERATE 0.05
PL_TARGET_DENSITY: 0.45
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 100
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
Area is defaulted
```

2. Trail #2 (7ns)

- **Slacks:**



- **Area:**

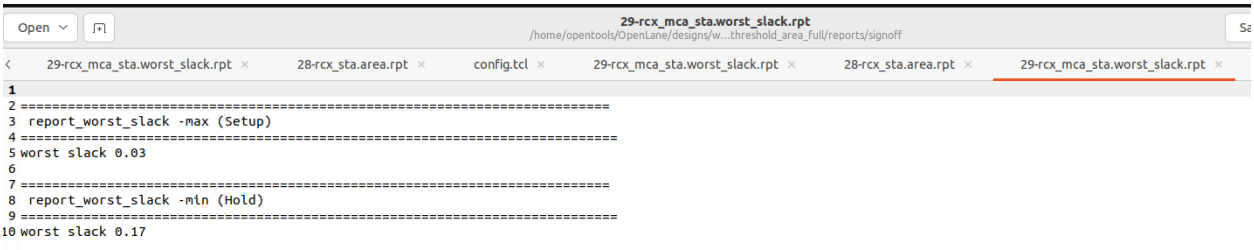


- **Configurations:**

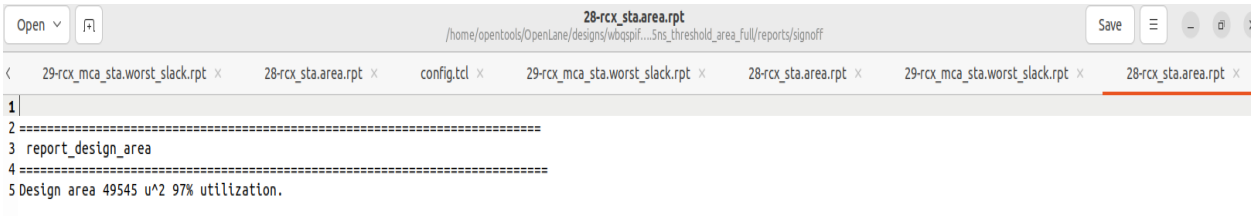
```
CLOCK_PERIOD "7"
PP_CORE_UTIL: 40
SYNTH_STRATEGY "AREA 3"
SYNTH_TIMING_DERATE 0.05
PL_TARGET_DENSITY: 0.45
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 100
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
Area is defaulted
```

3. Trail #3 (6.5ns)

- **Slacks:**



- **Area:**

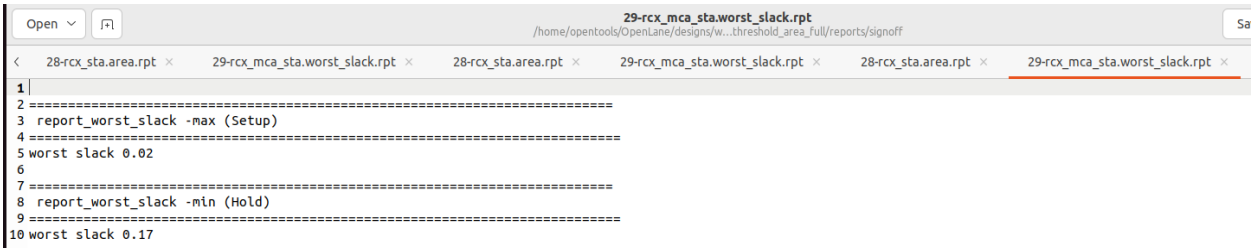


- **Configurations**

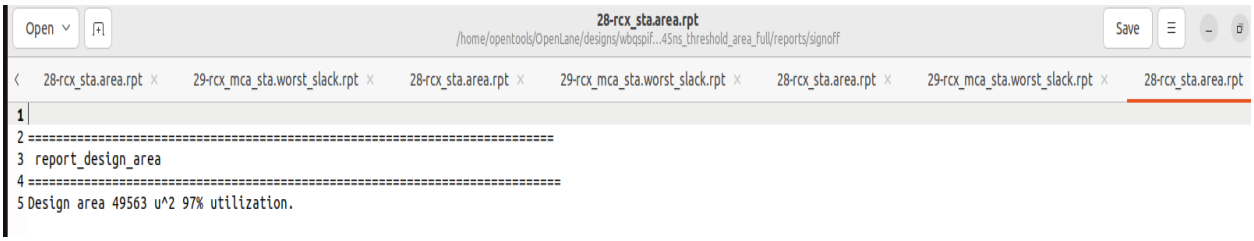
```
CLOCK_PERIOD "6.5"
PP_CORE_UTIL: 40
SYNTH_STRATEGY "AREA 3"
SYNTH_TIMING_DERATE 0.00
PL_TARGET_DENSITY: 0.45
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 100
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
Area is defaulted
```

4. Trail #4 (6.45ns)

- **Slacks:**



- **Area:**



- **Configurations:**

```
CLOCK_PERIOD "6.5"
PP_CORE_UTIL: 40
SYNTH_STRATEGY "AREA 3"
SYNTH_TIMING_DERATE 0.00
PL_TARGET_DENSITY: 0.45
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 100
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
Area is defaulted
```

Note: I tried many times to get a **lower clock period** but it always **violated the setup slack** in **Multiple Corner Analysis**

Summary Table:

TRIAL #	Clock Period	Frequency	Area	Timing Results (MCA Slacks)		DRCs Count
				Setup	Hold	
1	8 ns	125 MHz	Signoff Area: 49845 u^2	1.2	0.16	**No violations**
2	7 ns	142.8 MHz	Signoff Area: 49593 u^2	0.17	0.16	**No violations**
3	6.5 ns	153.8 MHz	Signoff Area: 49545 u^2	0.03	0.17	**No violations**
4	6.45 ns	155 MHz	Signoff Area: 49563 u^2	0.02	0.17	**No violations**

"Max Frequency design can handle"

Trails to get min Area with frequency threshold

We will do the same steps to **get the min area the design can work at**, but now we will set a **threshold for the frequency** and let that threshold to be **100 MHz (10 ns)** which is quite a **reasonable frequency threshold**

Note: the main parameters I'll be changing here are `PL_TARGET_DENSITY` and `FP_CORE_UTIL` as we will set `FP_SIZING` to be **relative**

Summary Table:

TRIAL #	Utilization & Target Density	Frequency threshold	Area	Timing Results (MCA Slacks)		DRCs Count
				Setup	Hold	
1	CORE_UTIL: 43 TARGET_DENSITY: 0.46	100 MHz	Signoff Area: 46054 u^2	3.38	0.18	No violations
2	CORE_UTIL: 45 TARGET_DENSITY: 0.5	100 MHz	Signoff Area: 43900 u^2	3.57	0.18	No violations
3	CORE_UTIL: 48 TARGET_DENSITY: 0.5	100 MHz	Signoff Area: 41411 u^2	3.55	0.18	No violations
4	CORE_UTIL: 52 TARGET_DENSITY: 0.55	100 MHz	Signoff Area: 38204 u^2	3.36	0.18	No violations
5	CORE_UTIL: 55 TARGET_DENSITY: 0.58	100 MHz	Signoff Area: 36030 u^2	2.7	0.18	No violations
6	"AREA 3" CORE_UTIL: 56 TARGET_DENSITY: 0.61	100 MHz	Signoff Area: 35105 u^2	1.3	0.18	No violations
7	"AREA 0" CORE_UTIL: 56 TARGET_DENSITY: 0.61	100 MHz	Signoff Area: 30638 u^2	0.89	0.18	**No violations**

"Min Area I could get for this frequency threshold"

I moved along the summary table as not to repeat the same steps again

Final Results

After performing multiple optimization iterations with different OpenLane configuration adjustments, the final implementation achieved:

- **Target Frequency:** **155 MHz** (Clock period ≈ **6.45 ns**)
- **Core Area:** **46,004 µm²**
- **Worst Slack (Setup, Multi-Corner Analysis):** **+0.03 ns**
- **Worst Slack (Hold, Multi-Corner Analysis):** **+0.17 ns**
- **Signoff Status:** Timing closure successfully achieved across all corners after signoff extraction.

This result was obtained after extensive tuning of synthesis, placement, and CTS parameters to balance **timing performance** and **area utilization**.

Reports:

- **Slacks in MCA**

Open

29-rcx_mca_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/w....45ns_min_area_full/reports/signoff

28-rcx_sta.area.rpt | 28-rcx_sta.area.rpt | 29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.worst_slack.rpt | drc.

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 0.03
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.17
```

- **Slacks in typical corner**

Open

28-rcx_sta.worst_slack.rpt
/home/opentools/OpenLane/designs/wbq.../6.45ns_min_area_full/reports/signoff

29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.area.rpt | 28-rcx_sta.area.rpt | 28-rcx_sta.worst_slack.rpt | 29-rcx_mca_sta.worst

```
1
2 ===========================================================================
3  report_worst_slack -max (Setup)
4 ===========================================================================
5 worst slack 3.00
6
7 ===========================================================================
8  report_worst_slack -min (Hold)
9 ===========================================================================
10 worst slack 0.34
```

- **Area after Signoff**

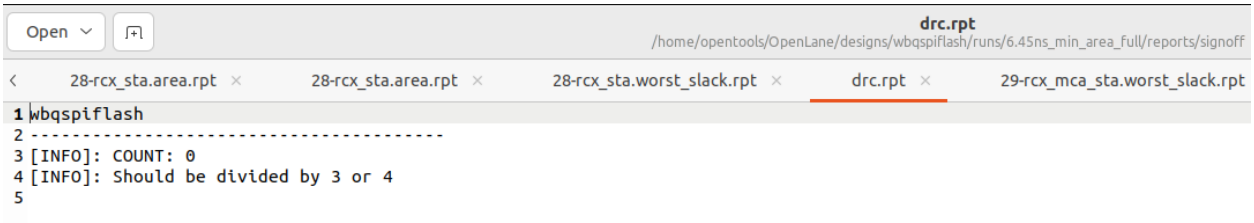
Open

28-rcx_sta.area.rpt
/home/opentools/OpenLane/designs/wbqspif...uns/6.45ns_min_area_full/reports/signoff

28-rcx_sta.area.rpt | 29-rcx_mca_sta.worst_slack.rpt | 28-rcx_sta.area.rpt | 28-rcx_sta.worst_slack.rpt | drc.rpt

```
1
2 ===========================================================================
3  report_design_area
4 ===========================================================================
5 Design area 46004 u^2 97% utilization.
```

- **DRCs count**



- **Configurations**

```
CLOCK_PERIOD "6.452"
PP_CORE_UTIL: 43
SYNTH_STRATEGY "AREA 3"
SYNTH_TIMING_DERATE 0.00
PL_TARGET_DENSITY: 0.46
CTS_TARGET_SKEW: 200
CTS_TOLERANCE: 100
CTS_SINK_CLUSTERING_SIZE:25
CTS_SINK_CLUSTERING_MAX_DIAMETER:50
Area is defaulted
```

- **Terminal**

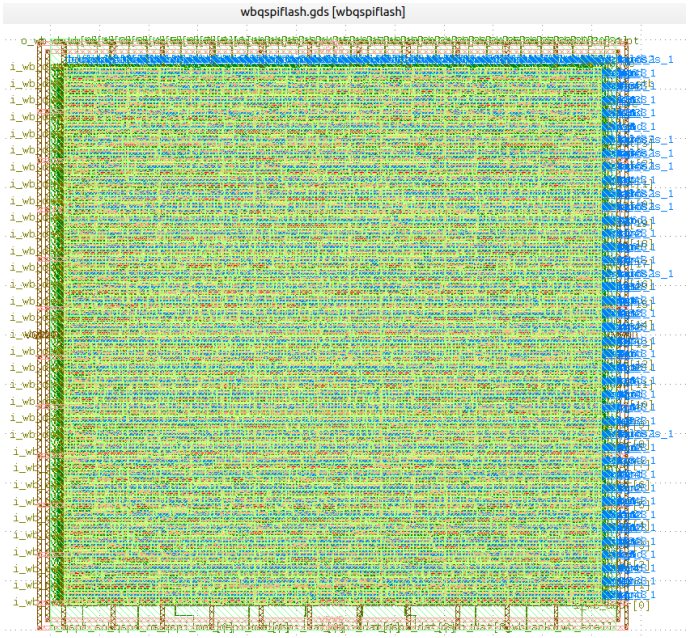
```
[STEP 38]
[INFO]: Running OpenROAD Antenna Rule Checker...
[INFO]: Saving current set of views in 'designs/wbqspiflash/runs/6.45ns_min_area
_full/results/final'...
[INFO]: Saving runtime environment...
[INFO]: Generating final set of reports...
[INFO]: Created manufacturability report at 'designs/wbqspiflash/runs/6.45ns_min
_area_full/reports/manufacturability.rpt'.
[INFO]: Created metrics report at 'designs/wbqspiflash/runs/6.45ns_min_area_full
/reports/metrics.csv'.
[INFO]: There are no max slew, max fanout or max capacitance violations in the d
esign at the typical corner.
[INFO]: There are no hold violations in the design at the typical corner.
[INFO]: There are no setup violations in the design at the typical corner.
[SUCCESS]: Flow complete.
icpedia@icpedia-virtual-machine:/home/opentools/OpenLane$
```

GDS and LEF

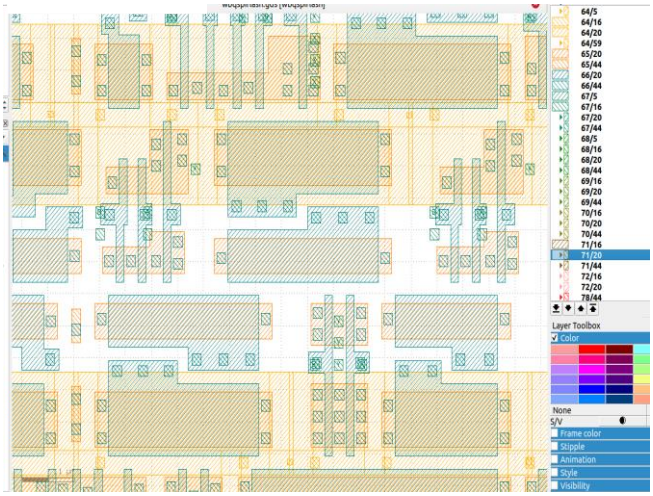
Required:

Open the final GDS and LEF of the design using Klayout and highlight the differences between them.

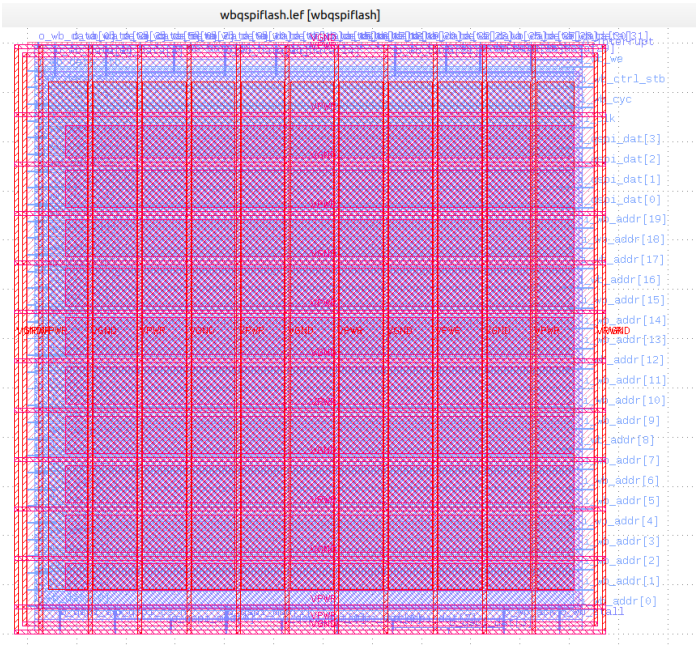
GDS File



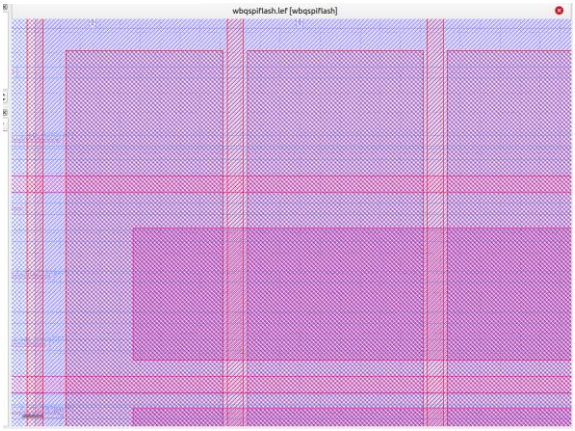
Closer look!



LEF File



Closer look!



Comparison

Aspect	LEF View	GDS View
Detail Level	**Abstract** (bounding boxes, pins)	**Full polygons and mask details**
Routing	No real routing (only blockages/tracks)	Actual wires and vias
Layers	Logical layers (abstract)	Complete layer stack
Use Case	Floorplanning and P&R guidance	Tapeout and fabrication
Size	Very small file	Large file with complete details

Required:

Using Klayout, validate the metals used for pins creation

Validation:

First, we want to know which metal layer is used for **vertical pins creation** and which is used for **horizontal pins creation** so we will go to this path**:** "/home/opentools/OpenLane/pdks/volare/sky130/versions/41c0908b47130d5675ff8484255b43f66463a7d6/sky130A/libs.tech/openlane", and here is what we got:

```
129 # I/O Layer info
130 set ::env(FP_IO_HLAYER) "met3"
131 set ::env(FP_IO_VLAYER) "met2"
```

- Metal 3 is used for horizontal pins creation (**all inputs**, remember the floorplan part at the beginning).
- Metal 2 is used for vertical pins creation (**all outputs**).

Second, we will go to **The PDK layer mapping (stream) file** is crucial because it **converts raw GDS layer numbers into meaningful process layers**, **ensures correct visualization in tools like KLayout**, **maintains consistency across design tools**, **and enables accurate DRC/LVS checks for proper tapeout**

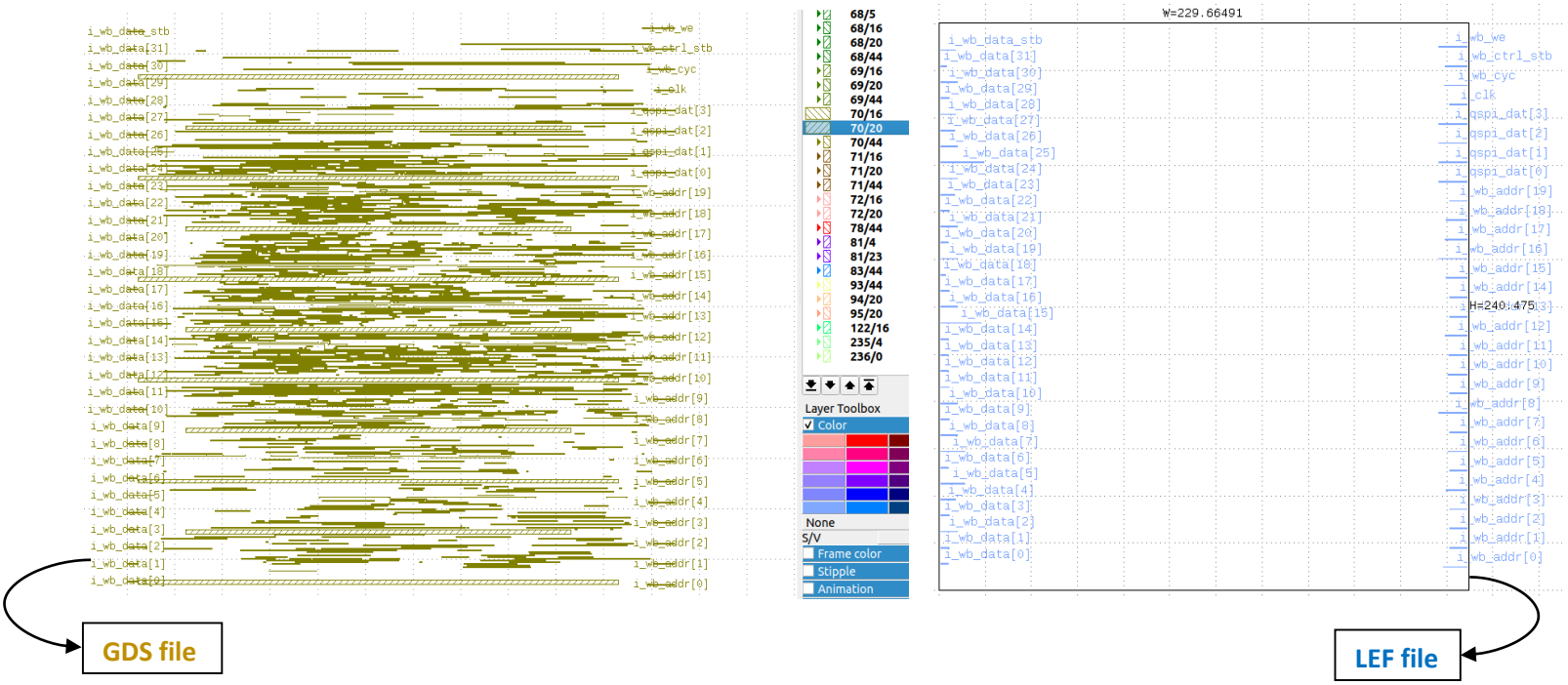
so we will go to this path**:**

"/home/opentools/OpenLane/pdks/volare/sky130/versions/41c0908b47130d5675ff8484255b43f66463a7d6/sky130A/libs.tech/klayout" and here is what we got:

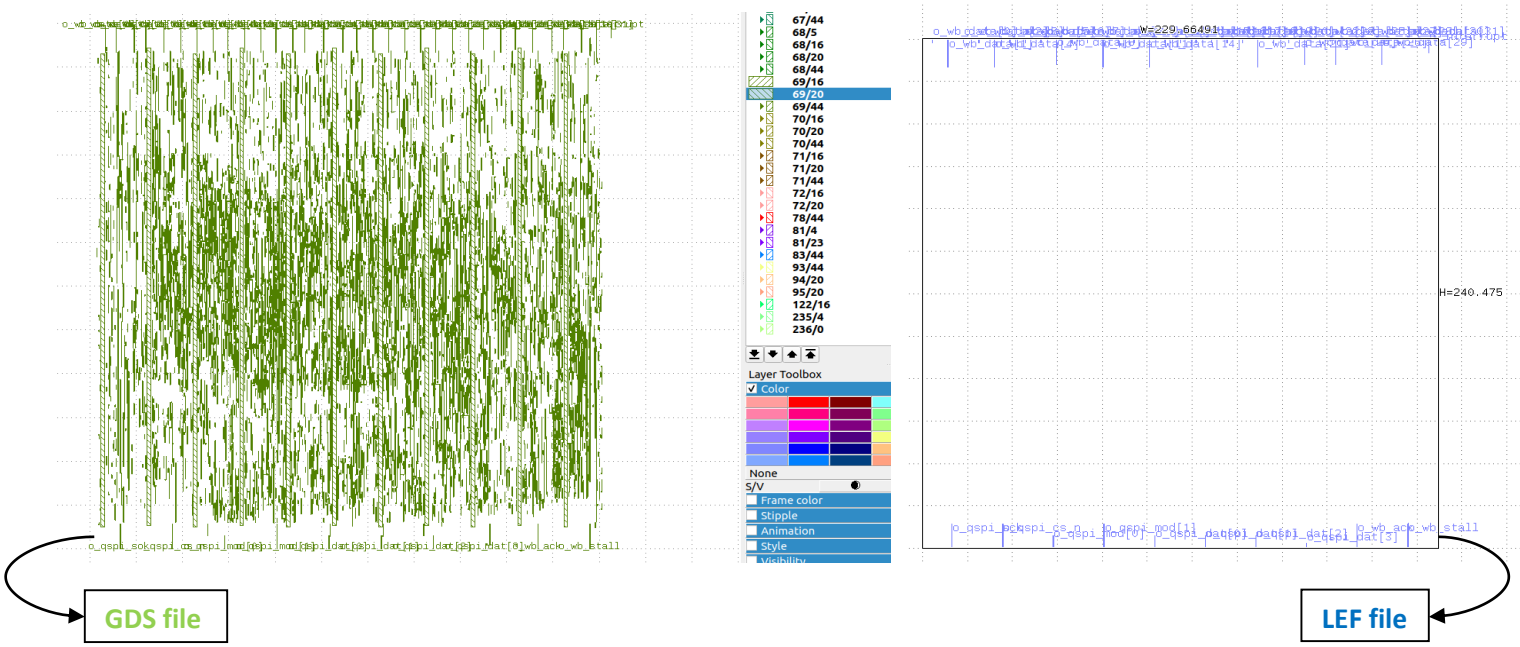
```
# layers definitions
#########################

# all except purpose (datatype) 5 -- label and 44 -- via
li_wildcard = "67/0-4,6-43,45-*"
mcon_wildcard = "67/44"

m1_wildcard = "68/0-4,6-43,45-*"
via_wildcard = "68/44"

m2_wildcard = "69/0-4,6-43,45-*"
via2_wildcard = "69/44"

m3_wildcard = "70/0-4,6-43,45-*"
via3_wildcard = "70/44"

m4_wildcard = "71/0-4,6-43,45-*"
via4_wildcard = "71/44"

m5_wildcard = "72/0-4,6-43,45-*"
```

- **Metal 2** has **layer no. 69** and has **datatypes of 0–4, 6–43, 45 and above.**
- **Metal 3** has **layer no. 70** and datatypes of **0–4, 6–43, 45 and above.**

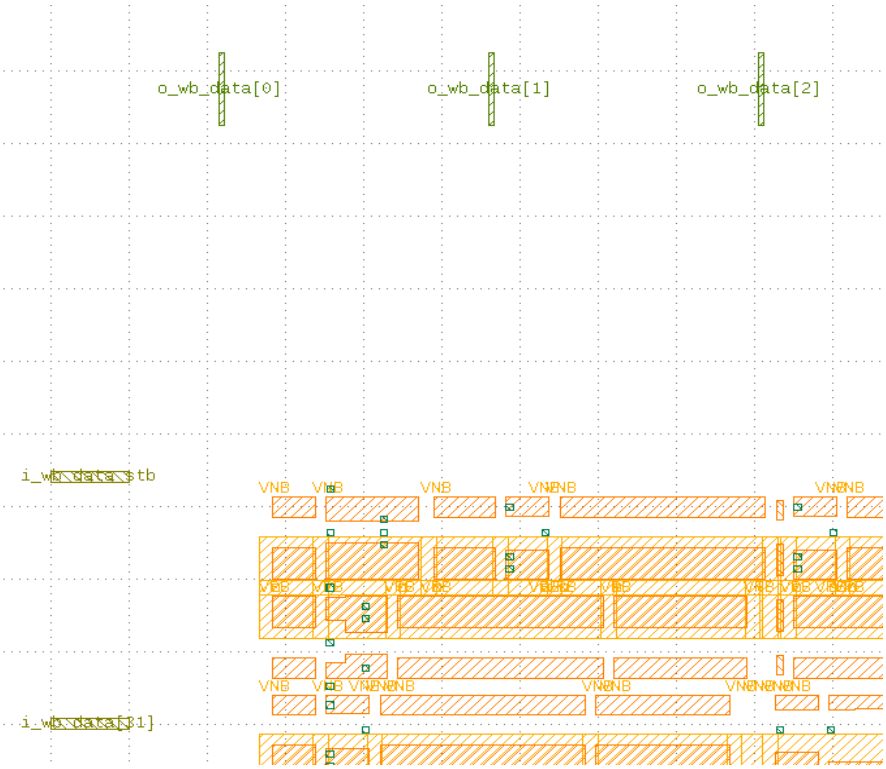
Metal 3 for input pins validation using **klayout (GDS & LEF)**:



Metal 2 for output pins validation using **klayout(GDS & LEF)**:



- Corner snapshot showing inputs and outputs for **metals 3** and **2:**



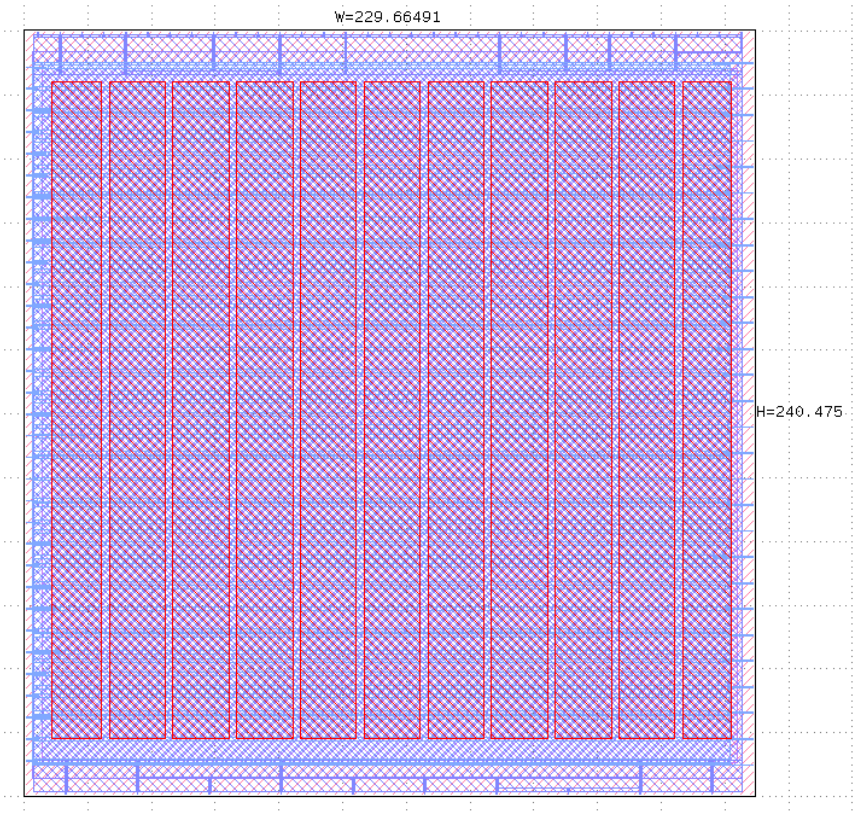
Required:

Validate that the LEF is created with the intended dimensions

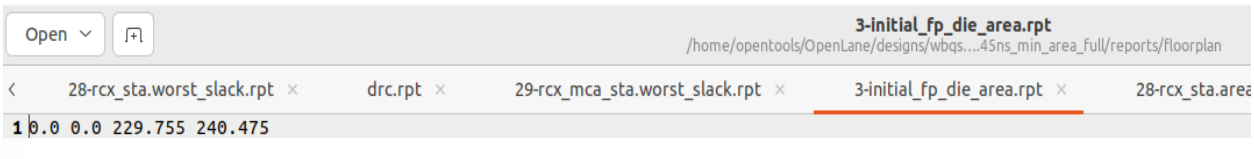
Validation:

We will get the dimensions of the **Die Area in LEF file** and **compare** it with the **Die Area dimensions in floorplan report**

1. LEF file Die Area dimensions:

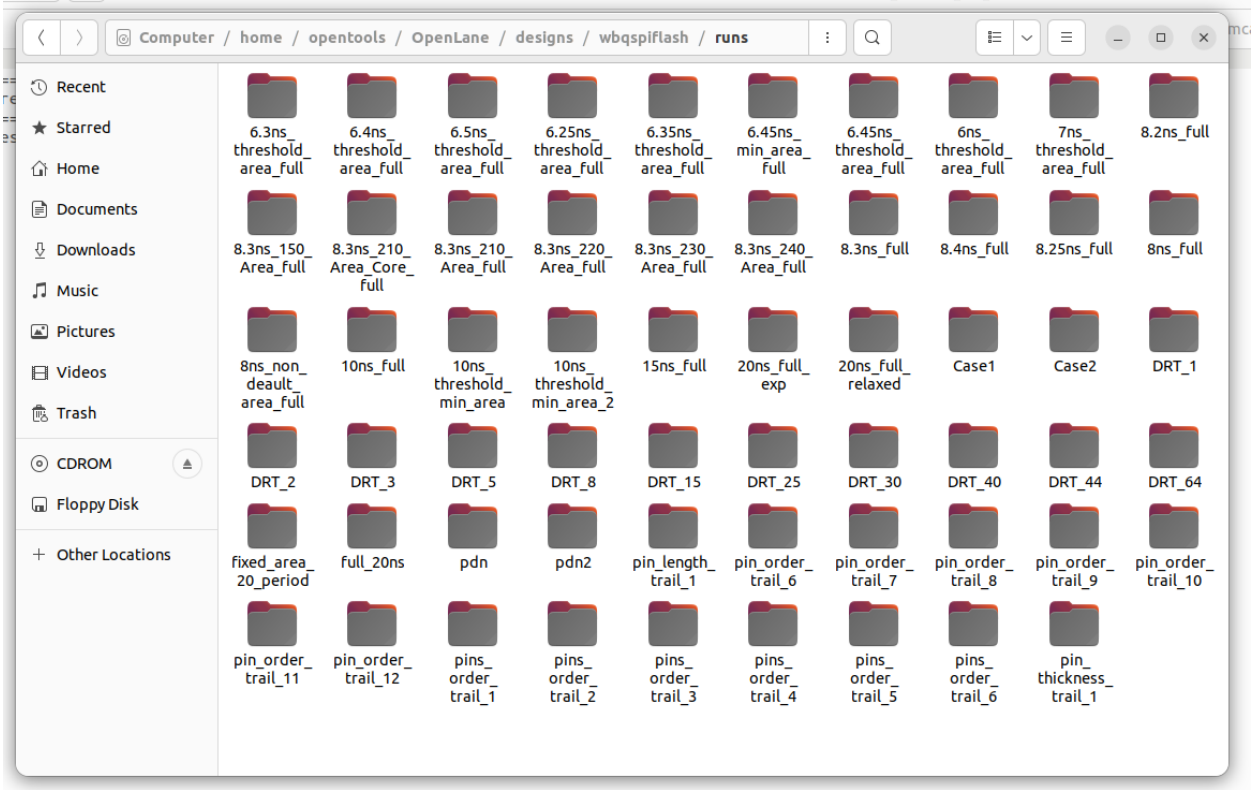


2. Floorplan Die Area Dimensions:



We notice that the Die Area dimensions in both are ***exactly matching each other!***

Documenting my effort:



All these runs and more but overwritten I've done in order to meet the requirements and specifications, also to get the Max Frequency and Min Area possible.

Check my GitHub Repository for the most important runs!

Thank you!