



DDS for 5G/6G Cellular Network Calibration and Ranging

Submitted by:

Ahmed Hossam Rafik

Ahmed Haitham Othman

Mohamed Ahmed Mohamed Hussein

Mohamed Adel Abdelrahem

Abdelrhman Khaled Fouad

Youssef Mohamed Mamdouh

Moustafa Saad Dawood

Supervised by:

Dr. Maged Ghoneima

Dr. Ahmed Mehana

ADI Team

Sponsorship:

Analog Devices, Inc

A Graduation Project submitted to the Faculty of Engineering at Ain Shams University
in partial fulfillment of the requirements for the degree of B.Sc. in
Electronics and Electrical Communications Engineering

January 26, 2026

Abstract

This graduation project explores the design and implementation of a Direct Digital Synthesis (DDS)-based waveform generation and correlation system for 5G/6G cellular network calibration and ranging within an Integrated Sensing and Communication (ISAC) framework. The project bridges high-level ISAC concepts with practical digital hardware realization, focusing on waveform design, system architecture, and implementation strategies. Through comprehensive analysis and simulation, we demonstrate the feasibility of using programmable DDS architectures to support joint communication and sensing functionalities in next-generation wireless networks.

Contents

1	Introduction	6
1.1	Background and Motivation	6
1.2	Evolution of Wireless Networks Toward ISAC	7
1.3	ISAC Waveform Design Considerations	7
1.4	Role of Direct Digital Synthesis (DDS)	8
1.5	Project Objectives	8
1.6	System Architecture Overview	9
1.7	Methodology and Implementation Approach	9
1.8	Significance and Expected Contributions	10
1.9	ISAC Transceiver Functional Diagram	10
1.9.1	TX Path Components	10
1.9.2	RX Path Components	11
2	Wireless Channels	12
2.1	Multipath Propagation	12
2.2	Fading	13
2.3	Doppler Effect	13
2.4	Parameters of Mobile Multipath Channels	13
2.5	Summary	13
3	Orthogonal Frequency Division Multiplexing (OFDM)	14
3.1	Motivation for OFDM	14
3.2	Basic Principle of OFDM	14
3.3	Orthogonality of Subcarriers	15
3.4	Transmission in Multi-Carrier Modulation (MCM)	15
3.5	IFFT and FFT Implementation	16

3.6 Cyclic Prefix (CP)	17
3.6.1 Cyclic Prefix Overhead	17
3.7 Symbol and Slot Durations	17
3.8 Pilot Tones and Preambles	19
3.8.1 Pilot Tones	19
3.8.2 Preambles	20
3.9 Receiver Operation	20
3.10 Advantages of OFDM	21
3.11 Disadvantages of OFDM	21
4 Reference Parameters	22
5 5G Frame Structure and Numerology	27
5.1 Frequency Range of FR2	27
5.2 Time – Frequency Grid in OFDM	27
5.3 5G Frame Structure	28
6 MATLAB Simulation	32
6.1 Rayleigh Only Channel	32
6.2 AWGN (thermal noise) Only Channel	36
6.3 Comparison and Combined Results	40
6.4 Theoretical Verification	42
7 Direct Digital Synthesis (DDS)	44
7.1 Fundamentals of DDS Technology	44
7.2 Understanding the Sampled Output of a DDS Device	48
7.3 Frequency/phase-hopping Capability of DDS	50
7.4 The Effect of DAC Resolution on Spurious Performance	50
7.4.1 DAC Resolution and Quantization Distortion	50
7.4.2 Effect of Output Level (Not Full-Scale Operation)	51
7.4.3 Oversampling and Its Effect on SQR	51

7.4.4	Phase Truncation and Spurious Performance (DDS-specific)	52
7.4.5	Phase Truncation Spur Magnitude	52
7.4.6	Tuning Words and Spur Severity	54
7.4.7	Detailed Summary: Phase Truncation and Truncation Word Behavior	56
7.4.8	What Are Spurs?	59
7.4.9	Jitter and Phase Noise Considerations in a DDS System	61
7.4.10	Output Filtering Considerations	63
7.4.11	Reference Clock Considerations	65
7.4.12	DDS SFDR Performance	68
8	FFT Implementation for OFDM + Chirp Sensing	69
8.1	FFT Introduction	69
8.2	FFT Overview	70
8.2.1	Fast Fourier Transform (FFT)	70
8.3	The Butterfly Operation	70
8.3.1	Types of Butterflies	71
8.4	DIT vs. DIF FFT	71
8.4.1	Decimation in Time (DIT)	71
8.4.2	Decimation in Frequency (DIF)	71
8.4.3	Comparison Table	72
8.5	FFT Hardware Architecture Types	74
8.5.1	Fixed Data Point FFT (Fixed-Length)	74
8.5.2	Variable Data Point FFT (Reconfigurable)	74
8.6	Radix-2 vs. Radix-4 FFT	74
8.6.1	Radix-2 FFT	74
8.6.2	Radix-4 FFT	75
8.7	Serial vs. Parallel Architectures	75
8.7.1	Parallel FFT	75
8.7.2	Serial FFT (Pipeline FFT)	76
8.8	FFT in OFDM and Chirp Sensing	77

8.8.1	FFT in OFDM	77
8.8.2	FFT for Chirp Sensing	77
8.9	IFFT for OFDM System	78
8.10	Summary for Our Project	80
8.10.1	Architecture Comparison	81
8.11	MATLAB Reference Model Results	82
8.11.1	Performance Metrics	84
9	Signal Processing Simulations	86
9.1	Signal Placement Strategies	86
9.2	DDS TOOL	87
9.2.1	Single Tone Generation	87
9.2.2	Different Filter Responses	89
9.3	LFM Signal "Chirp"	90
9.3.1	1. Theory: Why LFM Radar Can Measure Distance	90
9.3.2	2. Why LFM (Linear Frequency Modulated) Signals Are Used . .	90
9.3.3	Signal Model Used in Simulation	91
9.3.4	Figure-by-Figure Explanation	91
9.3.5	Results with RF-2 related parameters	97
9.4	OFDM + Chirp (Different Timeslots) Simulation	100
9.5	FDM Technique: OFDM + LFM (No-overlapping)	103
9.5.1	1. Objective	103
9.5.2	2. System Design	103
9.5.3	3. Guard Band Analysis	103
9.5.4	Results and Visualization	104
10	Conclusion	111
10.1	Key Achievements	112
10.2	Future Work	112

Chapter 1

Introduction

1.1 Background and Motivation

Wireless cellular communication systems have undergone continuous and rapid evolution over the past decades, driven by the ever-increasing demand for higher data rates, lower latency, improved reliability, and seamless connectivity. While early generations of cellular networks were primarily designed to support voice communication, modern systems such as 4G LTE and 5G New Radio (NR) have expanded their scope to include high-speed data services, multimedia streaming, and massive device connectivity. The upcoming sixth generation (6G) of wireless networks is expected to further extend these capabilities by integrating communication with sensing, localization, and environmental awareness.

One of the most significant challenges in modern and future cellular networks is the efficient utilization of available spectrum and hardware resources while meeting stringent performance requirements. To address this challenge, next-generation systems operate across a wide range of frequency bands, including sub-6 GHz, mid-band frequencies between 7–15 GHz, millimeter-wave bands from 24–43 GHz, and even frequencies beyond 60 GHz. In parallel, the number of antenna elements deployed at base stations has increased dramatically, ranging from a few elements in legacy systems to hundreds or even thousands of elements in massive multiple-input multiple-output (MIMO) configurations. These advancements enable high spectral efficiency and beamforming gains but also significantly increase system complexity.

In addition to communication performance, future networks are expected to provide spatial awareness capabilities such as ranging, localization, and environmental mapping. These features are essential for emerging applications including autonomous vehicles, intelligent transportation systems, smart cities, industrial automation, and augmented or virtual reality. As a result, sensing is no longer viewed as a separate function but rather as an integral component of the wireless network itself.

1.2 Evolution of Wireless Networks Toward ISAC

Traditional cellular networks were designed with a clear separation between communication and sensing functionalities. Communication systems focused on delivering data reliably between users and base stations, while sensing and radar systems operated independently using dedicated hardware, spectrum, and signal processing techniques. This separation led to inefficient use of resources and increased deployment costs.

Integrated Sensing and Communication (ISAC) has emerged as a promising paradigm to overcome these limitations. ISAC aims to use a unified wireless infrastructure to simultaneously support data communication and sensing tasks. By sharing spectrum, hardware components, and signal processing algorithms, ISAC improves spectral efficiency, reduces hardware redundancy, and enables new intelligent network services.

In 5G and especially 6G networks, ISAC plays a critical role in enabling ultra-reliable low-latency communication (URLLC) and high-precision localization. Accurate ranging information can be used to optimize beamforming, manage handovers, enhance interference mitigation, and support context-aware network control. Consequently, ISAC is considered a key enabler for future wireless systems rather than an optional feature.

1.3 ISAC Waveform Design Considerations

A fundamental aspect of ISAC system design is the selection of suitable waveforms that can efficiently support both communication and sensing requirements. Communication systems typically prioritize high spectral efficiency, robustness to interference, and compatibility with existing standards, while sensing systems emphasize high range resolution, accurate time delay estimation, and good autocorrelation properties.

Several waveform options have been proposed for ISAC, including orthogonal frequency-division multiplexing (OFDM)-based waveforms, linear frequency modulated (LFM) or chirp-based waveforms, and hybrid waveform designs. OFDM is widely used in 4G and 5G systems due to its robustness against multipath fading and efficient implementation. However, its sensing performance may be limited without additional processing. LFM-based waveforms, on the other hand, offer excellent ranging and resolution characteristics but may require more complex integration with communication payloads.

Hybrid and jointly designed waveforms attempt to combine the advantages of both approaches by embedding sensing information within communication signals or superimposing sensing and communication waveforms in the time or frequency domain. Each option presents trade-offs in terms of performance, implementation complexity, and hard-

ware requirements. Therefore, a flexible waveform generation mechanism is essential to explore and evaluate different ISAC signaling strategies.

1.4 Role of Direct Digital Synthesis (DDS)

Direct Digital Synthesis (DDS) is a digital technique used to generate precise and programmable waveforms from a reference clock source. A typical DDS architecture consists of a phase accumulator, a phase-to-amplitude converter, and a digital-to-analog converter (DAC). By digitally controlling the phase increment, DDS can generate a wide range of frequencies with fine resolution and fast switching capability.

DDS offers several advantages that make it particularly suitable for ISAC applications. First, it provides excellent frequency agility and phase coherence, which are critical for calibration, synchronization, and ranging. Second, DDS-based systems are highly programmable, allowing dynamic reconfiguration of waveform parameters such as frequency, bandwidth, and modulation type. Third, DDS can be efficiently implemented in digital hardware platforms such as field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs).

In the context of 5G and 6G networks, DDS can be used to generate calibration signals, communication payloads, and sensing waveforms using a unified digital engine. This makes DDS a powerful building block for low-physical-layer and digital front-end (DFE) architectures that support ISAC functionality.

1.5 Project Objectives

The primary objective of this graduation project is to design and implement a **DDS-based waveform generation and correlation system** for 5G/6G cellular network calibration and ranging within an ISAC framework. The project aims to bridge the gap between high-level ISAC concepts and practical digital hardware realization.

The specific objectives of the project include:

- Understanding the fundamental principles and application scenarios of integrated sensing and communication in modern and future cellular networks.
- Studying and comparing different ISAC waveform options in terms of sensing performance, communication efficiency, and implementation complexity.
- Designing a DDS-based waveform generator capable of producing wideband signals suitable for 5G/6G ISAC applications.

- Implementing correlation and processing blocks required for ranging and sensing functionality.
- Verifying system-level performance using MATLAB simulations.
- Implementing and validating the proposed design using Verilog and/or SystemVerilog on an FPGA platform, with consideration for ASIC prototyping.

1.6 System Architecture Overview

The proposed system follows a functional architecture that integrates waveform generation, transmission, reception, and signal processing within an ISAC-enabled transceiver. At the transmitter side, the DDS engine generates programmable waveforms occupying bandwidths ranging from 100 MHz up to 1600 MHz or higher. These waveforms can be configured for communication, sensing, or joint operation.

At the receiver side, the incoming signals are processed using correlation and detection algorithms to extract both communication data and sensing information such as time delay and range estimates. The use of a common DDS-based architecture ensures phase coherence and timing accuracy between transmitted and received signals, which is essential for precise ranging.

The system architecture is evaluated at the algorithmic level using high-level simulation tools and then mapped to digital hardware blocks suitable for FPGA implementation. This approach allows early validation of performance while ensuring hardware feasibility.

1.7 Methodology and Implementation Approach

The project adopts a structured design methodology that combines theoretical analysis, system-level simulation, and hardware implementation. Initially, mathematical models and algorithms for DDS waveform generation and correlation are developed and verified using MATLAB Simulations. These simulations provide insight into key performance metrics such as bandwidth, resolution, and ranging accuracy.

Following system-level verification, the design is translated into hardware description language (HDL) code using Verilog. The implementation targets FPGA platforms, enabling real-time operation and hardware validation. Special attention is given to resource utilization, timing constraints, and scalability to support future extensions.

1.8 Significance and Expected Contributions

This project contributes to the growing research and development efforts in integrated sensing and communication for 5G and 6G networks. By demonstrating a DDS-based ISAC waveform generation and processing system, the project highlights the feasibility of using programmable digital architectures to support joint communication and sensing functionalities.

The outcomes of this work are expected to provide valuable insights into ISAC waveform design, DDS-based implementation strategies, and FPGA realization of wideband digital front-end systems. These contributions are relevant to both academic research and practical development of next-generation wireless communication systems.

1.9 ISAC Transceiver Functional Diagram

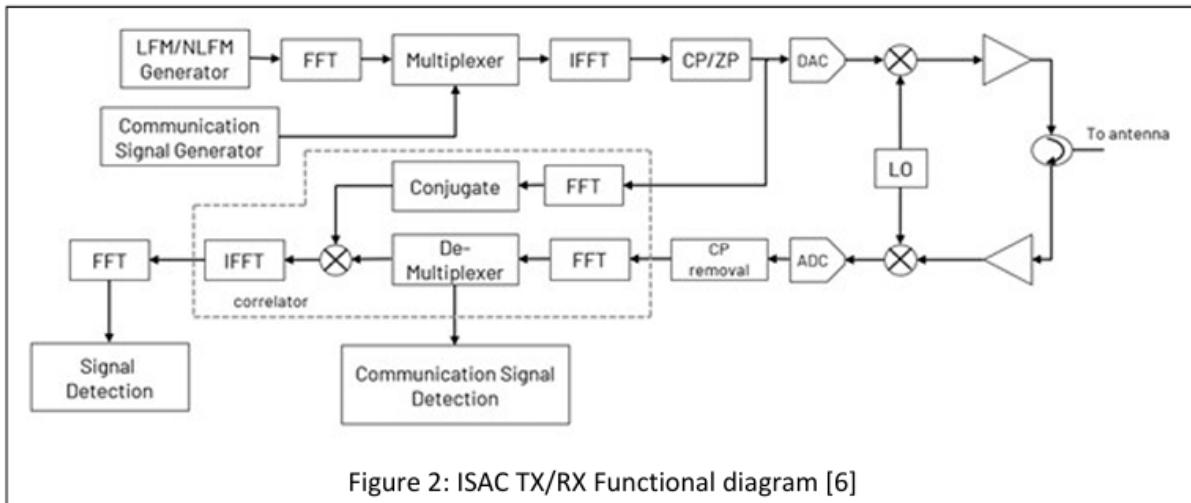


Figure 2: ISAC TX/RX Functional diagram [6]

Figure 1.1: ISAC Transmitter and Receiver Functional Diagram

1.9.1 TX Path Components

- **LFM/NLFM Generator (for sensing):** The provided DDS block is the core component of the LFM/NLFM generator. A control logic generates a linear ramp which is fed as the input to the phase accumulator. This ramp is the "Tuning Word" that makes the output frequency sweep over time.
- **Communication Signal Generator:** This block generates the payload data. It encodes and modulates this data onto the subcarriers of an OFDM symbol in the frequency domain.

- **IFFT:** Converts frequency domain signals to time domain.
- **Guard Interval (CP/ZP):** A guard interval is added to the beginning of each time-domain symbol.
- **DAC:** Digital-to-Analog Converter converts the digital signal to an analog signal which is then up-converted to radio frequency (RF) and transmitted through the antenna.

1.9.2 RX Path Components

- **Analog-to-Digital Conversion (ADC):** Converts the received analog signal back to digital format.
- **Remove Guard Interval (CP Removal):** Removes the cyclic prefix or zero padding added at the transmitter.
- **Fast Fourier Transform (FFT):** Transforms the signal from time domain to frequency domain.
- **De-Mux:** Used for:
 1. **Signal Detection:** This block analyzes the correlator's output. For communication, it decides which bits were sent based on the demodulated signal.
 2. **Sensing Signal (Echo):** It is sent to the Correlator. The correlator acts as a matched filter. It compares the received signal with a pristine, locally stored copy of the original transmitted chirp. The precise time delay (Δt) of the peak corresponds to the total travel time of the signal. Since the signal traveled to the target and back, the distance (d) to the target is calculated as:

$$d = \frac{c \cdot \Delta t}{2}$$

where c is the speed of light.

Chapter 2

Wireless Channels

The technical challenges of wireless communications systems:

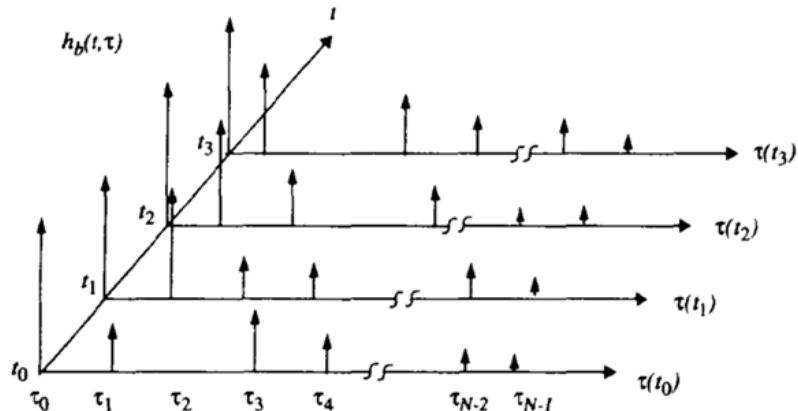
- Multipath propagation: the transmit signal reaches the receiver via different paths.
- Spectrum limitations – Frequency reuse.
- Energy limitations.
- User mobility \Rightarrow Handover and the need for HLR / VLR.

Let's take a dive in the problems.

2.1 Multipath Propagation

Each multipath component has a distinct amplitude, delay, direction of departure, direction of arrival, and phase shift.

ISI adds extra samples equal to the number of channel paths minus one, causing overlap with the next symbol. This is handled in OFDM using the cyclic prefix.



An example of the time-varying discrete-time impulse response model for a multipath radio channel.

2.2 Fading

Small-scale fading: Caused by multipath interference resulting in rapid signal fluctuations.

Large-scale fading: Caused by shadowing from large obstacles, leading to slow signal variations.

2.3 Doppler Effect

Occurs due to transmitter or receiver motion causing a frequency shift:

$$f_d = \frac{v}{\lambda} \quad (2.1)$$

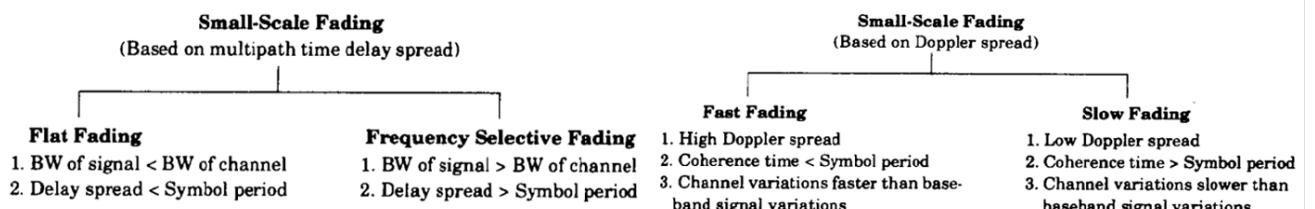
The maximum Doppler shift typically ranges from 1 Hz to 1 kHz.

2.4 Parameters of Mobile Multipath Channels

1. RMS delay spread S_τ
2. Coherence bandwidth B_{coh}
3. Doppler spread B_D
4. Coherence time T_{coh}

2.5 Summary

- Delay spread causes frequency-selective fading.
- Doppler spread causes time-selective fading.



Chapter 3

Orthogonal Frequency Division Multiplexing (OFDM)

3.1 Motivation for OFDM

Modern wireless systems require very high data rates, which necessitate the use of wide transmission bandwidths. As bandwidth increases, the symbol duration becomes very small compared to the channel delay spread:

$$T_{sym} \ll T_{delay}$$

This causes severe Inter-Symbol Interference (ISI), especially in multipath channels.

To overcome this problem, OFDM divides the high-rate data stream into multiple low-rate parallel streams, each transmitted over a narrowband subcarrier.

3.2 Basic Principle of OFDM

OFDM is a multi-carrier modulation technique where the available bandwidth is divided into N closely spaced orthogonal subcarriers.

$$BW_{sub} = \frac{B}{N}$$

As a result, the symbol duration of each subcarrier becomes:

$$T_{sym} \gg T_{delay}$$

This significantly reduces ISI and simplifies equalization.

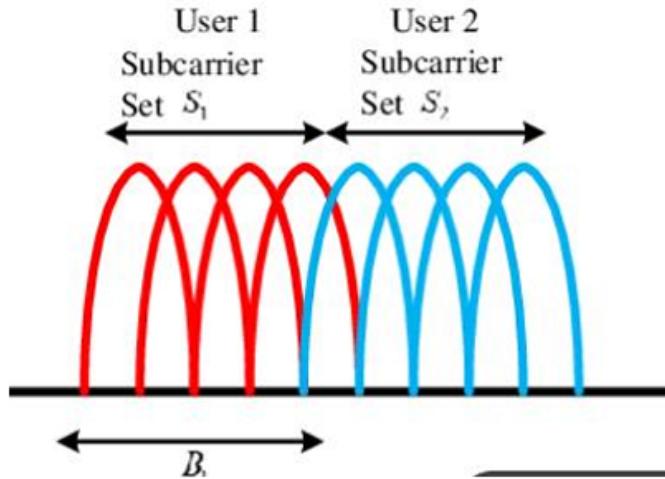


Figure 3.1: Division of bandwidth into orthogonal subcarriers

3.3 Orthogonality of Subcarriers

The key feature of OFDM is the orthogonality between subcarriers. Even though subcarriers overlap in frequency, they do not interfere with each other.

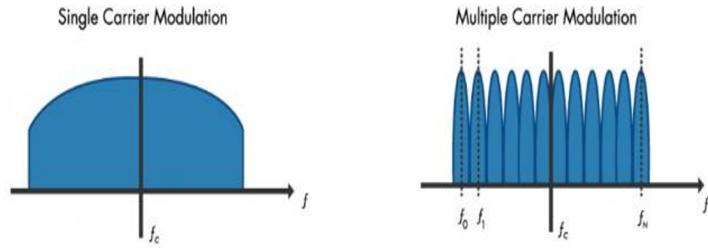
Mathematically, orthogonality is achieved when:

$$\int_0^T e^{j2\pi f_k t} e^{-j2\pi f_m t} dt = 0 \quad \text{for } k \neq m$$

This allows efficient spectrum utilization without inter-carrier interference (ICI).

3.4 Transmission in Multi-Carrier Modulation (MCM)

- The serial data stream is converted into parallel streams.
- Each stream modulates a different subcarrier.
- Subcarrier spacing is chosen as $\Delta f = \frac{1}{T}$.
- The k th subcarrier is centered at frequency $k\Delta f$.
- X_k represents the complex data symbol modulating the k th subcarrier.



3.5 IFFT and FFT Implementation

Instead of using multiple oscillators and modulators, OFDM uses IFFT and FFT blocks.

The discrete-time OFDM signal is given by:

$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{j2\pi kn/N} \quad (3.1)$$

- IFFT converts frequency-domain symbols into time-domain signal.
- FFT at the receiver recovers the transmitted symbols.
- This reduces system complexity and ensures orthogonality.

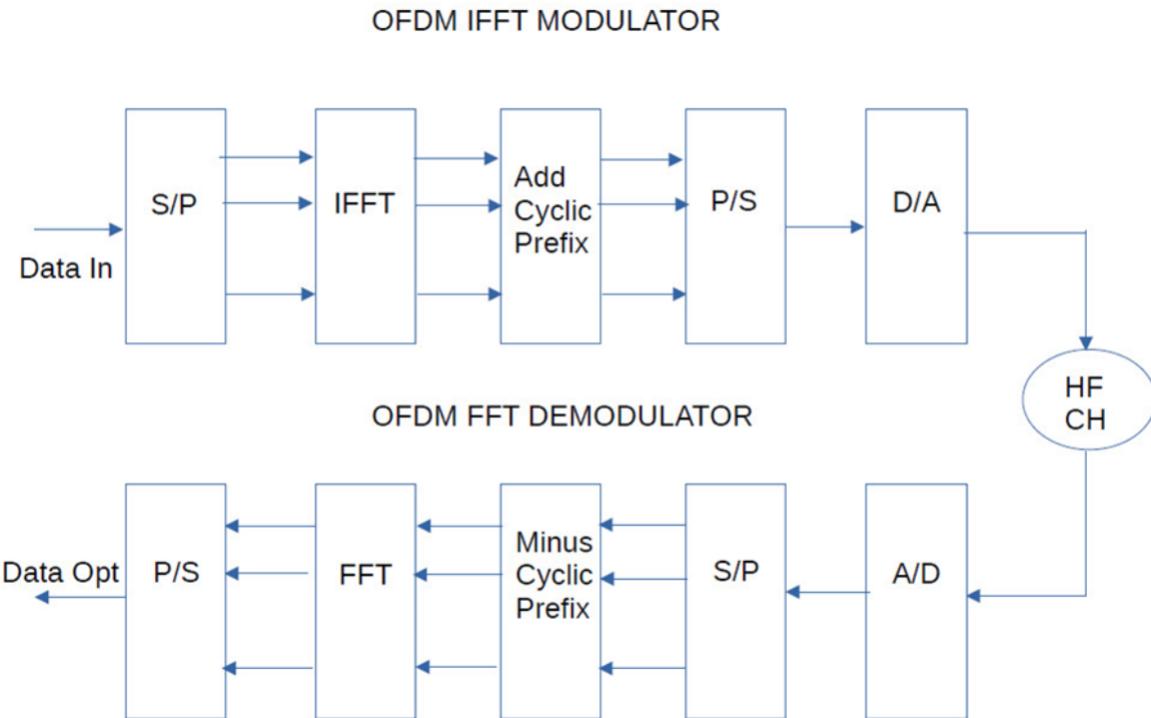


Figure 3.2: FFT/IFFT processing in OFDM

3.6 Cyclic Prefix (CP)

Multipath propagation causes delayed replicas of the transmitted signal, leading to ISI.

To eliminate ISI, a cyclic prefix is added by copying the last part of the OFDM symbol and appending it to the beginning.

- CP length is chosen longer than the maximum channel delay spread.
- Converts linear convolution into circular convolution.
- Preserves subcarrier orthogonality.

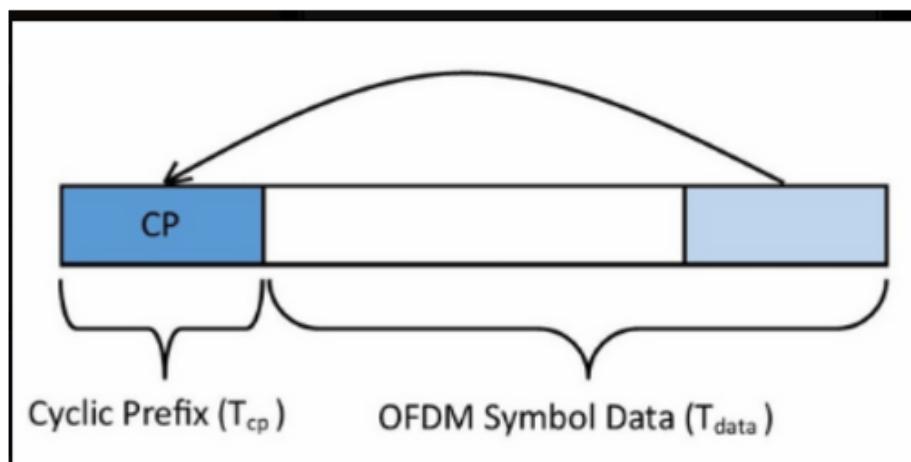


Figure 3.3: Cyclic prefix insertion

3.6.1 Cyclic Prefix Overhead

Although CP improves performance, it introduces overhead:

- Reduces spectral efficiency.
- Longer CP provides better ISI protection but wastes bandwidth.

3.7 Symbol and Slot Durations

In OFDM-based systems, the symbol duration is inversely proportional to the subcarrier spacing (SCS). Increasing the SCS reduces the symbol duration, which improves robustness against phase noise and Doppler effects, especially in high-frequency bands such as FR2.

The useful OFDM symbol duration is given by:

$$T_u = \frac{1}{\Delta f}$$

where Δf is the subcarrier spacing.

The total OFDM symbol duration includes the cyclic prefix:

$$T_{sym} = T_u + T_{CP}$$

In 5G NR, different numerologies are defined by scaling the subcarrier spacing as:

$$\Delta f = 15 \times 2^\mu \text{ kHz}$$

where μ is the numerology index.

- Larger SCS \Rightarrow shorter symbol duration.
- Smaller SCS \Rightarrow longer symbol duration and better frequency resolution.

A slot consists of multiple OFDM symbols:

- 14 OFDM symbols for normal cyclic prefix.
- 12 OFDM symbols for extended cyclic prefix.

The slot duration decreases as the subcarrier spacing increases, allowing flexible latency configurations in 5G systems.

Table 3.1: Comparison between Symbol Duration and Slot Duration

Feature	Symbol Duration	Slot Duration
Definition	The time it takes to transmit a single unit of data (a single point in a modulation constellation like QPSK or 256QAM).	A scheduling unit in the time domain that contains a fixed number of symbols.
What it Carries	The actual data bits (after modulation).	Multiple symbols, which together can carry user data, control information, and reference signals.
Duration & Flexibility	Fixed by SCS. It is directly inverse to the Subcarrier Spacing. Formula: $1/SCS$	Fixed by SCS. It is derived from the symbol duration. Formula: Number of Symbols per Slot \times (Symbol Duration + CP Duration)
Primary Purpose	To carry the modulated data across the channel.	To be the fundamental unit for resource scheduling and assignment from the base station to users.
Dependency	Depends only on the Subcarrier Spacing (SCS).	Depends on the SCS and the Cyclic Prefix (CP) type (which determines the number of symbols per slot).

3.8 Pilot Tones and Preambles

Pilot tones and preambles are essential components in OFDM systems for synchronization, channel estimation, and equalization.

3.8.1 Pilot Tones

Pilot tones are known reference symbols inserted at predefined time and frequency locations within the OFDM time–frequency grid.

Their main purposes include:

- Channel estimation.
- Tracking time-varying channels.

- Frequency and phase offset correction.

In 5G NR, pilot tones are commonly implemented as:

- Demodulation Reference Signals (DMRS).
- Phase Tracking Reference Signals (PTRS).
- Sounding Reference Signals (SRS) for uplink measurements.

Pilots enable per-subcarrier channel estimation, which allows simple one-tap equalization in the frequency domain.

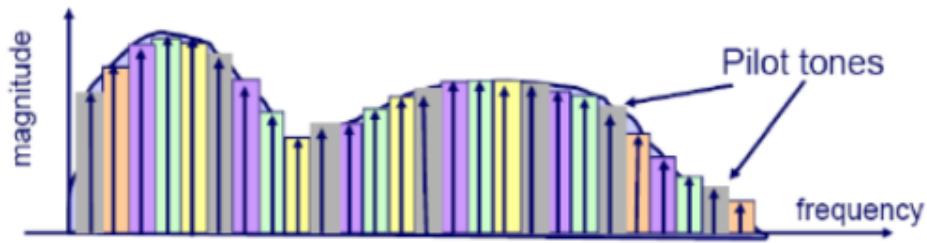


Figure 3.4: Pilot Tones insertion

3.8.2 Preambles

Preambles are special OFDM symbols transmitted at the beginning of a frame or burst.

They are used for:

- Time synchronization.
- Frequency synchronization.
- Initial channel estimation.

In 5G systems, preambles are particularly important in the Random Access Channel (RACH), where the user equipment transmits a predefined sequence to establish initial access with the base station.

Preambles are designed to have good autocorrelation properties to enable accurate detection even under low SNR conditions.

3.9 Receiver Operation

At the receiver:

Table 3.2: Comparison between Pilot Tones and Preambles

Feature	Pilot Tones	Preamble
Position	Scattered throughout data frame	At the start of frame or packet
Purpose	Channel estimation, phase correction	Synchronization (time, frequency, cell ID)
Frequency of use	Continuous (per symbol or few symbols)	Only once per burst/frame
Example (LTE)	DMRS, CSI-RS	PSS, SSS
In OFDM	Inserted among subcarriers	Used before first OFDM symbol

- Cyclic prefix is removed.
- FFT is applied to convert signal back to frequency domain.
- Channel equalization is performed per subcarrier.
- Data symbols are demodulated to recover the bit stream.

3.10 Advantages of OFDM

- Robust against multipath fading.
- Efficient spectrum utilization.
- Simple equalization.
- Suitable for high data rate systems.

3.11 Disadvantages of OFDM

- High Peak-to-Average Power Ratio (PAPR).
- Sensitive to frequency offset and phase noise.
- CP overhead reduces efficiency.

Chapter 4

Reference Parameters

Radiated transmitter characteristics

BS type 2-O: NR base station operating at FR2 with a requirement set consisting only of OTA requirements defined at the RIB.

Tested and specified using **Over-the-Air (OTA)** methods instead of direct conducted measurements.

RIB = Radiated Interface Boundary. It's a **virtual boundary** around the antenna system where OTA performance is evaluated.

Radiated transmit power:

Radiated power is described by its EIRP (in dBm or dBW) measured in the direction where that beam is strongest — the beam peak direction.

For **each declared beam and each tested direction (beam peak direction)** within the OTA peak direction set:

Test condition	Accuracy tolerance	What it means
Normal	± 3.4 dB	The measured EIRP must be within 3.4 dB of the manufacturer's claimed EIRP
Extreme	± 4.5 dB	Under harsh environmental limits, the measured EIRP can deviate up to 4.5 dB

OTA base station output power:

TRP = Total Radiated Power — it's the **sum of power radiated in all directions** by the base station's antennas. Mathematically, it's the **integral of radiated power over the whole sphere** around the antenna.

OTA occupied bandwidth:

The OTA occupied bandwidth is the width of a frequency band such that, below the lower and above the upper frequency limits, the mean powers emitted are each equal to a specified percentage $\beta/2$ (0.5 %) of the total mean transmitted power.

So, 1% only of the total mean transmitted power lies outside the specified bandwidth.

- Test applies per carrier (per signal), not across multiple aggregated carriers or MIMO layers.

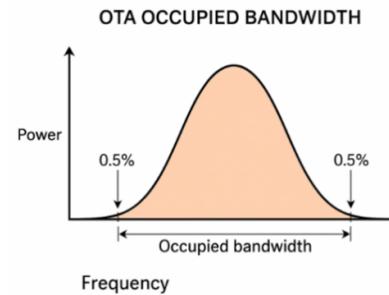


Figure 4.1: OTA Occupied Bandwidth

OTA Adjacent Channel Leakage Power Ratio (ACLR):

It is the ratio of the filtered mean power (Power after applying a measurement filter (like: BPF) that isolates one channel) centered on the assigned channel frequency to the filtered mean power centered on an adjacent channel frequency.

The measured power is **TRP**. The requirement shall be applied per RIB during the transmitter ON period.

- It measures how much of your transmitted signal's power leaks into neighboring frequency channels.
- The ACLR requirement must be met in all radiated directions (per RIB) where the base station is transmitting.

$$\text{ACLR (dB)} = 10 \log_{10} \left(\frac{P_{\text{in-channel}}}{P_{\text{adjacent-channel}}} \right)$$

Higher = better spectral containment.

OTA Adjacent Channel Leakage Power Ratio (ACLR):

The OTA ACLR defines how effectively a base station confines its transmitted power within its assigned channel. It is the ratio between the mean transmitted power in the assigned channel and that leaked into an adjacent channel, measured as **Total Radiated Power (TRP)** over the air at the **Reference Integration Boundary (RIB)**.

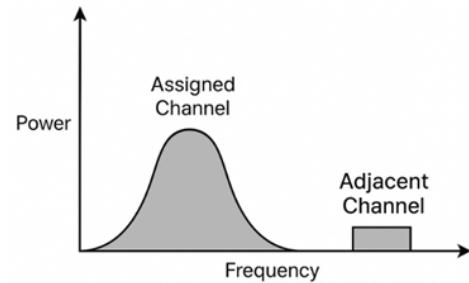


Figure 4.2: Assigned vs Adjacent Channel Power

$$\text{ACLR (dB)} = 10 \log_{10} \left(\frac{P_{\text{assigned channel}}}{P_{\text{adjacent channel}}} \right)$$

Minimum Requirement for type 2-O

Table 9.7.3.3-1: BS type 2-O ACLR limit

BS channel bandwidth of lowest/highest carrier transmitted $BW_{Channel}$ (MHz)	BS adjacent channel centre frequency offset below the lowest or above the highest carrier centre frequency transmitted	Assumed adjacent channel carrier	Filter on the adjacent channel frequency and corresponding filter bandwidth	ACLR limit (dB)
50, 100, 200, 400	$BW_{Channel}$	NR of same BW (Note 2)	Square (BW_{Config})	28 (Note 3) 26 (Note 4)

NOTE 1: $BW_{Channel}$ and BW_{Config} are the BS channel bandwidth and transmission bandwidth configuration of the lowest/highest carrier transmitted on the assigned channel frequency.

NOTE 2: With SCS that provides largest transmission bandwidth configuration (BW_{Config}).

NOTE 3: Applicable to bands defined within the frequency spectrum range of 24.25 – 33.4 GHz.

NOTE 4: Applicable to bands defined within the frequency spectrum range of 37 – 52.6 GHz.

In case of gaps between subcarrier (ACLR):

Table 9.7.3.3-4a: **BS type 2-O** ACLR absolute limit

BS class	ACLR absolute limit
Wide area BS	-13 dBm/MHz
Medium range BS	-20 dBm/MHz
Local area BS	-20 dBm/MHz

Radiated receiver characteristics

This section defines how well a base station (BS) can receive signals over the air (OTA).

- RIB = Radiated Interface Boundary (the point where OTA measurements are defined).
- BS Type 2-O RIB → integrated Active Antenna Systems (AAS). It must meet receiver performance requirements in radiated (OTA) conditions.

Minimum requirement for BS type 2-O

The Requirement — Throughput $\geq 95\%$

The throughput shall be $\geq 95\%$ of the maximum throughput of the reference measurement channel when the OTA test signal is at the EISREFSENS level.

“OTA in-band blocking”

OTA In-Band Blocking evaluates the base station receiver's resilience against very strong, out-of-channel interferers within the same operating band. This test is **significantly more stringent** than the Adjacent Channel Selectivity (ACS) test, using an interfering signal that is both more powerful and located further away from the desired channel.

Two types of interferers are defined:

1. **General Blocking:** A wideband interferer simulating a powerful transmitter from a nearby system.
2. **Narrowband Blocking:** A focused, high-power signal concentrated into a single resource block, testing the receiver's ability to reject intense, localized interference.

Minimum requirement for BS type 2-O

Table 10.5.2.3-1: General OTA blocking requirement for BS type 2-O

Frequency Range	BS channel bandwidth of the lowest/highest carrier received (MHz)	OTA wanted signal mean power (dBm)	OTA interfering signal mean power (dBm)	OTA interfering signal centre frequency offset from the lower/upper Base Station RF Bandwidth edge or sub-block gap (MHz)	Type of OTA interfering signal
FR2-1	50, 100, 200, 400	EIS _{REFSENS} + 6 dB	EIS _{REFSENS,50M} + 33 + Δ _{FR2,REFSENS}	±75	50 MHz DFT-s-OFDM NR signal, 60 kHz SCS, 64 RBs
FR2-2	100, 400, 800, 1600, 2000	EIS _{REFSENS} + 6 dB	EIS _{REFSENS,50M} + 36 + Δ _{FR2,REFSENS}	±150	100 MHz DFT-s-OFDM NR signal, 120 kHz SCS, 64 RBs

NOTE: EIS_{REFSENS} and EIS_{REFSENS,50M} are given in clause 10.3.3.

OTA out-of-band blocking

Answers the question: Is your receiver so sensitive that it can be deafened by literally any powerful radio transmitter in the environment, regardless of what frequency it's using?

Summary:

Test Type	Interferer Location	Interferer Examples	Interferer Power	Real-World Scenario
In-Band/Adjacent	Inside or immediately next to your band	Another 5G operator	Strong	Normal cellular operation
Out-of-Band (General)	Any other frequency (30 MHz - 12.75 GHz)	Military Radar, TV Broadcast, Wi-Fi	0.36 V/m (Very Strong Field)	General EM environment
Out-of-Band (Co-location)	Another cellular downlink band	2G, 3G, 4G base station on same tower	+46 dBm (Extremely Powerful)	Shared cell site

Chapter 5

5G Frame Structure and Numerology

5.1 Frequency Range of FR2

Frequency range designation	Band	Corresponding frequency range
FR1		410 MHz – 7125 MHz
FR2	FR2-1	24250 MHz – 52600 MHz
	FR2-2	52600 MHz – 71000 MHz
FR3		7100 – 24000 MHz

Table 5.1: Frequency Ranges

5.2 Time – Frequency Grid in OFDM

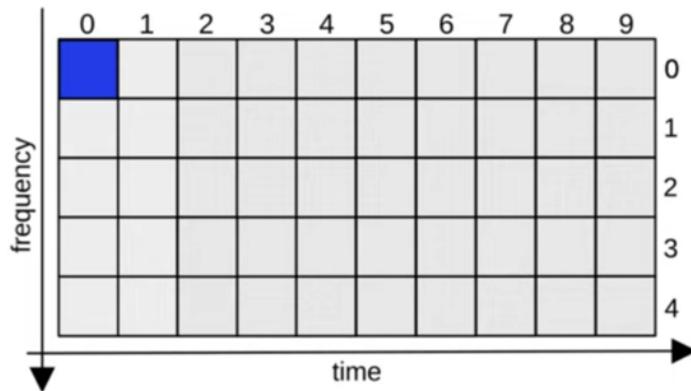


Figure 5.1: Time – Frequency Grid in OFDM

The OFDM Grid maps all QAM states in a 2D plane. Each cell represents a single QAM state. By selecting all states at a specific frequency, we obtain the set of QAM states

that modulate a single subcarrier. Taking all subcarrier states at a specific time index forms an OFDM symbol.

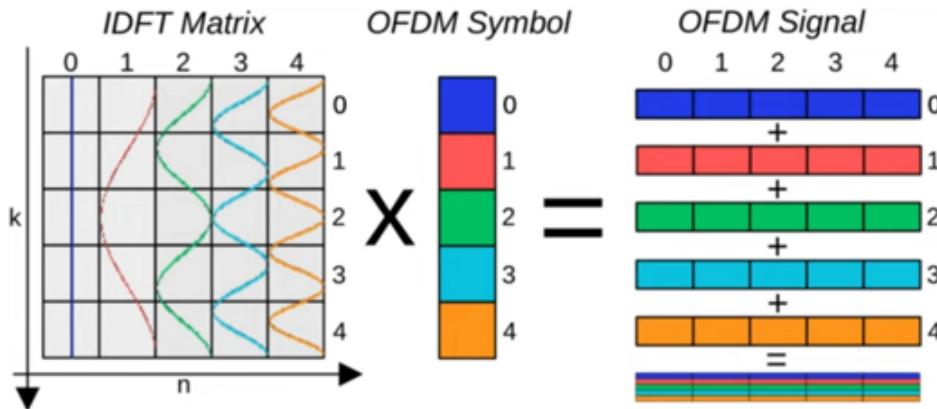


Figure 5.2: QAM modulation using IFFT

QAM modulation using IFFT:

- IFFT transforms frequency domain data into time domain signal using a matrix of sinusoidal waves.
- Each QAM state is multiplied by its corresponding carrier and all subcarriers are summed to produce a final signal vector.
- So, OFDM processes the signal symbol by symbol using IFFT to assign QAM states to each subcarrier then outputs of each IFFT operation are concatenated to form the transmitted signal.
- At the RX the inverse operation is executed (FFT).

5.3 5G Frame Structure

- Frames are 10ms long.
- Each frame is divided into ten subframes that are each 1ms long.
- Each subframe is split up into a number of slots, depending upon the SCS (Sub-carrier Spacing):
 - 15kHz = 1 slot
 - 30kHz = 2 slots
 - 60kHz = 4 slots

- $120\text{kHz} = 8 \text{ slots}$
- All slots within a subframe are not necessarily the same size; some symbols have a longer cyclic prefix than others, which impacts the slot duration.
- Each slot contains:
 - 14 OFDM symbols (if using normal cyclic prefix).
 - 12 OFDM symbols (if using extended cyclic prefix).
- Each symbol is uplink, downlink or a guard period.

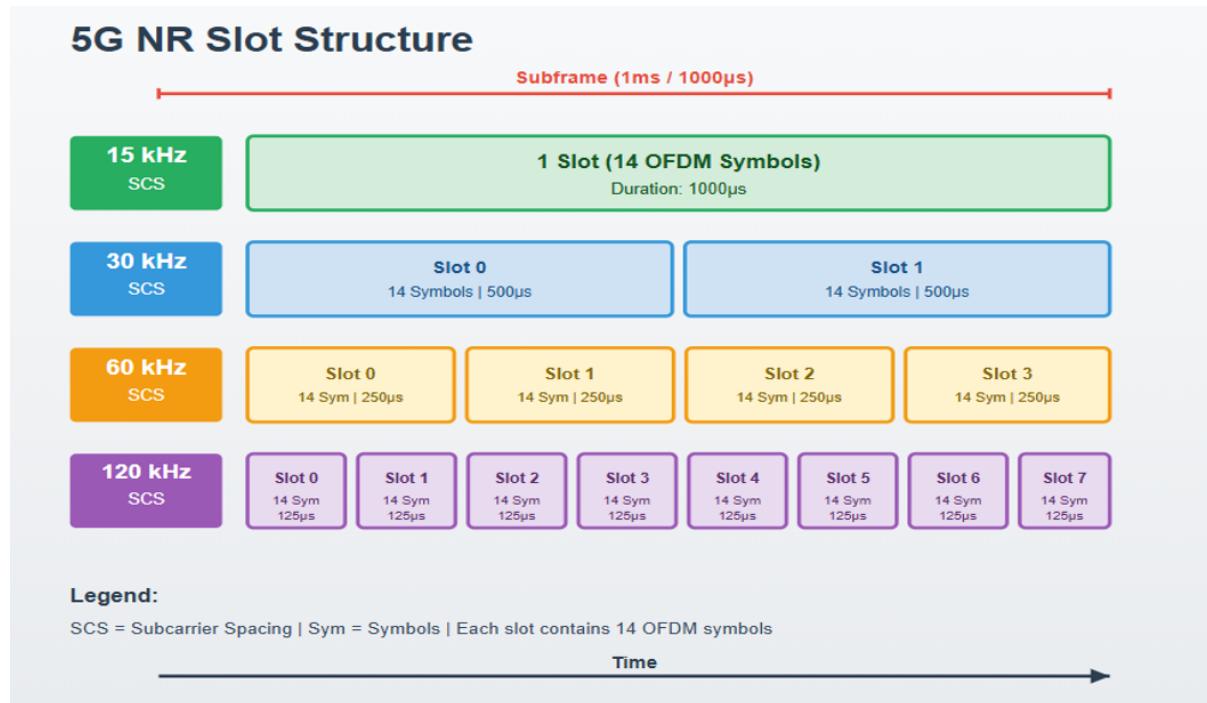


Figure 5.3: 5G NR Slot Structure

The slots are carried on the subcarriers using resource blocks. A resource block is defined as 12 consecutive subcarriers in the frequency domain. The slot format determines whether each symbol in a slot is uplink, downlink or a guard period.

Table 5.2: SCS Configuration (FR1 and FR2)

SCS (kHz)	50 MHz	100 MHz	200 MHz	400 MHz
60	66 (N_{RB})	132 (N_{RB})	264 (N_{RB})	N/A
120	32 (N_{RB})	66 (N_{RB})	132 (N_{RB})	264 (N_{RB})

Table 5.3: Extended SCS Configuration

SCS (kHz)	100 MHz	400 MHz	800 MHz	1600 MHz	2000 MHz
120	66	264	N/A	N/A	N/A
480	N/A	66	124	248	N/A
960	N/A	33	62	124	148

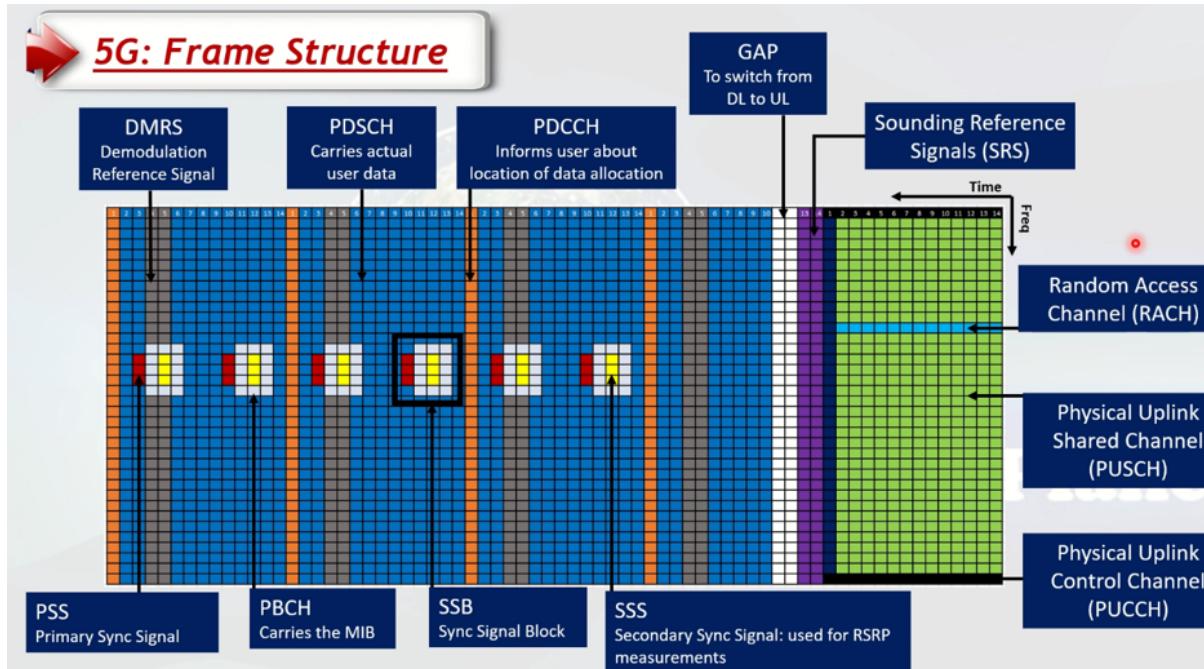


Figure 5.4: 5G Frame Structure Details

- Left side of the white region is for Downlink & the right side is for Uplink (TDD structure) so, we have 4 downlink slots and 1 uplink slot, each slot is 14 symbols.
- **Primary Sync Signal (PSS):** used for sync. As it gives the frequency of the block after it and part of the PCI (Physical Cell Identifier).
- **Secondary Sync Signal (SSS):** by reading this channel we can know whether the 5G coverage is good or not as it measures the channel power and gives the remaining part of the PCI for complete synchronization.
- **PBCH:** Carries the master information block (MIB) which carries the frame number and the configuration of some other channels.
- **Sync Signal Block (SSB):** It contains PSS, SSS and PBCH. If the user can't decode SSB successfully then he can't access the 5G cell.
- **Physical Downlink Control Channel (PDCCH):** usually in the first symbol and tells where the Data is allocated.

- **Physical Downlink Shared Channel (PDSCH):** Carries the actual data. The more channels we have the more capacity and Data rate 5G can support.
- **Demodulation Reference Signal (DMRS):** The pilot signals used to demodulate the PDSCH.
- **GAP:** Nothing is transmitted during the gap to switch from downlink to uplink.
- **Sounding Reference Signals (SRS):** symbols put after the GAP for uplink & downlink quality estimation.
- **Physical uplink Shared Channel (PUSCH):** Carries the uplink data.
- **Random Access Channel (RACH):** Preamble used for uplink Synchronization.
- **Physical Uplink Control Channel (PUCCH):** It carries the acknowledgements for the data sent during downlink or the requests for the data sent during uplink.

Chapter 6

MATLAB Simulation

6.1 Rayleigh Only Channel

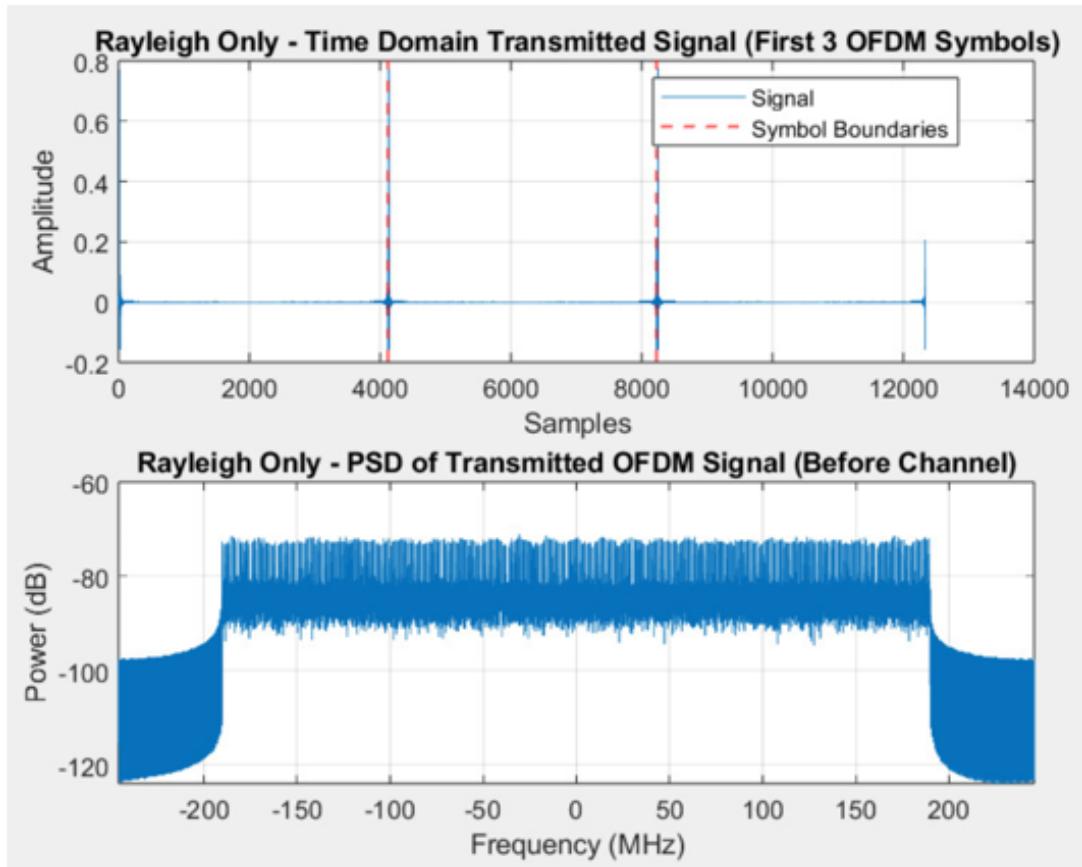


Figure 6.1: Rayleigh Only - Time Domain Transmitted Signal & PSD

First plot shows the transmitted OFDM waveform (time-domain samples). The PSD is flat over the used subcarriers (-200 MHz to +200 MHz), showing that OFDM evenly distributes power across all subcarriers (notice how it drops before 200 MHz due to guardband usage as the used bandwidth is equivalent to $12 \times N_{RB} \times \text{SCS}$ (380 MHz)).

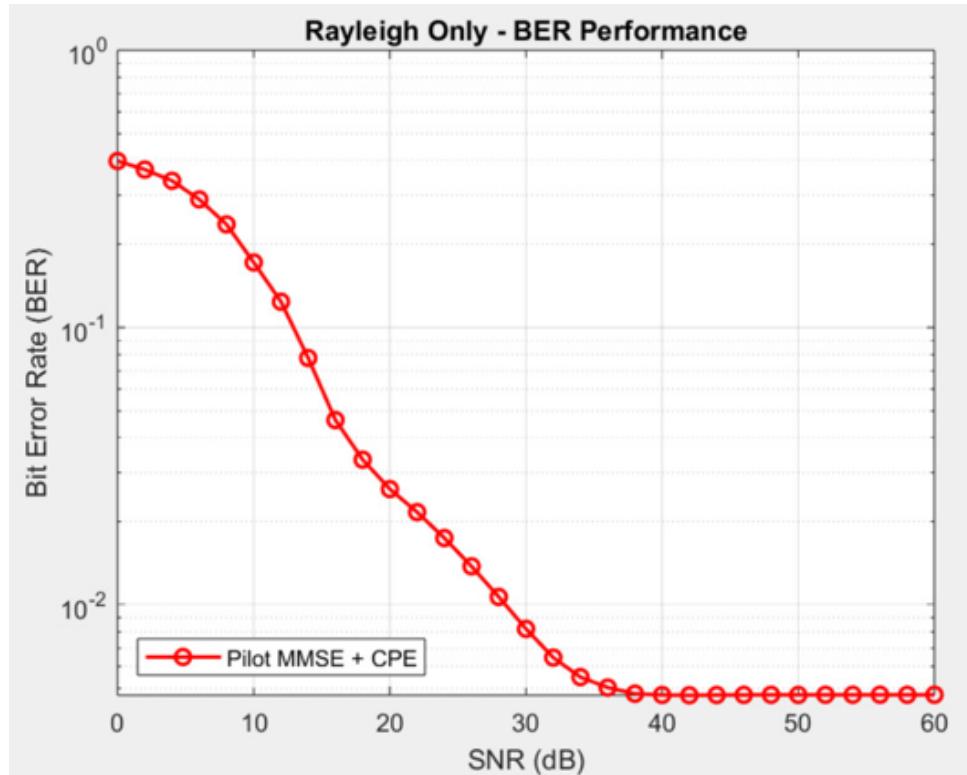


Figure 6.2: Rayleigh Only - BER Performance

Performance Plateau at High SNR: The curve shows that the Bit Error Rate (BER) improves significantly as SNR increases from 0 to approximately 40 dB. However, beyond this point, the BER saturates and fails to improve further, forming an "error floor."

Saturation Cause: Dominant Imperfect CSI: This saturation occurs because, in a Rayleigh fading channel, the limiting factor at high SNR is no longer background noise but residual errors in the channel estimation.

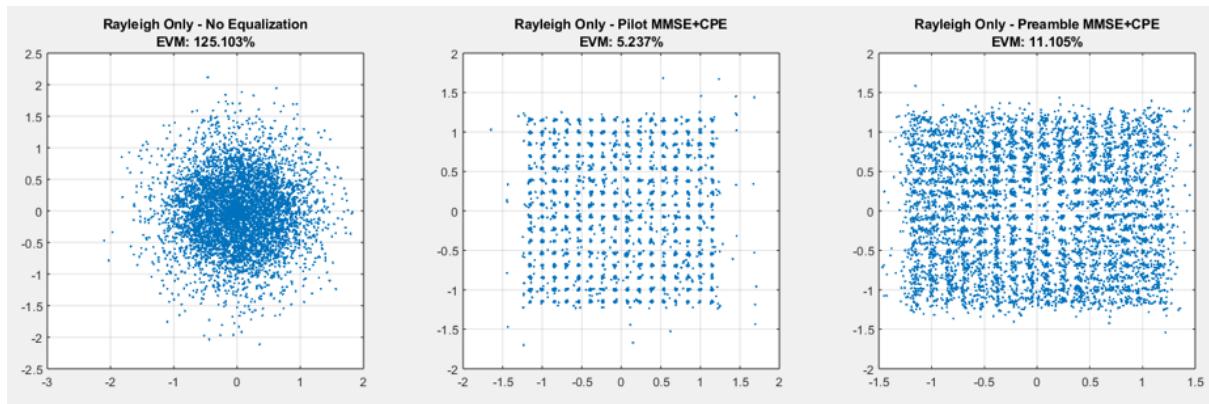


Figure 6.3: Rayleigh Only - Constellation Diagrams (No Equalization, Pilot MMSE, Preamble MMSE)

The difference between simulated and predicted SNR is less than 0.2 dB, indicating

precise normalization and correct noise modeling.

Pilot Efficiency: For 256-QAM, typical pilot overhead is around 5–10 %, depending on pilot spacing and modulation bandwidth.

$$\text{Pilot efficiency} = (\text{Data Subcarriers}/\text{Total Subcarriers})$$

e.g., if 8 out of 72 subcarriers are pilots \rightarrow efficiency $\approx (64/72) = 88.9\%$. Higher pilot efficiency improves throughput but slightly reduces channel estimation accuracy; a trade-off must be maintained.

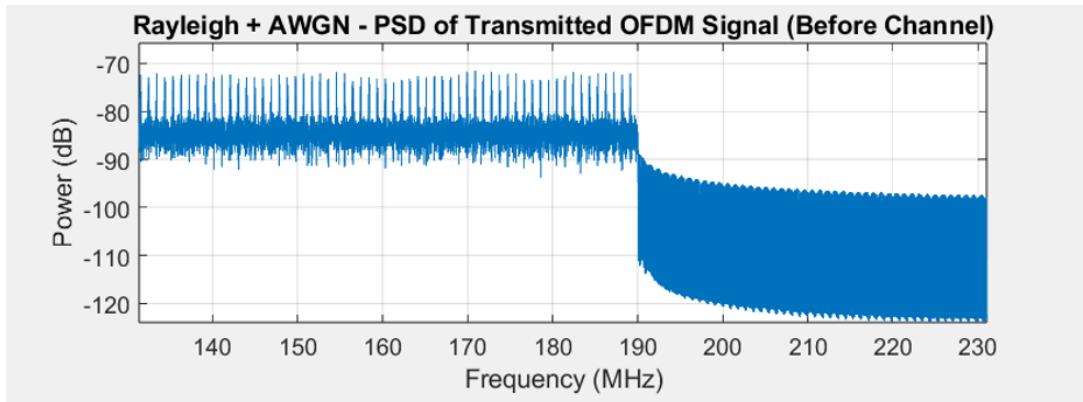


Figure 6.4: Rayleigh Only - Power Delay Profile & Channel Frequency Response

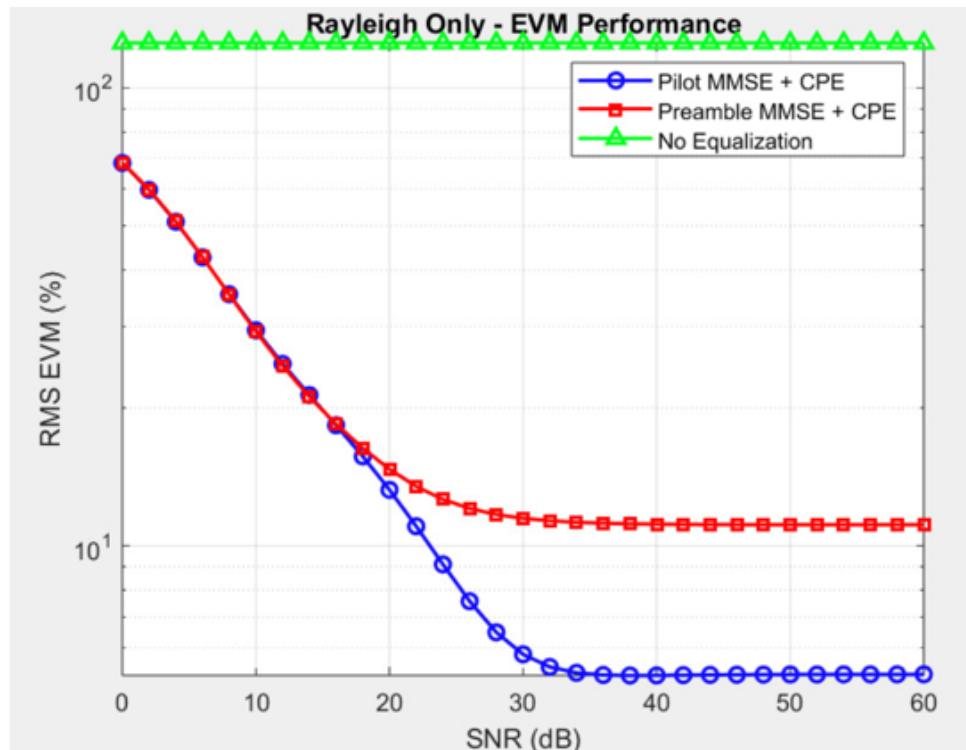


Figure 6.5: Rayleigh Only - EVM Performance

As SNR increases, EVM decreases exponentially, showing improved constellation accuracy and tighter symbol clustering.

Plot Purpose: Shows the Power Spectral Density (PSD) of the signal before passing through the channel. **Flat Spectrum:** The "No Equalization" curve represents the ideal OFDM signal with a flat spectrum, indicating efficient bandwidth use.

Equalization Methods Compared:

- **Preamble MMSE + CPE:** Uses a preamble for MMSE channel estimation and corrects Common Phase Error; effectively restores the flat spectrum.
- **Pilot MMSE + CPE:** Uses pilot symbols for MMSE estimation and CPE correction; also closely matches the ideal spectrum.

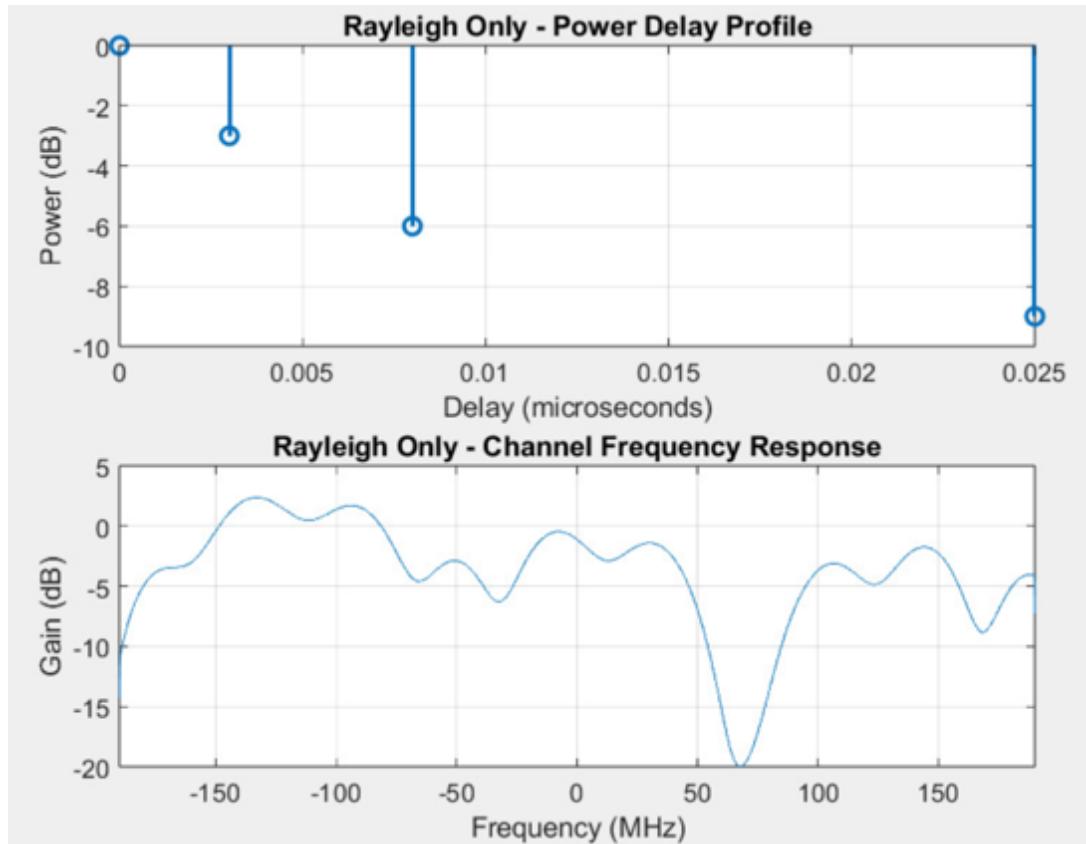


Figure 6.6: Rayleigh Only - PAPR Comparison

PAPR Reduction: The figure demonstrates a clear decrease in Peak-to-Average Power Ratio (PAPR) from approximately 34.27 dB for the transmitted signal to a lower value for the received signal, visually highlighting that the channel itself acts to reduce the peak power of the OFDM signal. **Channel-Induced Peak Limiting:** This reduction occurs because the Rayleigh fading channel, which causes multipath propagation,

introduces amplitude variations and destructive interference that effectively "clip" or attenuate the highest signal peaks, thereby lowering the overall PAPR by the time the signal is received.

6.2 AWGN (thermal noise) Only Channel

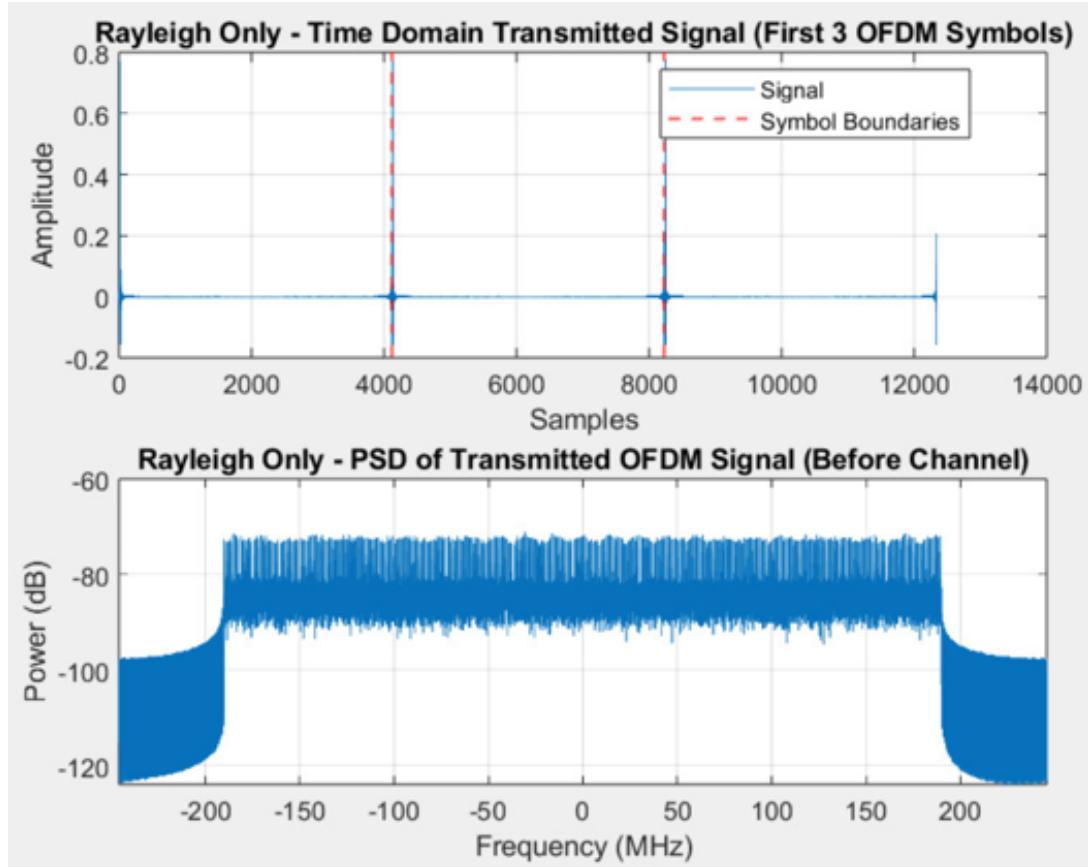


Figure 6.7: AWGN Only - Time Domain Transmitted Signal & PSD

First plot shows the transmitted OFDM waveform (time-domain samples). The PSD is flat over the used subcarriers (-200 MHz to +200 MHz), showing that OFDM evenly distributes power across all subcarriers.

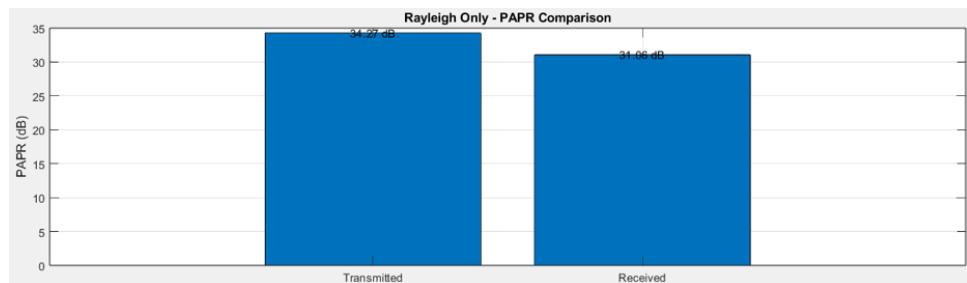


Figure 6.8: AWGN Only - BER Performance

Performance Plateau at High SNR: The curve shows that the BER improves significantly as SNR increases from 0 to approximately 40 dB. However, beyond this point, the BER saturates.

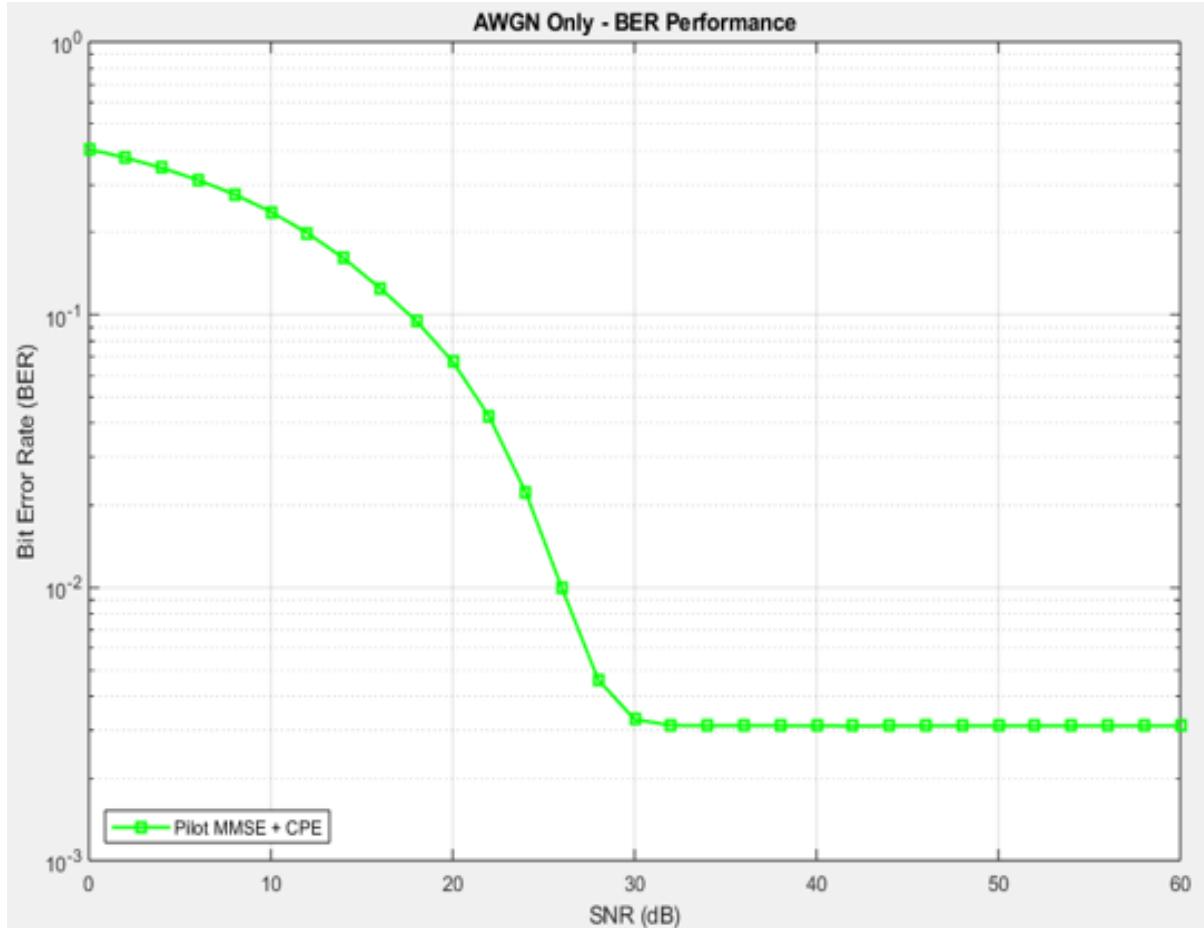


Figure 6.9: AWGN Only - Constellation Diagrams

Comparison of Equalization Techniques: This figure compares the performance of different channel equalization methods, specifically contrasting a Preamble-based MMSE approach with a Pilot-based MMSE approach, both combined with Common Phase Error (CPE) correction. In a pure AWGN channel, the optimal "equalizer" is effectively no equalizer at all.

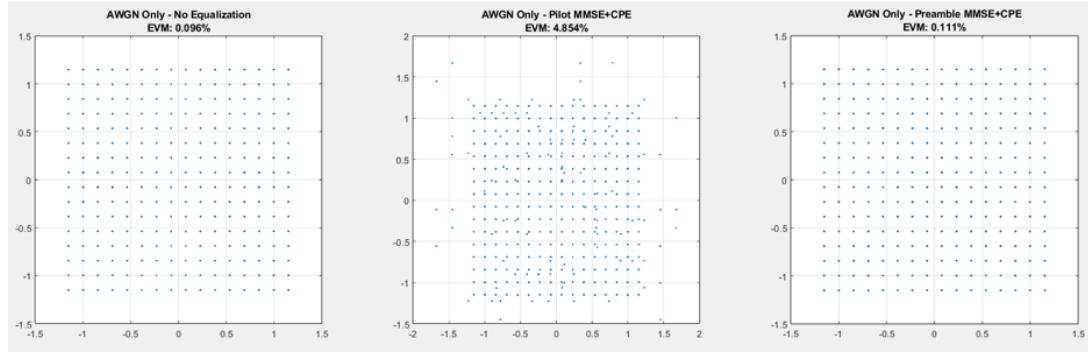


Figure 6.10: AWGN Only - Channel Frequency Response

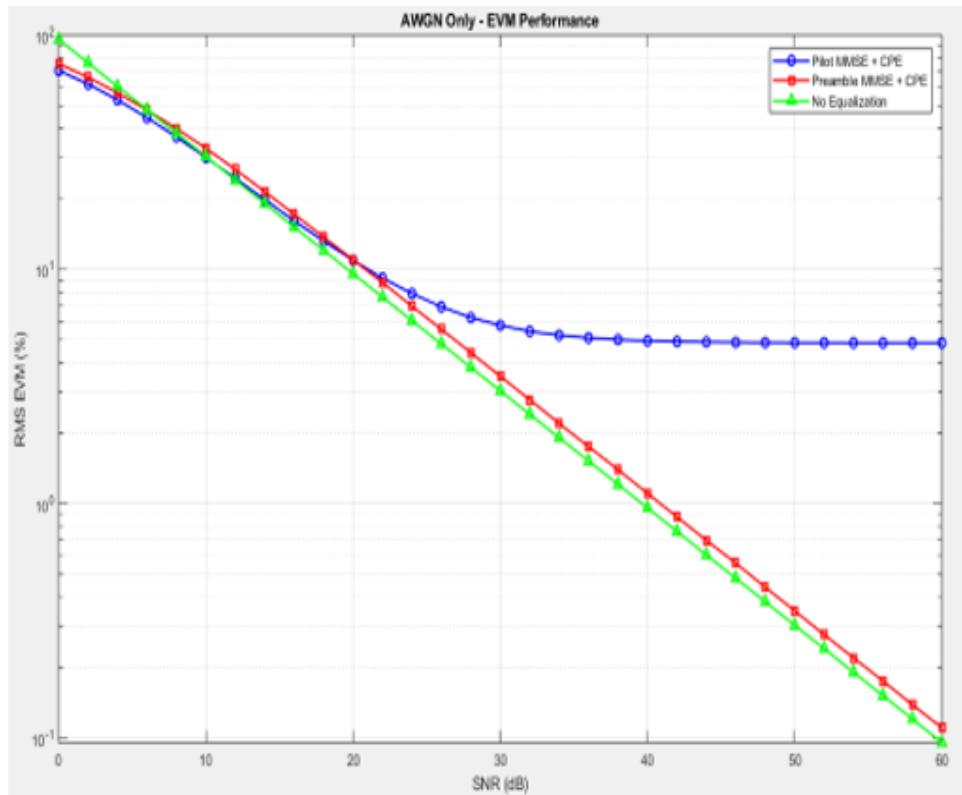


Figure 6.11: AWGN Only - EVM Performance

Plot Description:

- The figure shows the Error Vector Magnitude (EVM) performance versus Signal-to-Noise Ratio (SNR) under Additive White Gaussian Noise (AWGN) conditions.
- EVM (%) is plotted on a logarithmic scale (y-axis), while SNR (dB) is on the x-axis.

Performance Insights:

- At low SNR, all methods perform similarly, as noise dominates the performance.

- As SNR increases, the Preamble MMSE + CPE (red) and No Equalization (green) curves continue improving, showing lower EVM.
- The Pilot MMSE + CPE (blue) curve flattens out beyond 25 dB, indicating a performance floor—likely due to imperfect pilot estimation or limited pilot density.

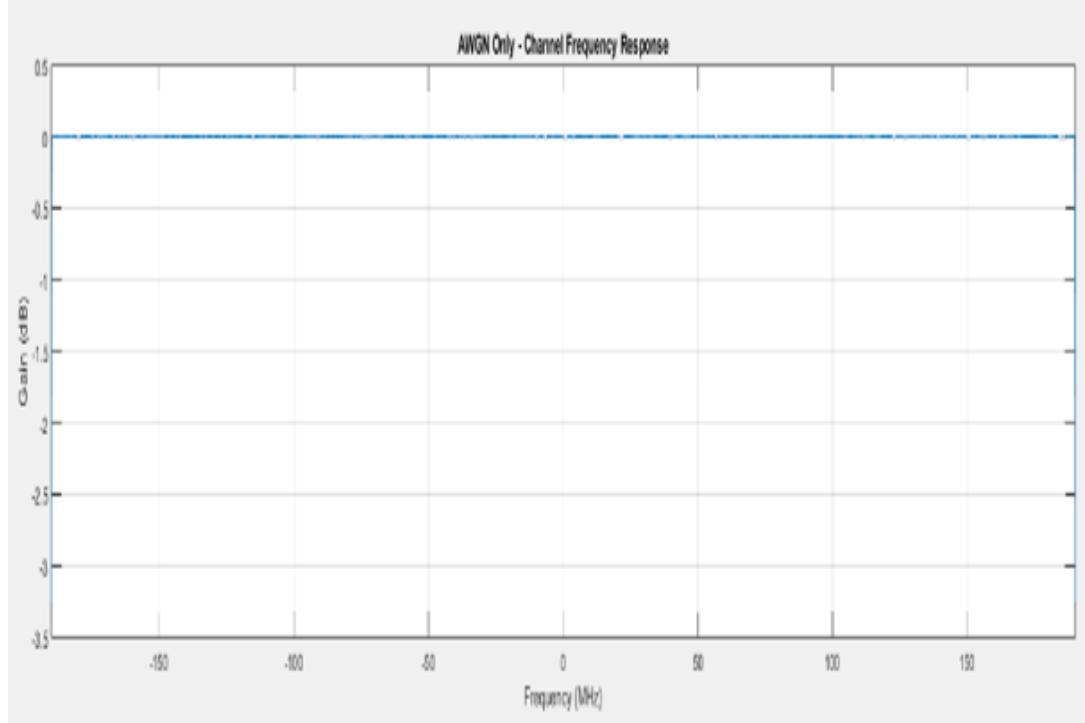


Figure 6.12: AWGN Only - PAPR Comparison

Minimal PAPR Change: The figure shows that the PAPR remains virtually unchanged between the transmitted signal (34.27 dB) and the received signal, with only a negligible difference (e.g., 34.26 dB). **AWGN Preserves Signal Structure:** This occurs because the AWGN channel only adds random noise and does not cause the amplitude fading or multipath interference that would distort the signal's peaks. As a result, the high-power peaks that characterize the OFDM signal are preserved.

6.3 Comparison and Combined Results

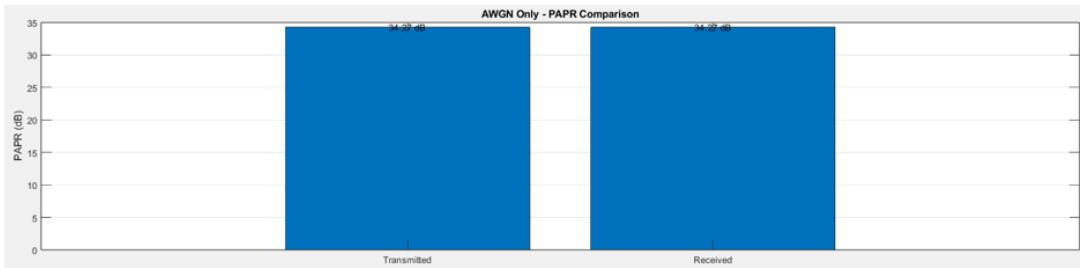


Figure 6.13: Combined: EVM vs SNR - All Channel Types

Performance in AWGN is better with preamble; EVM saturates in all environments using pilot MMSE.

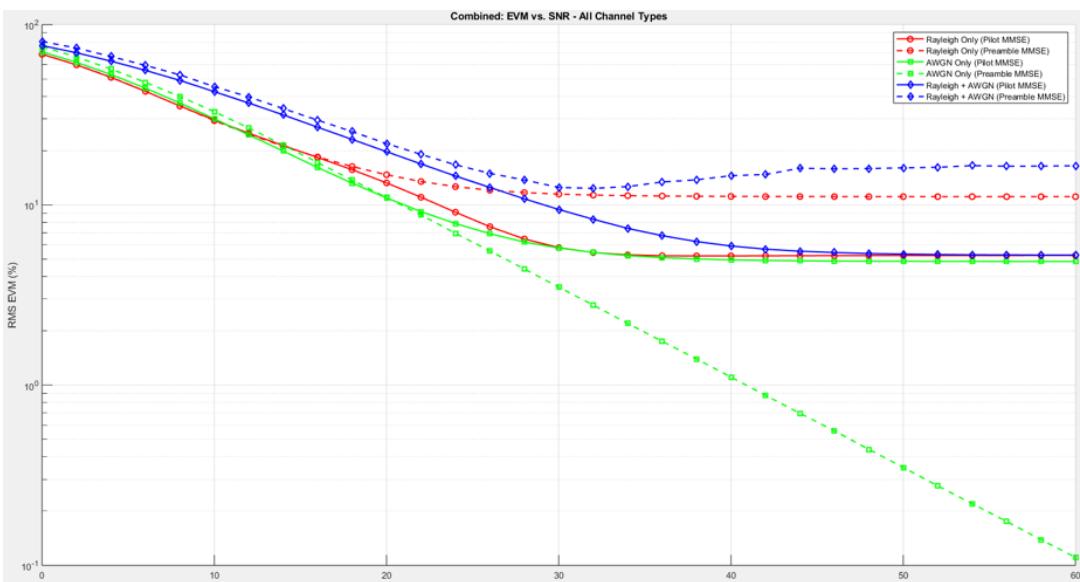


Figure 6.14: Combined: BER vs SNR - All Channel Types

AWGN Only (Intermediate Performance):

- Performs worse than Rayleigh Only but better than Rayleigh + AWGN.
- Impairment comes mainly from random noise.
- Channel is flat, so Pilot MMSE equalizer adds little benefit.
- Noise corrupts pilot estimates, slowing BER improvement.

Rayleigh Only (Best Performance):

- Fastest BER drop, reaching near zero around 35 dB.

- Rayleigh fading applied with very high SNR, so noise is negligible.
- Pilot MMSE equalizer effectively tracks fading, giving excellent performance.

Rayleigh + AWGN (Worst Performance):

- Slowest BER improvement and highest BER overall.
- Affected by both fading and noise simultaneously.
- Noise corrupts pilot-based channel estimates, leading to imperfect equalization.

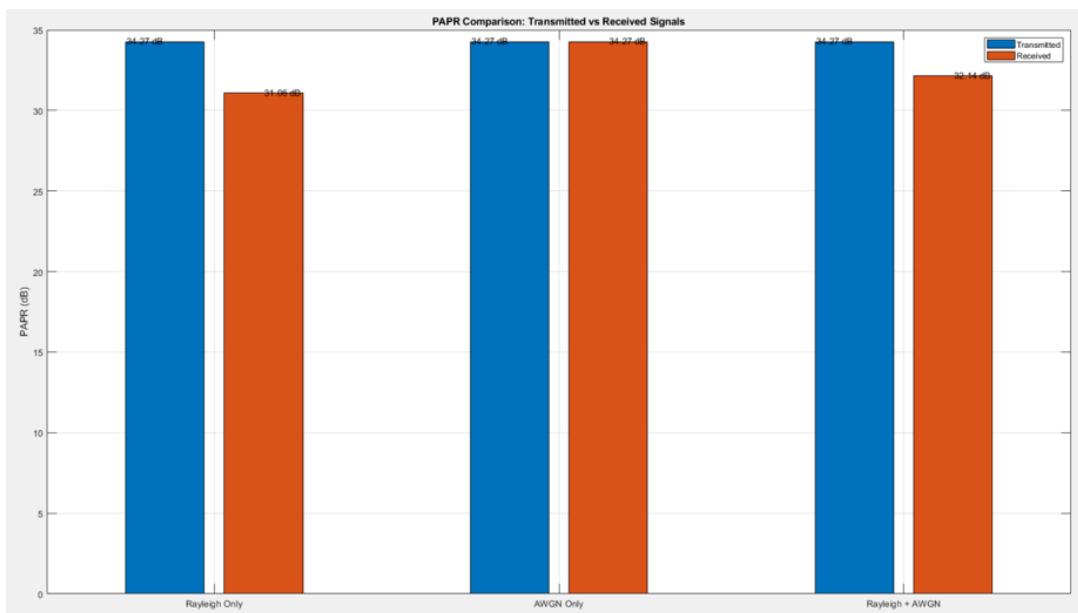


Figure 6.15: PAPR Comparison: Transmitted vs Received Signals

1. AWGN Only (34.27 dB) - Highest Received PAPR:

- What the channel does: Adds random noise but preserves the signal's fundamental shape.
- Why the PAPR is highest: The signal's original peaks remain largely intact.

2. Rayleigh + AWGN (32.14 dB) - Middle PAPR:

- What the channel does: Combines multipath fading with additive noise.
- Why the PAPR is in the middle: The Rayleigh fading reduces the peaks, but the AWGN adds noise that can slightly increase the average power.

3. Rayleigh Only (30.44 dB) - Lowest PAPR:

- What the channel does: Creates deep fades through multipath interference without adding significant background noise.

- Why the PAPR is lowest: The fading dramatically reduces peak amplitudes while the average power isn't boosted by noise. This creates the most "flattened" signal.

Table 6.1: PAPR Comparison Summary

Channel Condition	Effect on Signal	Impact on PAPR	Reason
AWGN Only	Adds noise, preserves signal shape.	Highest PAPR (34 dB)	Received Signal structure (including peaks) is largely intact.
Rayleigh AWGN	+ Fades peaks AND adds noise.	Middle PAPR (32.14 dB)	Combined effect of peak attenuation and noise masking.
Rayleigh Only	Causes multipath fading, smearing peaks.	Lowest PAPR (30.44 dB)	Fading aggressively attenuates the highest signal peaks without noise filling in the valleys.

6.4 Theoretical Verification

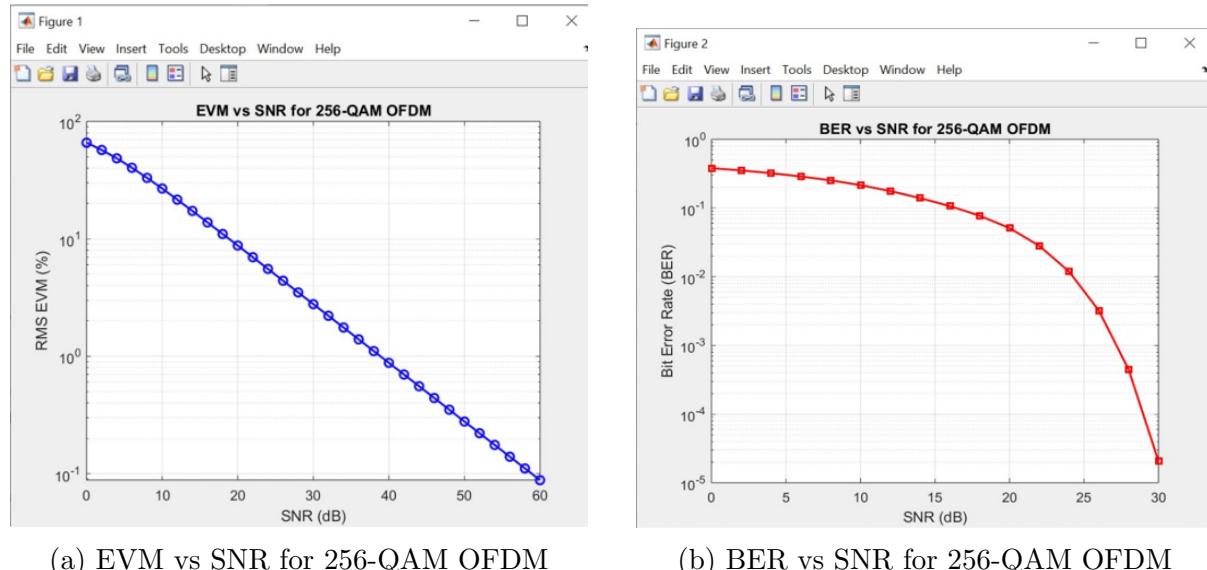


Figure 6.16: EVM and BER vs SNR for AWGN Channel

Mathematical formula for EVM vs SNR (linear region):

$$\text{SNR}_{\text{lin}} = \frac{1}{\text{EVM}_{\text{lin}}^2} \quad \text{or} \quad \text{SNR}_{\text{dB}} = -20 \log_{10}(\text{EVM}_{\text{lin}})$$

$$\text{SNR}_{\text{dB}} = 40 - 20 \log_{10}(\text{EVM}\%)$$

Chapter 7

Direct Digital Synthesis (DDS)

7.1 Fundamentals of DDS Technology

Direct Digital Synthesis (DDS) is a digital technique used to generate analog waveforms—most commonly sine waves—whose frequency and phase can be precisely controlled using digital inputs. A DDS system has a reference clock (a very stable, fixed-frequency oscillator, e.g. 100 MHz), and it produces a new frequency (say 5 MHz) by dividing or scaling that reference using a digital tuning word.

$$f_{out} = \frac{\text{Tuning Word}}{2^N} \times f_{clock} \quad (7.1)$$

where:

- f_{out} = generated output frequency
- f_{clock} = system clock frequency
- N = number of bits in the tuning word (e.g., 32 bits)
- “Tuning Word” = binary value you program (24–48 bits)

Theory of Operation:

direct digital synthesizer can be implemented from a precision reference clock, an address counter, a programmable read only memory (PROM), and a D/A converter

The clock drives the system — every clock pulse advances the address counter by one step. So, the frequency of this clock determines how fast we go through the lookup table. The address counter produces a sequence of binary numbers (addresses): 0, 1, 2, 3, ... These addresses point to memory locations inside the PROM where digital sine values are stored. When the counter reaches the end of the table (say after 1024 samples), it wraps around to 0 again — forming a repeating sine wave cycle.

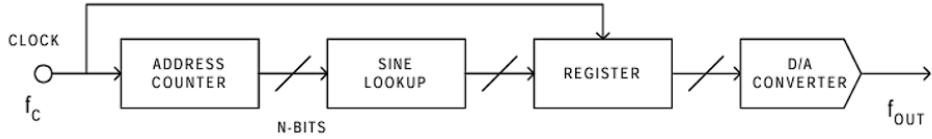


Figure 1-1. Simple Direct Digital Synthesizer

Figure 7.1: Figure 1-1. Simple Direct Digital Synthesizer

The PROM stores digital amplitude values representing one full cycle of a sine wave. For example, if the table has 1024 samples, each entry corresponds to:

$$\text{Amplitude}[n] = \sin\left(\frac{2\pi n}{1024}\right) \quad (7.2)$$

The address counter fetches each sample sequentially. Thus, the PROM acts as a digital memory-based waveform generator. The register latches (temporarily holds) the digital sine sample so it can be sent cleanly to the DAC at the next clock edge. This ensures timing synchronization between digital and analog stages. The DAC converts each digital sample from the PROM into an analog voltage. The output becomes a staircase approximation of a sine wave, which can be smoothed with a low-pass filter to get a clean analog sine output f_{OUT} .

The output frequency depends on:

$$f_{OUT} = \frac{f_C}{N} \quad (7.3)$$

where:

- f_C = reference clock frequency
- N = number of samples per sine period stored in the PROM

This architecture works, but it has two limitations:

1. **No fine frequency control:** Output frequency can only change by modifying the clock frequency or PROM contents. You can't just "dial in" any frequency easily.
2. **No fast frequency hopping:** Since frequency tuning depends on hardware changes (PROM reprogramming or clock adjustment), you can't switch frequencies quickly or digitally.

To fix that, a phase accumulator is added. It replaces the simple address counter and adds: A phase register, and A variable-modulus counter. These allow the system

to advance through the sine-wave table by variable step sizes. The output sine wave is imagined as a vector rotating around a circle — the phase wheel. Each position on the wheel corresponds to a phase of the sine wave (e.g. 0°, 90°, 180°, 270°). One full revolution → one full sine-wave cycle. The phase accumulator digitally performs this rotation: Each clock pulse adds a fixed value ("tuning word") to the accumulator. When it overflows, that means one full cycle has been completed. The number of discrete points around the phase wheel depends on the accumulator resolution N .

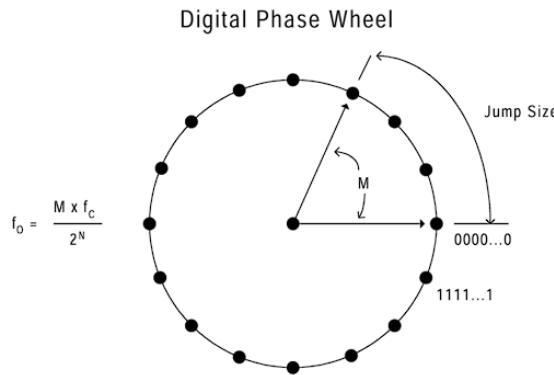


Figure 7.2: Digital Phase Wheel

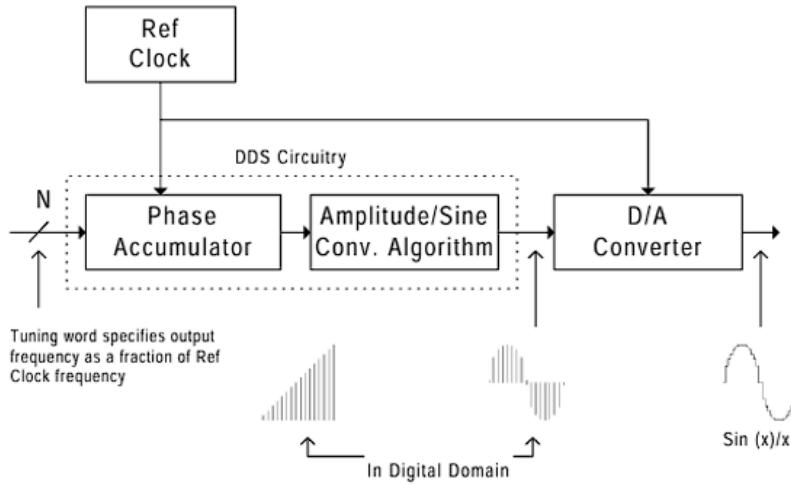
$$f_{OUT} = \frac{M \times f_C}{2^N} \quad (7.4)$$

where f_{OUT} = output frequency, f_C = reference-clock frequency, M = tuning word (phase-step size), N = phase-accumulator bit width. → Larger M means bigger "jump" around the phase wheel → higher output frequency.

The phase accumulator output by itself is just a ramp (linear phase increase). It must be converted into a waveform. A phase-to-amplitude lookup table (sine lookup) translates phase values into amplitude samples for the DAC. Usually, only $\frac{1}{4}$ of the sine table is stored; the rest of the cycle is generated by exploiting symmetry.

Reference clock drives the system. Phase accumulator adds the tuning word every clock cycle. Phase-to-amplitude converter (lookup or algorithm) generates digital sine values. DAC converts them to an analog waveform. Optional low-pass filter smooths it.

Changing the tuning word M gives instant, phase-continuous frequency changes — key DDS advantage. When you change M , the phase accumulator is not reset — it just continues from its current phase value, but with a new step size. That means there's no phase discontinuity and no glitch in the output waveform. The frequency change is smooth and immediate — the new frequency starts from the current phase point of the sine wave. This is called phase-continuous tuning — a key advantage of DDS over analog PLL synthesizers, which need time to settle after a frequency change.



In practical DDS chips: You don't write M directly into the phase accumulator. Instead, you first load it into an internal register (called a buffer or serial/byte-loaded register). Then, that register's value is transferred (clocked) into the actual delta phase register that drives the accumulator. This two-step approach has benefits:

- Minimizes pin count: you can use a serial or small parallel interface to send data to the chip.
- Synchronizes changes: all bits of M are updated together at a precise clock edge — ensuring clean, glitch-free frequency updates.

If the chip uses a parallel byte-load interface, it can receive data faster than a serial one. That's why high-speed DDS designs often use parallel interfaces — to support rapid frequency hopping in applications like radar.

Block	Function	Advantage
(A) REFCLK Multiplier	Multiplies external clock (e.g., $\times 4$ – $\times 20$).	Slower external clocks, high internal clock rates.
(B) Phase Offset Adder	Adds programmable phase offset.	Phase shifting and PSK modulation.
(C) Inverse SINC Filter	Compensates for DAC's $\sin(x)/x$ rolloff.	Keeps amplitude flat up to $\sim 45\%$.
(D) Digital Multiplier	Multiplies sine amplitude.	Amplitude modulation (AM) and envelope generation.
(E) Dual DACs (I/Q)	Second DAC for quadrature output.	I and Q outputs for modulators.
(F) Comparator	Squares the analog output.	DDS acts as a clock generator.
(G) Frequency/Phase Registers	Store pre-programmed tuning words.	FSK or PSK by switching values.

Performance Example:

- 48-bit frequency tuning word: $\sim 1 \mu\text{Hz}$ resolution.
- 14-bit phase tuning word: 0.022° phase resolution.

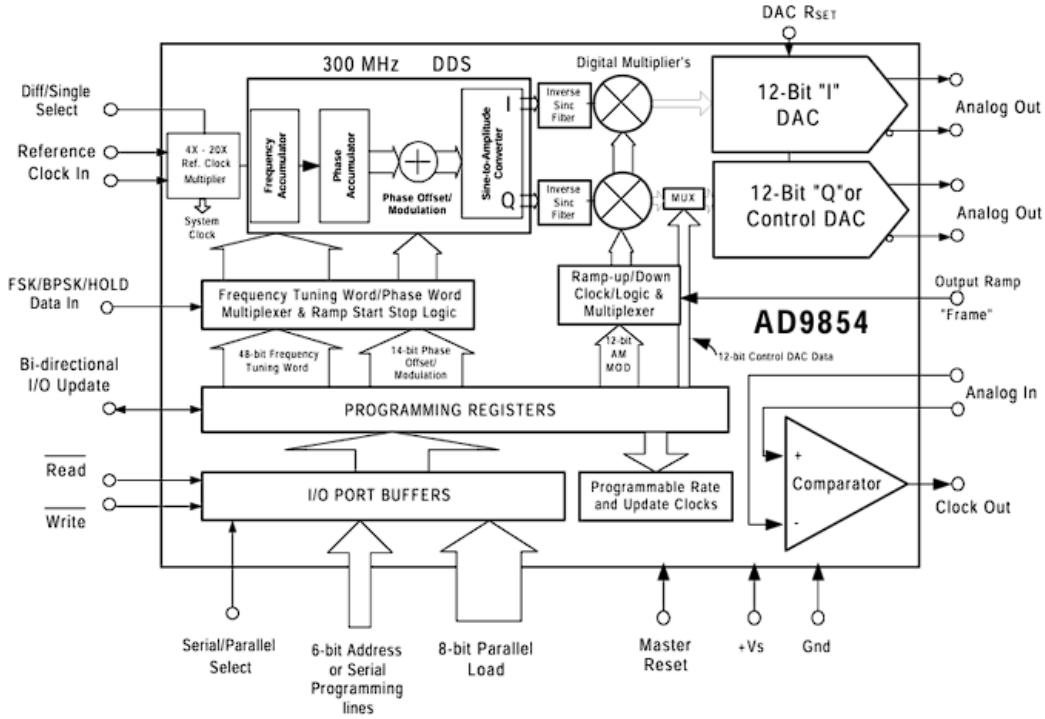


Figure 1-5. Full-featured 12-bit/300 MHz DDS Architecture

Figure 7.3: Figure 1-5. Full-featured 12-bit/300 MHz DDS Architecture

- REFCLK multiplier: $4\times\text{--}20\times$ range.
- Output bandwidth: $\approx 1/3$ of clock (e.g., 100 MHz at 300 MHz clock).
- Spurious-free dynamic range: 50 dB typical.
- I/Q output matching: 0.01° .
- Amplitude flatness: ± 0.01 dB (DC–Nyquist)

7.2 Understanding the Sampled Output of a DDS Device

A DDS works by sending digital samples of a sine wave (from the lookup table) to a DAC. Each clock pulse produces one sample → that means the output is discrete in time, not continuous. So the DDS output is:

$$x(t) = \sum_{n=-\infty}^{\infty} x[n] \cdot \delta(t - nT_s) \quad (7.5)$$

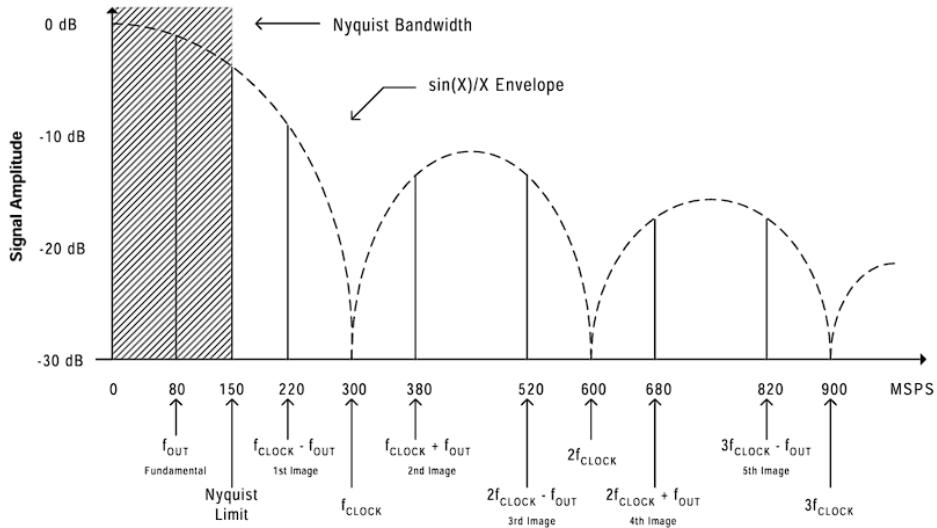


Figure 2-1. Spectral Analysis of Sampled Output

Figure 7.4: Figure 2-1. Spectral Analysis of Sampled Output

where $T_s = 1/f_{CLK}$ is the sampling period.

The DAC reconstructs this sampled waveform, but because of sampling, the spectrum repeats every clock frequency. The output spectrum of a DDS is periodic in frequency: The main desired tone appears at f_{OUT} , Mirror (image) signals appear at: $f = \pm f_{OUT} \pm kf_{CLK}, k = 1, 2, 3, \dots$. So, the DDS creates many copies of the waveform across the spectrum — one in each Nyquist zone. To isolate the real sine wave, a low-pass filter (called a reconstruction filter) is used to remove all higher-frequency images.

The Nyquist frequency is half the sampling rate: $f_N = \frac{f_{CLK}}{2}$. This is the maximum usable output frequency before aliasing occurs. If you go above this limit, frequencies "fold back" (alias) into the baseband. Therefore, practical DDS operation limits the output to roughly 0–40% of f_{CLK} to maintain low distortion and easier filtering.

A DAC holds each output sample for one clock period — this is called a zero-order hold. The frequency response of such a hold circuit is:

$$H(f) = \frac{\sin(\pi f/f_{CLK})}{\pi f/f_{CLK}} \quad (7.6)$$

That's the sinc() function ($\sin(x)/x$). Effect: The output amplitude decreases as frequency increases. At 0 Hz: gain = 1 (no loss). At half the clock (Nyquist): gain = ~ 0.64 (≈ -3.9 dB loss). So the higher the output frequency, the smaller the amplitude due to this sinc-shape. To correct that amplitude droop, modern DDS chips include a digital inverse-sinc filter before the DAC.

Spectrum Folding (Aliasing) Example: Imagine you generate 240 MHz from a 300 MHz clock: Desired tone: 240 MHz. But the DAC also produces an image at $f_{CLK} - f_{OUT} = 60$ MHz. → This is the alias that "folds back" into the first Nyquist zone. That's why the DDS output is usually restricted to ~ 100 MHz (one-third of the clock) — to make filtering practical and avoid alias overlap.

7.3 Frequency/phase-hopping Capability of DDS

Frequency hopping = quickly changing the output frequency between different values. Phase hopping = instantly changing the phase offset of the output waveform. Recall the DDS frequency equation:

$$f_{OUT} = \frac{M \times f_{CLK}}{2^N} \quad (7.7)$$

Changing M changes the output frequency instantly — the DDS simply starts stepping through the phase accumulator faster or slower. When M changes, the phase accumulator's current value is preserved (not reset). So, the output waveform continues from its current phase position, avoiding glitches or discontinuities. This is called phase-continuous frequency hopping.

Why DDS Hopping is Instantaneous? In a DDS, frequency and phase are digitally defined — there's no feedback loop, voltage tuning, or analog settling as in PLLs. Suppose the DDS control interface runs at 100 MHz. You can update the tuning word every 10 ns. DDS also allows instant phase changes. Each DDS typically has a phase offset register (e.g., 14 bits → 0.022° resolution). Use case: Phase-shift keying (PSK) modulation — e.g. BPSK, QPSK, or $\pi//4$ -QPSK — where phase changes represent digital data bits. Internally, a DDS has: frequency tuning registers (for different frequencies), Phase registers (for different phase offsets), A multiplexer or control logic to select among them.

7.4 The Effect of DAC Resolution on Spurious Performance

7.4.1 DAC Resolution and Quantization Distortion

Main Idea: The higher the number of bits (resolution) in a DAC, the lower the distortion in the output spectrum.

Why: More bits mean smaller quantization steps → less quantization error → cleaner sine wave → fewer unwanted spurs in the frequency spectrum.

Equation (Signal-to-Quantization-Noise Ratio):

$$SQR = 1.76 + 6.02B \quad (\text{dB}) \quad (7.8)$$

where B = DAC resolution in bits.

Example: An 8-bit DAC $\rightarrow SQR = 1.76 + 6.02 \times 8 = 49.92$ dB (Shows better noise performance than a 4-bit DAC.)

7.4.2 Effect of Output Level (Not Full-Scale Operation)

When the DAC does not operate at full scale (e.g., 70% of max output), signal power decreases but quantization noise stays the same.

The correction factor is:

$$A = 20 \log(FFS) \quad (7.9)$$

where FFS = fraction of full scale.

The full equation becomes:

$$SQR = 1.76 + 6.02B + 20 \log(FFS) \quad (7.10)$$

Example: If DAC = 8-bit and output = 70% full scale $\rightarrow A = 20 \log(0.7) = -3.1$ dB \rightarrow new SQR = 46.82 dB (a 3.1 dB drop).

7.4.3 Oversampling and Its Effect on SQR

Oversampling = sampling faster than the Nyquist rate (using a higher clock rate than strictly necessary).

Quantization noise power stays constant, but when spread across a wider frequency range, the in-band noise (within the useful signal band) decreases. So oversampling improves SNR.

The improvement factor is:

$$C = 10 \log \left(\frac{F_{sOS}}{F_s} \right) \quad (7.11)$$

Combined equation:

$$SQR = 1.76 + 6.02B + 20 \log(FFS) + 10 \log \left(\frac{F_{sOS}}{F_s} \right) \quad (7.12)$$

Example: If oversampling by $3\times$ and operating at 70% full scale $\rightarrow \text{SQR} = 51.6 \text{ dB}$, an improvement of 1.7 dB over full-scale, non-oversampled case.

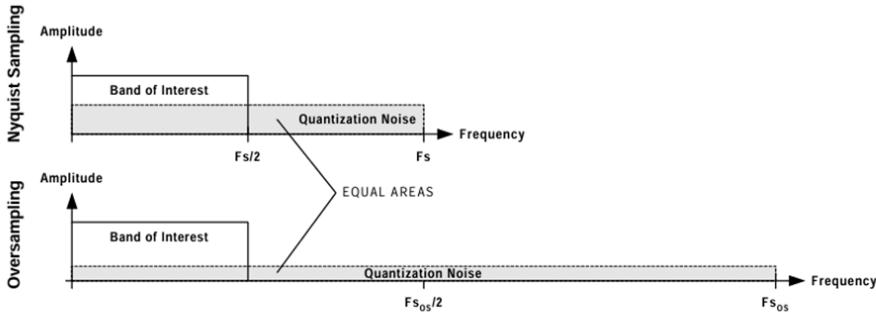


Figure 4.3. The Effect of Oversampling on SQR

Figure 7.5: The Effect of Oversampling on SQR

7.4.4 Phase Truncation and Spurious Performance (DDS-specific)

Problem: A full 32-bit phase accumulator would need 2^{32} lookup entries \rightarrow impractical in memory.

Solution: Use only the most significant bits (MSBs) for phase lookup and truncate the rest (e.g., use top 12 bits of a 32-bit accumulator).

Result: Truncation introduces periodic phase errors because the ignored bits cause small phase mismatches between actual and truncated phase values.

Consequence: These periodic errors \rightarrow amplitude distortion \rightarrow spurious tones (spurs) in frequency domain, known as phase truncation spurs.

Spur characteristics depend on:

- Accumulator size (A) — total bits in the accumulator
- Phase word size (P) — number of bits after truncation
- Tuning word (T) — the step size per clock cycle

7.4.5 Phase Truncation Spur Magnitude

Background In a Direct Digital Synthesizer (DDS):

- The phase accumulator generates a digital phase ramp each clock cycle.
- Only the upper P bits (out of the total A bits) are used to select the sine amplitude from the lookup table.

- The remaining $A - P$ bits are truncated (discarded).
- This truncation causes periodic phase errors, which create spurious frequency components (spurs) in the output spectrum.

How Spur Magnitude Depends on Truncation The size (magnitude) of these truncation spurs depends mainly on:

- The phase word size (P) — how many bits we keep for lookup.
- The accumulator size (A) — how many total bits the phase accumulator has.
- The tuning word (T) — the digital value added to the accumulator each clock (it sets the output frequency).

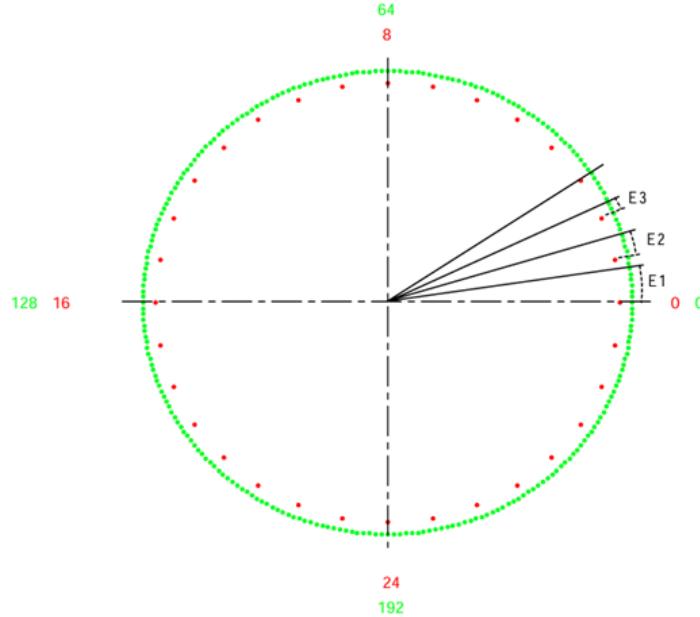


Figure 4.4. Phase Truncation Error and the Phase Wheel

Figure 7.6: Phase Truncation Error and the Phase Wheel

Key Rule for Spur Magnitude When the accumulator is large enough that $A - P \geq 4$ (which is almost always true in real DDS designs), then the maximum possible spur caused by phase truncation can be approximated as:

$$\text{Spur Level (dBc)} \approx -6.02P \quad (7.13)$$

That means the worst-case spur is about 6.02 dB lower for every bit used in the phase word.

Example: If we have:

- $A = 32$ bits (accumulator)
- $P = 12$ bits (phase word to lookup table)

Then the worst-case spur $\approx -6.02 \times 12 = -72$ dBc \rightarrow The spurious tones are 72 dB below the main signal — quite low (good spectral purity). This holds regardless of the tuning word, unless it happens to produce a "worst-case" pattern described below.

7.4.6 Tuning Words and Spur Severity

Not all tuning words (frequency settings) produce the same spur behavior. Some tuning words:

- Produce maximum spurs (worst spectral purity).
- Others produce no spurs at all (best possible purity).
- Most fall somewhere in between.

Finding the Worst-Case Tuning Words The worst-case spur happens when the tuning word T satisfies:

$$\text{GCD}(T, 2^{(A-P)}) = 2^{(A-P-1)} \quad (7.14)$$

where GCD = greatest common divisor.

This mathematical condition means the tuning word pattern repeats with a periodic error that aligns perfectly with the truncation error pattern — causing maximum correlation (and therefore strong spurs).

Bit Pattern for Worst-Case Tuning Word For these cases, the tuning word's binary form looks like this:

- A -bit accumulator
- MSB ... P bits used ... $A - P$ truncated bits
- $0xxxxxx10000...0000$
- The bit at position $2^{(A-P-1)}$ is 1
- All less significant bits are 0
- The MSB of the tuning word is 0 (to prevent aliasing)

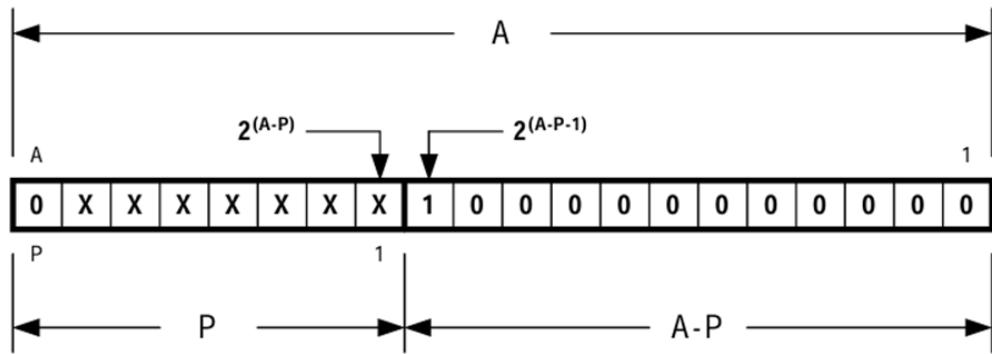


Figure 4.5. Tuning Word Patterns That Yield Maximum Spur Level

Figure 7.7: Tuning Word Patterns That Yield Maximum Spur Level

This bit configuration causes the worst phase truncation spur, equal to roughly $-6.02P$ dBc.

Tuning Words That Produce No Spurs At the other extreme, some tuning words produce no truncation spurs at all. These occur when:

$$GCD(T, 2^{(A-P)}) = 2^{(A-P)} \quad (7.15)$$

Bit Pattern for Spur-Free Case

- A -bit accumulator
 - MSB ... P bits used ... $A - P$ truncated bits
 - $0xxxxxx010000...0000$
 - A 1 appears at bit position $2^{(A-P)}$
 - All less significant bits are 0

Such tuning words cause the accumulator and truncated phase word to line up perfectly each cycle — so no periodic phase mismatch occurs → no truncation spurs.

All Other Cases If a tuning word does not match either special pattern above:

- The phase error partially correlates with the truncation pattern,
 - Producing intermediate-level spurs somewhere between:
 - 0 dBc (no spurs)
 - and $-6.02P$ dBc (worst case).

Summary Table

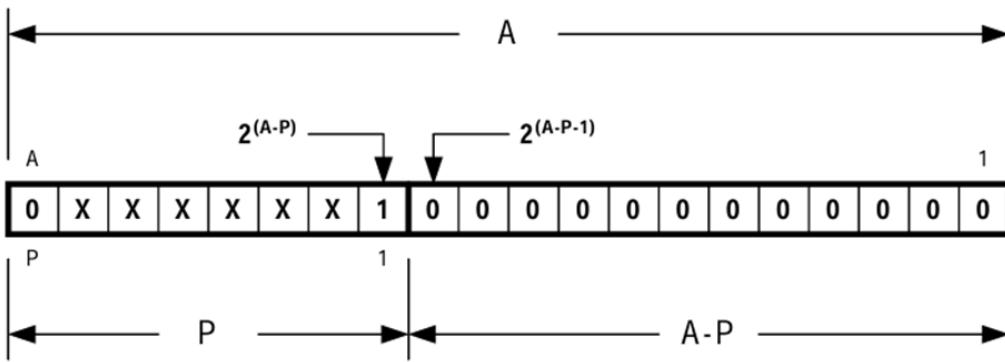


Figure 4.6. Tuning Word Patterns That Yield No Phase Truncation Spurs

Figure 7.8: Tuning Word Patterns That Yield No Phase Truncation Spurs

Case	Condition	GCD Equation	Bit Pattern
Worst-case spurs	Tuning word aligns with truncation pattern	$GCD(T, 2^{A-P}) = 2^{A-P-1}$	1 at bit
No spurs	Tuning word perfectly aligns	$GCD(T, 2^{A-P}) = 2^{A-P}$	1 at bit
Typical case	All other tuning words	—	—

7.4.7 Detailed Summary: Phase Truncation and Truncation Word Behavior

In a Direct Digital Synthesizer (DDS), the phase accumulator produces a high-resolution digital phase value. This value ideally consists of A bits. However, for practical reasons (such as reducing memory size in the lookup table), only the P most significant bits (MSBs) are used to generate the output waveform through the phase-to-amplitude converter. The remaining lower bits, known as the B -bit truncation word (where $B = A - P$), are discarded. These truncated bits represent fine phase information that is lost in the output waveform. Because this truncation is not random but systematic, it introduces a periodic phase error, which in turn produces spurious frequency components (spurs) in the DDS output.

1. Concept of the Truncation Word The P -bit phase word drives the waveform generator (lookup table and DAC). The B -bit truncation word is ignored—but this ignored portion still has an effect: it represents a residual phase error between the "true" high-resolution phase and the truncated (lower-resolution) phase that's used for output. This residual error behaves like a separate, periodic signal, and its characteristics depend on how the truncation bits change over time.

Thus, the output signal can be thought of as:

$$\text{Output} = \text{Ideal Signal (no truncation)} + \text{Error Signal (from truncation bits)} \quad (7.16)$$

The error signal is the main source of phase truncation spurs.

2. Analyzing the Truncation Word as Its Own Accumulator If we focus only on the B truncated bits, these can be modeled as a smaller B -bit accumulator on their own. The equivalent tuning behavior of this "mini-accumulator" is determined by the Equivalent Tuning Word (ETW):

$$ETW = T \pmod{2^B} \quad (7.17)$$

Where:

- T = the main tuning word of the DDS
- 2^B = the range of the truncation bits

So, the ETW represents the portion of the tuning word that directly affects the truncated bits.

3. Example In the example given in the reference:

- $A = 12$ (truncation bits being analyzed)
- $B = 12$
- $T = 2674$

Thus, $ETW = 2674$ (in decimal)

4. Determining the Truncation Word's Repetition and Overflow (a) Grand Repetition Rate (GRR) The GRR represents how often the truncation word's pattern repeats over time. It depends on how the accumulator cycles through all possible states before repeating. For the given parameters:

$$GRR = 2048 \quad (7.18)$$

This means the truncation word sequence repeats every 2048 clock cycles.

(b) Capacity and Overflow The capacity of the B -bit truncation accumulator is:

$$2^B = 4096 \quad (7.19)$$

Before finding how often it overflows, we must check if the MSB of the ETW is 1 (which indicates aliasing). In this example, it is 1, so we adjust the ETW by subtracting it from the capacity:

$$\text{Overflow Period} = \frac{2^B}{ETW_{adj}} = \frac{4096}{1422} = 2.88 \text{ cycles} \quad (7.20)$$

Thus, the truncation accumulator overflows roughly every 2.88 clock cycles.

(c) Number of Overflows within One GRR)

$$\text{Number of Overflows} = \frac{GRR}{\text{Overflow Period}} = \frac{2048}{2.88} \approx 711 \quad (7.21)$$

Hence, during each 2048-clock sequence, the truncation word overflows 711 times.

5. Sawtooth Behavior of the Truncation Word When plotted over time, the truncation word follows a sawtooth-shaped waveform because it accumulates linearly and then resets upon overflow.

- Period of the sawtooth ≈ 2.88 clock cycles
- Complete pattern repeats every 2048 clock cycles

This periodic sawtooth error creates a repetitive pattern in the DDS output phase.

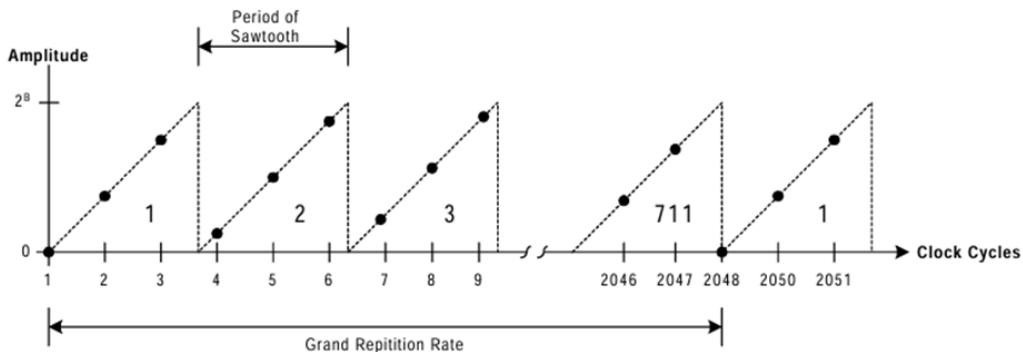


Figure 4.8. Behavior of the Truncation Word

Figure 7.9: Behavior of the Truncation Word

6. Frequency-Domain Implications Because the truncation word's error pattern is periodic, its Fourier transform consists of discrete spectral lines — these are the truncation spurs. Since the truncation word sequence is real, the Fourier spectrum is symmetric, so there are half as many unique frequency components as time-domain samples. → For 2048 time samples, there are 1024 discrete spur frequencies.

The fundamental frequency of this sawtooth is:

$$f_{fundamental} = F_s \times \frac{ETW_{adj}}{2^B} = F_s \times 0.3472 \quad (7.22)$$

The spectrum of a sawtooth wave contains harmonics of this fundamental frequency. These harmonics are evenly spaced at intervals of $0.3472F_s$.

7. Aliasing and Spur Folding Because these harmonics extend beyond the Nyquist frequency ($F_s/2$), they fold back (alias) into the Nyquist band.

- Odd multiples of $F_s/2$ fold directly into the Nyquist band.
- Even multiples fold as mirrored images.

This folding causes many closely spaced truncation spurs to appear across the DDS output spectrum, as illustrated in the reference's Figure 4.9.

8. Key Takeaways

- Truncation introduces a periodic phase error represented by the truncation word.
- The ETW defines how this truncation word evolves over time.
- The GRR defines how often the truncation sequence repeats.
- The sawtooth nature of the truncation error leads to harmonics and spurious tones.
- Aliasing folds these spurs into the Nyquist band, making them part of the observed output spectrum.

7.4.8 What Are Spurs?

Spurs (short for spurious signals) are undesired spectral components that appear in the output of a DAC (Digital-to-Analog Converter) or DDS (Direct Digital Synthesizer). They result from nonlinearities, switching transients, or coupling effects in the DAC system. Spurs degrade the spectral purity of the output signal and can limit system performance (e.g., in communication systems, ADC testing, or waveform synthesis).

How Spurs Are Calculated (Aliased Frequency) To find the aliased frequency of the N th harmonic spur: Compute remainder:

$$R = \text{remainder of } \frac{Nf_o}{F_s} \quad (7.23)$$

where:

- N = harmonic order (integer)
- f_o = fundamental output frequency
- F_s = DAC sampling frequency

Aliased Spur Frequency:

$$SPUR_N = \begin{cases} R, & R \leq \frac{F_s}{2} \\ F_s - R, & R > \frac{F_s}{2} \end{cases} \quad (7.24)$$

This gives the location (frequency) of each spur in the output spectrum. Magnitude depends on DAC nonlinearity, so it's device dependent.

Types of Spurs and Their Origins

Type	Cause	Description / Effect
Harmonic Spurs	DAC nonlinearities	Arise from imperfect DAC transfer characteristics — harmonics of the fundamental frequency that fold (alias) into the output band.
Switching Transient Spurs	Unequal rise/fall times, internal switching	Caused by non-symmetric or slow transitions in DAC elements; may cause ringing at the circuit's resonant frequency, visible as narrow spectral lines.
Clock Feedthrough Spurs	Capacitive/inductive coupling from internal clocks	High-frequency clocks couple into DAC output or sample clock, producing spikes at clock frequencies or symmetrical sidebands around the output tone.

Prevention / Control

- Use proper PCB layout and grounding.
- Isolate and shield high-frequency clock lines.
- Ensure balanced switching in DAC design.
- Maintain good power supply decoupling and clock integrity.

In Short

- Spurs = unwanted tones in DAC output.
- Equation: computed via aliasing of harmonics using $R = (Nf_o) \pmod{F_s}$.
- Sources: nonlinearities, switching transients, and clock coupling.
- Impact: reduce spectral purity, create interference, and limit SFDR (Spurious-Free Dynamic Range).

Wideband Spurs Definition: Measure of spurious signals across the entire Nyquist band of the DDS output spectrum. Depending on:

- DAC harmonics (main contributor).
- DDS core architecture — mainly phase truncation spurs caused by limited phase bit resolution.

Notes: Phase truncation spurs are randomly distributed across the spectrum and add to overall wideband spur content.

Narrowband Spurs Definition: Measure of spurious signals near the DDS output frequency (typically within 1% of the clock frequency). Depending on:

- System clock purity (jitter and noise) — main factor.
- Phase truncation spurs (only significant if they fall close to the output tone).

PLL Effect on Narrowband Spurs PLL (Phase-Locked Loop) introduces phase noise because it continuously adjusts its output phase and frequency to track a reference. This causes spectral line spreading (broadening) around the output frequency, degrading narrowband spur performance.

Predicting and Exploiting Spur "Sweet Spots" in DDS Concept: In DDS systems, if the exact output frequency is flexible, designers can choose a frequency within a band that minimizes spurious noise (spurs) in the desired passband. Key Idea: Since harmonic spurs (from DAC nonlinearity) appear at predictable frequencies, designers can tune the output frequency so that these spurs fall outside the band of interest. Result: By selecting a "spur sweet spot", the DDS output achieves cleaner spectral performance and lower in-band noise after filtering.

7.4.9 Jitter and Phase Noise Considerations in a DDS System

- **Jitter Sources:** The maximum achievable spectral purity in a synthesized sine wave is ultimately limited by the purity of the system clock used to drive the DDS. The ideal assumption of constant time intervals between samples is not perfectly met in practice due to variations known as timing jitter. The two primary causes of timing jitter are thermal noise (random motion of electrons in electric circuits, which sets the theoretical limit for minimizing jitter) and coupled noise (e.g., crosstalk, ground loops, or external EMI 'electromagnetic interference').

$$V_{\text{noise}} = \sqrt{4kTRB} \quad (7.25)$$

Ex on thermal noise: So, in a 3000 Hz bandwidth at room temperature (300°K) a 50Ω resistor produces a noise voltage of 49.8 nVrms. The important thing to note is that it

makes no difference where the center frequency of the 3kHz bandwidth is located. The noise voltage of the room temperature 50Ω resistor is 49.8 nVrms whether measured at 10kHz or 10MHz (as long as the bandwidth of the measurement is 3kHz).

Effects of Jitter on Spectrum: The way jitter affects the spectrum depends on its nature:

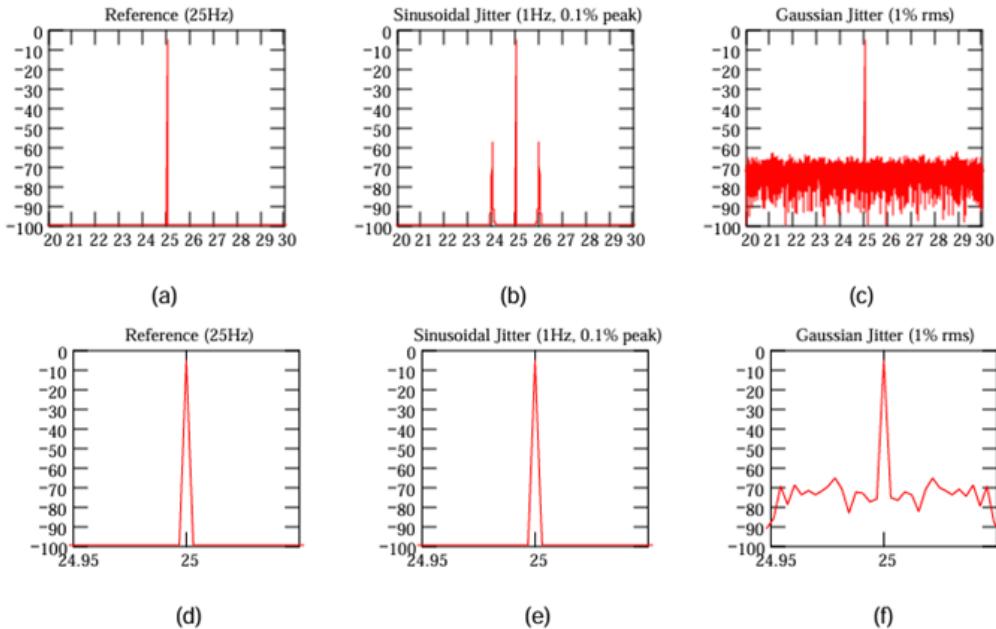


Figure 4.11. Effect of System Clock Jitter

Figure 7.10: Effect of System Clock Jitter

- **Sinusoidal Jitter:** Causes modulation sidebands to appear symmetrically around the fundamental output frequency. The separation distance from the fundamental equals the jitter frequency. Figure 4.11(a) and (d) show the spectrum of a pure sinusoid at a frequency of 25Hz. Note the single spectral line at 25Hz. This is the spectral signature of a pure sinusoid. The widening of the spectral line in Figure 4.11 (d) is a result of the finite resolution of the FFT used in the simulation. Easily we can determine the jitter frequency by separations of the sidebands (in figure b) is 1 Hz. Also we can measure the amplitude of the jitter by this equation:

$$\text{Peak Jitter Magnitude} = \frac{10^{(\text{dBc}/20)}}{\pi} \quad (7.26)$$

In our case (figure b):

$$\frac{10^{(-50/20)}}{\pi} = 0.001 \quad (\text{or } 0.1\%) \quad (7.27)$$

This value is relative to the period of the fundamental. Thus, the absolute jitter

magnitude is found by multiplying this result by the period of the fundamental (40ms). Thus, the peak jitter magnitude is $40\mu\text{s}$ (0.1% of 40ms).

- **Random (Gaussian) Jitter:** Results in an increase in the noise floor level and a broadening of the fundamental spectral line, a phenomenon known as phase noise, Figure (c, e).

- **Spectral Purity Limit:** Phase noise is important because it sets a limit on the maximum quality of the output signal. The overall DDS output phase noise is the sum of the phase noise contribution from the reference clock (which improves by due to frequency division) and the inherent residual phase noise of the DDS device and DAC. The output phase noise will never be better than the DDS device's inherent residual phase noise specification.

7.4.10 Output Filtering Considerations

This topic addresses the necessity and methods for conditioning the DDS output signal.

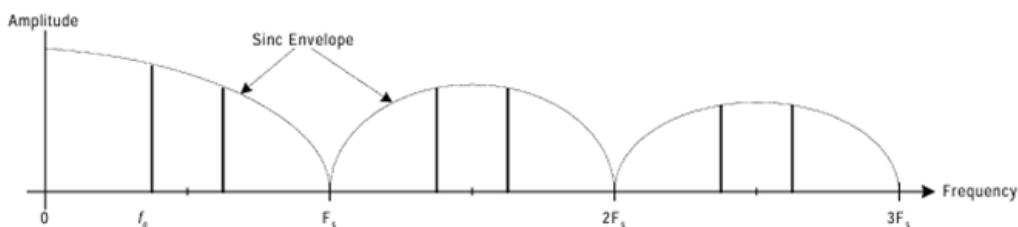


Figure 4.12. DDS Output Spectrum

Figure 7.11: DDS Output Spectrum

- **Sampled System Output:** The DDS is a sampled system, meaning its theoretical output spectrum is infinite. The output contains the desired fundamental frequency (f_o) plus numerous unwanted alias images at integer multiples of the sampling frequency ($F_s \pm f_o$, $2F_s \pm f_o$, etc.).

- **Sinc Rolloff:** The amplitudes of these frequencies follow a sinc ($\sin(x)/x$) rolloff envelope due to the Digital-to-Analog Converter's (DAC's) zero-order-hold characteristic.

- **Need for Anti-aliasing Filter:** To suppress these unwanted alias images in most applications, the DDS output must be followed by a lowpass "antialiasing" filter.

Filter Design Constraints: Because an ideal anti-alias filter (unity response up to and zero elsewhere) is not physically possible, some output bandwidth must be sacrificed to allow the filter to provide sufficient attenuation of alias images beyond the Nyquist limit ($1/2F_s$). A common rule limits the output bandwidth to approximately 40% of the clock frequency (F_{clock}) to allow for an economical lowpass filter implementation.

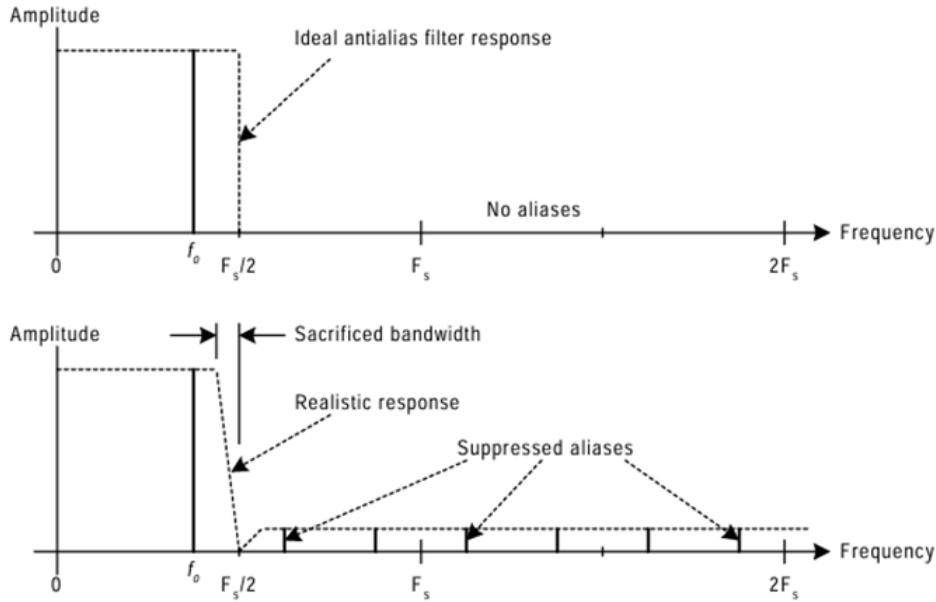


Figure 4.13. Antialias Filter

Figure 7.12: Antialias Filter

- **Filter Types:** The selection of a specific filter depends on the application's priority regarding frequency domain sharpness versus time domain smoothness.

- **Chebyshev Family:** Offers sharp frequency domain characteristics (steep roll-off), but typically results in poor time domain characteristics (overshoot and ringing). Examples include Butterworth, Chebyshev, Inverse Chebyshev, and Cauer-Chebyshev (elliptical). Elliptical filters are often preferred for antialiasing due to their steep transition region.

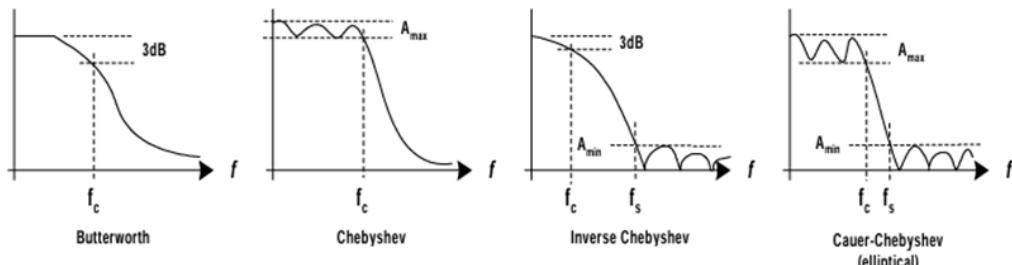


Figure 4.17. The Chebyshev Family of Responses

Figure 7.13: The Chebyshev Family of Responses

- **Gaussian Family:** Optimized for smooth time domain characteristics (minimal overshoot/ringing and constant group delay). Examples include Gaussian Magnitude, Bessel (optimized for maximally flat group delay), and Equiripple Group Delay responses.

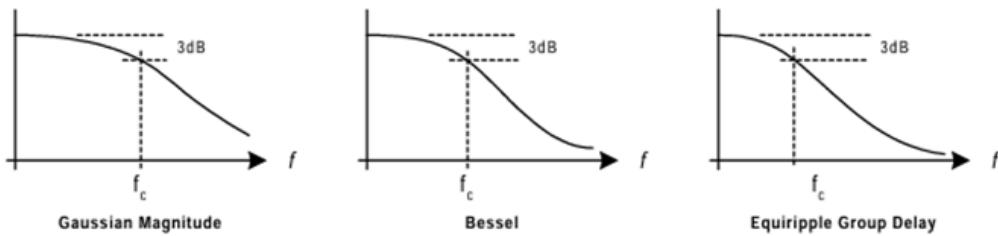


Figure 4.18. The Gaussian Family of Responses

Figure 7.14: The Gaussian Family of Responses

Characteristic	Chebyshev Family	Gaussian Family
Primary Optimization	Sharp frequency domain characteristics.	Smooth time domain characteristics.
Frequency Response	Exhibits a sharp, well-defined passband and a steep transition to the stopband.	Features a completely monotonic frequency response, meaning the attenuation curve always maintains a negative slope with no peaking in the passband or stopband.
Time Domain Response	Generally poor, characterized by significant overshoot and ringing and nonlinear group delay.	Well behaved, with little to no ringing or overshoot. Furthermore, the group delay is fairly constant.
Trade-off	Achieves a sharp frequency response at the cost of poor time domain performance (ringing and overshoot).	Achieves a smooth time domain response at the cost of a non-sharp transition between the passband and stopband.
Ideal Application	Applications where frequency domain characteristics are the dominant concern and where ringing/overshoot is not a major issue.	Applications where smooth time domain characteristics (minimal overshoot/ringing and constant group delay) are required.

7.4.11 Reference Clock Considerations

Why the Reference Clock Matters in DDS Systems: In a Direct Digital Synthesizer (DDS), the reference clock defines the timing of every output sample. Any imperfection in the clock (jitter, phase noise, or frequency drift) directly affects the output waveform quality. The DDS output accuracy depends on:

- Amplitude accuracy → (DAC performance)

- Time accuracy → (reference clock purity)

Phase-Noise Scaling Rule: Phase noise at the DDS output is lower than the clock's by the following formula:

$$20 \log_{10} \left(\frac{F_{out}}{F_{clk}} \right) \quad (7.28)$$

Reference clock edge uncertainty adversely affects DDS output signal quality.

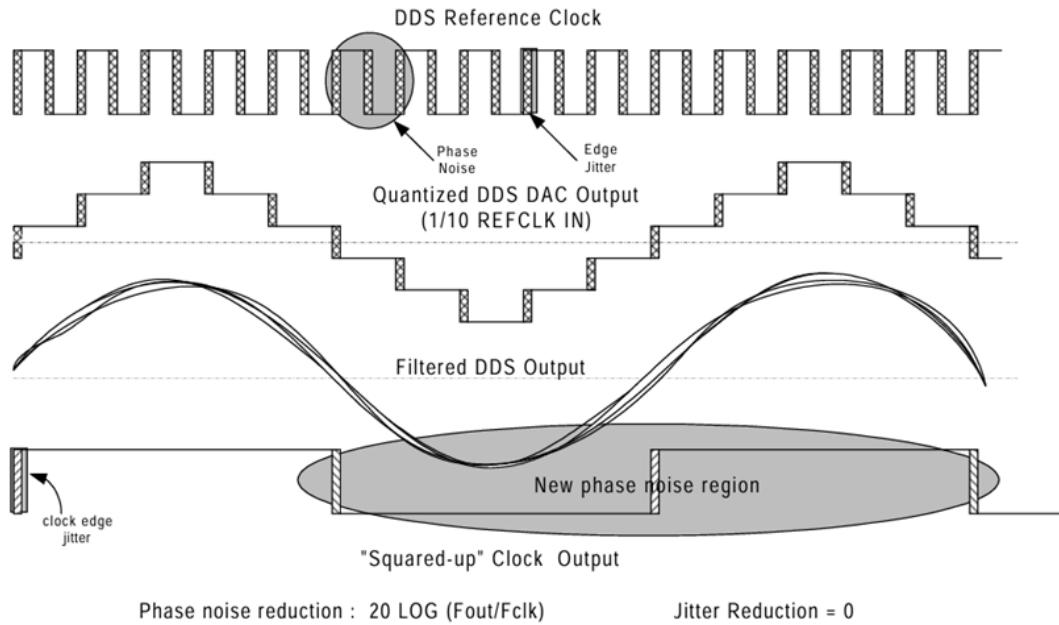


Figure 7.15: "Squared-up" Clock Output

while absolute edge jitter remains constant across frequencies, its percentage of the total period decreases as frequency decreases. Thus, dividing frequency reduces phase-noise percentage even though the actual time jitter is unchanged. This explains why frequency division improves phase-noise performance in DDS systems.

In order for the digital phase step to be properly positioned in the analog domain two criteria must be met:

- Appropriate amplitude (this is the DAC's job)
- Appropriate time (the clock's job)

The phase noise improvement of the DDS output relative to the input clock becomes more apparent in the frequency domain.

Figures 5-2 and 5-3 compare two DDS clock sources: the 100 MHz clock source 1 has higher phase noise than source 2, resulting in a noisier DDS output. At 10 MHz output, source 1 shows a 20 dB ($10\times$) phase-noise improvement relative to its input,

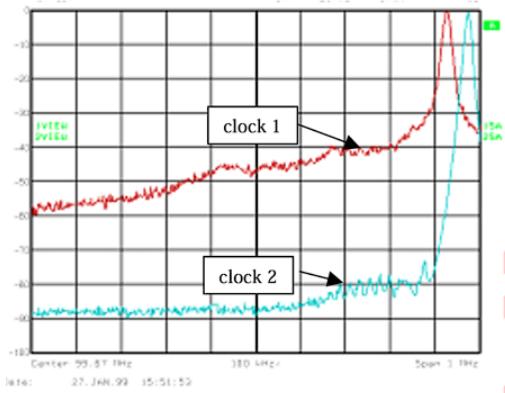


Figure 5-2: Good and poor clock phase noise

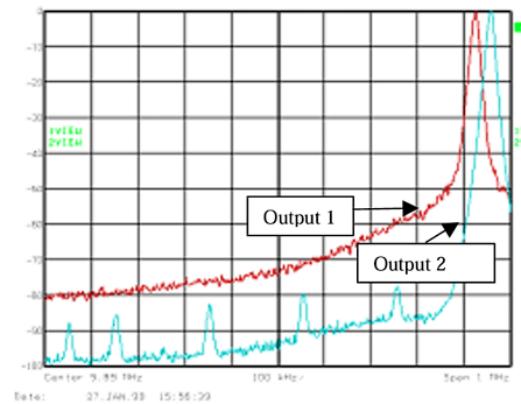


Figure 5-3: DDS output Response

Figure 7.16: Good and poor clock phase noise

Figure 7.17: DDS output Response

while source 2's improvement is limited by the analyzer's noise floor. Low-level spurious signals appear on the skirts of output 2 due to phase-bit truncation and transformation algorithms, also present but masked in output 1. This demonstrates that low phase noise is essential for maintaining a high signal-to-noise ratio in radio and other noise-sensitive systems. Overall DDS output phase noise is the sum of the phase noise of the reference clock source (after it has been enhanced by the frequency division quality of the DDS) and the residual phase noise of the DDS.

Using an Internal Reference Clock Multiplier Circuit:

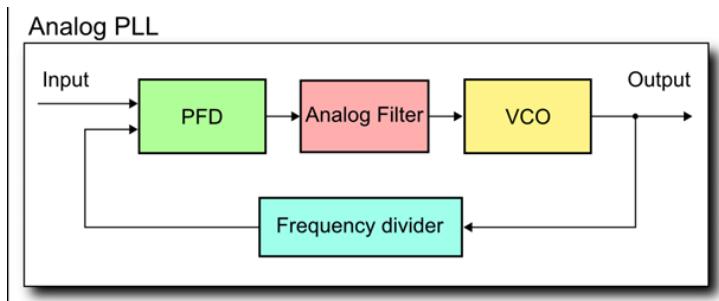


Figure 7.18: Analog PLL

Many Analog Devices DDS products include on-chip reference clock multipliers ($\times 4$, $\times 20$) that can be enabled or bypassed, allowing the use of lower-frequency oscillators while achieving high internal clock rates. This simplifies synchronization with system "master clocks" and reduces oscillator cost. However, using the REFCLK multiplier involves a tradeoff in output signal quality, since frequency multiplication degrades phase noise by a factor.

for example, a $6\times$ multiplier worsens -110 dBc/Hz noise to -94.5 dBc/Hz. Additionally, the PLL loop filter may cause phase-noise peaking near its cutoff frequency. Figure

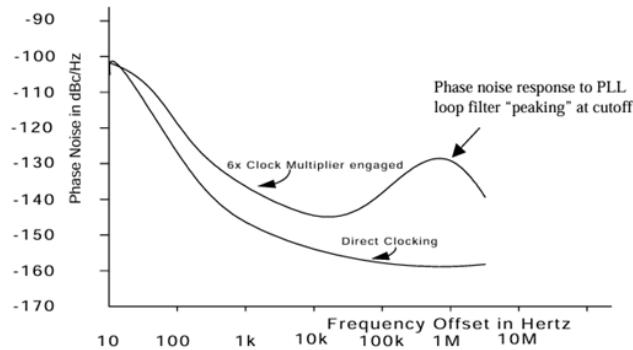


Figure 7.19: Phase noise response to PLL loop filter "peaking" at cutoff

5-4 illustrates this degradation in the AD9851, where the entire loop filter is on-chip.

7.4.12 DDS SFDR Performance

Use of reference clock multiplication also has an impact on SFDR.

Figure compares DDS outputs with and without a $6\times$ clock multiplier. The multiplied output shows -68 dBc SFDR, while the directly clocked output achieves -78 dBc, indicating about 10 dB degradation. Output 1 also exhibits a slightly higher noise floor, confirming the phase-noise penalty of clock multiplication.

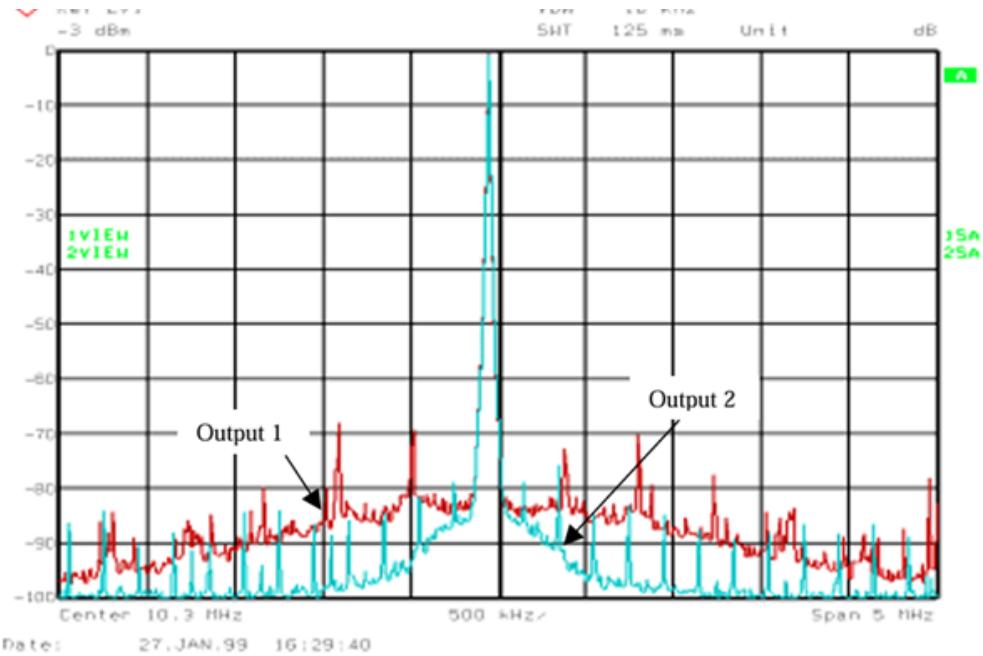


Figure 5-5. Spectral Plot of DDS Output With & Without Reference Clock Multiplication

Figure 7.20: Spectral Plot of DDS Output With & Without Reference Clock Multiplication

Chapter 8

FFT Implementation for OFDM + Chirp Sensing

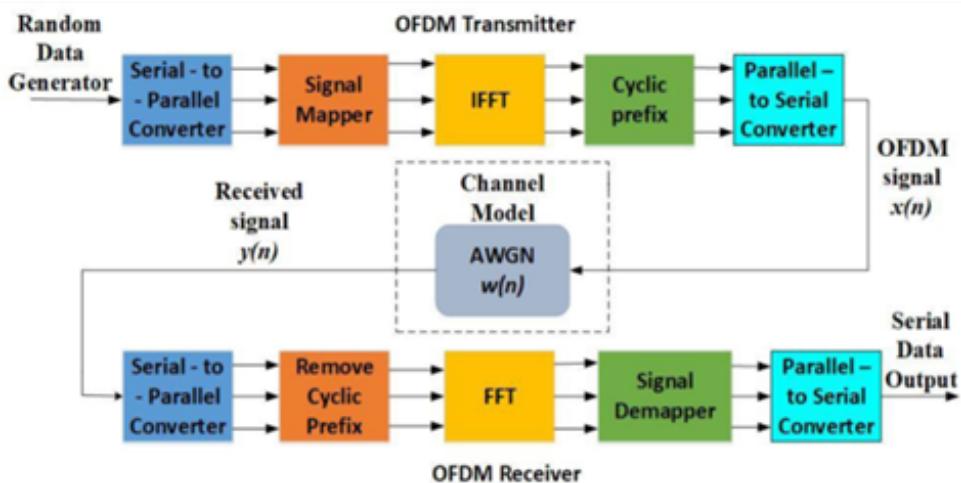
8.1 FFT Introduction

In modern communication systems—especially OFDM (Orthogonal Frequency Division Multiplexing) and chirp-based sensing systems—the Fast Fourier Transform (FFT) is one of the most critical building blocks. The FFT performs efficient transformation between the time domain and the frequency domain, enabling modulation, demodulation, spectrum shaping, multi-carrier processing, and channel estimation.

In our project, which combines OFDM signaling with chirp sensing, the FFT plays a dual role:

- **OFDM Demodulation / Modulation:** IFFT at transmitter, FFT at receiver.
- **Chirp Radar Sensing:** Spectral analysis of reflected chirp signals.

Because both functionalities rely heavily on frequency-domain operations, an optimized FFT architecture is essential.



8.2 FFT Overview

The Discrete Fourier Transform (DFT) is given by:

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{kn} \quad (8.1)$$

where:

$$W_N = e^{-j \frac{2\pi}{N}}$$

A direct DFT takes $O(N^2)$ operations, which is too slow for communication systems operating in real time.

8.2.1 Fast Fourier Transform (FFT)

FFT algorithms reduce complexity to:

$$O(N \log_2 N)$$

This is achieved by:

- Exploiting symmetry properties of complex exponentials.
- Decomposing the input sequence into smaller sub-sequences.
- Using butterfly operations repeatedly.

This computational efficiency is crucial in OFDM and radar, where FFT must run every symbol or frame.

8.3 The Butterfly Operation

A butterfly is the fundamental building block of the FFT. It performs two outputs using two inputs. For Decimation in Frequency (DIF), the operation is defined as:

$$\begin{aligned} A &= x[n] + x[n + N/2] \\ B &= (x[n] - x[n + N/2]) \cdot W_N^k \end{aligned}$$

Where W is a twiddle factor.

8.3.1 Types of Butterflies

Butterflies differ by:

- Order of inputs.
- Order of outputs.
- How twiddle factors are applied.
- Whether they are used in Decimation in Time (DIT) or Decimation in Frequency (DIF).

Most common types:

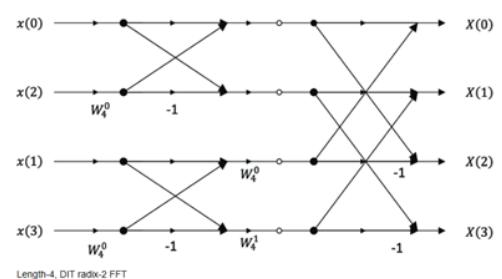
- **Radix-2:** Simple, widely used, low area.
- **Radix-4:** Faster, but more complex.
- **Mixed-radix:** Flexible.
- **Split-radix:** Optimal mathematically but complex to hardware-implement.

For OFDM hardware (like LTE/WiFi modems), **Radix-2 DIF** or **Radix-4 DIF** is the strongest candidate because it maps well to pipelined structures.

8.4 DIT vs. DIF FFT

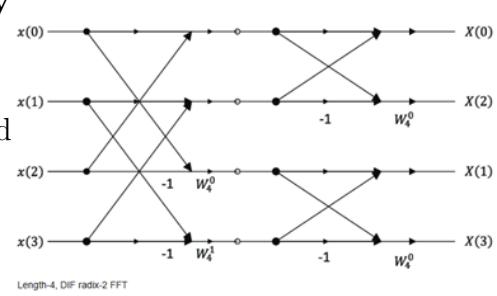
8.4.1 Decimation in Time (DIT)

- Splits input sequence into even and odd indices.
- Bit-reversal required at the input.
- Twiddle factors multiply early.



8.4.2 Decimation in Frequency (DIF)

- Splits the output spectrum into even- and odd-indexed parts
- Bit-reversal applied at the output.
- Twiddle factors multiply later.



Which is better for hardware?

DIF is generally preferred for hardware FFTs because:

- Early stages require fewer twiddle multipliers
- Easier pipeline mapping
- Data flow is more regular

Which do we use in OFDM?

Most OFDM FFT IP cores use **Radix-2 or Radix-4 DIF**.

Summary: DIF vs DIT FFT

Decimation-in-Time (DIT) breaks the input sequence into even and odd samples, performs butterflies **after twiddle multiplication**, and produces output in **normal order** but requires the **input to be bit-reversed**.

Decimation-in-Frequency (DIF) breaks the frequency spectrum into even and odd bins, performs butterflies **before twiddle multiplication**, starts with only add/sub operations (no multipliers in stage 1), and produces **bit-reversed output** from **normal input**.

They compute the same FFT, but their internal data flow, twiddle placement, and memory ordering differ—leading to different performance and hardware cost.

8.4.3 Comparison Table

Below is a comparison to determine which is better for hardware. Most OFDM FFT IP cores use Radix-2 or Radix-4 DIF.

Table 8.1: Detailed Comparison: DIT vs. DIF Architecture

Feature	DIT (Decimation-in-Time)	DIF (Decimation-in-Frequency)
Main Concept	Splits the input sequence in the time domain (even/odd samples)	Splits the frequency domain output into even/odd frequency bins
Butterfly Structure	Twiddle factor multiplication happens before add/sub	Add/sub happens first, twiddle multiplication applied after
First Stage Complexity	Multipliers required in stage 1	No multipliers in stage 1 (only adders/subtractors)
Last Stage Complexity	Last stage needs no twiddle factors	Last stage uses twiddles
Input Order	Requires bit-reversed input	Accepts normal input order
Output Order	Output in normal sequence	Produces bit-reversed output
Memory Access Pattern	Complicated on input side	Complicated on output side
Twiddle Factor Count	Uniform across stages	More twiddles in later stages, none in first
Latency Characteristics	Higher early-stage latency due to multiplications	Lower early-stage latency; multipliers appear later
Pipelining Suitability	Harder to pipeline early stages	Highly pipeline-friendly (SDF, MDC architectures)
Hardware Area	Larger (multipliers active from stage 1)	Smaller area (stage 1 = adder-only)
Power Consumption	Higher due to multipliers in more stages	Lower power, especially in first half of pipeline
Best Use Case in Comm. Systems	Often preferred for IFFT (OFDM transmitter)	Dominant choice for FFT (OFDM receiver)
Data Reordering Needed	Input needs reordering	Output needs reordering
Numerical Accuracy	Slightly higher rounding noise early	More balanced noise over stages
Industry Use (LTE/5G/WiFi)	Used mostly in TX IFFT cores	Widely used in RX FFT cores

- **DIT FFT:** Bit-reversed input → Multiply by Twiddles → Butterfly → Normal Output.
- **DIF FFT:** Normal Input → Butterfly → Multiply by Twiddles → Bit-reversed Output.

8.5 FFT Hardware Architecture Types

Modern FFT hardware generally falls into three major architectural families depending on how they handle scaling, dynamic range, and FFT size flexibility. These are:

- Fixed Data Point FFT (Fixed-Length FFT)
- Variable Data Point FFT (Reconfigurable FFT)

8.5.1 Fixed Data Point FFT (Fixed-Length)

Definition: Hardware designed for one fixed FFT size (e.g., 64 or 4096 points).

Pros: Simple, low power.

Cons: Completely inflexible. If the size changes, hardware must be redesigned.

8.5.2 Variable Data Point FFT (Reconfigurable)

Definition: Flexible architecture supporting multiple sizes (e.g., 128/256/512) using the same hardware.

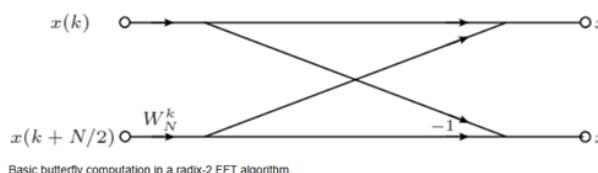
Pros: One design supports many bandwidths (ideal for LTE, 5G, Wi-Fi).

Mechanism: Dynamically changes stages, memory addressing, and twiddle selection.

8.6 Radix-2 vs. Radix-4 FFT

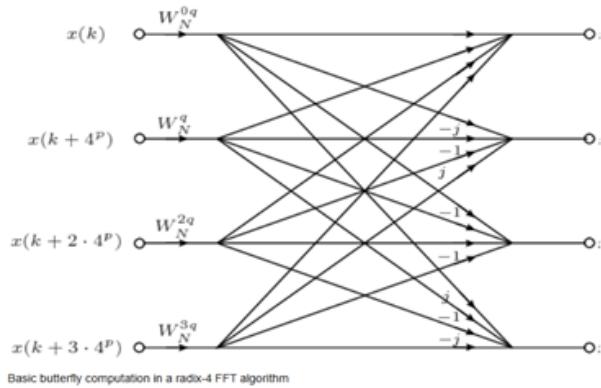
8.6.1 Radix-2 FFT

- **Structure:** Each butterfly processes 2 inputs. Number of stages = $\log_2(N)$.
- **Pros:** Simple hardware, easy to pipeline, small twiddle ROM.
- **Cons:** More stages, more total multiplications, higher latency for large N.



8.6.2 Radix-4 FFT

- **Structure:** Groups 4 samples. Number of stages = $\frac{1}{2} \log_2(N)$.
- **Pros:** Fewer stages (lower latency), lower power for high N.
- **Cons:** Complex butterfly, harder to pipeline.



8.7 Serial vs. Parallel Architectures

8.7.1 Parallel FFT

All butterfly stages operate simultaneously.

Advantages

- Very high throughput
- One FFT per clock (if fully parallel)
- Suitable for high-bandwidth systems (5G NR, WiFi 6, radar processing)

Disadvantages

- **Large area**
- Higher power consumption
- Requires many multipliers + adders

Summary: Parallel FFT = high performance, high area.

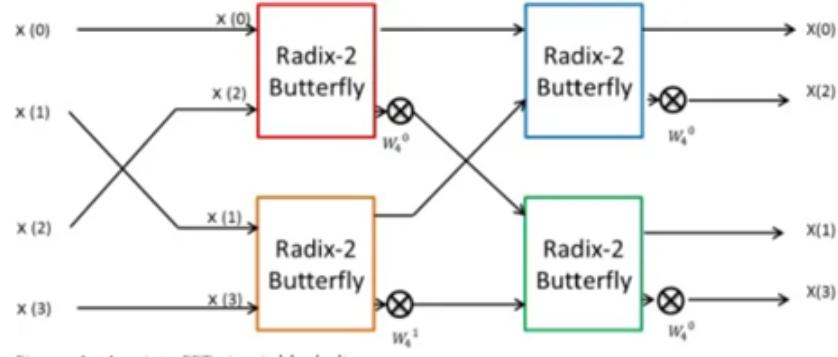


Figure 4: 4 points FFT circuit block diagram

Figure 8.1: 4 points FFT circuit block diagram

8.7.2 Serial FFT (Pipeline FFT)

Single-path Delay Feedback (SDF)

- Data flows in serially.
- Buffers (delay lines) store intermediate results.
- Only one butterfly unit is reused across all stages.

Multi-path Delay Commutator (MDC)

- Multiple data paths
- Higher throughput than SDF
- Still much smaller than full parallel

Advantages

- **Huge area reduction** because only one butterfly is reused
- Very efficient for ASIC and FPGA
- Fits low-power or resource-constrained systems

Disadvantages

- Higher latency

- Throughput limited to "one output every clock" after pipeline fill

8.8 FFT in OFDM and Chirp Sensing

OFDM uses FFT/IFFT for modulation and demodulation:

8.8.1 FFT in OFDM

Transmitter

- IFFT maps frequency-domain QAM symbols onto subcarriers
- Output is the composite OFDM waveform

Receiver

- FFT converts received signal to frequency-domain
- Subcarriers are separated
- QAM symbols recovered

Why FFT is essential for OFDM

Because OFDM uses **orthogonal** subcarriers spaced by:

$$\Delta f = \frac{1}{T_{\text{symbol}}}$$

The FFT perfectly reconstructs these subcarriers due to its orthogonality property.

8.8.2 FFT for Chirp Sensing

Chirp-based sensing uses FMCW signals:

- A chirp sweeps frequency linearly.
- Reflected signal mixes with transmitted.
- FFT converts beat signal to "range spectrum".

Thus:

- Range = FFT of beat frequency
- Velocity = FFT across chirps (Doppler FFT)

Our project blends OFDM communications with chirp sensing, so FFT appears in **both communication and sensing pipelines**.

8.9 IFFT for OFDM System

IFFT Rule in OFDM system

The IFFT's job is to transform digital data into a transmittable waveform – it takes parallel frequency-domain QAM symbols and converts them into a serial time-domain signal that can be modulated and sent over the air.

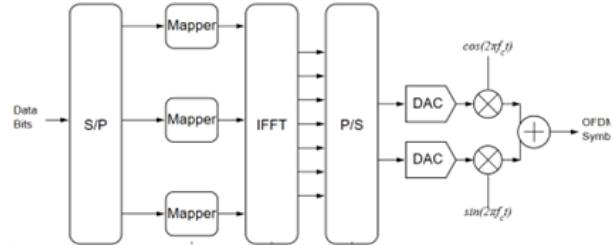


Figure 8.2: OFDM Transmitter Block Diagram

Mathematical approach

So far we have considered algorithms to compute the DFT in a fast and efficient way using different FFT Architectures.

What about the inverse DFT?

There are two approaches we can use. Consider the equation of the inverse DFT:

$$\begin{aligned}
x[n] &= \frac{1}{N} \sum_{k=0}^{N-1} X[k] W_N^{-kn} \\
&= \frac{1}{N} \left(\sum_{k=0}^{N-1} X^*[k] W_N^{kn} \right)^* \\
&= \frac{1}{N} (\text{DFT}\{X^*[k]\})^* \\
&= \frac{1}{N} \text{Conj}(\text{DFT}\{\text{Conj}(X[k])\})
\end{aligned}$$

The DFT equation can be written as follows:

$$\mathbf{X} = \mathbf{W} \cdot \mathbf{x}$$

Thus we can write the inverse DFT equation in the matrix form as follows:

$$\mathbf{x} = \frac{1}{N} \mathbf{W}^* \cdot \mathbf{X}$$

That is:

$$x = \frac{1}{N} \sum_{k=0}^{N-1} X[k] w_k^*$$

Hardware Implementation Steps

Circularly fold input $X[k]$, feed folded sequence to FFT block, and scale output by $1/N$.

We need a **Reorder Block** that converts the FFT's negative exponent into the positive exponent of the IDFT by applying the index transformation:

$$k \rightarrow -k$$

before the FFT.

Advantages

- Reuses FFT hardware
- No complex conjugators are needed

Disadvantages

- Needs Reorder buffer (N memory elements)
- Extra latency from Reordering
- Complex address generation for folding

8.10 Summary for Our Project

Here is the final tailored summary that ties everything back to our OFDM + chirp sensing system:

- We use **FFT/IFFT** as the backbone of both OFDM communication and chirp sensing.
- The **butterfly** is the core computation unit (Radix-2 DIF recommended).
- **DIF FFT** is preferable for hardware due to better pipeline structure.
- Since our OFDM system processes data **per symbol**, we do **not need** fully parallel FFT.
 - **Serial SDF FFT** gives huge area savings while meeting throughput.
- In MATLAB, we use FFT as a golden model and verify:
 - OFDM symbol recovery
 - Range-Doppler maps for chirp sensing
 - Correctness of FFT architecture

8.10.1 Architecture Comparison

Table 8.2: Detailed Comparison of FFT Architectures

Architecture	Hardware Complexity	Memory Requirement	Throughput	Latency	Area Efficiency	Notes
Radix-2 DIF/DIT (Fully Parallel / Single-Stage)	Very High (many butterflies)	Very High	Very High (one FFT per clock)	Very Low	Very Low	Used only in high-performance ASIC; hardware-heavy and expensive.
Radix-2 Multi-Path Delay Commutator (MDC)	Medium-High	Medium	High (streaming: 1 sample/clock)	Medium	Medium	Good for real-time systems; pipelined; requires several delay lines.
Radix-2 Single-Path Delay Feedback (SDF)	Low	Very Low	High (1 sample/clock)	Higher than MDC	High	Most area-efficient streaming architecture, widely used in FPGA/ASIC.
Radix-2 Memory-Based / Iterative (In-place)	Very Low	Medium (full RAM for N points)	Low ($N \log N$ clocks per transform)	Very High	Excellent	Best for low-power systems where time is not critical.
Radix-2 Folded Architecture	Low-Medium	Very Low	Moderate	High	Very High	Reduces hardware by time-multiplexing butterflies; good for ASIC with moderate throughput.

Table 8.3: Comparison of FFT Architectures for Project Selection

Architecture	Complexity	Memory	Throughput	Latency	Area
Fully Parallel	Very High	Low	Max	Min	Worst
MDC	High	Medium	High	Medium	Medium-High
SDF	Low	Lowest	1 sample/clk	Highest	Best
Folded	Low-Medium	Low	Moderate	High	Very High

Selected Architecture: SDF (Single-Path Delay Feedback)

- Best choice for a production-quality 4,096-point FFT (streaming, balanced area & throughput, good for FPGA/ASIC RTL): SDF (Single-Path Delay Feedback).

Reason: very area-efficient, 1 sample/clock streaming, mature control patterns, widely used in RTL implementations.

- Easiest choice (fast to model and verify; minimal RTL complexity): Iterative / Memory-Based In-Place FFT (single butterfly reused).

Reason: very simple control and dataflow, simplest RTL FSM and memory addressing — great to get a correct, fixed-point FFT working quickly.

- **Recommended project approach:** Start with **Iterative (memory-based)** in MATLAB to verify numerics and fixed-point choices, then move to **SDF RTL** for the final implementation.

8.11 MATLAB Reference Model Results

A floating-point FFT and IFFT model was created for one OFDM symbol with Cyclic Prefix (CP).

```

5      %% Parameters (5G NR-like)
6      N = 4096;           % FFT size
7      Ncp = 288;          % Cyclic prefix length (approx)
8      fs = 122.88e6;       % 122.88 MHz sampling rate (5G NR
9      subcarrier_spacing = 30e3; % 30 kHz
10

55     %% Channel (optional real-world channel)
56
57     % AWGN SNR test
58     snr_dB = 30;
      y_cp = awgn(x_cp, snr_dB, 'measured');

```

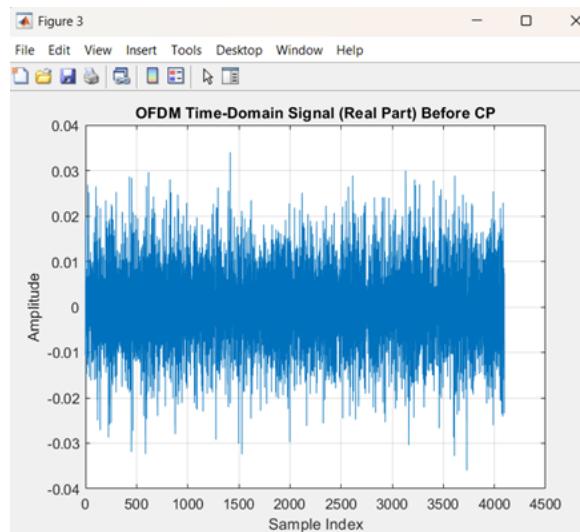


Figure 8.3: Ofdm symbol(Ifft)

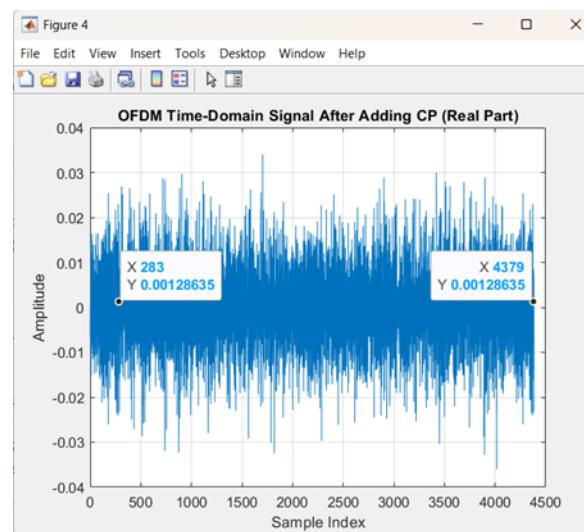


Figure 8.4: Ofdm after adding cyclic prefix

The cyclic prefix (CP) is formed by copying the first N_{cp} samples of the OFDM symbol and appending them to the end of the symbol. In this case, the original symbol length is 4096 samples. After adding a cyclic prefix of length $N_{\text{cp}} = 288$, the total symbol length becomes

$$4096 + 288 = 4384 \text{ samples.}$$

The two highlighted points in the graph verify that the cyclic prefix is an exact copy of the first N_{cp} samples of the symbol. For example, sample number 283 in the cyclic prefix corresponds to sample number

$$4096 + (288 - 5) = 4079$$

in the original symbol. Both samples have the same amplitude, confirming the cyclic prefix construction.

By extension, this relationship holds for all samples in the cyclic prefix; that is, the first 288 samples of the symbol are identical to the last 288 samples after the cyclic prefix is added.

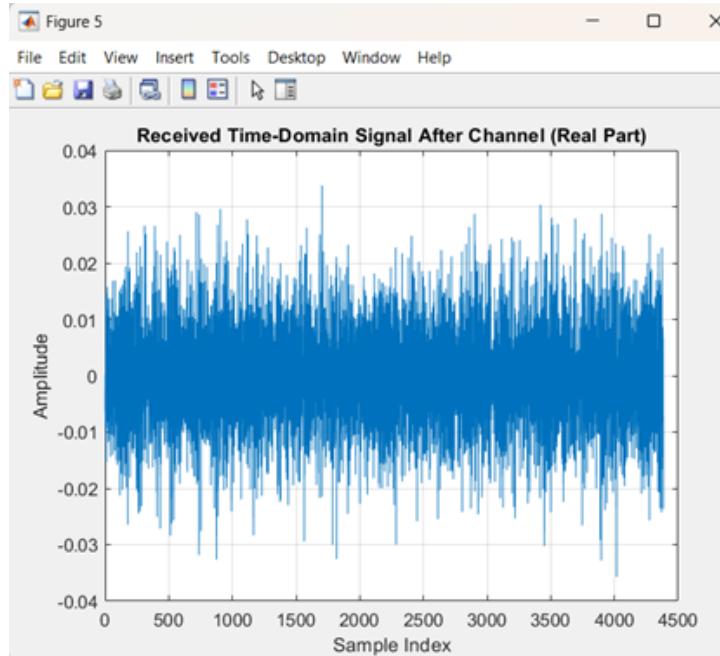


Figure 8.5: Received OFDM Before removing CP (after FFT).

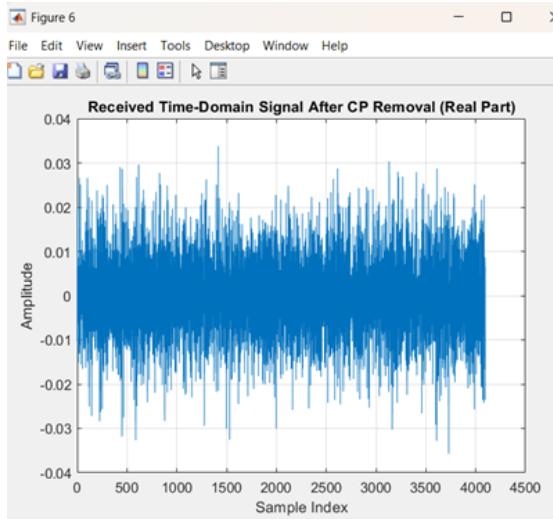


Figure 8.6: Received OFDM after removing CP.

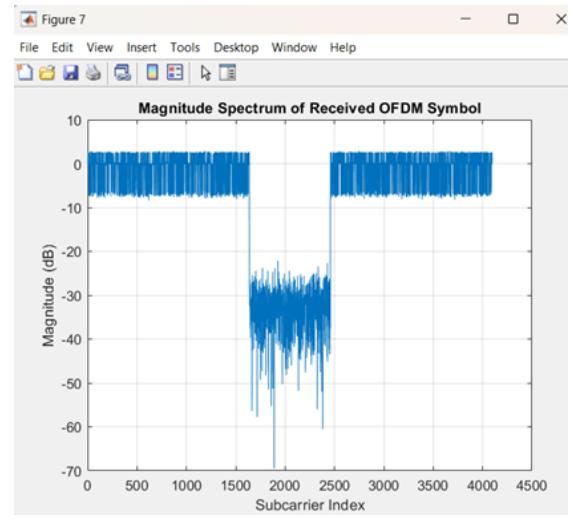


Figure 8.7: Magnitude Spectrum of OFDM.

8.11.1 Performance Metrics

- **SNR = 30 dB with 16-QAM randomized symbols:**

The received constellation shows noticeable noise effects.

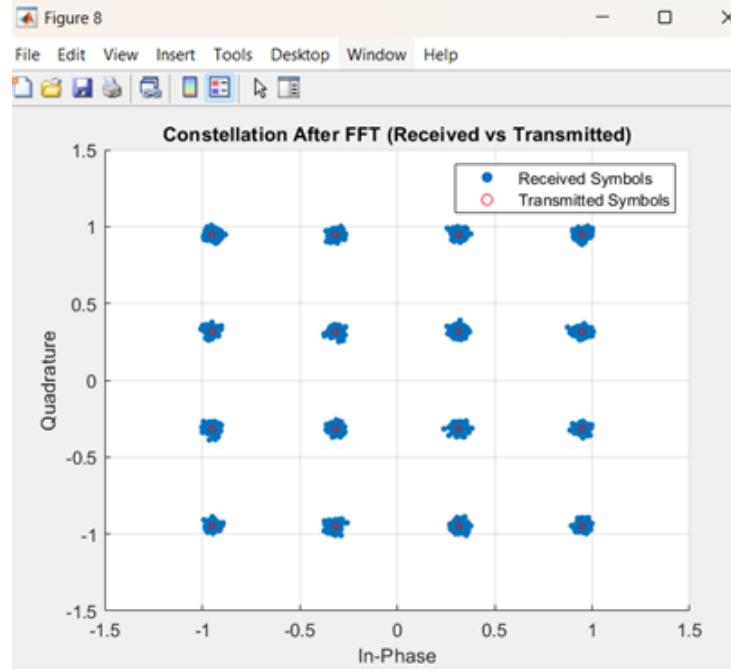


Figure 8.8: Performance metrics at SNR = 30 dB

Observation:

Significant clustering is observed around the ideal 16-QAM coordinates.

- **SNR = 60 dB:**

The constellation of the received symbols is approximately identical to the transmitted symbols.

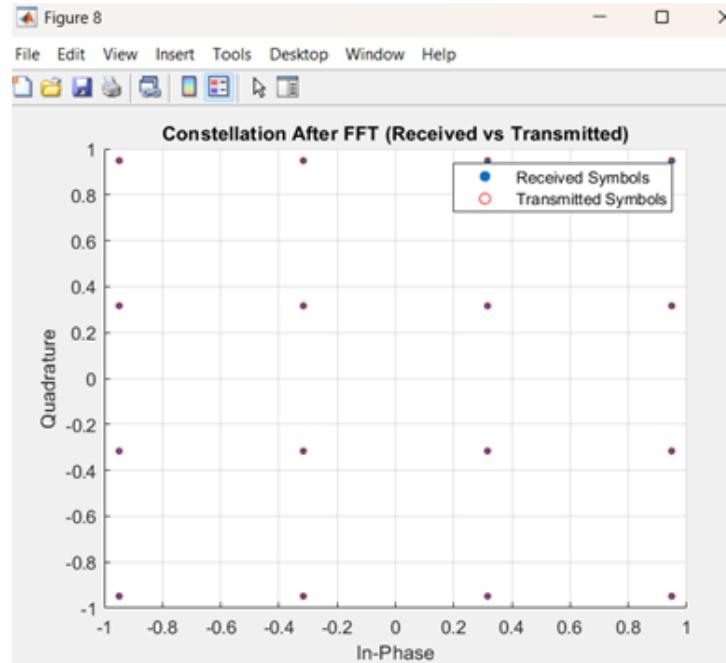


Figure 8.9: Performance metrics at SNR = 60 dB

- **MSE:**

The comparison of the mean square error at different SNR levels is shown below.

```
MSE between transmitted X and received FFT Y = 0.000804364458
fx >> |
```

Figure 8.10: MSE at SNR = 30 dB

```
MSE between transmitted X and received FFT Y = 0.000000000082
fx >>
```

Figure 8.11: Mean Square Error comparison at different SNR levels

Chapter 9

Signal Processing Simulations

9.1 Signal Placement Strategies

The following table summarizes the different strategies for placing radar and communication signals:

Case	Description	How Signals are Placed	Pros	Cons
Separate Bandwidth (Non-overlapping)	Chirp and OFDM occupy different frequency bands.	- Chirp centered at one carrier - OFDM centered at a different carrier	- No mutual interference - Easy to separate at receiver (filters) - Lower EVM	- Wastes spectrum - Larger total bandwidth needed - Higher Cost
Same Bandwidth (Overlapping)	Chirp and OFDM occupy overlapping frequencies.	Both signals occupy the same band	- Efficient use of spectrum - Single band for TX/RX - Lower Cost	- Interference between radar and communication - More complex separation - Higher EVM
Time-Division Multiplexing (TDM)	Transmit chirp and OFDM in different time slots.	- First transmit chirp → sense → then transmit OFDM → communicate	- No spectral interference - Uses same hardware	- Reduced real-time data throughput - Latency introduced

Table 9.1: Comparison of Signal Placement Strategies

9.2 DDS TOOL

9.2.1 Single Tone Generation

We were able to verify theoretical information in the reference through the simulation results.

Different Target output frequencies:

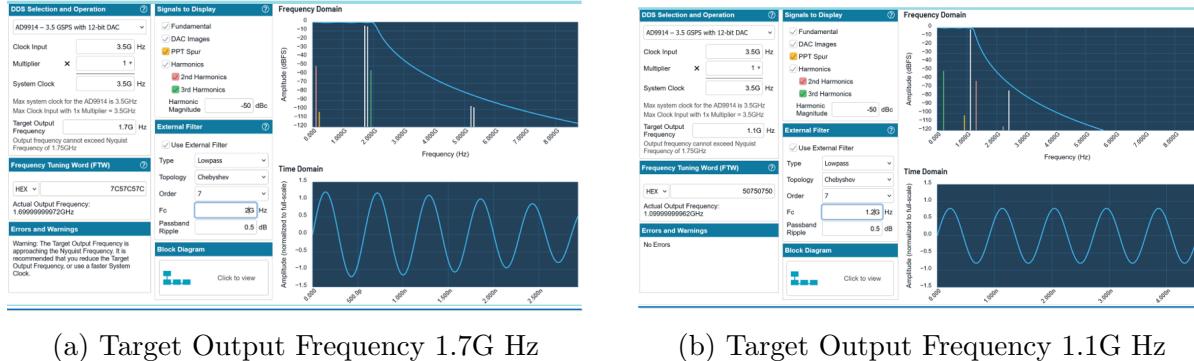


Figure 9.1: DDS Selection and Operation

Signal is less distorted when following the criterion of $F_{out} <$ a third of the system clock frequency as the number of images and harmonics included in the passband are less.

Testing the example from the reference:

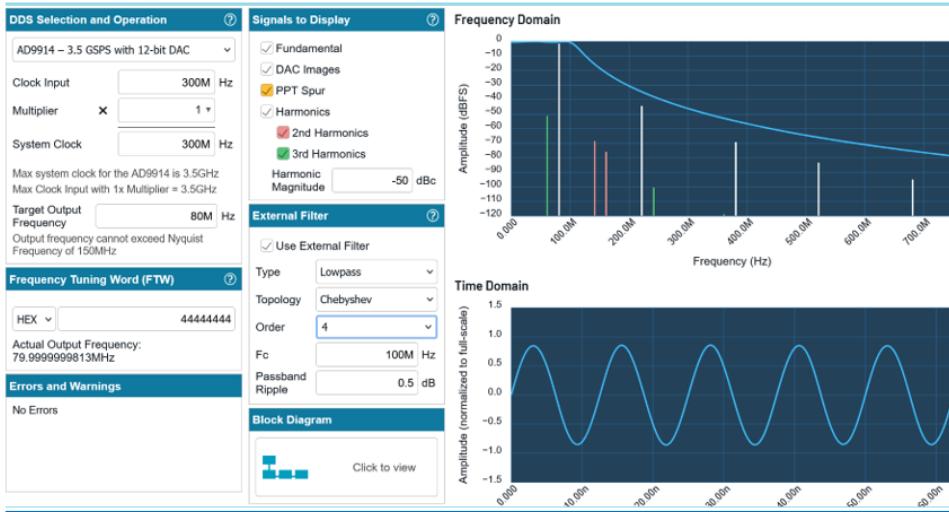


Figure 9.2: Testing reference example with $F_{clk} = 300$ MHz

An understanding of sampling theory is necessary when analyzing the sampled output of a DDS-based signal synthesis solution. The spectrum of a sampled output is illustrated

below. In this example, the sampling clock (f_{CLOCK}) is 300 MHz and the fundamental output frequency (f_{OUT}) is 80 MHz.

An understanding of sampling theory is necessary when analyzing the sampled output of a DDS-based signal synthesis solution. The spectrum of a sampled output is illustrated in Figure 2-1. In this example, the sampling clock (f_{CLOCK}) is 300 MHz and the fundamental output frequency (f_{OUT}) is 80 MHz.

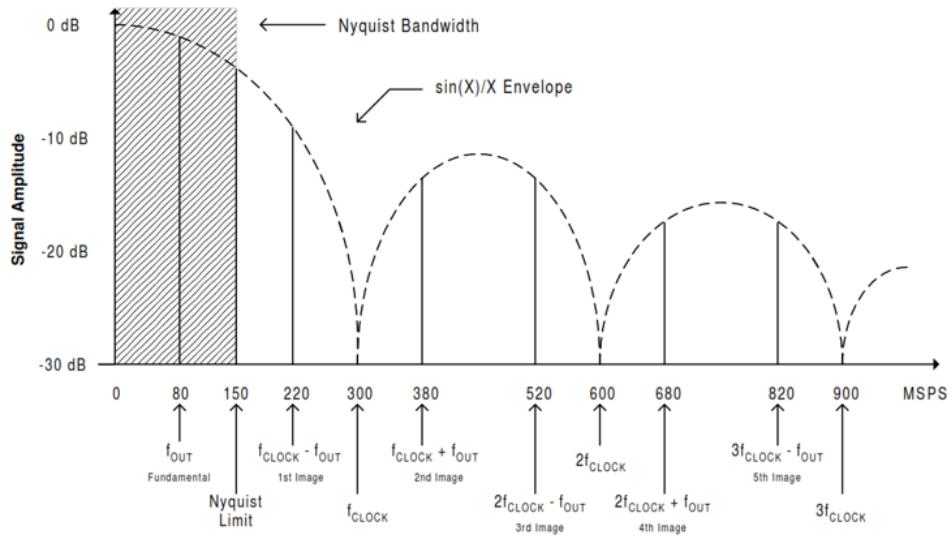


Figure 9.3: Sampling Theory Illustration

We can see that the results match where: With $F_{clk} = 300$ MHz and $f_0 = 80$ MHz, the first few images are:

- $1 \cdot F_{clk} - f_0 = 300 - 80 = 220$ MHz
- $1 \cdot F_{clk} + f_0 = 380$ MHz
- $2 \cdot F_{clk} - f_0 = 600 - 80 = 520$ MHz
- $2 \cdot F_{clk} + f_0 = 680$ MHz

Harmonics (integer multiples of the fundamental) occur at $2 \cdot f_0, 3 \cdot f_0, 4 \cdot f_0, \dots$:

- 2nd harmonic: occur at distances F_0 from images = 80 MHz
- 3rd harmonic: occur at distances $2 \cdot F_0$ from images = 160 MHz

9.2.2 Different Filter Responses

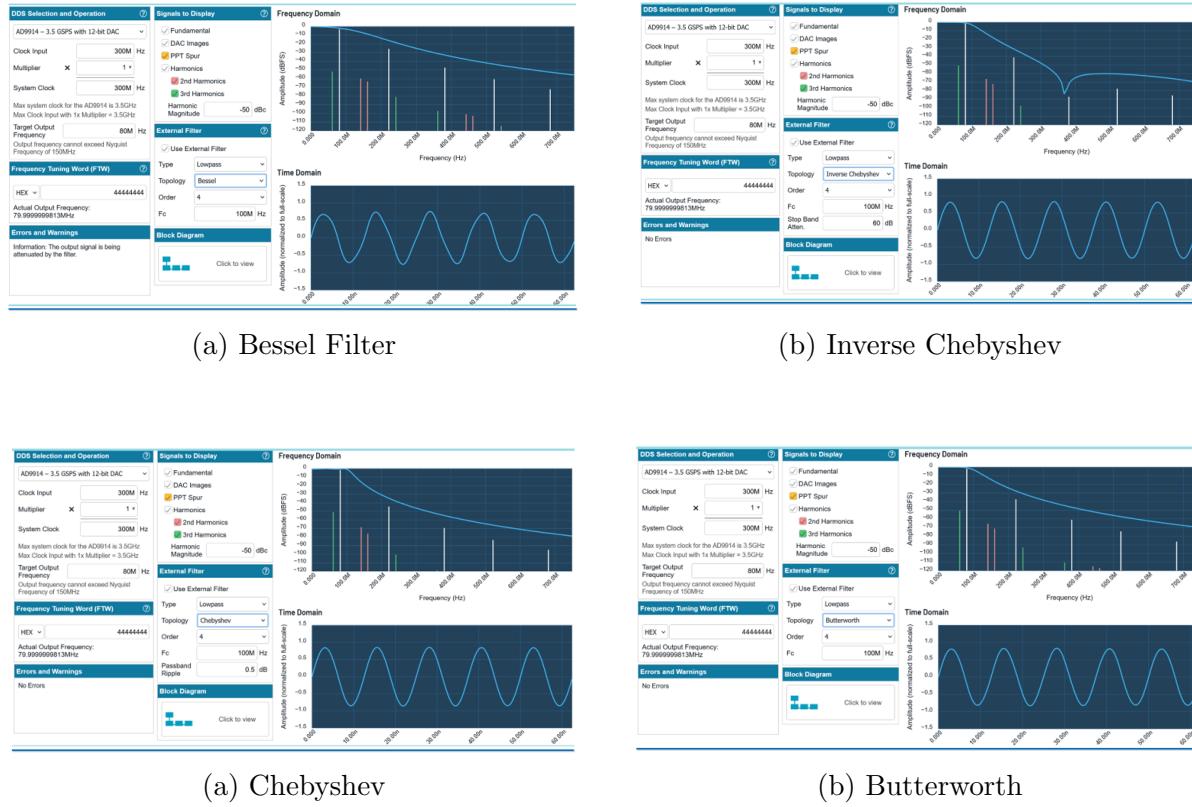


Figure 9.5: Comparison of different filter types

When trying different filter responses we see that they match with their known characteristics and in this case the Chebyshev filter provided the best response.

Filter Type	Passband Ripple	Stopband Ripple	Transition Sharpness
Butterworth	None (flat)	None	Gentle (slow)
Chebyshev Type I	Ripple in passband	Flat stopband	Sharper
Chebyshev Type II	Flat passband	Ripple in stopband	Sharper
Elliptic	Ripple in passband	Ripple in stopband	Sharpest for given order

Table 9.2: Filter Characteristics

9.3 LFM Signal "Chirp"

9.3.1 1. Theory: Why LFM Radar Can Measure Distance

When a radar transmits a signal $s(t)$, it travels to a target at distance R , reflects, and returns back. The round-trip propagation delay is:

$$\tau = \frac{2R}{c} \quad (9.1)$$

where:

- R : distance to target
- $c = 3 \times 10^8$ m/s: speed of light

When this delayed echo returns, the radar correlates it with a **reference copy** of the transmitted signal. The correlation (matched filter output) produces a **sharp peak** at the location that matches the delay. Thus:

$$R = \frac{c \times \tau_{est}}{2} \quad (9.2)$$

where τ_{est} is the time where the correlation peak occurs.

9.3.2 2. Why LFM (Linear Frequency Modulated) Signals Are Used

An LFM chirp is:

$$s(t) = A \cos(2\pi(f_0 t + \frac{K}{2}t^2) + \theta) \quad (9.3)$$

with:

- f_0 : start frequency
- $K = B/T$: chirp rate
- B : bandwidth
- T : pulse duration

Its instantaneous frequency is: $f_{inst}(t) = f_0 + Kt$. The **linearly increasing frequency** gives LFM excellent matched filter gain, a very sharp correlation peak, high SNR improvement, and very good range resolution.

Range resolution:

$$\Delta R = \frac{c}{2B} \quad (9.4)$$

Higher bandwidth \rightarrow better resolution.

9.3.3 Signal Model Used in Simulation

- Transmitted signal: Real LFM chirp $s(t)$
- Received echo: $r(t) = \alpha s(t - \tau) + n(t)$
- Matched filter output: $z(t) = (r * s \sim)(t)$ where $s \sim(t) = s(-t)$

At the correct delay \rightarrow a strong correlation peak.

Simulation Parameters:

```
c = 3e8; % speed of light (m/s)
A = 1; % amplitude
f0 = 0; % start frequency
B = 1e6; % bandwidth (Hz)
T = 100e-6; % pulse duration
K = B / T; % chirp rate
Fs = 5e7; % sampling frequency
SNR_dB = 10; % desired SNR
R_true = 300; % true range
alpha = 0.3; % attenuation
```

9.3.4 Figure-by-Figure Explanation

FIGURE 1 — LFM Signal Analysis This figure has 6 subplots.

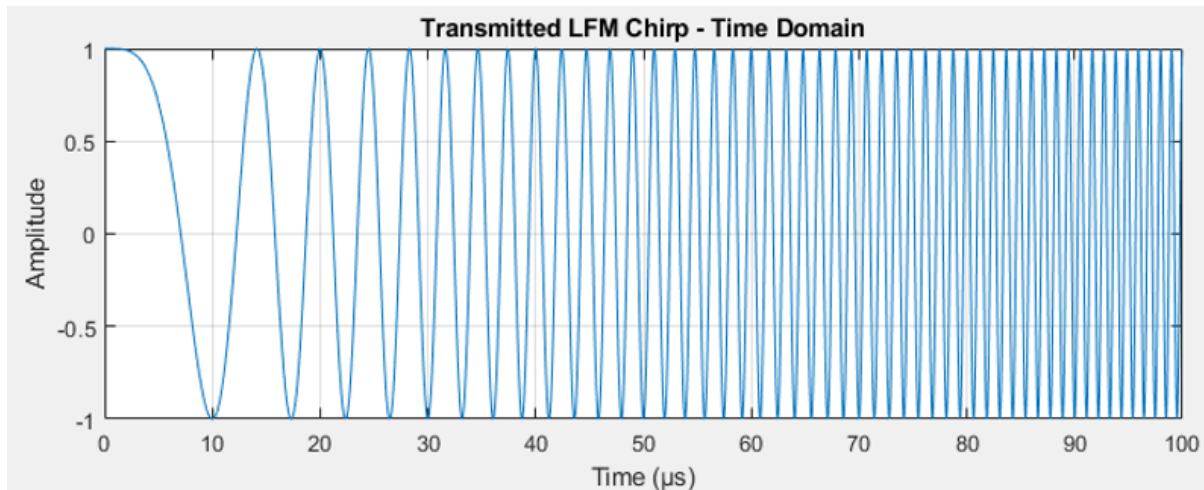


Figure 9.6: LFM Signal Analysis Overview

- **Plot 1 (Transmitted LFM Chirp - Time Domain):** Shows the real LFM signal $s(t)$. It looks like a sinusoid whose frequency increases gradually along the pulse (up-chirp).
- **Plot 2 (Frequency Domain):** Shows $|S(f)|$. The spectrum spreads across the bandwidth B , occupying $[f_0, f_0 + B]$.
- **Plot 3 (Instantaneous Frequency):** A straight line from f_0 to $f_0 + B$. This confirms $f_{inst}(t) = f_0 + Kt$.
- **Plot 4 (Received Signal - Time Domain):** The received echo appears **later** than the transmitted pulse due to propagation delay. It is attenuated and contains noise.
- **Plot 5 (Received Signal - Frequency Domain):** The FFT of the received echo. The spectrum is essentially the same as transmitted, confirming delay causes phase shift, not frequency shift.
- **Plot 6 (Matched Filter Output $|z(t)|$):** Shows the magnitude of correlation. A large, sharp peak occurs at the estimated delay. $\tau_{est} = (\text{peak time index})/Fs$.

FIGURE 2 — Detailed Frequency Analysis

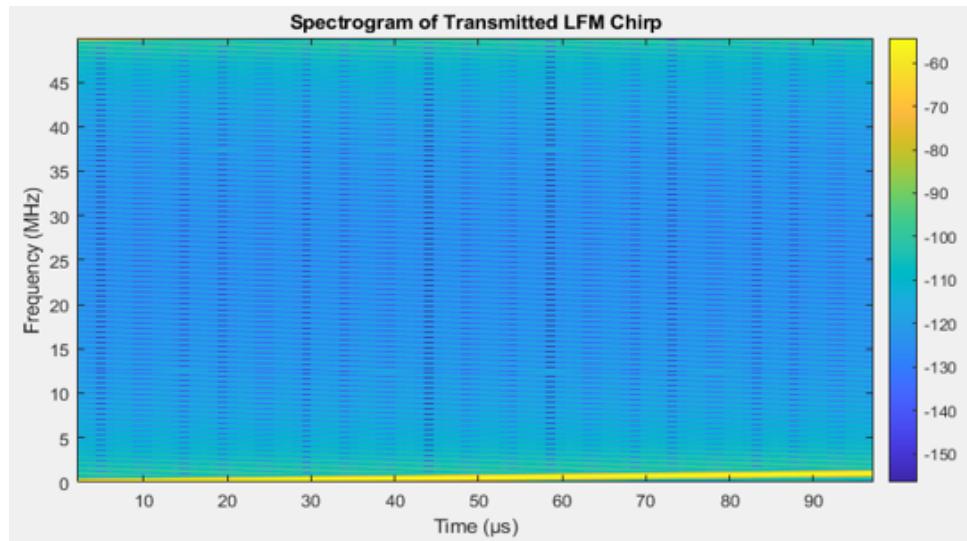


Figure 9.7: Spectrogram of Transmitted LFM Chirp

Plot 1 — Spectrogram: Visually confirms the chirp's instantaneous frequency sweep linearly.

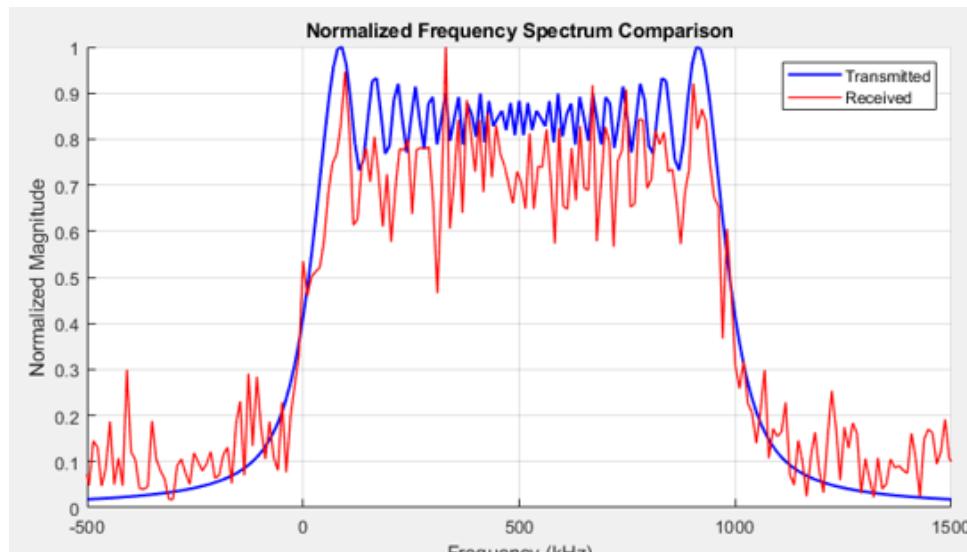


Figure 9.8: Normalized Frequency Spectrum Comparison

Plot 2 — Spectrum Comparison: Overlays transmitted and received spectra. The echo preserves chirp structure; noise slightly distorts it.

Explanation for the 4 PSD Subplots:

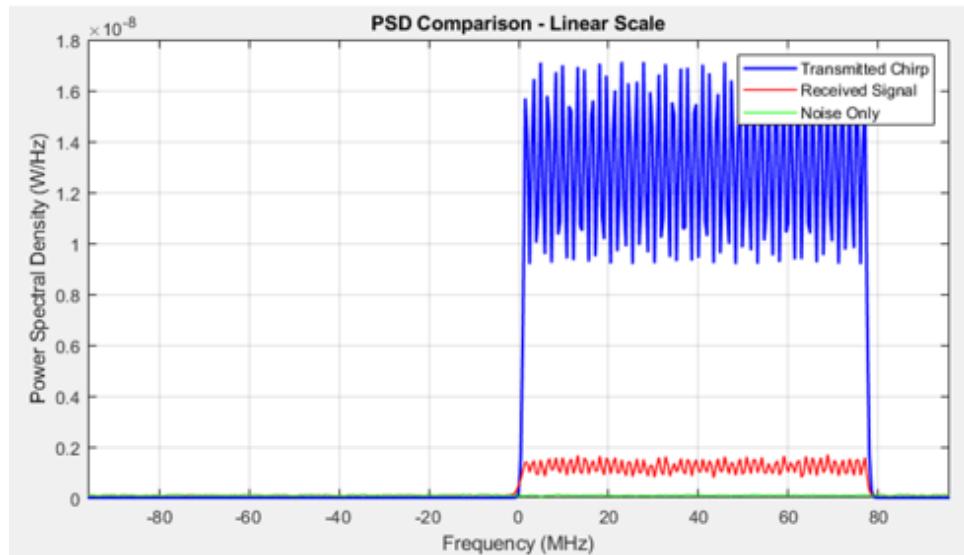


Figure 9.9: PSD Comparison – Linear Scale

(1) **PSD Comparison – Linear Scale:** Shows transmitted chirp has nearly flat PSD over 80 MHz. Received echo appears attenuated. Noise PSD is flat and low (AWGN).

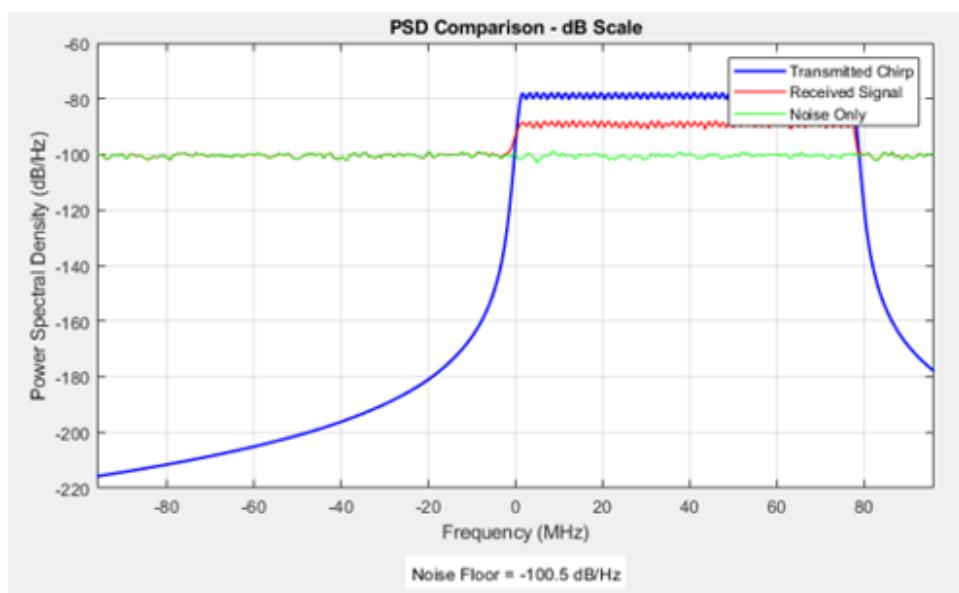


Figure 9.10: PSD Comparison – dB Scale

(2) **PSD Comparison – dB Scale:** Transmitted chirp forms a clean, flat plateau. Noise floor appears as a horizontal flat line.

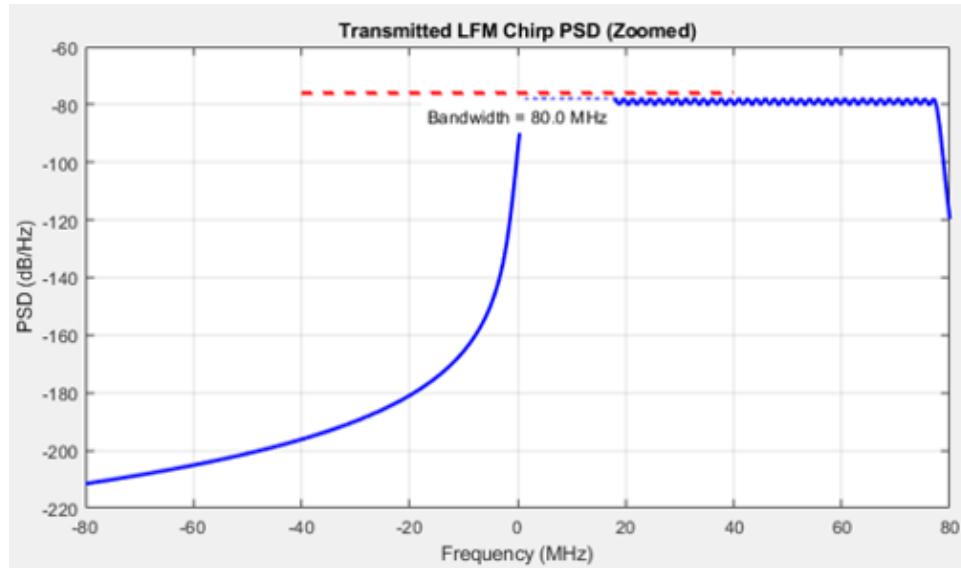


Figure 9.11: Transmitted LFM Chirp PSD (Zoomed)

(3) **Transmitted LFM Chirp PSD (Zoomed):** Focuses on the transmitted signal, showing the precise sweep bandwidth (~ 80 MHz) and sharp roll-offs.

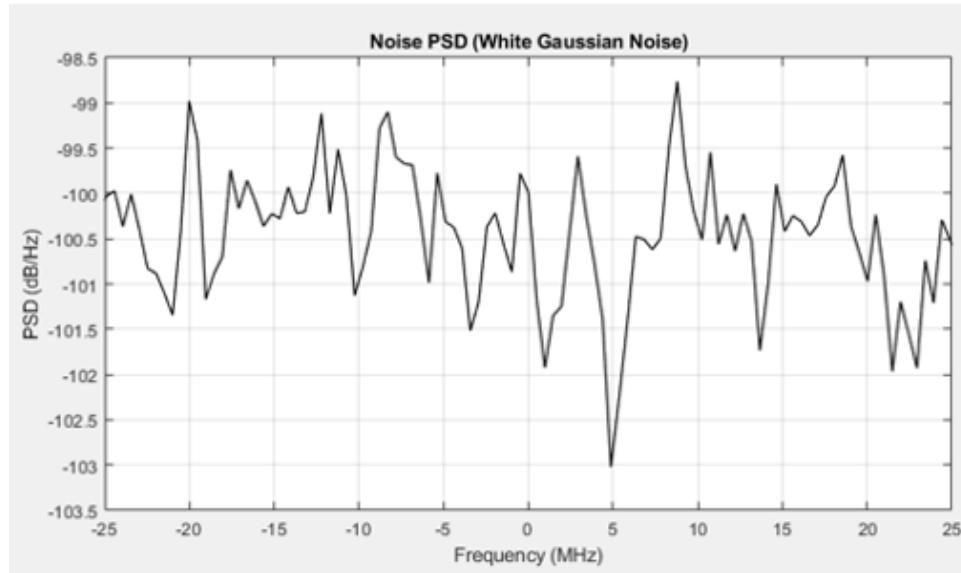


Figure 9.12: Noise PSD (White Gaussian Noise)

(4) **Noise PSD:** Exhibits expected flat spectral density of ideal AWGN with small random fluctuations.

FIGURE 3 — Matched Filter Peak (Zoom)

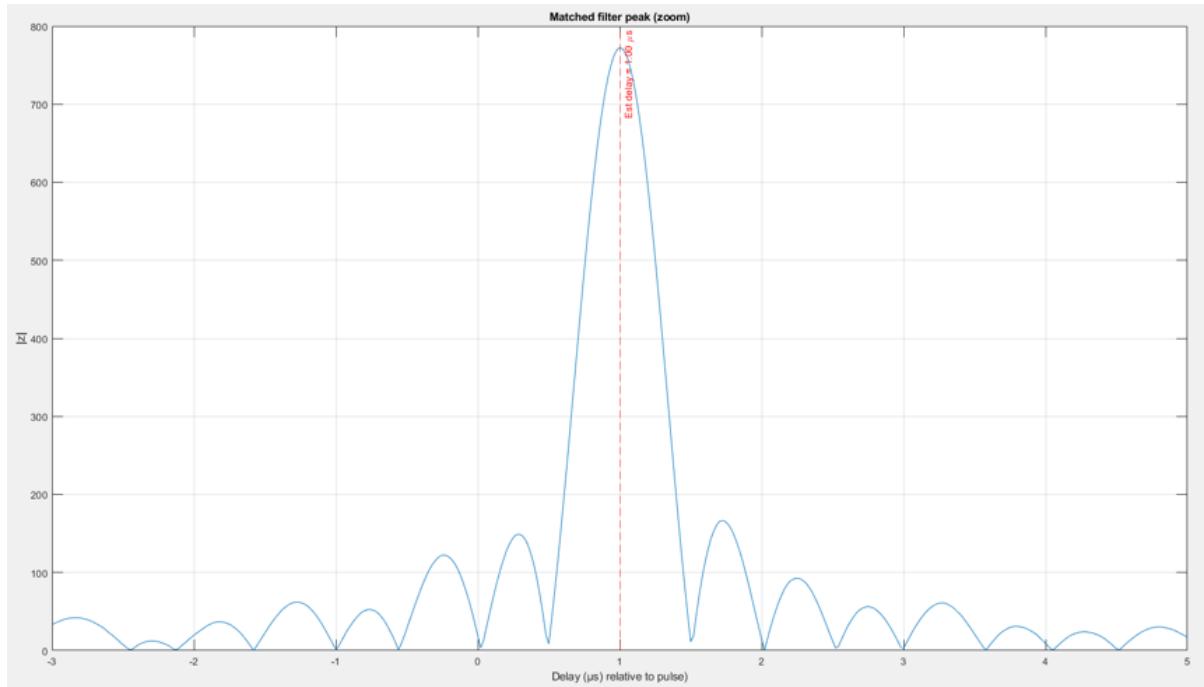


Figure 9.13: Matched Filter Peak (Zoom)

The matched filter output is extremely sharp. The location of the peak corresponds exactly to the echo delay.

Result (AWGN only):

```
True round-trip delay = 2.000e-06 s -> delay samples = 100
Requested SNR = 0.0 dB, Actual SNR = 0.3 dB
Received echo power (approx) = 4.612e-02 ; noise sigma = 2.082e-01
Estimated delay samples = 100 -> est_tau = 2.000e-06 s -> R_est = 300.000 m
Theoretical range resolution (c / (2B)) = 150.000 m
Range estimate error (R_est - R_true) = 0.000 m
```

Results (AWGN + Multipath Components + Doppler Effect):

```
Main delay (s) = 1.000e-06 -> main delay samples = 50
MP 1 extra range = 30.0 m -> extra delay (samples) = 10
MP 2 extra range = 25.0 m -> extra delay (samples) = 8
...
Doppler shift = 37.50 Hz
Estimated (strongest) delay samples = 53 -> est_tau = 1.060e-06 s -> R_est = 159.000 m
Range estimate error (R_est - R_true) = 9.000 m
```

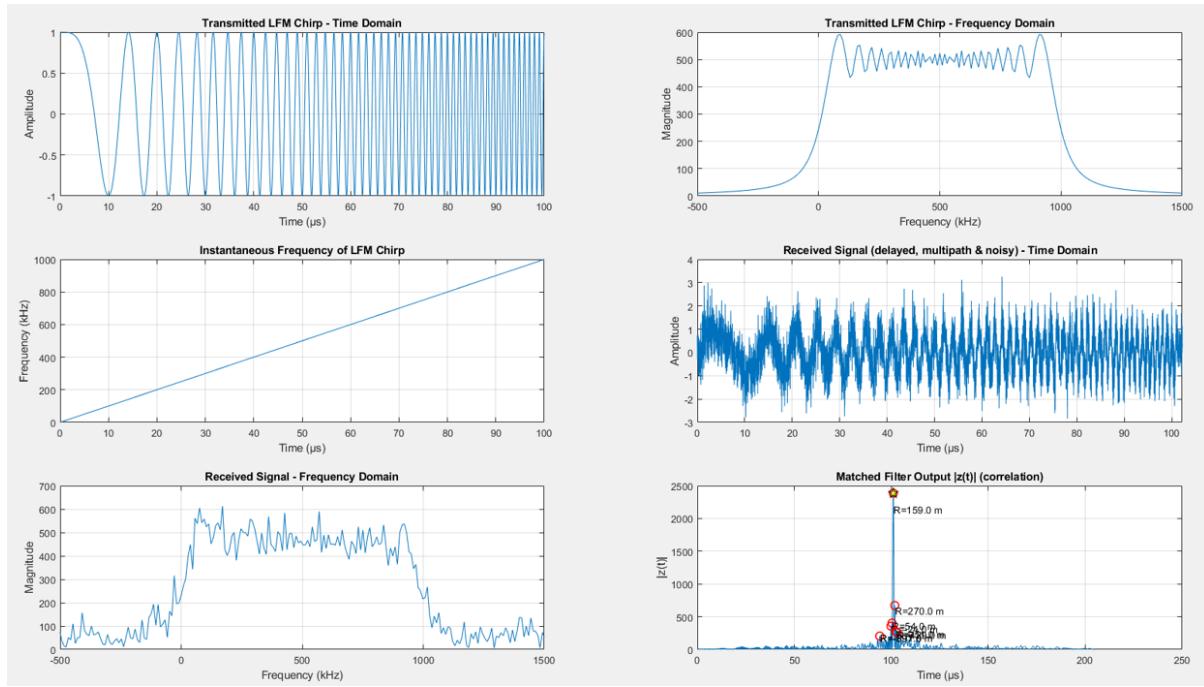


Figure 9.14: Multipath and Doppler Simulation Results

9.3.5 Results with RF-2 related parameters

Parameters: $B = 80 \text{ MHz}$, $T = 50\mu\text{s}$, $F_s = 500 \text{ MHz}$.

```
Command Window
True round-trip delay = 2.000e-06 s -> delay samples = 1000
Requested SNR = 0.0 dB, Actual SNR = 0.2 dB
Received echo power (approx) = 4.518e-02 ; noise sigma = 2.078e-01
Estimated delay samples = 1000 -> est_tau = 2.000e-06 s -> R_est = 300.000 m
Theoretical range resolution (c / (2B)) = 1.875 m
Range estimate error (R_est - R_true) = 0.000 m
```

Figure 9.15: Console Output RF-2

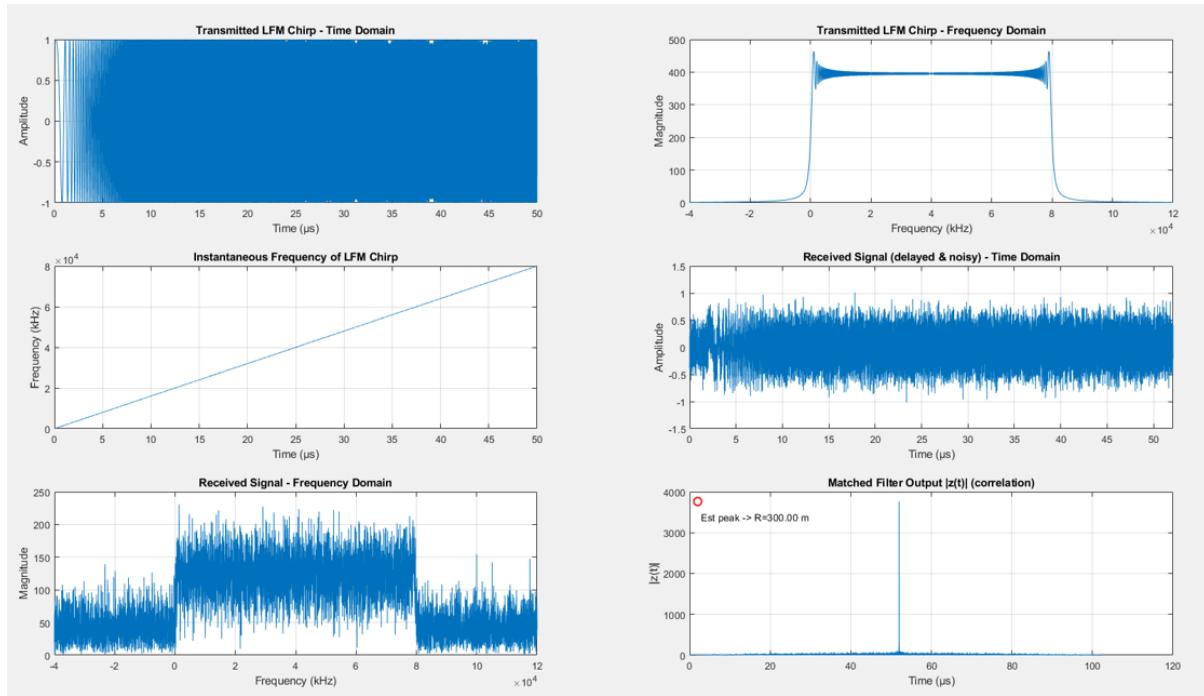


Figure 9.16: Signal Analysis RF-2

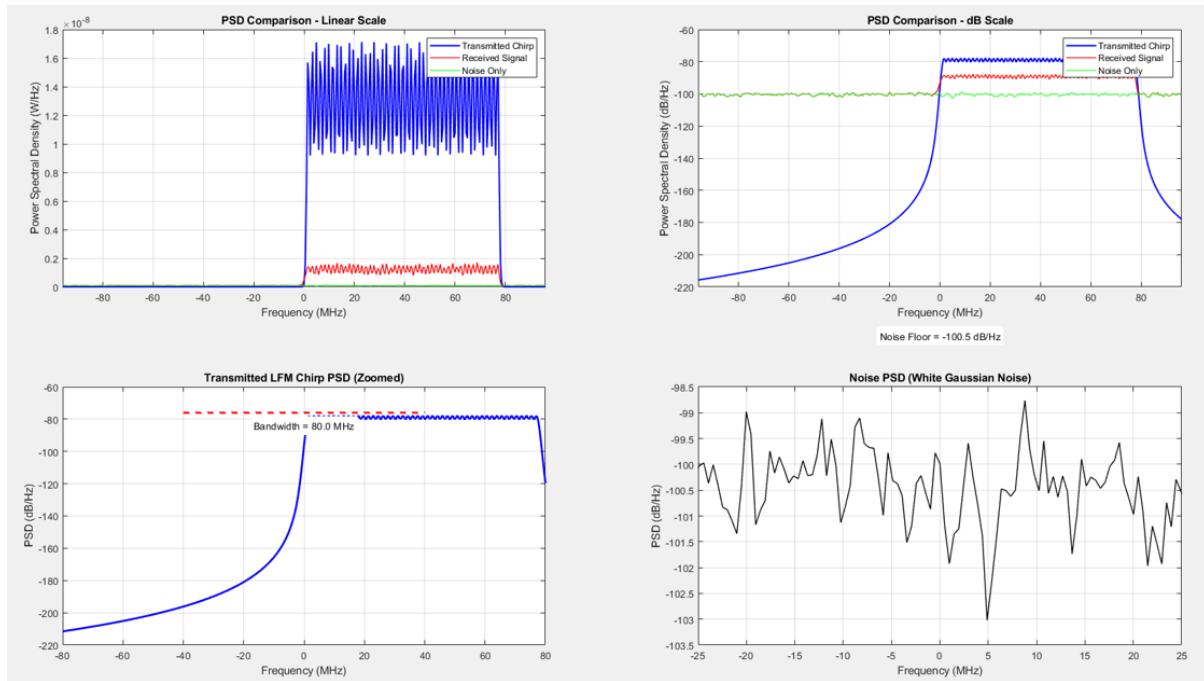


Figure 9.17: PSD RF-2

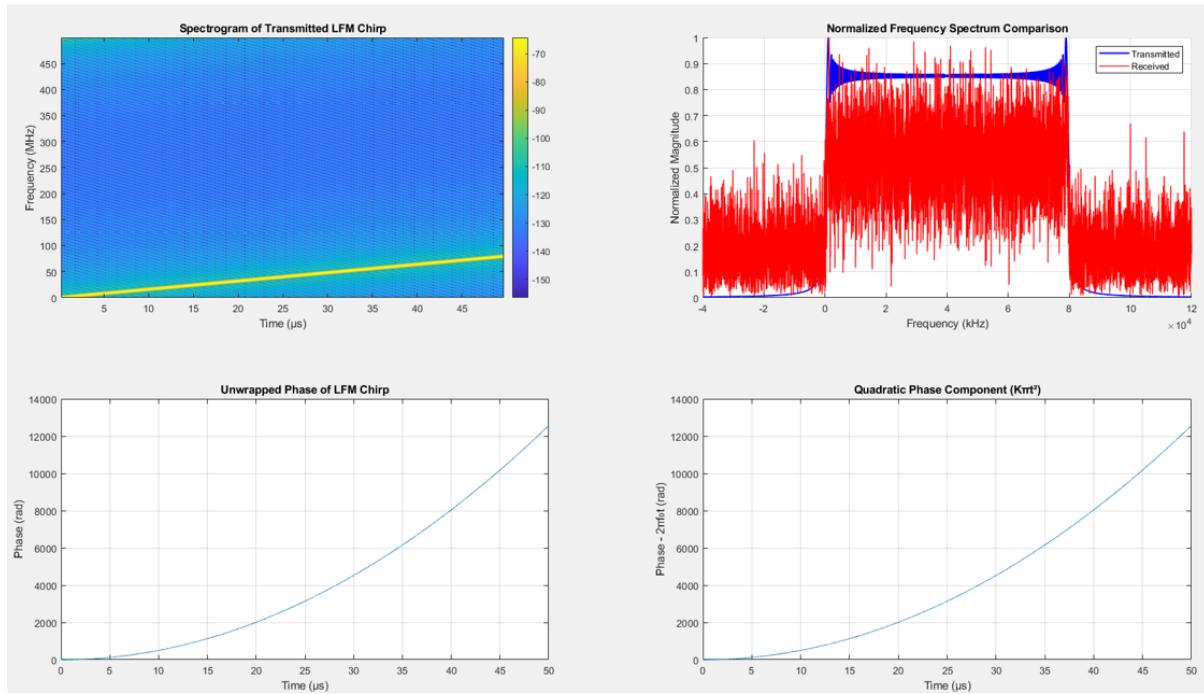


Figure 9.18: Spectrogram and Phase RF-2

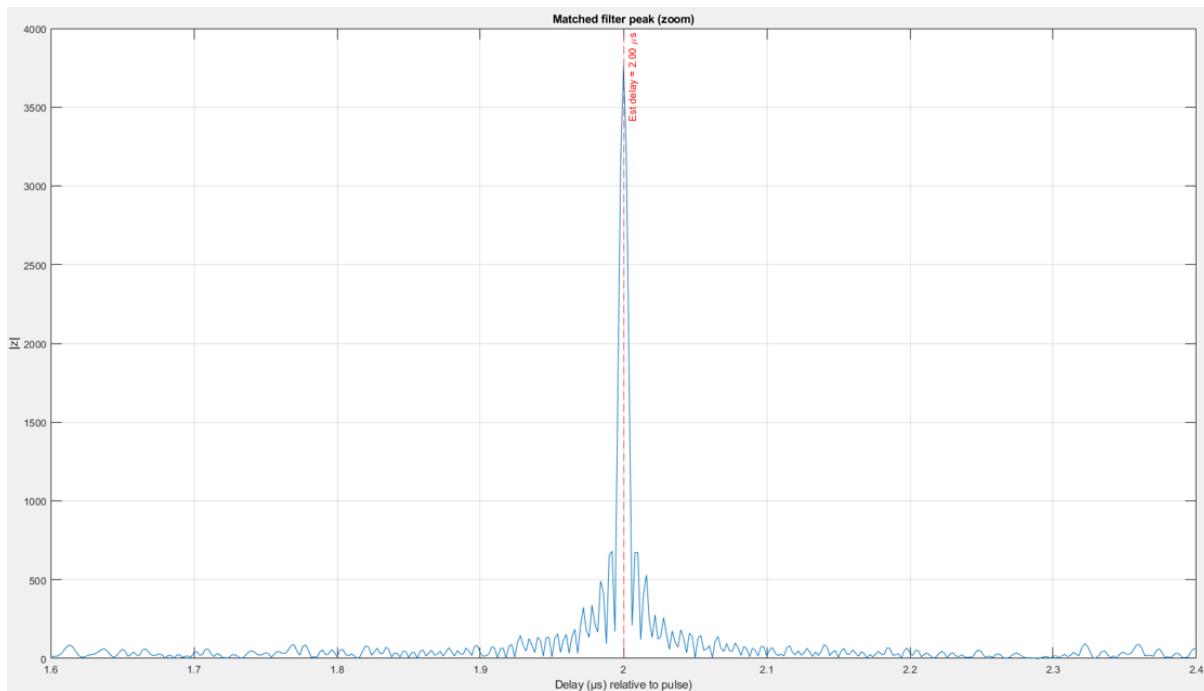


Figure 9.19: Matched Filter Peak RF-2

Conclusion from Simulation Results:

- **AWGN only:** Matched filter correctly identifies the main peak. Range error is 0 m.

- **AWGN + Multipath + Doppler:** Multiple peaks appear. Strongest peak is shifted, leading to range errors. SNR decreases.
- **Bandwidth vs. Range Estimation Error:**
 - Low BW (0.1 MHz) → Wide peak → High error (≈ 30 m).
 - High BW (1 MHz) → Sharp peak → Low error (≈ 0 m).
 - Theoretical relationship: $\Delta R = c/2B$.

9.4 OFDM + Chirp (Different Timeslots) Simulation

Fixed Parameters: NFFT = 4096, SCS = 120e3 Hz, NRBs = 264, 256-QAM, AWGN channel.

1st Test Case: All slots are OFDM

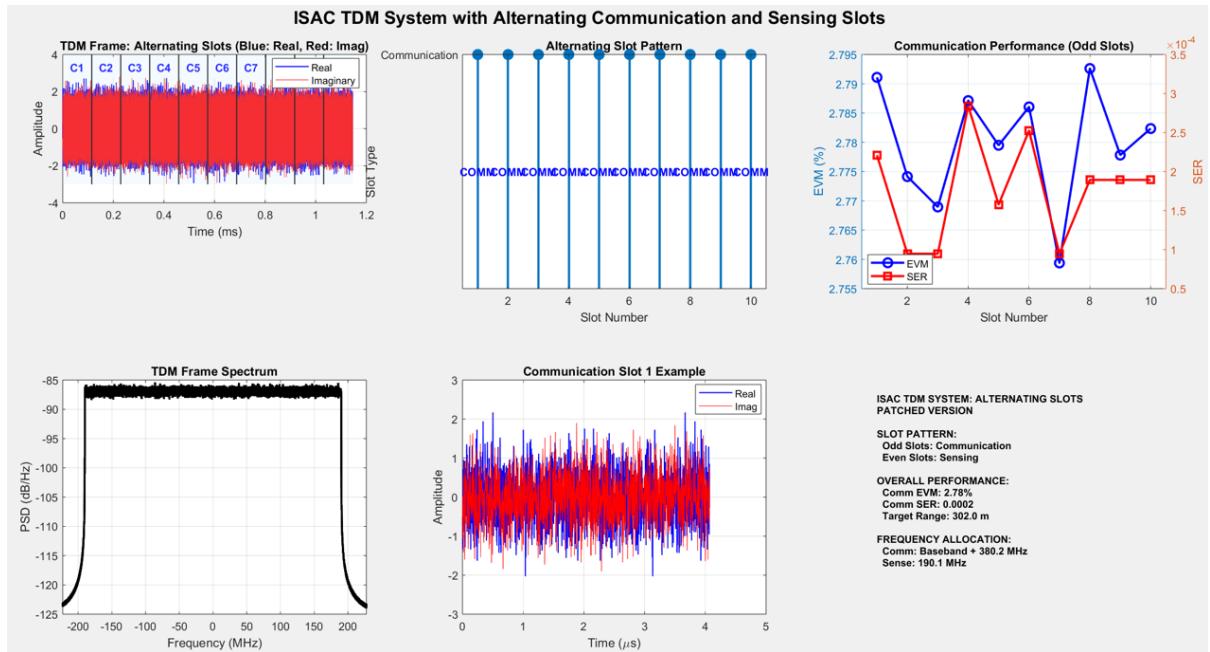


Figure 9.20: ISAC TDM System with Alternating Slots (Baseline)

EVM: 2.78%.

2nd Test Case: Slots are alternating between OFDM and Chirp

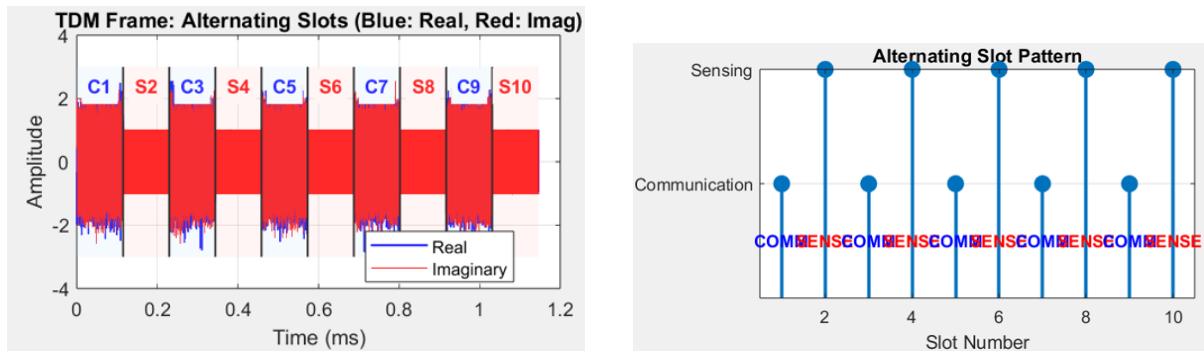


Figure 9.21: Time allocation distribution between alternating signals

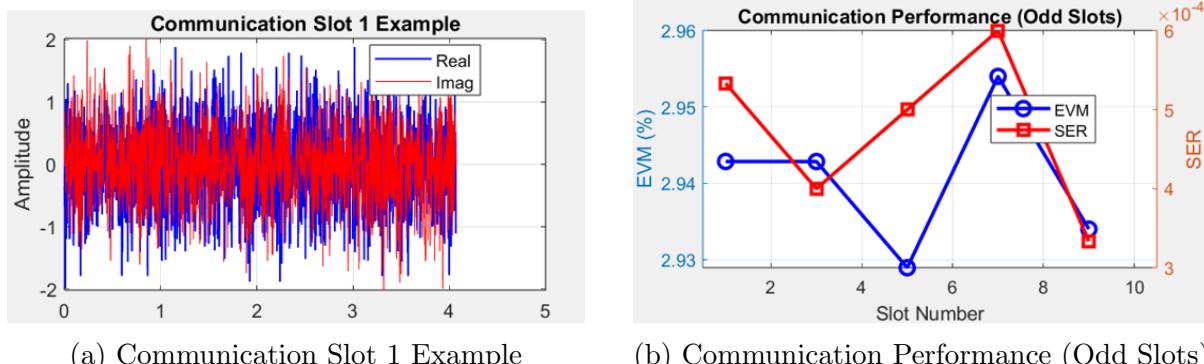


Figure 9.22: OFDM Signal and EVM per slot

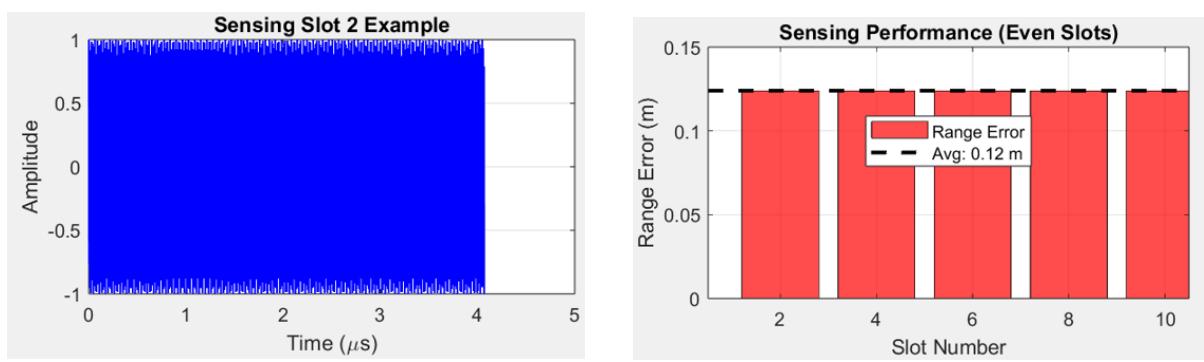


Figure 9.23: Chirp signal and Range Error (Bandwidth 20 MHz)

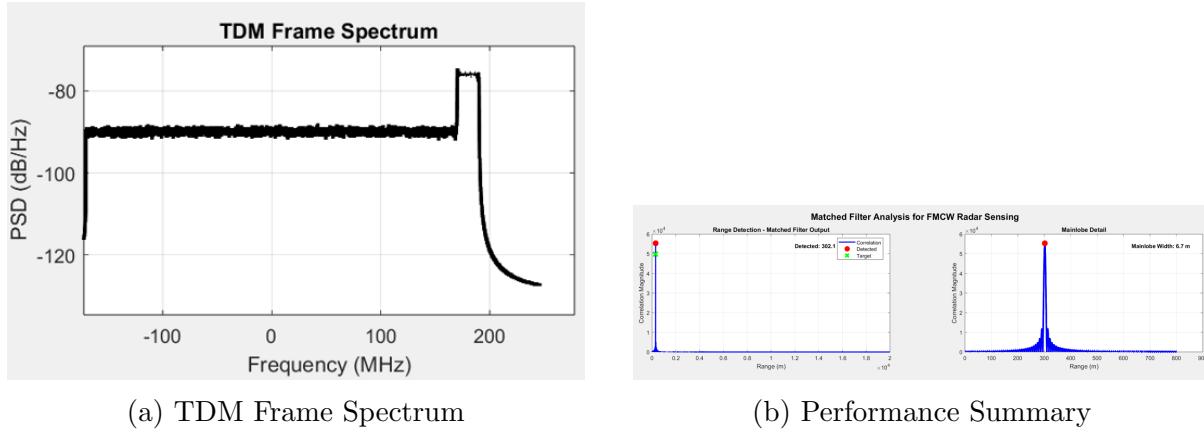


Figure 9.24: Spectrum of OFDM and Chirp signals

In the spectrum graph, we see normally we have limited bandwidth to allocate for both and have to study the tradeoffs:

- High Comm BW → High data rate + Poor sensing resolution.
- Low Comm BW → Low data rate + Excellent sensing resolution.

EVM is approximately the same as signals are in different timeslots.

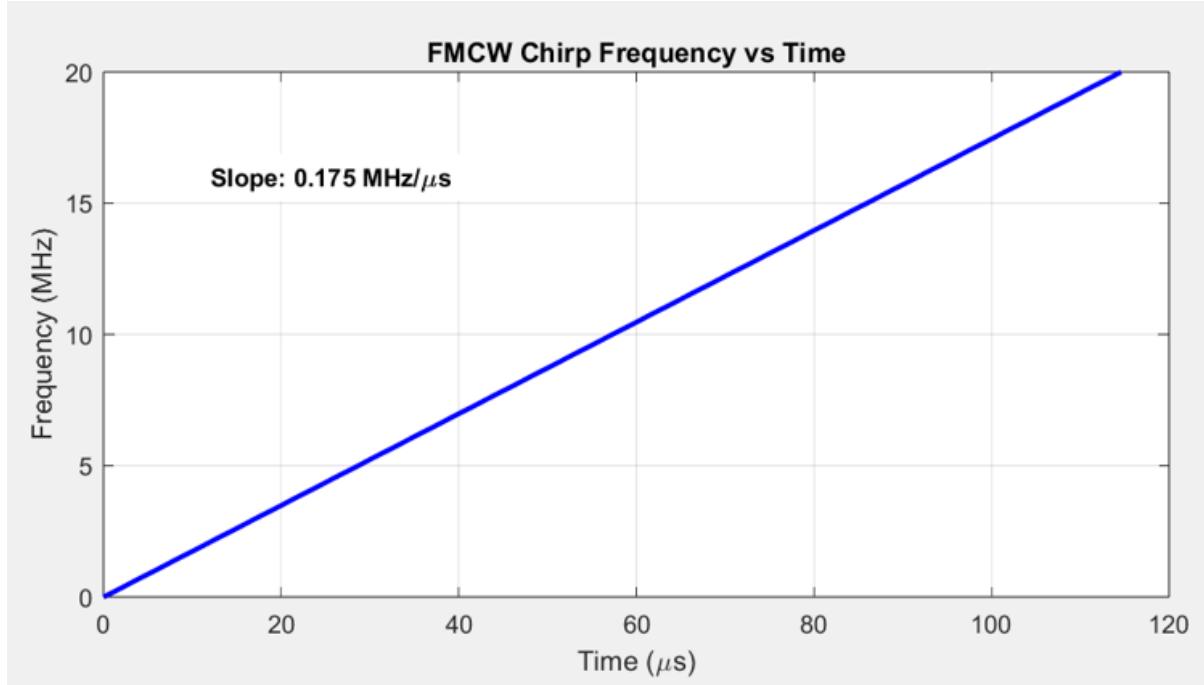


Figure 9.25: Matched Filter Analysis for FMCW Radar Sensing



Figure 9.26: Matched Filter Performance Metrics

Correlation is done between the original and received signal where the delay is used to calculate the distance with an error depending on the radar resolution.

9.5 FDM Technique: OFDM + LFM (No-overlapping)

9.5.1 1. Objective

Implementation of Frequency-Division Multiplexing (FDM) to transmit OFDM communication signals and LFM radar chirp simultaneously in the same time slot.

9.5.2 2. System Design

- **OFDM Signal:** BW = 380 MHz (Communication). Metric: EVM.
- **LFM Radar Signal:** BW = 80 MHz (Sensing). Resolution $\Delta R \approx 1.88$ m.
- **Arrangement:** Total Spectrum = OFDM BW + Guard Band + LFM BW.

9.5.3 3. Guard Band Analysis

- **Small Guard Band:** EVM increased; slight spectral leakage; Radar performance unaffected.

- **Large Guard Band:** EVM decreased; Radar performance unaffected.

Conclusion: EVM is sensitive to guard band size; Radar sensing is robust.

9.5.4 Results and Visualization

```
CP length = 128 samples
OFDM Band: +/- 190.08 MHz
LFM Band: 200.08 MHz to 280.08 MHz (BW=80.00 MHz)
OFDM Power: 0.00 | LFM Power: 0.00
SNR: 0 dB | Preamble EVM: 191.285 %
SNR: 2 dB | Preamble EVM: 126.653 %
SNR: 4 dB | Preamble EVM: 83.729 %
SNR: 6 dB | Preamble EVM: 67.723 %
SNR: 8 dB | Preamble EVM: 44.940 %
SNR: 10 dB | Preamble EVM: 35.343 %
SNR: 12 dB | Preamble EVM: 27.335 %
SNR: 14 dB | Preamble EVM: 21.579 %
SNR: 16 dB | Preamble EVM: 17.321 %
SNR: 18 dB | Preamble EVM: 13.753 %
SNR: 20 dB | Preamble EVM: 10.848 %
SNR: 22 dB | Preamble EVM: 8.591 %
SNR: 24 dB | Preamble EVM: 6.796 %
SNR: 26 dB | Preamble EVM: 5.447 %
SNR: 28 dB | Preamble EVM: 4.287 %
SNR: 30 dB | Preamble EVM: 3.399 %
SNR: 32 dB | Preamble EVM: 2.735 %
SNR: 34 dB | Preamble EVM: 2.164 %
SNR: 36 dB | Preamble EVM: 1.721 %
SNR: 38 dB | Preamble EVM: 1.356 %
SNR: 40 dB | Preamble EVM: 1.084 %
--- LFM Radar (Correlation) ---
True R = 302.00 m | Estimated R = 302.12 m | Error = 0.12 m | Radar resolution = 1.88 m
```

Figure 9.27: Simulation Parameters and EVM results

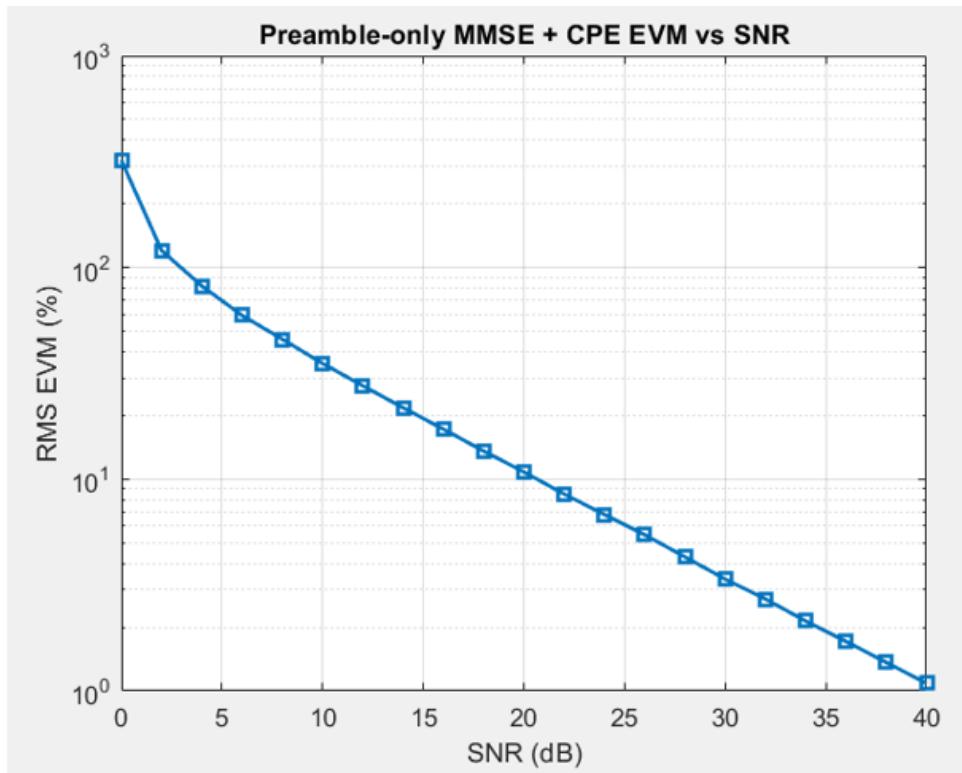


Figure 9.28: Preamble-only MMSE + CPE EVM vs SNR

EVM decreases with increasing SNR.

Effect of decreasing guard band (SNR = 30 dB):

- Guard band 20 MHz → EVM ≈ 3.589%
- Guard band 2 MHz → EVM ≈ 3.406%

Note: By decreasing the guard band, interference increases.

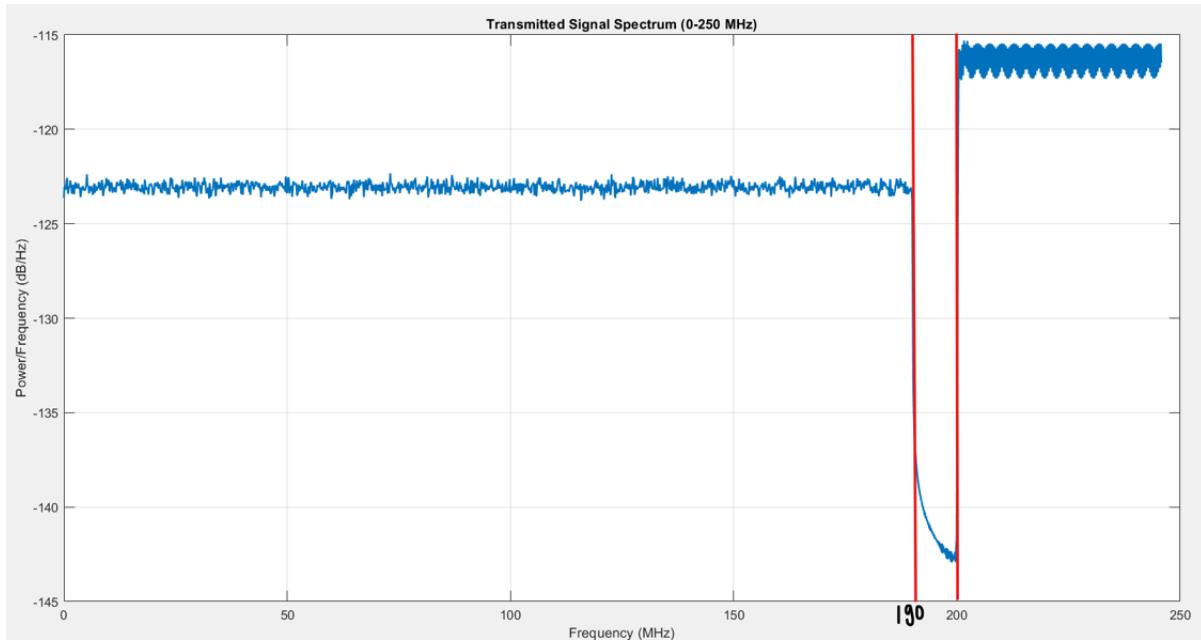


Figure 9.29: Transmitted Signal Spectrum (0-250 MHz)

OFDM BW = 380 MHz (baseband). Guard band is visible between OFDM and LFM (200-240 MHz).

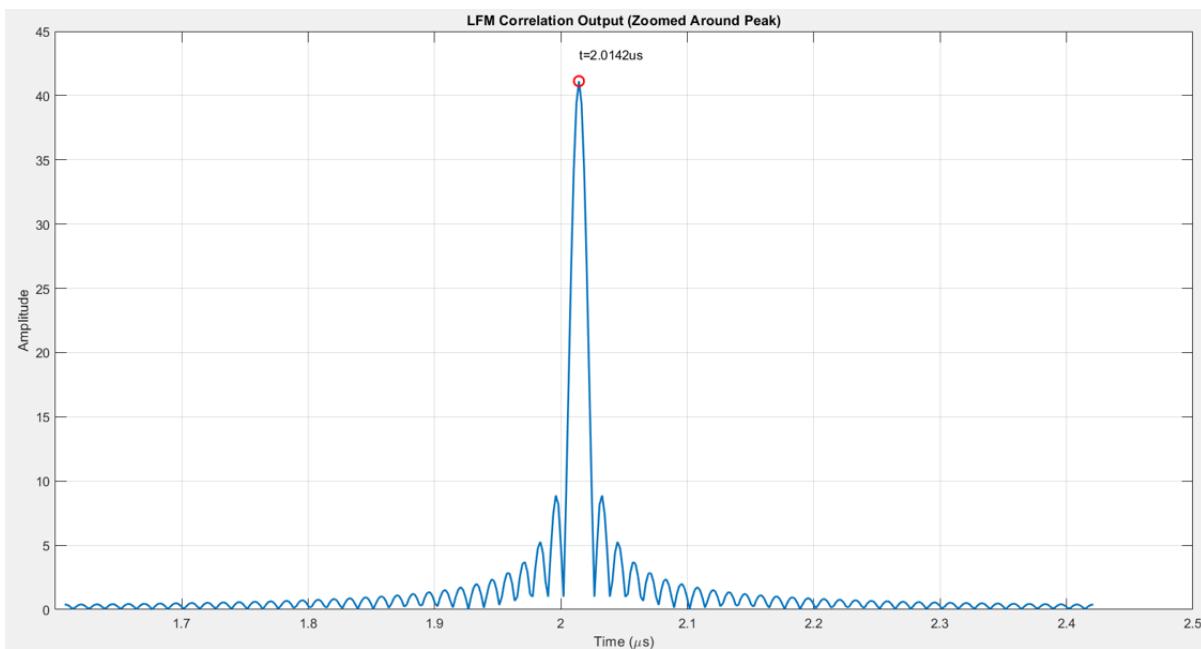


Figure 9.30: LFM Correlation Output (Zoomed Around Peak)

Peak at $t = 2.0142\mu s$ corresponds to the target distance.

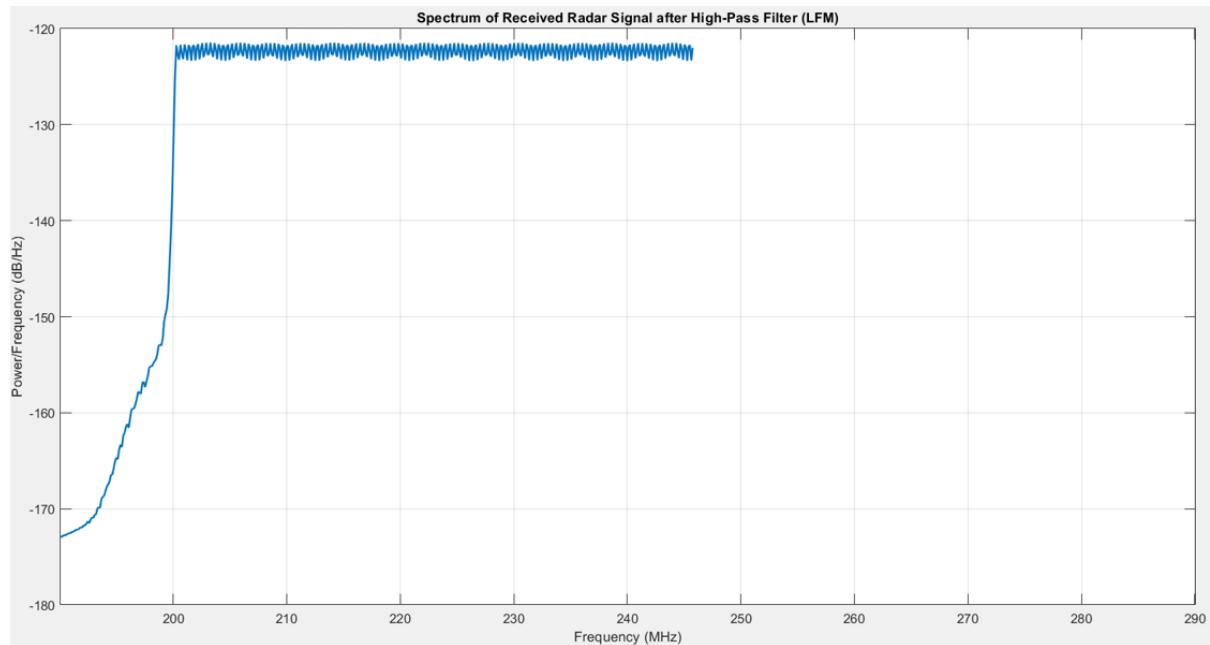


Figure 9.31: Spectrum of Received Radar Signal after Low-Pass Filter (OFDM)

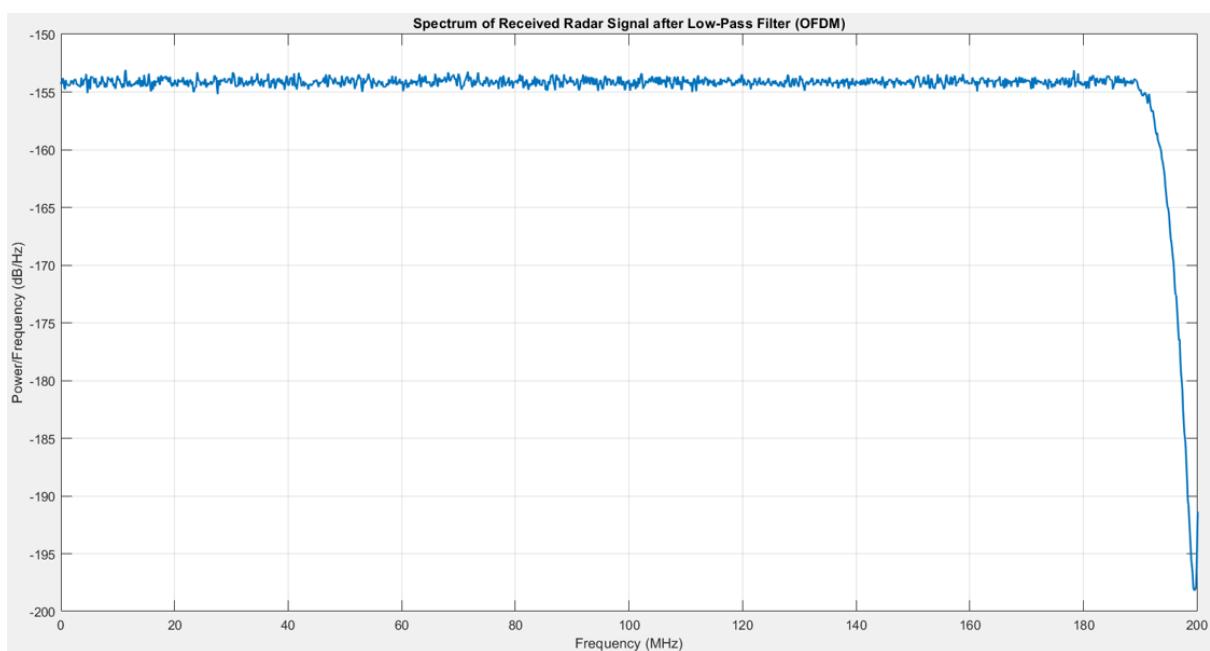


Figure 9.32: Spectrum of Received Radar Signal after High-Pass Filter (LFM)

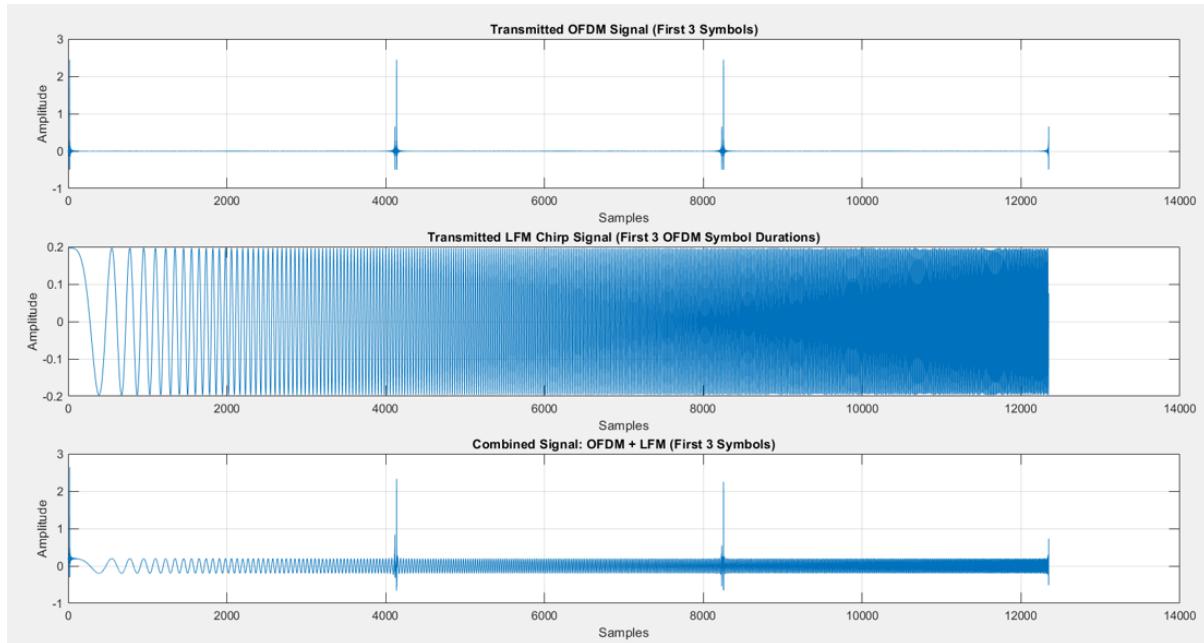


Figure 9.33: Signal Time-Domain Zooms

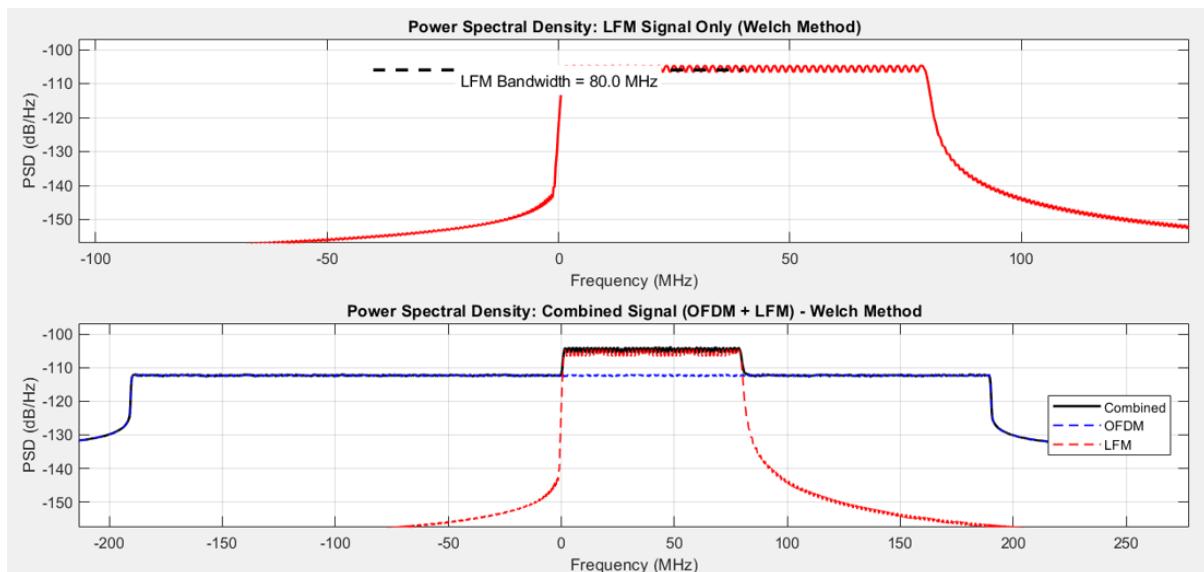


Figure 9.34: Combined Signal (OFDM + LFM)

The 3rd graph shows the superposition. Amplitude variations are more extreme.

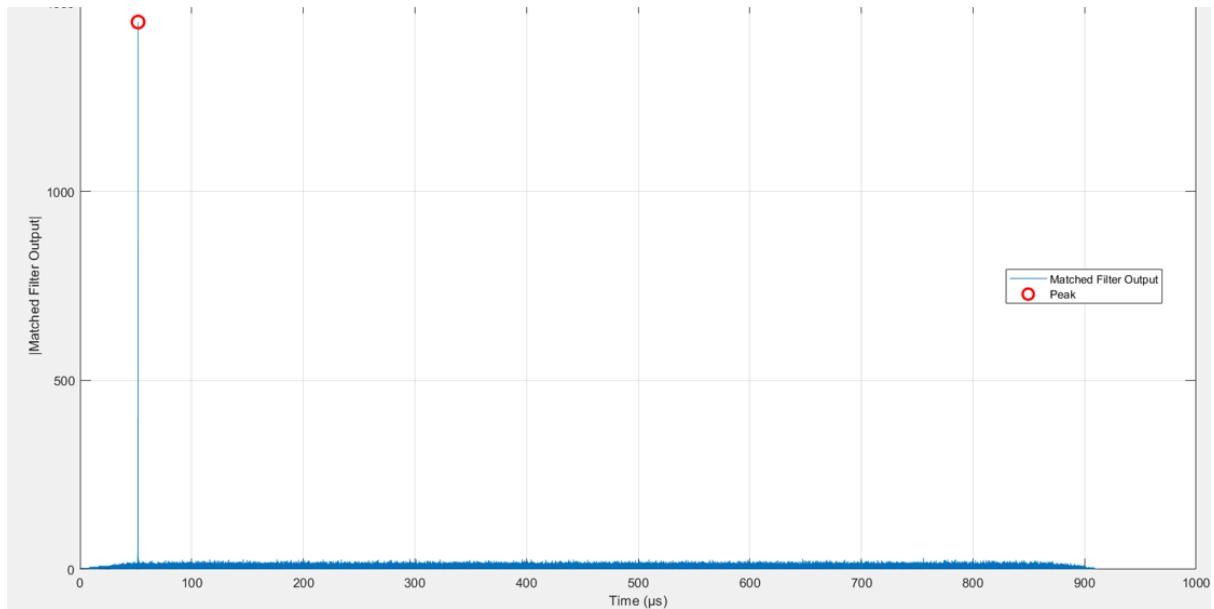


Figure 9.35: Power Spectral Density: LFM and Combined

- **Blue dashed (OFDM):** Flat across ± 190 MHz.
- **Red dashed (LFM):** Concentrated 0 to 80 MHz.

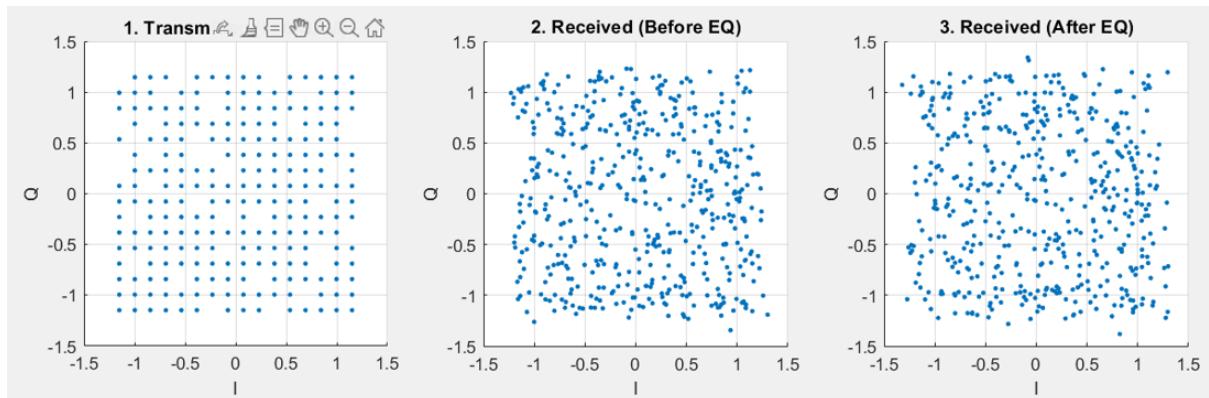


Figure 9.36: Received Constellations and EVM

Factors affecting EVM:

1. **SNR:** EVM decreases as SNR increases (saturates around 19% in the table provided).
2. **Relative Power (LFM vs OFDM):** If LFM power is high, interference increases, worsening EVM.

LFM relative power (dB)	EVM
-10	4.17%
-5	6.26%
0	10.33%
5	17.76%
10	31.62%
15	56.66%
20	101.26%

Table 9.3: Effect of LFM Relative Power on EVM

Multipath Effect on Distance: Distance error increases with the number of multipath components.

Multipath Components	Distance Error (m)
0	0.1363
1	7.5
2	15
3	67.5

Chapter 10

Conclusion

This graduation project has successfully explored the design and implementation of a DDS-based waveform generation and correlation system for 5G/6G cellular network calibration and ranging within an Integrated Sensing and Communication (ISAC) framework. The comprehensive analysis covers:

- **Introduction to ISAC:** Understanding the evolution of wireless networks toward integrated sensing and communication, and the role of DDS in this paradigm.
- **Wireless Channel Fundamentals:** Analysis of multipath propagation, fading, Doppler effects, and channel parameters that affect both communication and sensing systems.
- **OFDM System Design:** Detailed implementation of OFDM with cyclic prefix, pilot tones, and synchronization mechanisms for reliable communication.
- **5G NR Standards:** Examination of frame structures and numerology for modern wireless systems operating in FR2 frequency bands.
- **DDS Technology:** Comprehensive study of Direct Digital Synthesis for precise waveform generation, essential for both communication and sensing applications.
- **FFT Hardware Implementation:** Analysis of various FFT architectures suitable for OFDM and chirp processing, with recommendations for hardware implementation.
- **Signal Processing Simulations:** Demonstration of multiple signal placement strategies including TDM and FDM approaches for combined communication and sensing.

The project demonstrates that integrated sensing and communication (ISAC) systems are feasible with careful design considerations. Key trade-offs between communication performance (EVM) and sensing accuracy (range resolution) have been quantified through extensive MATLAB simulations.

10.1 Key Achievements

- Successfully designed and simulated a DDS-based waveform generation system capable of producing signals suitable for 5G/6G ISAC applications.
- Implemented and verified correlation algorithms for precise ranging and distance estimation.
- Compared different ISAC waveform strategies and quantified their performance trade-offs.
- Developed MATLAB reference models for system-level validation.
- Analyzed FFT architectures and selected optimal implementations for hardware realization.

10.2 Future Work

Future work could focus on:

- Hardware implementation of the optimized FFT and DDS architectures on FPGA platforms.
- Real-time implementation and testing with hardware-in-the-loop simulations.
- Advanced interference cancellation techniques for overlapping communication and sensing signals.
- Integration with MIMO systems for improved spatial resolution and beamforming.
- Development of adaptive waveform strategies that dynamically adjust based on channel conditions and sensing requirements.
- ASIC prototyping of the most critical digital signal processing blocks.

This work provides a solid foundation for the development of next-generation wireless systems that seamlessly integrate communication and sensing capabilities, paving the way for more intelligent, efficient, and context-aware wireless networks.