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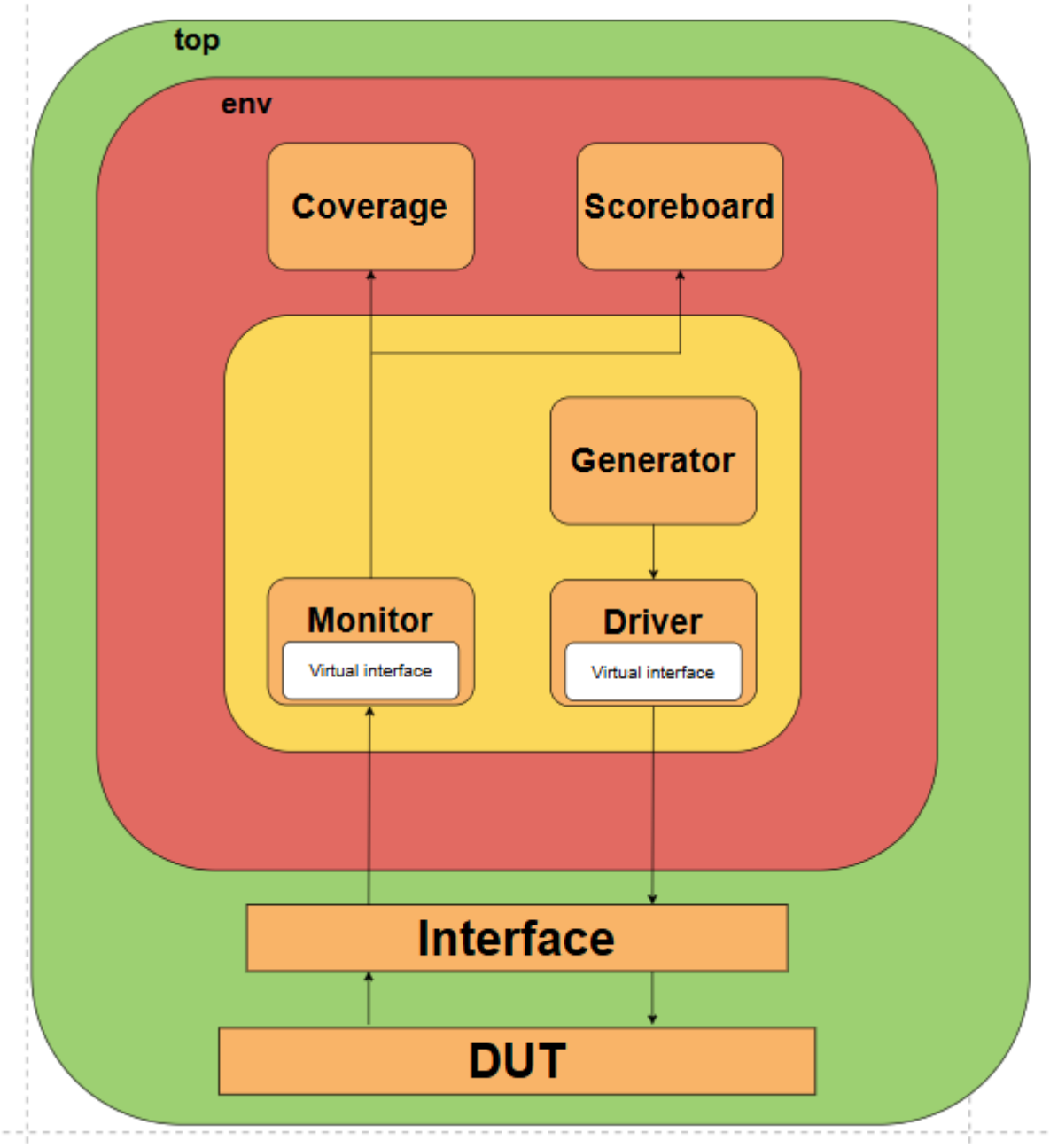
Verification Documentation of ALU

Verification Diagram



Verification plan

Label	Description	Stimulus generation	Functional Coverage
ALU_1	**Testing add operation one with carry flag and one without carry flag**	**Exhaustive testing throughout the simulation**	**Bin for op = add coverage & bins for all a & b values**
ALU_2	**Testing XOR operation**	**Exhaustive testing throughout the simulation**	**Bin for op = XOR coverage & bins for all a & b values**
ALU_3	**Testing AND operation**	**Exhaustive testing throughout the simulation**	**Bin for op = AND coverage & bins for all a & b values**
ALU_4	**Testing OR operation**	**Exhaustive testing throughout the simulation**	**Bin for op = OR coverage & bins for all a & b values**

Errors detected

1) **Carry flag assertion error**

   - Carry (c) becomes high during non-add operations, which is incorrect.

2) **Incorrect arithmetic and logical operations**

   - Some ADD, AND XOR, and OR results do not match the expected golden model outputs.

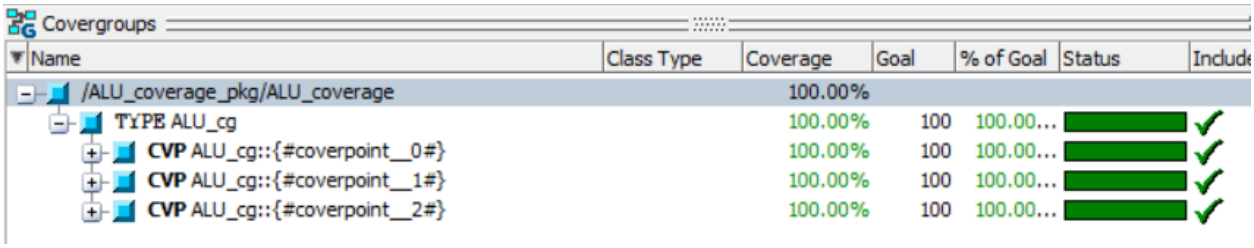
3) **Incorrect dependency in output logic**

   - The output behavior appears to depend improperly on operands a and b rather than being controlled correctly by the opcode.
   - This indicates inefficient or incorrect ALU design implementation.

Report summary

```
# Simulation summary: Correct=750 Errors=300
# ** Note: $stop    : ALU_top.sv(37)
#    Time: 2100 ns  Iteration: 0  Instance: /ALU_top
# Break in Module ALU_top at ALU_top.sv line 37
```

Functional Coverage



Code Coverage

```
================================================================================
=== Instance: /ALU_top/DUT
=== Design Unit: work.ALU
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                      1025      1024         1    99.90%
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                    1026      1026         0   100.00%
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                         40        40         0   100.00%
```