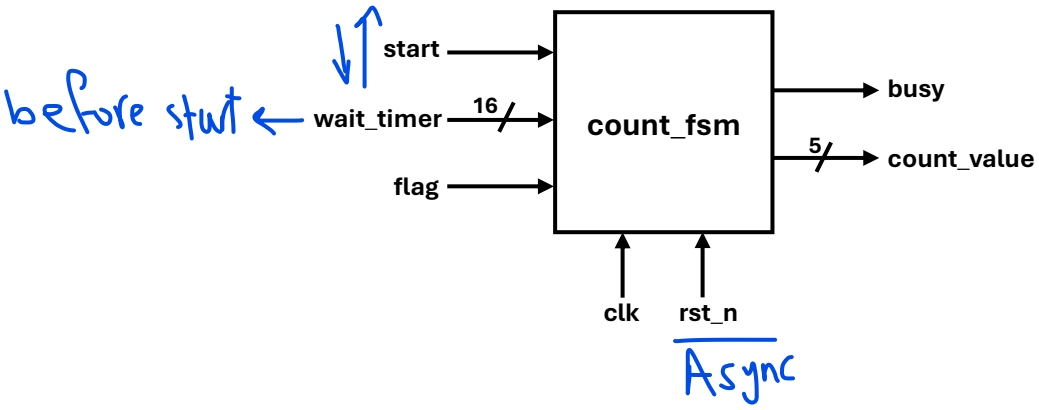
# ASU GP 2026

## Task 2

## Block Diagram




## Description

This design implements a small finite state machine (FSM) that operates on the positive edge of the clock, with an active-low asynchronous reset. The FSM starts counting when it detects a rising edge on start. Once active, it repeatedly waits for a programmable number of clock cycles (wait_timer) and then checks the flag input. If flag becomes high, or if count_value reaches its maximum, the FSM stops and returns to the idle state. While running, it asserts busy and increments count_value each time a wait_timer interval finishes without the flag being asserted.