

Design of Combined Radix-2, Radix- 4 and Radix-8 based Single Path Delay Feedback (SDF) FFT

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Abstract

Objectives: FFT algorithm is used for enhancing the performance of DFT. In the previous years, various types of FFT algorithms have been introduced. Particularly, the pipeline algorithms have been reputed as proper algorithms for processing high-speed data. Some pipeline FFT algorithms like split radix, radix-2 and the mixed radix have been developed. **Methods:** In the existing method of Radix-2 SDF FFT has more hardware utilization and also computational stages are increased.

Findings: To conquer this problem, we developed a combined radix-2, 4 & 8 butterfly elements based Single path Delay Feedback (SDF) fast fourier transform method for reducing the computational stages in this paper. The developed method has the identical number of multipliers and the smaller number of stages and butterfly elements than the existing radix-2 FFT.

Improvements: This architecture offers 62.47% reduction in LUTs, 58.78% reduction in slices, and 37.85% reduction in delay and 30.86% reduction in power consumption than the existing method.

Keywords: Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Look Up Tables (LUTs), Single path Delay Feedback (SDF).

1. Introduction

The special kind of FFT algorithms has been planned to accumulate real-time processing needs and to shrink the hardware complexity over the most recent decades. As the pipeline FFT algorithms are well appropriate for DSP applications where high-speed data throughput is the most important requirement, some sequential FFT algorithm have been implemented. The combined radix FFT algorithm is depend on sub-transform modules with greatly optimized small length FFT which are combined to produce large FFT. Though, this algorithm does not recommend the simple bit reversing for ordering the output sequences.

The high radix algorithms are lessening the complex multiplications but the butterfly structure becomes complex with some input complex adders. N-point DFT transform is divided into smaller transform known as butterfly in the prime design of FFT. A 2-point DFT and 4-point DFT are known as Radix-2 and Radix-4 FFT in smaller transform.

The structure of two-point butterfly elements has 1 complex multiplication and 2 complex additions and the structure of four-point butterfly structure has 3 complex multiplications and 8 complex additions. In this work, the architecture of combined radix-2, 4 and 8 Single path Delay Feedback FFT has been developed. To enhance the speed of the FFT processor, the combined or mixed radix FFT can be used. We proposed a proficient method to realize a mixed-radix in a small area but maintaining high throughput.

The FFT algorithm is applicable for high and mixed radix FFT in ¹ and this computational complexity is low. The method is given to FFT lengths and in/out patterns. A radix-2/8 FFT algorithm² is depending on the use of a mixture of radix-2 and radix-8 FFT. The number of addition and subtraction operations are needed in the FFT algorithm is equal to that of the radix-2/4 FFT algorithm. The implementation of radix-8 FFT algorithm in ³ explained the high radix FFT algorithm have some advantages are less multiplications and reduced memory access so power consumption can be reduced. The

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disadvantages are more complex multipliers and large silicon area will be consumed. To overcome this problem, efficient approach of high radix butterfly elements has been proposed.

The pipelined structure of radix-4 FFT processor has been presented in ⁴ the pipeline architecture develops the minimum requirement of memory size and reducing power consumption and also speedup the FFT process. The higher radix design algorithms are performed in ⁵ and the implementation of all three algorithms are completed using minimum latency as parameter for similar number of points. The radix-8 FFT can be developed for real valued signals. In ⁶ presented a low power FFT processor using radix-2 algorithm with an 8-parallel multipath delay Commutator. It can achieve better performances and throughput rate.

The 256-point FFT processor⁷ has designed in this architecture, which are apt for low power applications. It is based on radix-4 FFT algorithm. The multiplier structure is presented in 8 high speed, this structure gives a transaction between the high speed of radix-4 multiplier and low power of radix-8 multiplier architecture. Novel Radix-2 Single path Delay Commutator (R2SDC) based Fast Fourier Transformation (FFT)⁹ architecture is introduced for estimating the frequency analysis of discrete time signals.

2. Radix-2 FFT and Radix-4 FFT Algorithm

For calculating DFT, Fast Fourier Transform algorithm is used. The DFT signal is expressed by

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \quad 0 \leq k \leq N-1$$

The fundamental structure of radix-2 butterfly element FFT is illustrated in Figure 1. The Fig.1 shows that butterfly is fundamentally a DFT of size-2. It takes two inputs x_0, x_1 and gives two outputs a_0, a_1 .

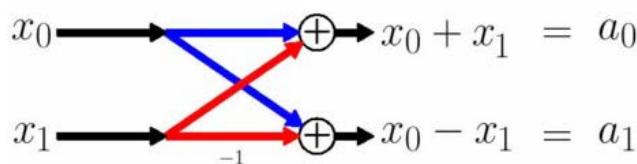


Figure 1. Radix-2 butterfly FFT.

The simplest radix-2 FFT algorithm continuously

divide a DFT into two 1/2 length DFTs of the odd and even indexed time samples. The outputs of smaller FFT's are reused, to determine the large number of outputs, thus generally reducing the total computation cost. All the FFTs, they attain their speed by reusing the outcome of smaller and intermediate calculation to compute several DFT frequency outputs.

Radix-4 FFT algorithm is used to increase the speed by reducing the computational stages. If base increases, the power will decrease. The computational stages are reduced to 50% in radix-4 FFT. It follows in-place algorithm. The computational cost is totally reduced. The radix-4 FFTs need only 75% as many complex multiplications than the radix-2 FFT. The primary block of radix-4 FFT butterfly structure is shown in Figure 2.

$$Y[K] = \sum_{n=0}^{\frac{N}{4}-1} \left\{ y(n) + W_N^{NK/4} (y(n+N/4)) + W_N^{3NK/4} (y(n+3N/4)) \right\} W_N^{nk}$$

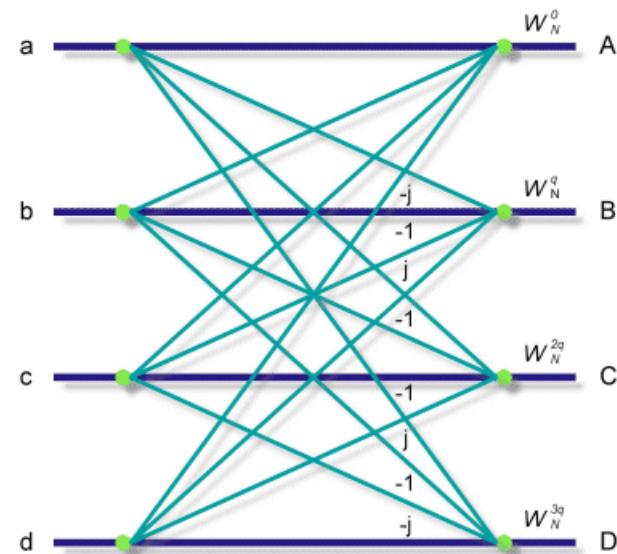


Figure 2. Radix-4 butterfly FFT.

The complex multiplication values are reduced by 25% but the complex addition values are increased by 50% in radix-4 FFT.

3. Radix-8 FFT Algorithm

Radix-8 FFT is used for enhancing the speed of the architecture. The computational stages are reduced to 75% and the value of r is 8, in this algorithm. It is splitted into eight quarter-length DFTs of groups of every eighth section. In radix-8 FFT, the computational path will

be expansively reduced than the radix-2 & 4 FFT. The radix-8 FFT is illustrated in Figure 3. The real addition is 1032 and real multiplication is 264 in radix-2 FFT. The real addition is 976 and the real multiplication is 208 in radix-4 FFT. The Radix-8 FFT of real addition is 972 and the real multiplication is 204.

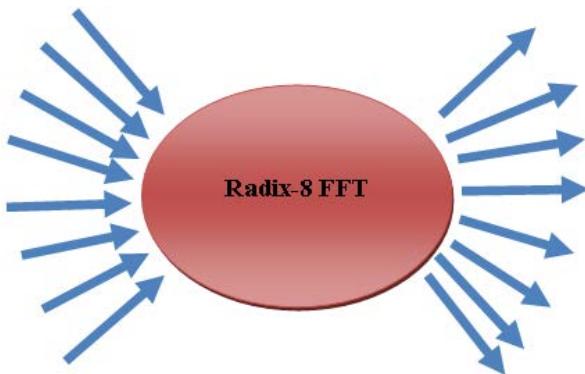


Figure 3. Radix-8 butterfly FFT.

4. Proposed Combined Radix-2, 4 & 8 based Single Path Delay Feedback (SDF) FFT

The method of combined Radix-2, 4 and 8 based SDF FFT has been implemented in this paper. This architecture has a lesser amount of computational path and also enhances the performances of FFT processor. SDF architecture, the data sequences of inputs are pass through one single path. The butterfly processing element performs the computation on the data. The addition and subtraction operation is done in butterfly elements. The carry select adder circuit is used for adder operation in this architecture. This adder structure is very efficient in this architecture. Though, the hardware utilization is more in this architecture and also the power consumption is increase due to using bulk of worthless intermediate processing digital signals. To conquer this problem, the design of radix-2, 4 based SDF FFT architectures are combined to reduce the hardware operation of the processor. The proposed method which is drastically reduces the occupied slices, power consumption and latency. The computational stages are reduced than the existing R2SDF method. The structure of combined radix-2, 4 and 8 FFT is shown in Figure 4. The architecture of sixteen point SDF FFT is illustrated in Figure 5.

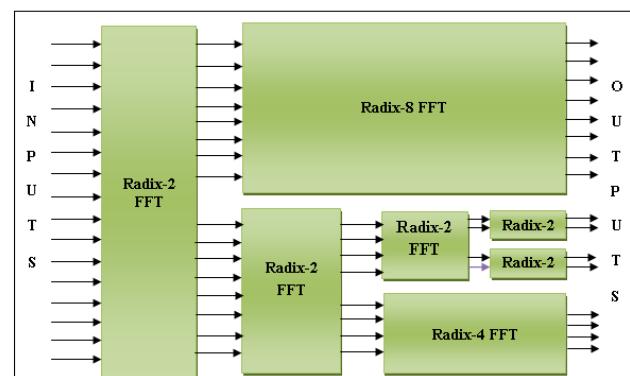


Figure 4. Structure of combined Radix-2, 4 and 8 FFT.

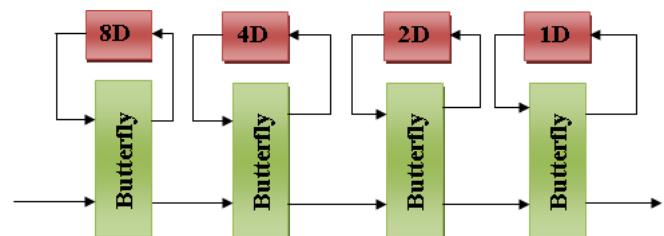


Figure 5. Architecture of 16 Point Single path Delay Feedback (SDF) FFT.

5. Results and Discussion

By using MODELSIM 6.3C, the combined radix-2, 4, and 8 based SDF FFT has been designed. The Xilinx ISE 10.1i design tool is used for synthesizing the performance of FFT architecture. The simulation result is illustrated in Figure 6. Table 1 illustrates the comparison analysis of existing R2SDF FFT and proposed combined radix-2, 4 and 8 based SDF FFT. Figure 7 illustrates the performance of existing and proposed combined Radix-2, 4 and 8 based SDF FFT.

Table 1. Comparison of existing R2SDF FFT and proposed combined Radix-2, 4 and 8 based SDF FFT

Types of parameters	No of occupied Slices	No of LUTs	Delay(ns)	Power(w)
Existing Radix-2 SDF FFT	609	850	15.062	2.197
Proposed Combined radix-2,4 and 8 based SDF FFT	251	319	9.360	1.519
Percentage reduction %	58.78	62.47	37.85	30.86

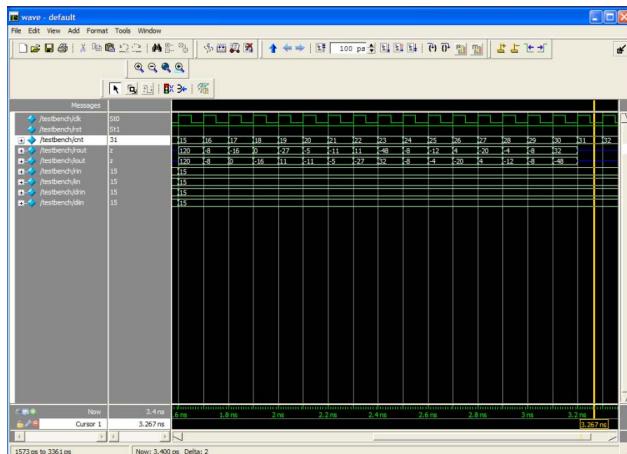


Figure 6. Simulation result of combined radix-2,4 and 8 based SDF FFT.

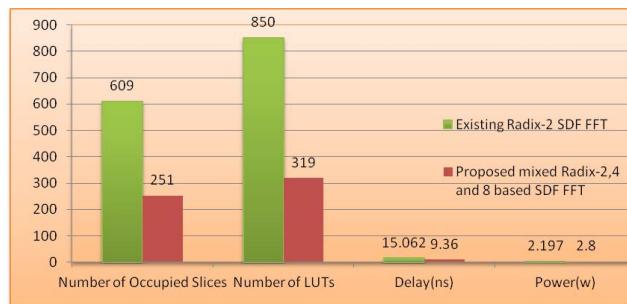


Figure 7. Performance evaluation of existing R2SDF FFT and proposed combined Radix-2, 4 and 8 based SDF FFT.

6. Conclusion

The combined radix-2, 4 and 8 based SDF FFT has been developed in this paper. The goal is to shrink the area, power and latency of the processor. The proposed architecture offers 58.78% decrease in slices, 62.47% decrease in LUTs, and 37.85% reduction in delay and

30.86% decrease in power consumption than the existing method. Compared to existing method, the proposed method of computational stages is reduced and gives better performances than the traditional one. Thus, this design is particularly useful for low power applications such as WLAN, OFDM etc. For future work, we plan to optimize complex multiplier for more power reduction.

7. References

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