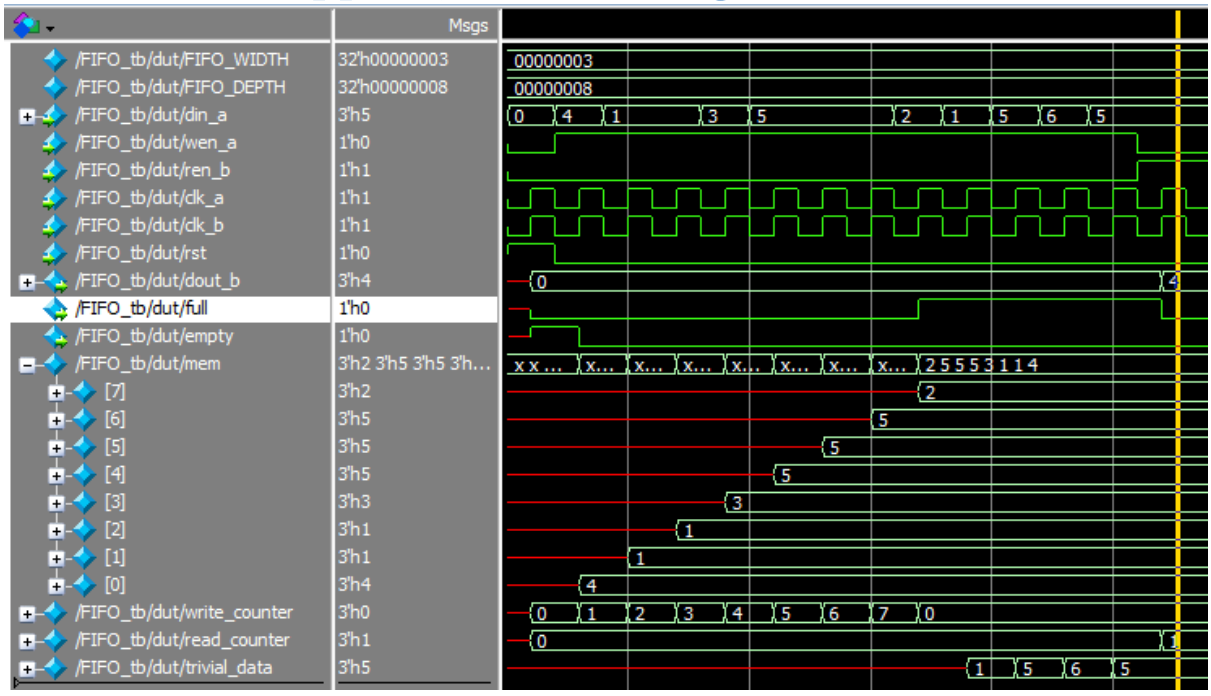
By	Mohamed Ahmed Mohamed Hussein

FIFO Documentation

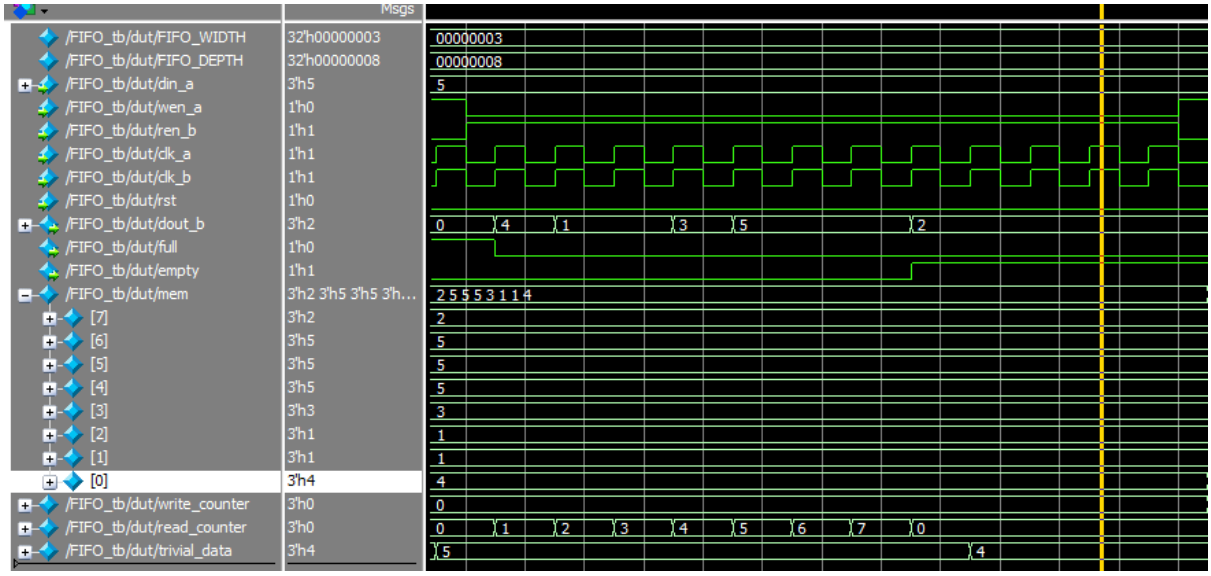
Test bench snippets**(case: writing until full):**



Notes:

- output
- Inputs
- you can copy the code
- focus on the full flag and the freezing of write_counter
- you can check the ignored data in trivial_data

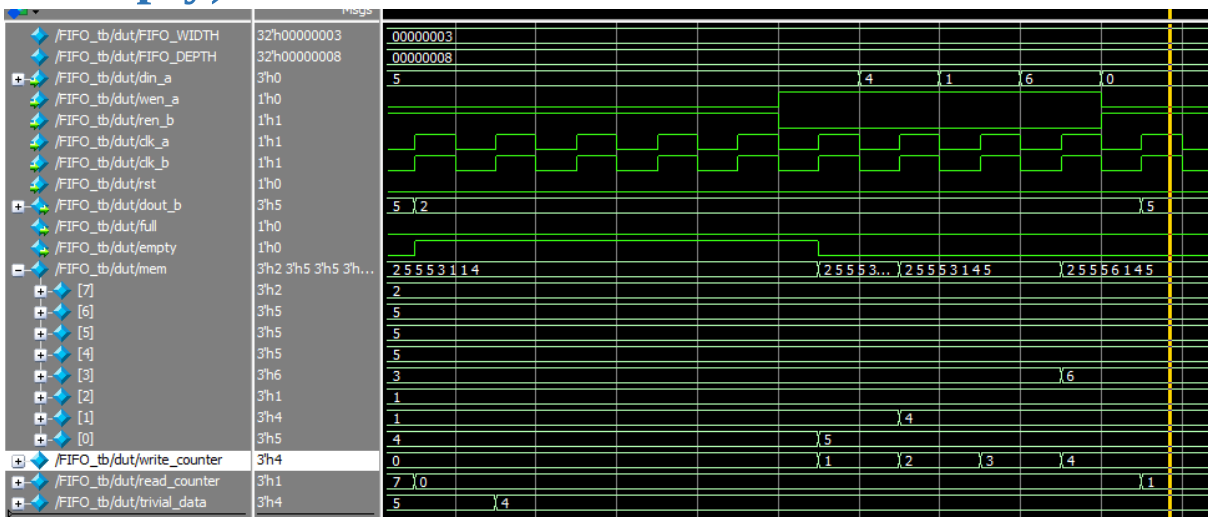
Test bench snippets**(case: reading until it's empty):**



Notes:

- output
- Inputs
- you can copy the code
- focus on the empty flag and the freezing of read_counter
- focus on dout_b you will find the data which was kept in the memory from previous writing

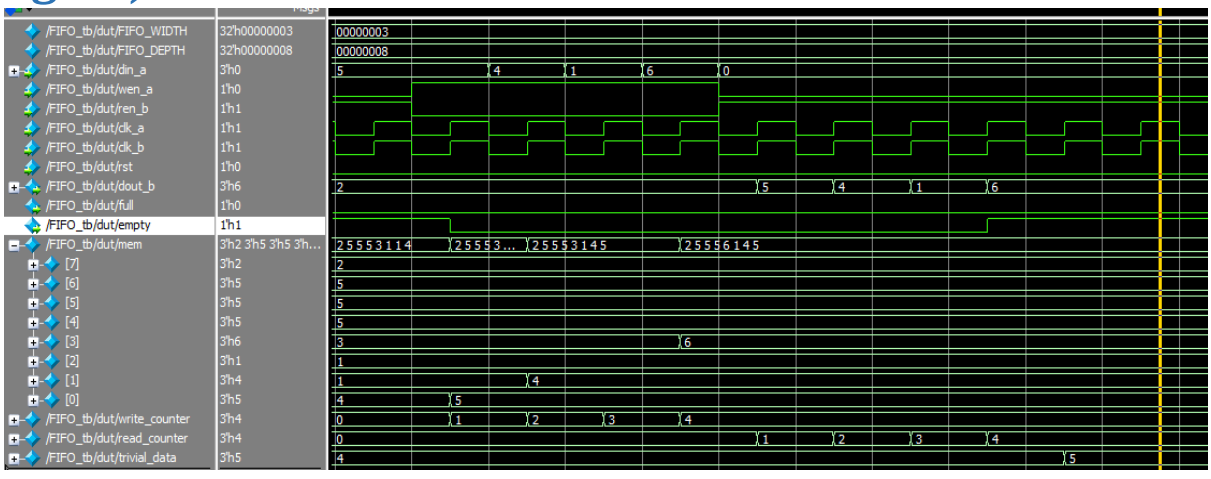
Test bench snippets**(case: writing again so it's not full or empty):**



Notes:

- output
- Inputs
- you can copy the code
- focus on the full and empty flags they are not asserted

Test bench snippets**(case: reading until it's empty again):**

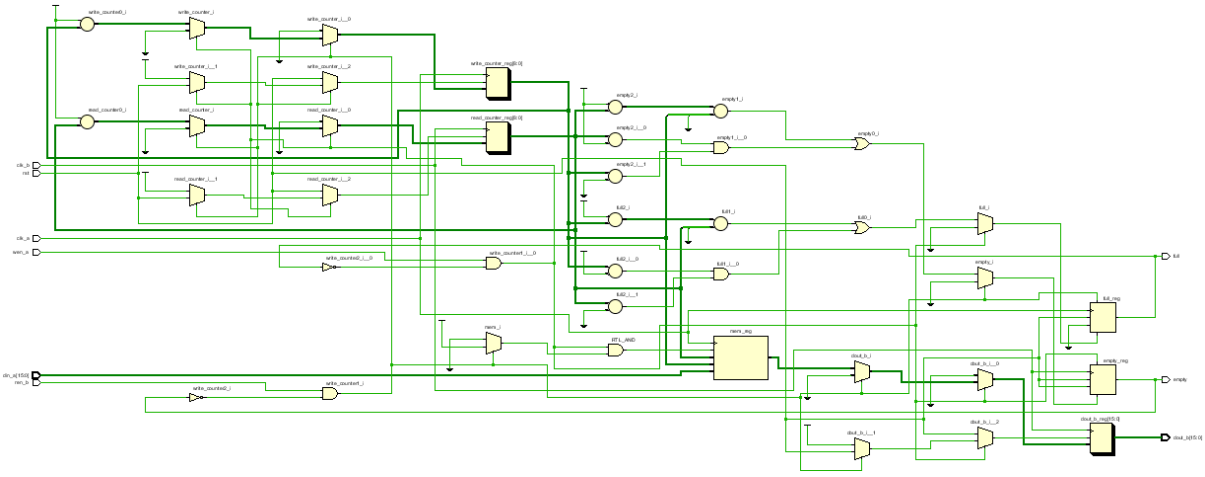


Notes:

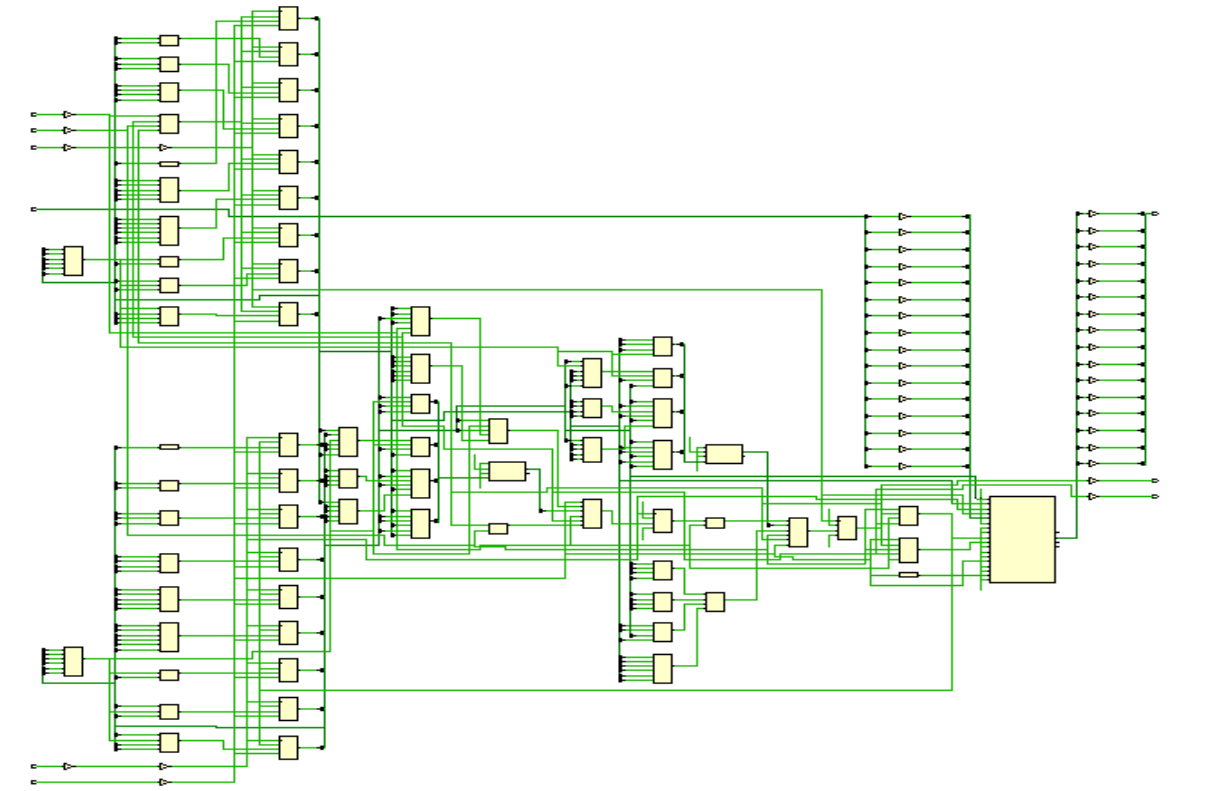
- output
- Inputs
- you can copy the code

- I made this case to test the functionality in the middle of the memory
- focus on the empty flag

Elaboration:



Synthesis:



Utilization Report:

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Debug

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<1%)

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
FIFO_Model	39	20	0.5	39	2

Timing Report:

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | Debug

- General Information
- Timer Settings
- Design Timing Summary
- Check Timing (154)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	113	Total Number of Endpoints:	113	Total Number of Endpoints:	NA

There are no user specified timing constraints.

Implementation: