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Spartan 6-DSP48A1



Introduction to DSP Blocks in FPGAs

Digital Signal Processing (DSP) Blocks are specialized hardware components within Field-Programmable Gate Arrays (FPGAs) designed to efficiently perform complex mathematical operations required in digital signal processing tasks. These blocks are crucial for applications that involve real-time processing of signals, such as audio and video processing, communications, and control systems.

Key Functions of DSP Blocks

1. Multiplication and Accumulation:

- DSP blocks are optimized for performing multiply-accumulate operations, which are fundamental to many DSP algorithms. These operations can be executed in a single clock cycle, significantly speeding up processing times compared to using general-purpose logic.

2. Arithmetic Operations:

- Besides multiplication, DSP blocks can perform a variety of arithmetic operations such as addition, subtraction, and division. They are designed to handle these operations with high precision and efficiency.

3. Filtering:

- In signal processing, filtering is a common operation used to remove unwanted components from a signal. DSP blocks can implement various types of filters (e.g., FIR, IIR) with high performance, which is essential for applications like audio signal processing and communication systems.

4. Fourier Transform:

- DSP blocks can accelerate the computation of Fourier transforms, which are used to convert signals from the time domain to the frequency domain. This is particularly useful in applications such as spectral analysis and modulation/demodulation in communications.

5. Signal Modulation and Demodulation:

- These blocks are capable of handling complex modulation and demodulation schemes, which are critical in modern digital communication systems.

6. Data Compression and Decompression:

- DSP blocks can be used to implement algorithms for data compression and decompression, which are vital for efficient storage and transmission of data.

Advantages of Using DSP Blocks in FPGAs

• High Performance:

- DSP blocks provide high-speed processing capabilities, enabling real-time signal processing.

• Resource Efficiency:

- They offload computationally intensive tasks from the general-purpose logic, freeing up FPGA resources for other functions.

• Flexibility:

- The configurability of FPGAs allows designers to tailor DSP blocks to specific applications, achieving optimal performance for diverse tasks.

- **Parallelism:**
 - Multiple DSP blocks can operate in parallel, offering significant advantages in terms of processing throughput for large-scale signal processing tasks.

Spartan-6 DSP48A1 Block

The **Spartan-6** family of FPGAs from Xilinx includes the **DSP48A1** block, a versatile and powerful DSP slice designed to deliver high-performance digital signal processing capabilities. The DSP48A1 block supports the following features:

- **25 x 18-bit two's complement multiplication**
- **48-bit addition/subtraction**
- **Dedicated cascaded routing for efficient pipelining**
- **Pre-adder functionality for symmetric FIR filter implementations**

The DSP48A1 block is an essential component for implementing high-speed digital signal processing algorithms in Spartan-6 FPGAs, providing the necessary hardware acceleration for applications requiring intensive mathematical computations.

QuestaSim Snippets:

Before beginning I want to clarify some notes:

- I divided the test bench to 7 cases and as so will be the snippets, the divided cases were explained well in the test bench code above
- I removed all the resets and clock enables from the snippets except for (RSTA , CEA) that all the other resets are the same as RSTA and all other clock enables are the same as CEA, and I've done that so by that the snippets will be more detectable
- I arranged the signals in an order that the more related signals are above or below each other to give more readability
- In each case I might take some of the following case as the output is showed after a one positive edge from changing the opmode_out
- Focus on the signals has (_out) in it's name
- Happy tracing!

- **Case 1 :**

	Address	Value
+ DSP48A1_tb/A	18'h000014	000000000000c
+ DSP48A1_tb/B	18'h000006	0000000000000
+ DSP48A1_tb/BCIN	18'h00000d	000000000000c
+ DSP48A1_tb/D	18'h00001c	0000000000008
+ DSP48A1_tb/C	48'h00000000000017	00000000000000007
+ DSP48A1_tb/PCIN	48'h0000000000000f	000000000000000016
+ DSP48A1_tb/dut/B_in	18'h000006	000000000000c
+ DSP48A1_tb/dut/mux_opmode4_...	18'h000005	000000000000c
+ DSP48A1_tb/BCOUT	18'h000005	000000000000c
+ DSP48A1_tb/OPMODE	8'b01010001	00000000011000000
+ DSP48A1_tb/dut/OPMODE_OUT	8'b01100000	00000000011000000
DSP48A1_tb/CARRYIN	1'h1	00000000011000000
DSP48A1_tb/dk	1'h0	00000000011000000
+ DSP48A1_tb/dut/multiplier_out	36'h0000000096	00000000000000150
+ DSP48A1_tb/M	36'h00000000000	00000000000000150
+ DSP48A1_tb/P	48'h0000000000000	00000000000000000
+ DSP48A1_tb/PCOUT	48'h00000000000000	00000000000000000
+ DSP48A1_tb/dut/post_out	48'h00000000000001	00000000000000001
DSP48A1_tb/dut/carry_out_post	1'h0	00000000000000001
DSP48A1_tb/CARRYOUT	1'h0	00000000000000001
DSP48A1_tb/CARRYOUTF	1'h0	00000000000000001
+ DSP48A1_tb/dut/A_OUT	18'h00001e	0000000000001c
+ DSP48A1_tb/dut/B_OUT	18'h000005	0000000000000c
+ DSP48A1_tb/dut/D_OUT	18'h000010	00000000000008
+ DSP48A1_tb/dut/C_OUT	48'h00000000000017	00000000000000007
+ DSP48A1_tb/dut/pre_out	18'h00000b	0000000000001b
+ DSP48A1_tb/dut/ACOUT	18'h00001e	0000000000001c
+ DSP48A1_tb/dut/X_OUT	48'h0000000000000	00000000000000000
+ DSP48A1_tb/dut/Z_OUT	48'h0000000000000	00000000000000000
DSP48A1_tb/dut/carry_in_casca...	1'h1	00000000000000000
DSP48A1_tb/dut/CIN	1'h1	00000000000000000
DSP48A1_tb/CEA	1'h1	00000000000000000
DSP48A1_tb/RSTA	1'h0	00000000000000000

• Case 2 :

	Msgs	
/DSP48A1_tb/A	18'h00008	00014 0001f 00005 00018 0000e
/DSP48A1_tb/B	18'h00001	00006 00007 0000e 00001
/DSP48A1_tb/BCIN	18'h0000f	0000d 0000e 00002 00009 0000f
/DSP48A1_tb/D	18'h00015	0001c 0000c 0001b 00000 0001a
/DSP48A1_tb/C	48'h0000000000017	000000000017
/DSP48A1_tb/PCIN	48'h0000000000014	00000000... 00000000000c 000000000012 000000000002 00000000
/DSP48A1_tb/dut/B_in	18'h00001	00006 00007 0000e 00001
/DSP48A1_tb/dut/mux_opmode4_...	18'h3ffff	00016 00013 0000d 3fff
/DSP48A1_tb/BCOUT	18'h3ffff	00016 00013 0000d 3fff
/DSP48A1_tb/OPMODE	8'b11110010	01010001 10010001 11010001 11110010
/DSP48A1_tb/dut/OPMODE_OUT	8'b11110010	01010001 10010001 11010001 11110010
/DSP48A1_tb/CARRYIN	1'h0	
/DSP48A1_tb/dut/multiplier_out	36'h0005fffe8	0000001b8 00000024d 000000041 0005fffe8
/DSP48A1_tb/M	36'h000000041	000000096 0000001b8 00000024d 000000041
/DSP48A1_tb/P	48'hffffffffdb3	000000000001 000000000097 ffffffff48 ffffffffdb3
/DSP48A1_tb/PCOUT	48'hffffffffdb3	000000000001 000000000097 ffffffff48 ffffffffdb3
/DSP48A1_tb/dut/post_out	48'h000000000024d	000000000097 ffffffff48 ffffffffdb3 000000000024d
/DSP48A1_tb/dut/carry_out_post	1'h1	
/DSP48A1_tb/CARRYOUT	1'h1	
/DSP48A1_tb/CARRYOUTF	1'h1	
/DSP48A1_tb/dut/A_OUT	18'h00018	00014 0001f 00005 00018
/DSP48A1_tb/dut/B_OUT	18'h00001	00006 00007 0000e 00001
/DSP48A1_tb/dut/D_OUT	18'h00000	0001c 0000c 0001b 00000
/DSP48A1_tb/dut/C_OUT	48'h0000000000017	000000000017
/DSP48A1_tb/dut/pre_out	18'h3ffff	00016 00013 0000d 3fff
/DSP48A1_tb/dut/ACOUT	18'h00018	00014 0001f 00005 00018
/DSP48A1_tb/dut/X_OUT	48'hffffffffdb3	000000000096 000000001b8 000000000024d ffffffffdb3
/DSP48A1_tb/dut/Z_OUT	48'h0000000000000	000000000000
/DSP48A1_tb/dut/carry_in_casca...	1'h1	
/DSP48A1_tb/dut/CIN	1'h0	
/DSP48A1_tb/CEA	1'h1	
/DSP48A1_tb/RSTA	1'h0	

• Case 3 :

/DSP48A1_tb/A	18'h00013	00018	00008	0000d	00018	00013
/DSP48A1_tb/B	18'h00005	00001		00005		
/DSP48A1_tb/BCIN	18'h0000e	00009	0000f	00008	00002	0000e
/DSP48A1_tb/D	18'h0000f	00000	00015	00017	00002	0000f
/DSP48A1_tb/C	48'h000000000017	000000000017				
/DSP48A1_tb/PCIN	48'h000000000019	0000... 000000000014	00000000001d	000000000011	0000000000	
/DSP48A1_tb/dut/B_in	18'h00005	00001		00005		
/DSP48A1_tb/dut/mux_opmode4_...	18'h00007	3ffff	00014	00016	00007	0
/DSP48A1_tb/BCOUT	18'h00007	3ffff	00014	00016	00007	0
/DSP48A1_tb/OPMODE	8'b00110011	11110010		00110011		
/DSP48A1_tb/dut/OPMODE_OUT	8'b00110011	11110010		00110011		
/DSP48A1_tb/CARRYIN	1'h1					
/DSP48A1_tb/dk	1'h0					
/DSP48A1_tb/dut/multiplier_out	36'h0000000a8	0005ffffe8	0000000a0	00000011e	0000000a8	0
/DSP48A1_tb/M	36'h00000011e	000000041	0005ffffe8	0000000a0	00000011e	0
/DSP48A1_tb/P	48'h00000000024d	ffffffffdb3	00000000024d	ffffffffdb2	00000000024d	0
/DSP48A1_tb/PCOUT	48'h00000000024d	ffffffffdb3	00000000024d	ffffffffdb2	00000000024d	0
/DSP48A1_tb/dut/post_out	48'h00f000600008	00000000024d	ffffffffdb2	00000000024d	00200... 00f00...	0
/DSP48A1_tb/dut/carry_out_post	1'h0					
/DSP48A1_tb/CARRYOUT	1'h1					
/DSP48A1_tb/CARRYOUTF	1'h1					
/DSP48A1_tb/dut/A_OUT	18'h00018	00018	00008	0000d	00018	0
/DSP48A1_tb/dut/B_OUT	18'h00005	00001		00005		
/DSP48A1_tb/dut/D_OUT	18'h00002	00000	00015	00017	00002	0
/DSP48A1_tb/dut/C_OUT	48'h000000000017	000000000017				
/DSP48A1_tb/dut/pre_out	18'h00007	3ffff	00014	00016	00007	0
/DSP48A1_tb/dut/ACOUT	18'h00018	00018	00008	0000d	00018	0
/DSP48A1_tb/dut/X_OUT	48'h00f000600007	ffffffffdb3	00000000024d	ffffffffdb2	00200... 00f00...	0
/DSP48A1_tb/dut/Z_OUT	48'h000000000000	000000000000				
/DSP48A1_tb/dut/carry_in_casca...	1'h1					
/DSP48A1_tb/dut/CIN	1'h1					
/DSP48A1_tb/CEA	1'h1					
/DSP48A1_tb/RSTA	1'h0					



































































- **Case 4 :**

		msgs
+	/DSP48A1_tb/A	18'h00017
+	/DSP48A1_tb/B	18'h0000d
+	/DSP48A1_tb/BCIN	18'h00008
+	/DSP48A1_tb/D	18'h00003
+	/DSP48A1_tb/C	48'h000000000017
+	/DSP48A1_tb/PCIN	48'h000000000001
+	/DSP48A1_tb/dut/B_in	18'h0000d
+	/DSP48A1_tb/dut/mux_opmode4...	18'h000020
+	/DSP48A1_tb/BCOUT	18'h000020
+	/DSP48A1_tb/OPMODE	8'b00010100
+	/DSP48A1_tb/dut/OPMODE_OUT	8'b00010100
	/DSP48A1_tb/CARRYIN	1'h1
	/DSP48A1_tb/dk	1'h0
+	/DSP48A1_tb/dut/multiplier_out	36'h0000000020
+	/DSP48A1_tb/M	36'h000000176
+	/DSP48A1_tb/P	48'h0180002c0023
+	/DSP48A1_tb/PCOUT	48'h0180002c0023
+	/DSP48A1_tb/dut/post_out	48'h000000000002
	/DSP48A1_tb/dut/carry_out_post	1'h0
	/DSP48A1_tb/CARRYOUT	1'h0
	/DSP48A1_tb/CARRYOUTF	1'h0
+	/DSP48A1_tb/dut/A_OUT	18'h00001
+	/DSP48A1_tb/dut/B_OUT	18'h00008
+	/DSP48A1_tb/dut/D_OUT	18'h00018
+	/DSP48A1_tb/dut/C_OUT	48'h000000000017
+	/DSP48A1_tb/dut/pre_out	18'h000020
+	/DSP48A1_tb/dut/ACOUT	18'h00001
+	/DSP48A1_tb/dut/X_OUT	48'h000000000000
+	/DSP48A1_tb/dut/Z_OUT	48'h000000000001
	/DSP48A1_tb/dut/carry_in_casca...	1'h0
	/DSP48A1_tb/dut/CIN	1'h1
	/DSP48A1_tb/CEA	1'h1
	/DSP48A1_tb/RSTA	1'h0

• Case 5 :

	18'h00014	00001	00017	00015	00009	00014	
+ /DSP48A1_tb/A	18'h00005	00008	0000d	0000a	00006	00005	
+ /DSP48A1_tb/B	18'h0000f	00001	00008	00009	0000a	0000f	
+ /DSP48A1_tb/BCIN	18'h00003	00018	00003	00016	0001f	00003	
+ /DSP48A1_tb/D	48'h000000000017	000000000017					
+ /DSP48A1_tb/C	48'h00000000001e	000...	000000000001	000000000013	000000000000	000000000001	
+ /DSP48A1_tb/PCIN	18'h00005	00008	0000d	0000a	00006	00005	
+ /DSP48A1_tb/dut/B_in	18'h00006	00020	00010	00020	00006	00005	
+ /DSP48A1_tb/dut/mux_opmode4_...	18'h00006	00020	00010	00020	00006	00005	
+ /DSP48A1_tb/BCOUT	8'b00001000	00010100			00001000		
+ /DSP48A1_tb/OPMODE	8'b00001000	00010100			00001000		
+ /DSP48A1_tb/dut/OPMODE_OUT	1'h0						
+ /DSP48A1_tb/CARRYIN	1'h0						
+ /DSP48A1_tb/dut/multiplier_out	36'h0000000036	0000000020	000000170	0000002a0	000000036	00	
+ /DSP48A1_tb/M	36'h0000002a0	0000000176	0000000020	000000170	0000002a0	00	
+ /DSP48A1_tb/P	48'h000000000000	0180002c0023	000000000002	000000000013	000000000000		
+ /DSP48A1_tb/PCOUT	48'h000000000000	0180002c0023	000000000002	000000000013	000000000000		
+ /DSP48A1_tb/dut/post_out	48'h000000000000	000...	00000...	00000...	000000000013	000000000000	
+ /DSP48A1_tb/dut/carry_out_post	1'h0						
+ /DSP48A1_tb/CARRYOUT	1'h0						
+ /DSP48A1_tb/CARRYOUTF	1'h0						
+ /DSP48A1_tb/dut/A_OUT	18'h00009	00001	00017	00015	00009	00	
+ /DSP48A1_tb/dut/B_OUT	18'h00006	00008	0000d	0000a	00006	00	
+ /DSP48A1_tb/dut/D_OUT	18'h0001f	00018	00003	00016	0001f	00	
+ /DSP48A1_tb/dut/C_OUT	48'h000000000017	000000000017					
+ /DSP48A1_tb/dut/pre_out	18'h00025	00020	00010	00020	00025	00	
+ /DSP48A1_tb/dut/ACOUT	18'h00009	00001	00017	00015	00009	00	
+ /DSP48A1_tb/dut/X_OUT	48'h000000000000	000000000000					
+ /DSP48A1_tb/dut/Z_OUT	48'h000000000000	000...	000000000001	000000000013	000000000000		
+ /DSP48A1_tb/dut/carry_in_casca...	1'h0						
+ /DSP48A1_tb/dut/CIN	1'h0						
+ /DSP48A1_tb/CEA	1'h1						
+ /DSP48A1_tb/RSTA	1'h0						

• Case 6 :

	Msgs								
  /DSP48A1_tb/A	18'h00009	00...	00014	0000e	00013	00009			
  /DSP48A1_tb/B	18'h00009	00...	00005	0000d	00003	00009			
  /DSP48A1_tb/BCIN	18'h00001	00...	0000f	00008	0000c	00001			
  /DSP48A1_tb/D	18'h0001e	00...	00003	0001a	00011	0001e			
  /DSP48A1_tb/C	48'h0000000000017	0000000000017							
  /DSP48A1_tb/PCIN	48'h000000000000d	00...	0000000001e	00000000002	0000000001d	0000000000d			
  /DSP48A1_tb/dut/B_in	18'h00009	00...	00005	0000d	00003	00009			
  /DSP48A1_tb/dut/mux_opmode4_...	18'h00003	00006	00005	0000d	00003	00009			00009
  /DSP48A1_tb/BCOUT	18'h00003	00006	00005	0000d	00003	00009			00009
  /DSP48A1_tb/OPMODE	8'b00001100	00001000			00001100				
  /DSP48A1_tb/dut/OPMODE_OUT	8'b00001100	00001000			00001100				
  /DSP48A1_tb/CARRYIN	1'h0								
  /DSP48A1_tb/clk	1'h0								
  /DSP48A1_tb/dut/multiplier_out	36'h0000000039	0000000036	0000000064	00000000b6	0000000039	0000000039			0000000039
  /DSP48A1_tb/M	36'h00000000b6	00000002a0	0000000036	0000000064	00000000b6	00000000b6			00000000b6
  /DSP48A1_tb/P	48'h0000000000000	0000000000000							0000000000000
  /DSP48A1_tb/PCOUT	48'h0000000000000	0000000000000							0000000000000
  /DSP48A1_tb/dut/post_out	48'h0000000000017	0000000000000				0000000000017			
  /DSP48A1_tb/dut/carry_out_post	1'h0								
  /DSP48A1_tb/CARRYOUT	1'h0								
  /DSP48A1_tb/CARRYOUTF	1'h0								
  /DSP48A1_tb/dut/A_OUT	18'h00013	00009	00014	0000e	00013	00009			00009
  /DSP48A1_tb/dut/B_OUT	18'h00003	00006	00005	0000d	00003	00009			00009
  /DSP48A1_tb/dut/D_OUT	18'h00011	0001f	00003	0001a	00011	0001e			0001e
  /DSP48A1_tb/dut/C_OUT	48'h0000000000017	0000000000017							
  /DSP48A1_tb/dut/pre_out	18'h00014	00025	00008	00027	00014	00027			00027
  /DSP48A1_tb/dut/ACOUT	18'h00013	00009	00014	0000e	00013	00009			00009
  /DSP48A1_tb/dut/X_OUT	48'h0000000000000	0000000000000							
  /DSP48A1_tb/dut/Z_OUT	48'h0000000000017	0000000000000				0000000000017			
  /DSP48A1_tb/dut/carry_in_casca...	1'h0								
  /DSP48A1_tb/dut/CIN	1'h0								
  /DSP48A1_tb/CEA	1'h1								
  /DSP48A1_tb/RSTA	1'h0								

- **Case 7 :**

Msgs																	
	/DSP48A1_tb/A	18'h00008	00009			00008											
	/DSP48A1_tb/B	18'h00004	00009			00004											
	/DSP48A1_tb/BCIN	18'h0000d	00001			0000d											
	/DSP48A1_tb/D	18'h00014	0001e			00014											
	/DSP48A1_tb/C	48'h000000000017	0000000000017														
	/DSP48A1_tb/PCIN	48'h000000000008	00000000000d			000000000008											
	/DSP48A1_tb/dut/B_in	18'h00004	00009			00004											
	/DSP48A1_tb/dut/mux_opmode4_...	18'h00004	00003	00009				00004									
	/DSP48A1_tb/B/COU	18'h00004	00003	00009				00004									
	/DSP48A1_tb/OPMODE	8'b00001100	00001100														
	/DSP48A1_tb/dut/OPMODE_OUT	8'b00001100	00001100														
	/DSP48A1_tb/CARRYIN	1'h1															
	/DSP48A1_tb/clk	1'h1															
	/DSP48A1_tb/dut/multiplier_out	36'h0000000020	0000...	0000000051				0000000020									
	/DSP48A1_tb/M	36'h0000000020	0000...	0000000039				0000000051				0000000020					
	/DSP48A1_tb/P	48'h0000000000017	0000...	000000000017													
	/DSP48A1_tb/PCOUT	48'h0000000000017	0000...	000000000017													
	/DSP48A1_tb/dut/post_out	48'h0000000000017	0000000000017														
	/DSP48A1_tb/dut/carry_out_post	1'h0															
	/DSP48A1_tb/CARRYOUT	1'h0															
	/DSP48A1_tb/CARRYOUTF	1'h0															
	/DSP48A1_tb/dut/A_OUT	18'h00008	00013	00009				00008									
	/DSP48A1_tb/dut/B_OUT	18'h00004	00003	00009				00004									
	/DSP48A1_tb/dut/D_OUT	18'h00014	00011	0001e				00014									
	/DSP48A1_tb/dut/C_OUT	48'h0000000000017	0000000000017														
	/DSP48A1_tb/dut/pre_out	18'h00018	00014	00027				00018									
	/DSP48A1_tb/dut/ACOUT	18'h00008	00013	00009				00008									
	/DSP48A1_tb/dut/X_OUT	48'h0000000000000	0000000000000														
	/DSP48A1_tb/dut/Z_OUT	48'h0000000000017	0000000000017														
	/DSP48A1_tb/dut/carry_in_casca...	1'h0															
	/DSP48A1_tb/dut/CIN	1'h0															
	/DSP48A1_tb/CEA	1'h1															
	/DSP48A1_tb/RSTA	1'h0															

Elaboration:

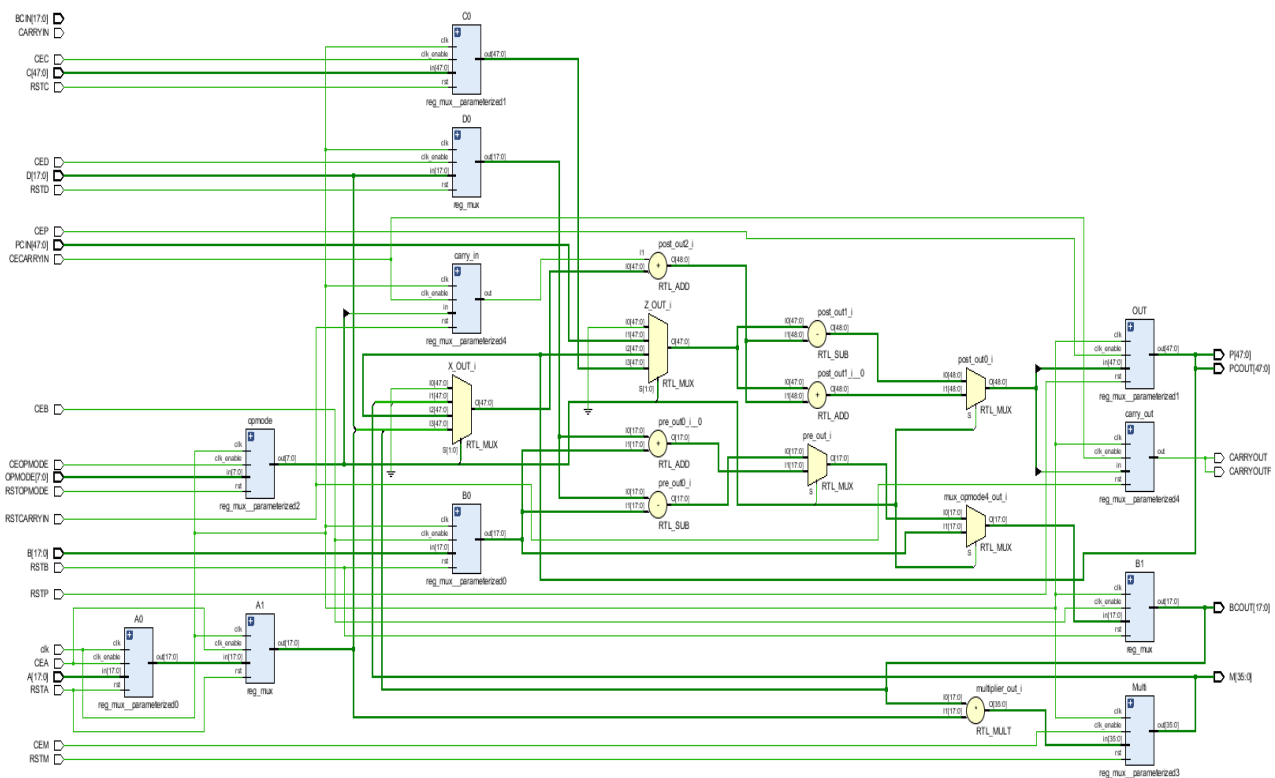
• Messages:

Tcl Console Messages x Log Reports Design Runs

Info (5) Status (9) Show All

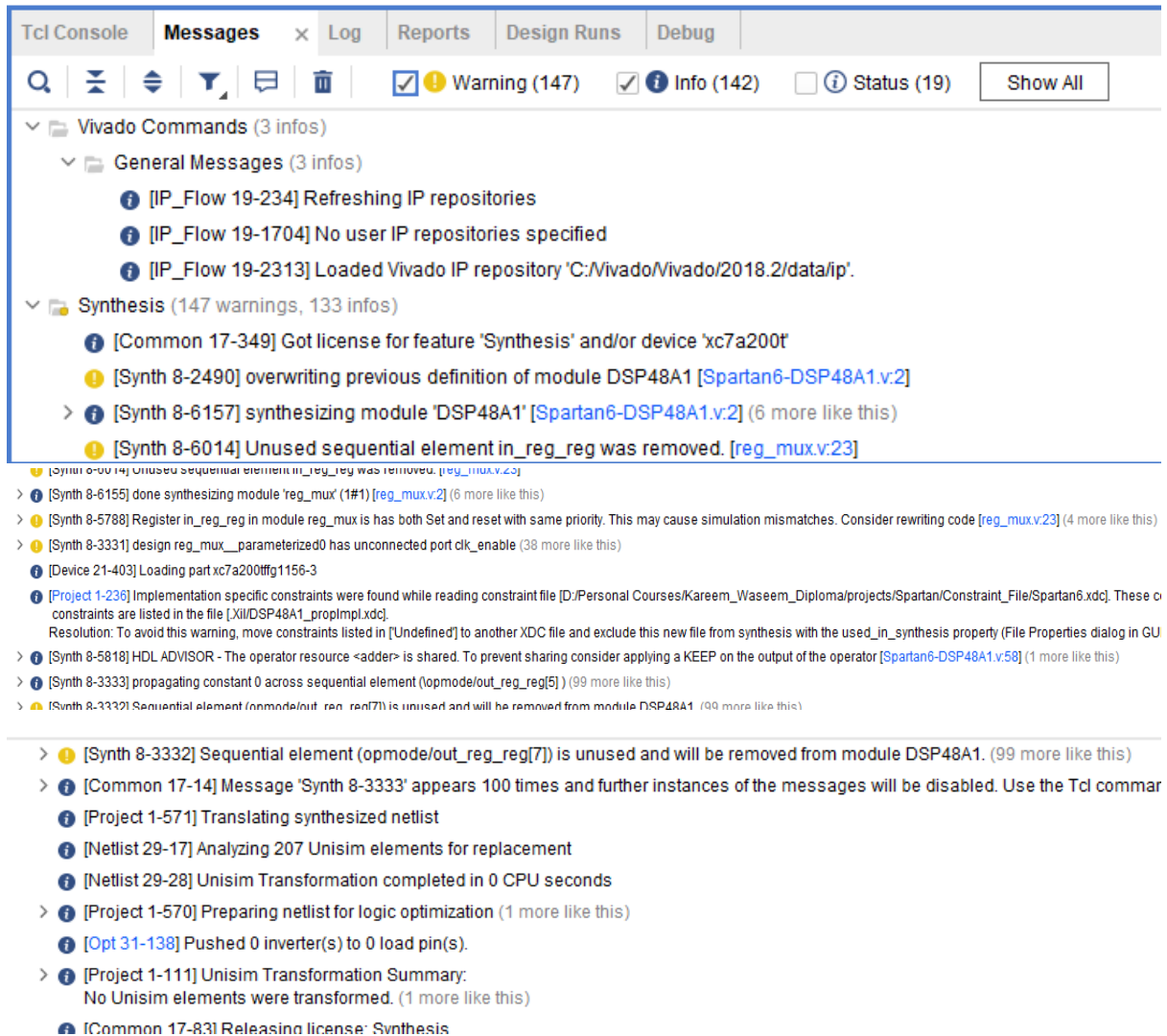
- Vivado Commands (3 infos)
 - General Messages (3 infos)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Mivado/Vivado/2018.2/data/ip'.
 - Elaborated Design (2 infos)
 - General Messages (2 infos)
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

• Schematic:



Synthesis:

• Messages:



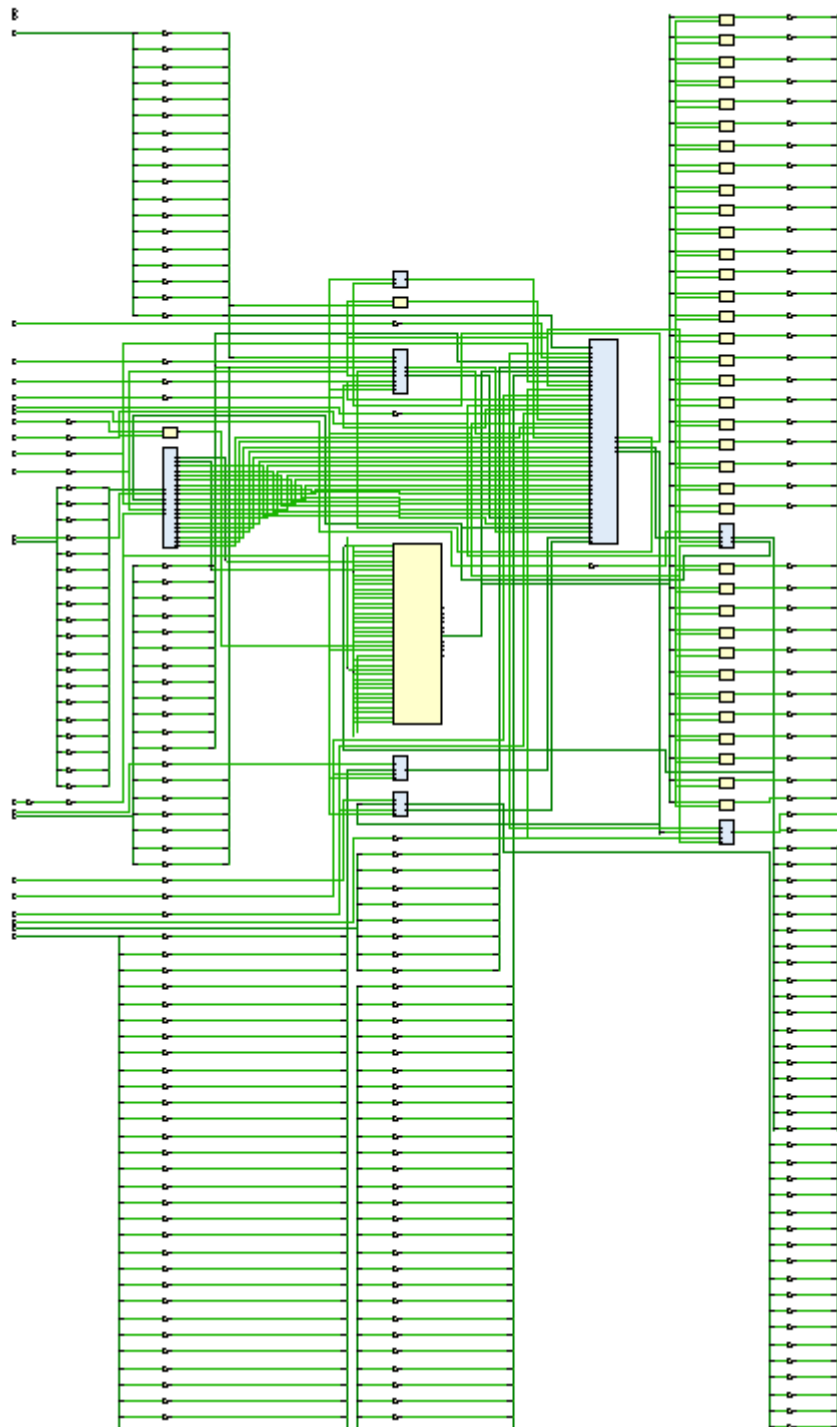
The screenshot displays the Vivado Messages window, which is organized into tabs: Tcl Console, Messages (selected), Log, Reports, Design Runs, and Debug. The Messages tab shows a list of messages categorized by type: Warning (147), Info (142), and Status (19). A 'Show All' button is visible in the top right corner of the message list.

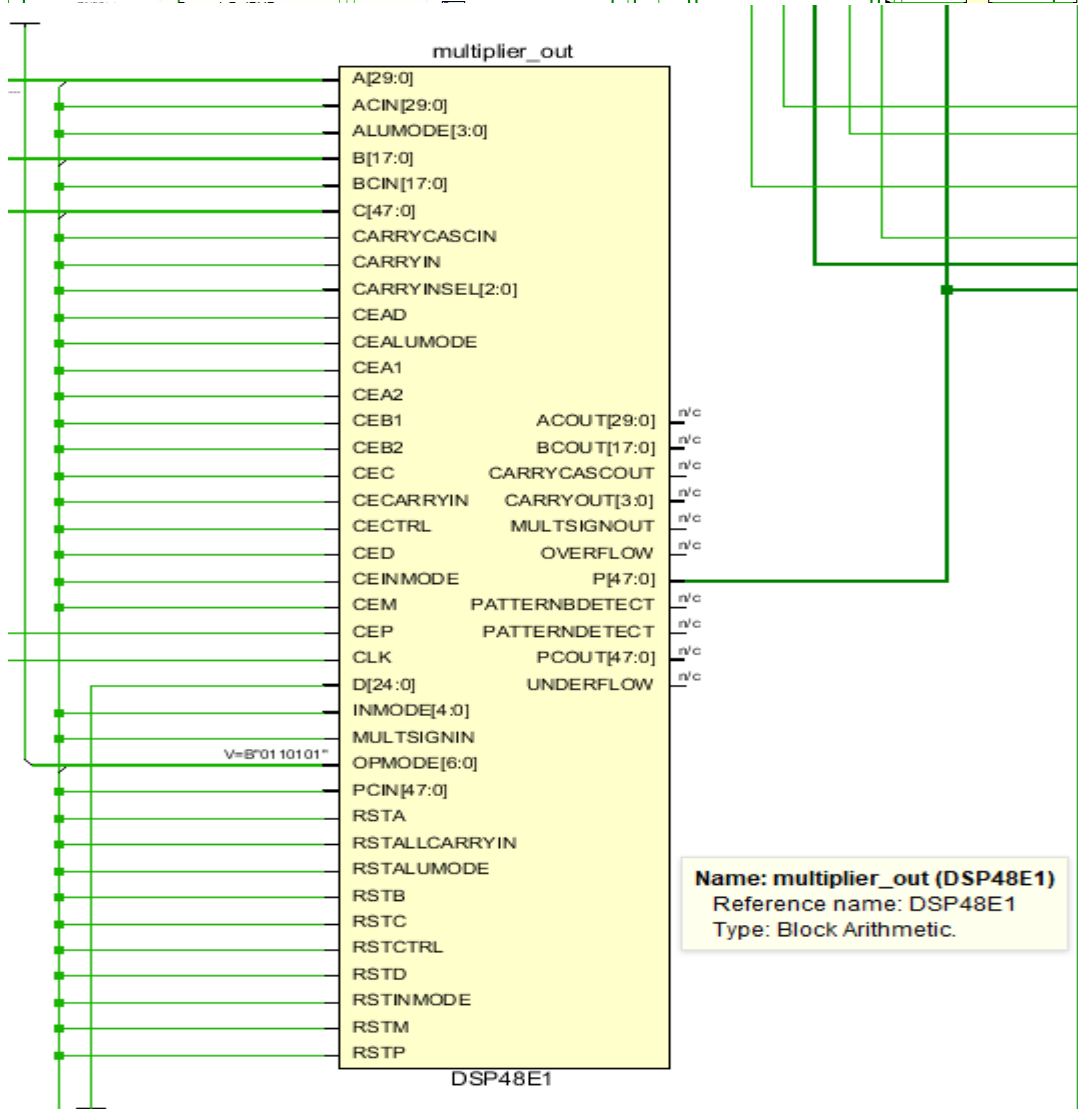
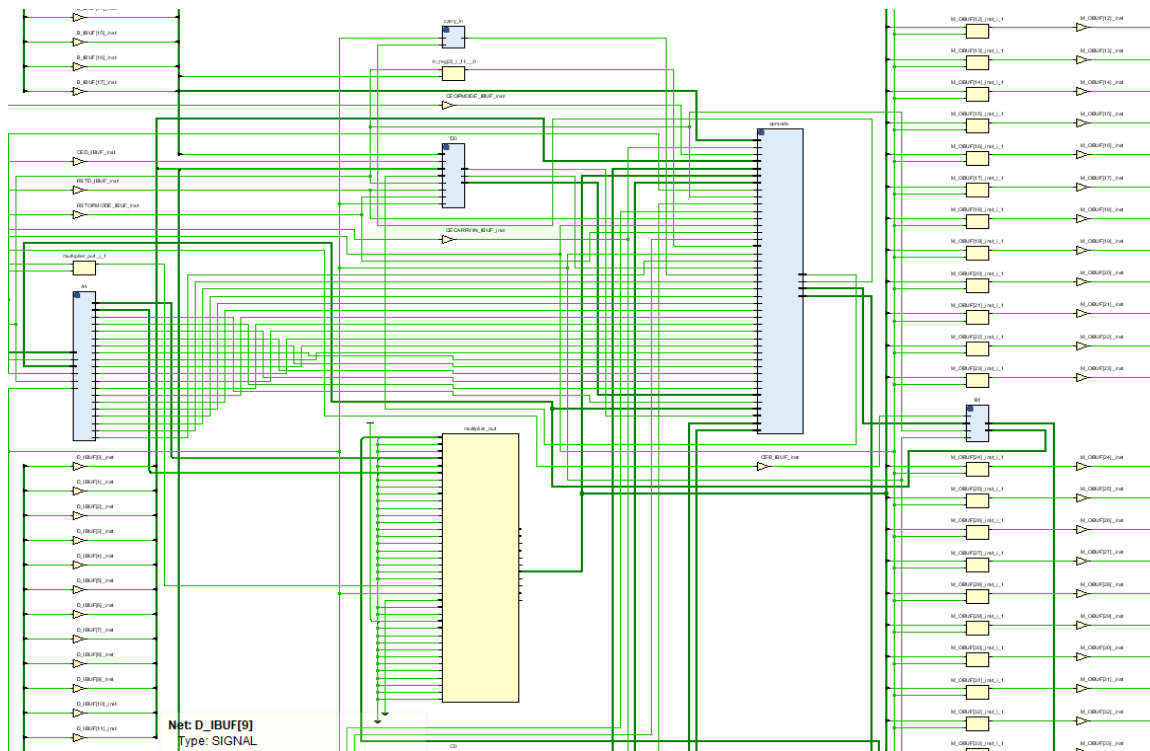
The messages are grouped into folders: Vivado Commands (3 infos), General Messages (3 infos), and Synthesis (147 warnings, 133 infos). The Synthesis folder is expanded, showing a list of messages. The first message in the Synthesis folder is a warning: [Synth 8-6014] Unused sequential element in_reg_reg was removed. [reg_mux.v:23]. This message is highlighted with a yellow background. Below this message, there is a link to the source file: [reg_mux.v:23].

Other messages in the Synthesis folder include:

- [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
- [Synth 8-2490] overwriting previous definition of module DSP48A1 [Spartan6-DSP48A1.v:2]
- [Synth 8-6157] synthesizing module 'DSP48A1' [Spartan6-DSP48A1.v:2] (6 more like this)
- [Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [reg_mux.v:2] (6 more like this)
- [Synth 8-5788] Register in_reg_reg in module reg_mux is has both Set and reset with same priority. This may cause simulation mismatches. Consider rewriting code [reg_mux.v:23] (4 more like this)
- [Synth 8-3331] design reg_mux_parameterized0 has unconnected port clk_enable (38 more like this)
- [Device 21-403] Loading part xc7a200tfg1156-3
- [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Personal Courses/Kareem_Waseem_Diploma/projects/Spartan/Constraint_File/Spartan6.xdc]. These constraints are listed in the file [Xilinx/DSP48A1_prop1mpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GU
- [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [Spartan6-DSP48A1.v:58] (1 more like this)
- [Synth 8-3333] propagating constant 0 across sequential element (opmode/out_reg_reg[5]) (99 more like this)
- [Synth 8-3332] Sequential element (opmode/out_reg_reg[7]) is unused and will be removed from module DSP48A1. (99 more like this)
- [Common 17-14] Message 'Synth 8-3333' appears 100 times and further instances of the messages will be disabled. Use the Tcl command
- [Project 1-571] Translating synthesized netlist
- [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-570] Preparing netlist for logic optimization (1 more like this)
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)
- [Common 17-83] Releasing license: Synthesis

- Schematic:





● Utilization Report:

Tcl Console Messages Log Reports Design Runs Utilization x Debug						
Hierarchy						
Hierarchy						
Summary						
v Slice Logic						
v Slice LUTs (<1%)						
LUT as Logic (<1%)						
v Slice Registers (<1%)						
Register as Flip Flop (<1%)						
Memory						
v DSP						
v DSPs (<1%)						
DSP48E1 only						
v IO and GT Specific						
v Bonded IOB (65%)						
Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
▼ N DSP48A1	313	160	1	327	1	
A1 (reg_mux)	37	18	0	0	0	
B1 (reg_mux_0)	19	18	0	0	0	
C0 (reg_mux_param...	1	48	0	0	0	
carry_in (reg_mux_pa...	0	1	0	0	0	
carry_out (reg_mux_p...	2	1	0	0	0	
D0 (reg_mux_1)	3	18	0	0	0	
opmode (reg_mux_p...	207	8	0	0	0	
OUT (reg_mux_para...	25	48	0	0	0	

● Timing Report:

Tcl ConsoleMessagesLogReportsDesign RunsTiming x UtilizationDebug

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General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (326)

▼ Intra-Clock Paths

▼ sys_clk_pin

Setup 4.471 ns (10)

Hold 0.131 ns (10)

Pulse Width 4.500 ns (30)

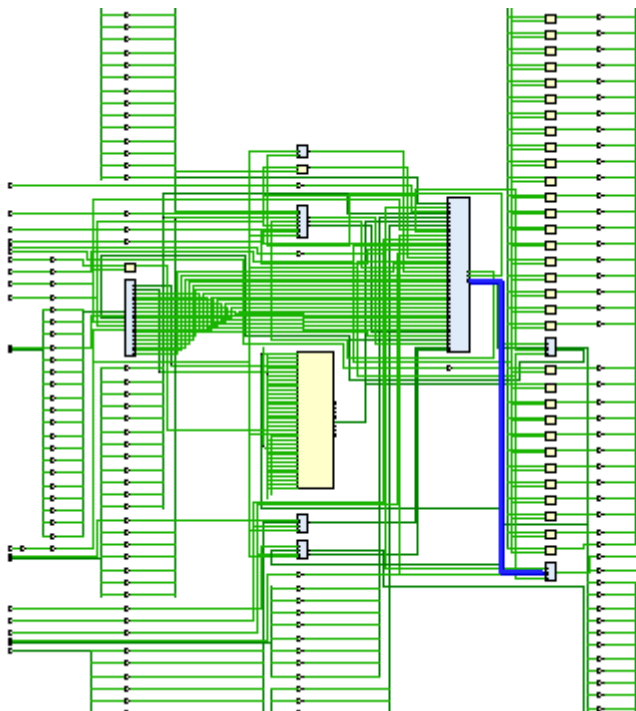
Timing Summary - timing_Spartan6

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.471 ns	Worst Hold Slack (WHS): 0.131 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 121	Total Number of Endpoints: 121	Total Number of Endpoints: 162

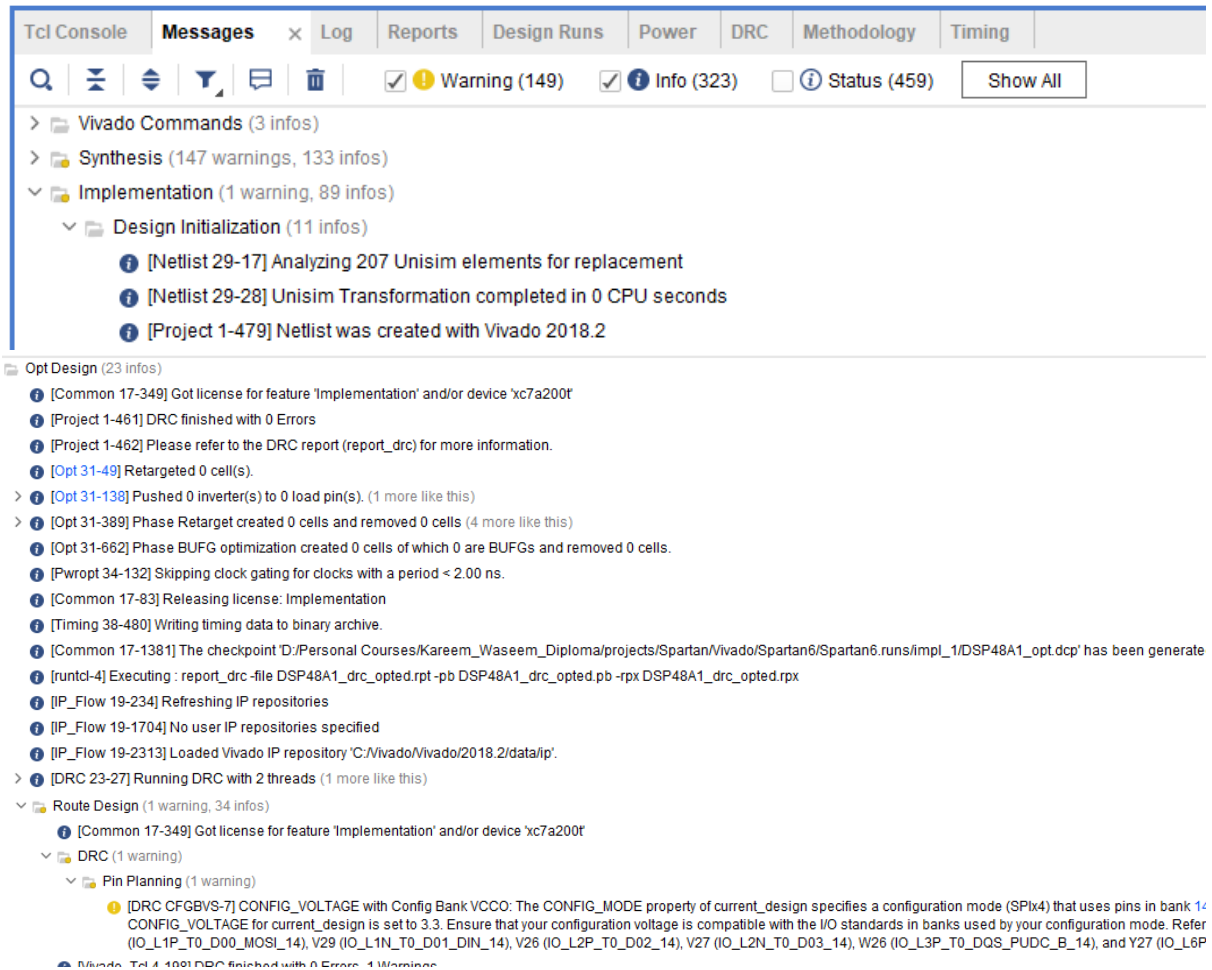
All user specified timing constraints are met.

Worst -ve slack:



Implementation:






• Messages:



The screenshot displays the Vivado Messages window with the following structure:










- Tab Bar:** Includes 'Tcl Console', 'Messages' (active), 'Log', 'Reports', 'Design Runs', 'Power', 'DRC', 'Methodology', and 'Timing'.
- Toolbar:** Contains icons for search, expand/collapse, filter, and a 'Show All' button. Summary counts are shown: Warning (149), Info (323), and Status (459).
- Message Tree:**
 - Vivado Commands (3 infos)
 - Synthesis (147 warnings, 133 infos)
 - Implementation (1 warning, 89 infos)
 - Design Initialization (11 infos)
 - [Netlist 29-17] Analyzing 207 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
- Opt Design (23 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - [Project 1-461] DRC finished with 0 Errors
 - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
 - [Opt 31-49] Retargeted 0 cell(s).
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
 - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
 - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-1381] The checkpoint 'D:/Personal Courses/Kareem_Waseem_Diploma/projects/Spartan/Vivado/Spartan6/Spartan6.runs/impl_1/DSP48A1_opt.dcp' has been generate
 - [runtcl-4] Executing : report_drc -file DSP48A1_drc_opted.rpt -pb DSP48A1_drc_opted.pb -rpx DSP48A1_drc_opted.rpx
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Vivado/Vivado/2018.2/data/ip'.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
- Route Design (1 warning, 34 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
 - DRC (1 warning)
 - Pin Planning (1 warning)
 - [DRC CFGBVS-7] CONFIG_VOLTAGE with Config Bank VCCO: The CONFIG_MODE property of current_design specifies a configuration mode (SP1x4) that uses pins in bank 14. CONFIG_VOLTAGE for current_design is set to 3.3. Ensure that your configuration voltage is compatible with the I/O standards in banks used by your configuration mode. Refer (IO_L1P_T0_D00_MOSI_14), V29 (IO_L1N_T0_D01_DIN_14), V26 (IO_L2P_T0_D02_14), V27 (IO_L2N_T0_D03_14), W26 (IO_L3P_T0_DQS_PUDC_B_14), and Y27 (IO_L6P

Place Design (21 infos)

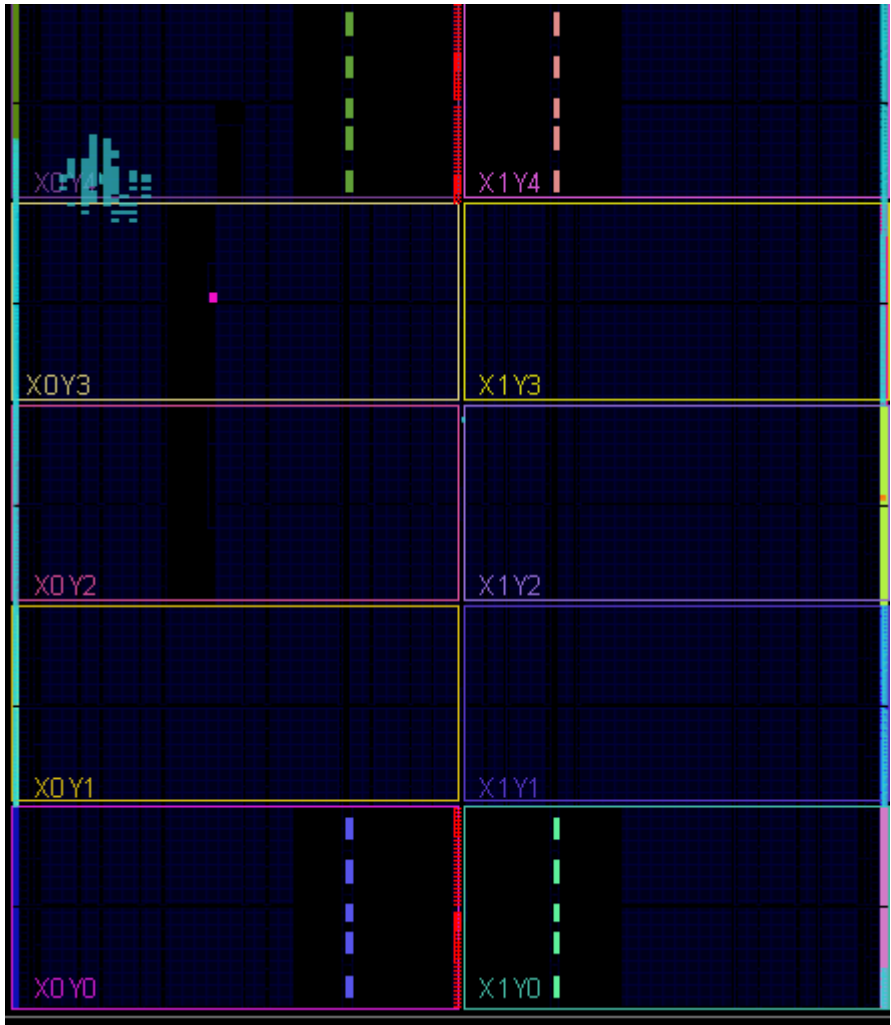
-  [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
- >  [DRC 23-27] Running DRC with 2 threads (1 more like this)
- >  [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
- >  [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 -  [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 -  [Physopt 32-65] No nets found for high-fanout optimization.
 -  [Physopt 32-232] Optimized 0 net. Created 0 new instance.
 -  [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- >  [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 -  [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
 -  [Place 30-746] Post Placement Timing Summary WNS=4.061. For the most accurate timing information please run report_timing.
 -  [Common 17-83] Releasing license: Implementation
 -  [Timing 38-480] Writing timing data to binary archive.
 -  [Common 17-1381] The checkpoint 'D:/Personal Courses/Kareem_Waseem_Diploma/projects/Spartan/Vivado/Spartan6/Spartan6.runs/impl_1/DSP48A1_plac
- >  [runtcl-4] Executing : report_io -file DSP48A1_io_placed.rpt (2 more like this)

Implemented Design (9 infos)

General Messages (9 infos)

-  [Netlist 29-17] Analyzing 207 Unisim elements for replacement
-  [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
-  [Project 1-479] Netlist was created with Vivado 2018.2
-  [Project 1-570] Preparing netlist for logic optimization
-  [Timing 38-478] Restoring timing data from binary archive.
-  [Timing 38-479] Binary timing data restore complete.
-  [Project 1-856] Restoring constraints from binary archive.
-  [Project 1-853] Binary constraint restore complete.
-  [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

● Schematic:



● Utilization Report:

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization x									
Hierarchy									
Hierarchy									
Summary									
▼ Slice Logic									
▼ Slice LUTs (<1%)									
LUT as Logic (<1%)									
▼ Slice Registers (<1%)									
Register as Flip Flop (<1%)									
▼ Slice Logic Distribution									
▼ Slice (1%)									
SLICEM									
SLICEL									
▼ LUT Flip Flop Pairs (<1%)									
LUT-FF pairs with one unused LU									
LUT-FF pairs with one unused Fli									
Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	
▼ DSP48A1	303	160	115	303	68	1	327	1	
A1 (reg_mux)	33	18	21	33	0	0	0	0	
B1 (reg_mux_0)	19	18	18	19	0	0	0	0	
C0 (reg_mux_param...	1	48	20	1	0	0	0	0	
carry_in (reg_mux_pa...	0	1	1	0	0	0	0	0	
carry_out (reg_mux_p...	2	1	2	2	0	0	0	0	
D0 (reg_mux_1)	3	18	7	3	0	0	0	0	
opmode (reg_mux_p...	207	8	76	207	0	0	0	0	
OUT (reg_mux_para...	25	48	27	25	0	0	0	0	

● **Timing Report:**

Tcl Console

Messages

Log

Reports

Design Runs

Power

DRC

Methodology

Timing

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Utilization

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Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

> Check Timing (326)

> Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

> Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 4.176 ns	Worst Hold Slack (WHS): 0.112 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 121	Total Number of Endpoints: 121	Total Number of Endpoints: 162

All user specified timing constraints are met.