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Spartan 6-DSP48A1

Introduction to DSP Blocks in FPGAs

Digital Signal Processing (DSP) Blocks are specialized hardware components within Field-Programmable Gate Arrays (FPGAs) designed to efficiently perform complex mathematical operations required in digital signal processing tasks. These blocks are crucial for applications that involve real-time processing of signals, such as audio and video processing, communications, and control systems.

Key Functions of DSP Blocks

1. **Multiplication and Accumulation:**
   - DSP blocks are optimized for performing multiply-accumulate operations, which are fundamental to many DSP algorithms. These operations can be executed in a single clock cycle, significantly speeding up processing times compared to using general-purpose logic.
2. **Arithmetic Operations:**
   - Besides multiplication, DSP blocks can perform a variety of arithmetic operations such as addition, subtraction, and division. They are designed to handle these operations with high precision and efficiency.
3. **Filtering:**
   - In signal processing, filtering is a common operation used to remove unwanted components from a signal. DSP blocks can implement various types of filters (e.g., FIR, IIR) with high performance, which is essential for applications like audio signal processing and communication systems.
4. **Fourier Transform:**
   - DSP blocks can accelerate the computation of Fourier transforms, which are used to convert signals from the time domain to the frequency domain. This is particularly useful in applications such as spectral analysis and modulation/demodulation in communications.
5. **Signal Modulation and Demodulation:**
   - These blocks are capable of handling complex modulation and demodulation schemes, which are critical in modern digital communication systems.
6. **Data Compression and Decompression:**
   - DSP blocks can be used to implement algorithms for data compression and decompression, which are vital for efficient storage and transmission of data.

Advantages of Using DSP Blocks in FPGAs

- **High Performance:**
  - DSP blocks provide high-speed processing capabilities, enabling real-time signal processing.
- **Resource Efficiency:**
  - They offload computationally intensive tasks from the general-purpose logic, freeing up FPGA resources for other functions.
- **Flexibility:**
  - The configurability of FPGAs allows designers to tailor DSP blocks to specific applications, achieving optimal performance for diverse tasks.

- **Parallelism:**
  - Multiple DSP blocks can operate in parallel, offering significant advantages in terms of processing throughput for large-scale signal processing tasks.

Spartan-6 DSP48A1 Block

The **Spartan-6** family of FPGAs from Xilinx includes the **DSP48A1** block, a versatile and powerful DSP slice designed to deliver high-performance digital signal processing capabilities. The DSP48A1 block supports the following features:

- **25 x 18-bit two's complement multiplication**
- **48-bit addition/subtraction**
- **Dedicated cascaded routing for efficient pipelining**
- **Pre-adder functionality for symmetric FIR filter implementations**

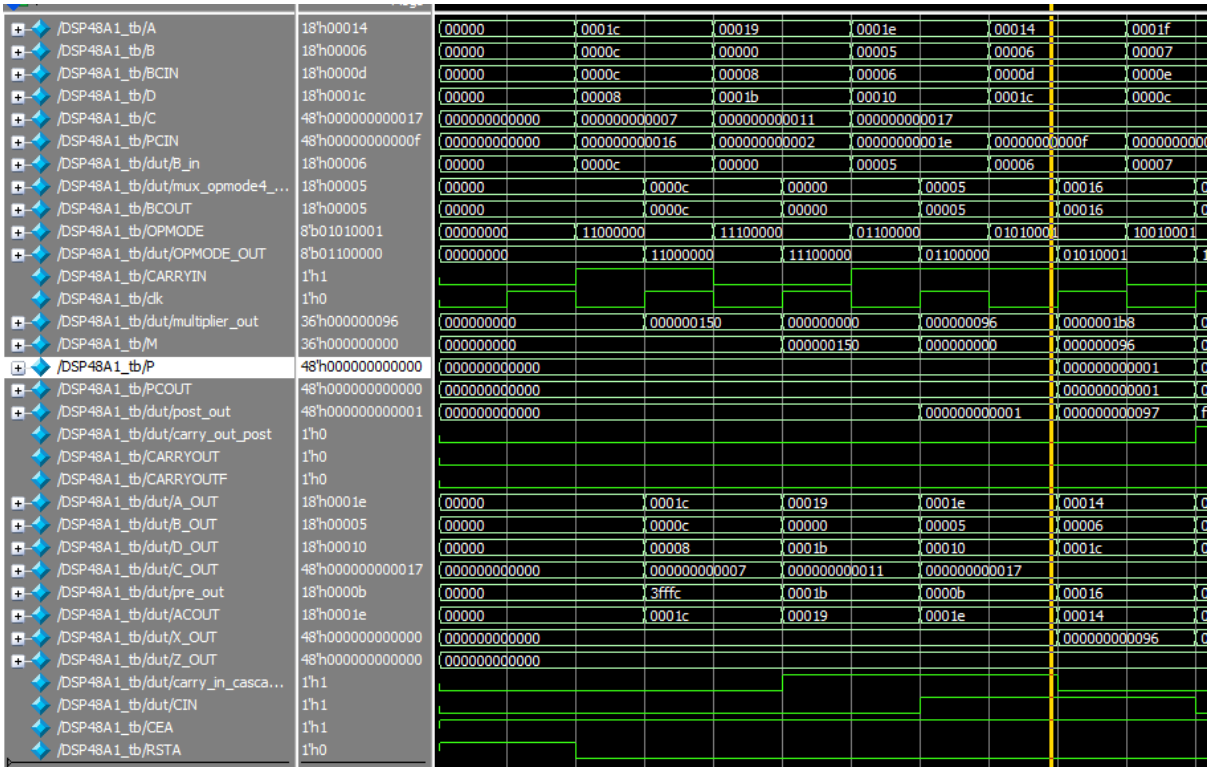
The DSP48A1 block is an essential component for implementing high-speed digital signal processing algorithms in Spartan-6 FPGAs, providing the necessary hardware acceleration for applications requiring intensive mathematical computations.

QuestaSim Snippets:

Before beginning I want to clarify some notes:

- I divided the test bench to 7 cases and as so will be the snippets, the divided cases were explained well in the test bench code above
- I removed all the resets and clock enables from the snippets except for (RSTA , CEA) that all the other resets are the same as RSTA and all other clock enables are the same as CEA, and I've done that so by that the snippets will be more detectable
- I arranged the signals in an order that the more related signals are above or below each other to give more readability
- In each case I might take some of the following case as the output is showed after a one positive edge from changing the opmode_out
- Focus on the signals has (_out) in it's name
- Happy tracing!

- **Case 1 :**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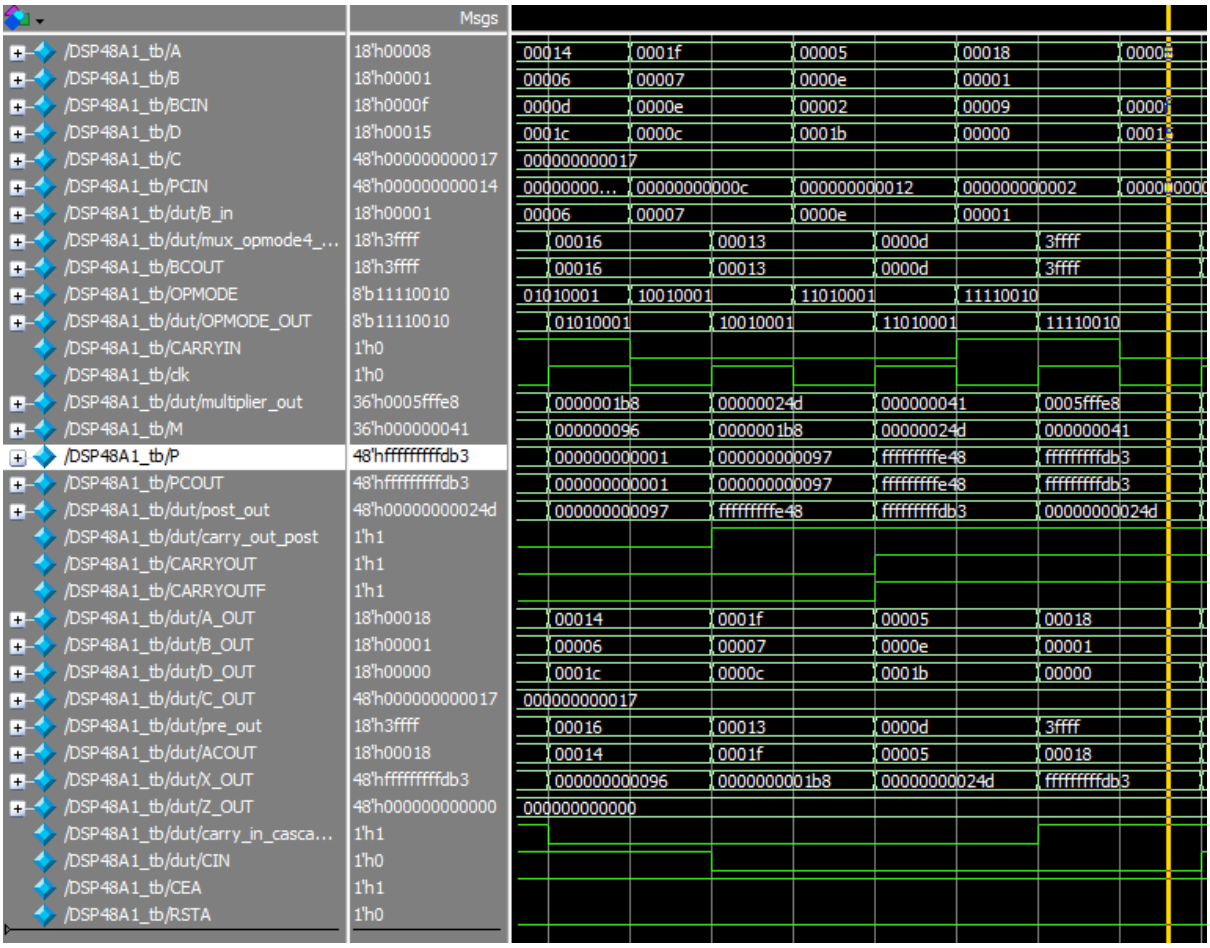
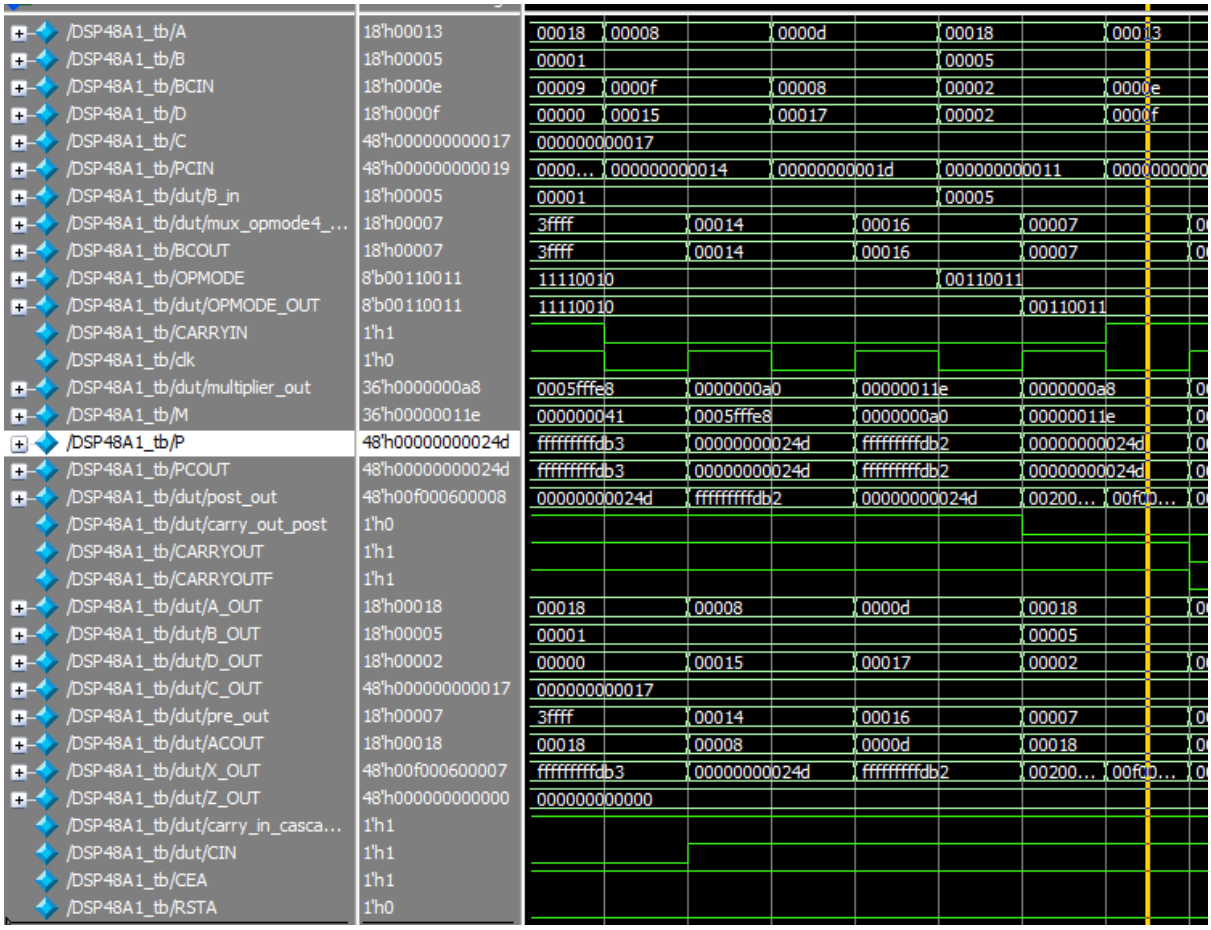
/DSP48A1_tb/B 18'h00006
/DSP48A1_tb/BCIN 18'h0000d
/DSP48A1_tb/D 18'h0001c
/DSP48A1_tb/C 48'h000000000017
/DSP48A1_tb/PCIN 48'h00000000000f
/DSP48A1_tb/dut/B_in 18'h00006
/DSP48A1_tb/dut/mux_opmode4_... 18'h00005
/DSP48A1_tb/BCOUT 18'h00005
/DSP48A1_tb/OPMODE 8'b01010001
/DSP48A1_tb/dut/OPMODE_OUT 8'b01100000
/DSP48A1_tb/CARRYIN 1'h1
/DSP48A1_tb/clk 1'h0
/DSP48A1_tb/dut/multiplier_out 36'h000000096
/DSP48A1_tb/M 36'h000000000
/DSP48A1_tb/P 48'h000000000000
/DSP48A1_tb/PCOUT 48'h000000000000
/DSP48A1_tb/dut/post_out 48'h000000000001
/DSP48A1_tb/dut/carry_out_post 1'h0
/DSP48A1_tb/CARRYOUT 1'h0
/DSP48A1_tb/CARRYOUTF 1'h0
/DSP48A1_tb/dut/A_OUT 18'h0001e
/DSP48A1_tb/dut/B_OUT 18'h00005
/DSP48A1_tb/dut/D_OUT 18'h00010
/DSP48A1_tb/dut/C_OUT 48'h000000000017
/DSP48A1_tb/dut/pre_out 18'h0000b
/DSP48A1_tb/dut/ACOUT 18'h0001e
/DSP48A1_tb/dut/X_OUT 48'h000000000000
/DSP48A1_tb/dut/Z_OUT 48'h000000000000
/DSP48A1_tb/dut/carry_in_casca... 1'h1
/DSP48A1_tb/dut/CIN 1'h1
/DSP48A1_tb/CEA 1'h1
/DSP48A1_tb/RSTA 1'h0

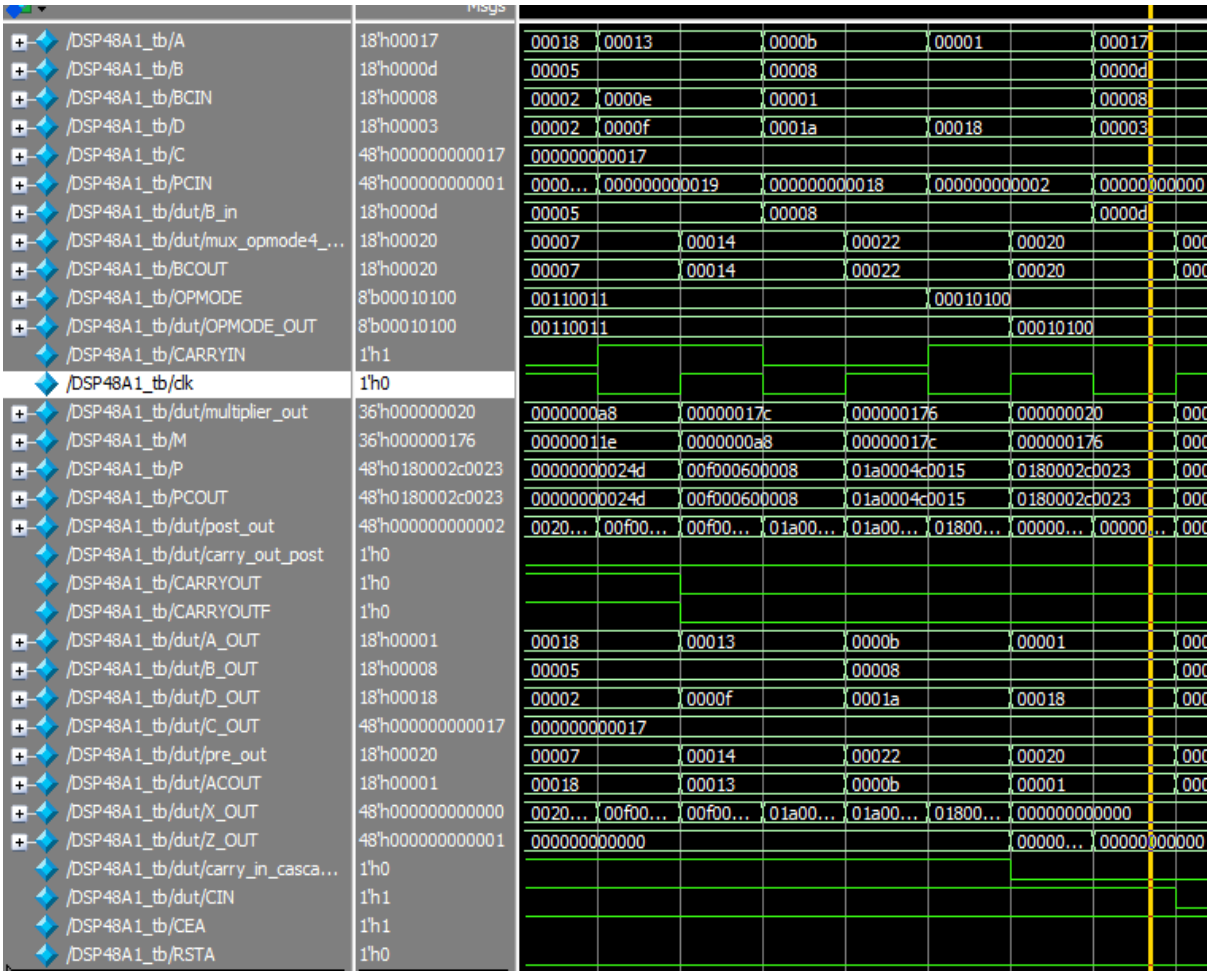
- **Case 2 :**


Msgs
/DSP48A1_tb/A
/DSP48A1_tb/B
/DSP48A1_tb/BCIN
/DSP48A1_tb/D
/DSP48A1_tb/C
/DSP48A1_tb/PCIN
/DSP48A1_tb/dut/B_in
/DSP48A1_tb/dut/mux_opmode4_...
/DSP48A1_tb/BCOUT
/DSP48A1_tb/OPMODE
/DSP48A1_tb/dut/OPMODE_OUT
/DSP48A1_tb/CARRYIN
/DSP48A1_tb/clk
/DSP48A1_tb/dut/multiplier_out
/DSP48A1_tb/M
/DSP48A1_tb/P
/DSP48A1_tb/PCOUT
/DSP48A1_tb/dut/post_out
/DSP48A1_tb/dut/carry_out_post
/DSP48A1_tb/CARRYOUT
/DSP48A1_tb/CARRYOUTF
/DSP48A1_tb/dut/A_OUT
/DSP48A1_tb/dut/B_OUT
/DSP48A1_tb/dut/D_OUT
/DSP48A1_tb/dut/C_OUT
/DSP48A1_tb/dut/pre_out
/DSP48A1_tb/dut/ACOUT
/DSP48A1_tb/dut/X_OUT
/DSP48A1_tb/dut/Z_OUT
/DSP48A1_tb/dut/carry_in_casca...
/DSP48A1_tb/dut/CIN
/DSP48A1_tb/CEA
/DSP48A1_tb/RSTA
18'h00008
18'h00001
18'h0000f
18'h00015
48'h000000000017
48'h000000000014
18'h00001
18'h3ffff
18'h3ffff
8'b11110010
8'b11110010
1'h0
1'h0
36'h0005fffe8
36'h000000041
48'hffffffffdb3
48'hffffffffdb3
48'h00000000024d
1'h1
1'h1
1'h1
18'h00018
18'h00001
18'h00000
48'h000000000017
18'h3ffff
18'h00018
48'hffffffffdb3
48'h000000000000
1'h1
1'h0
1'h1
1'h0

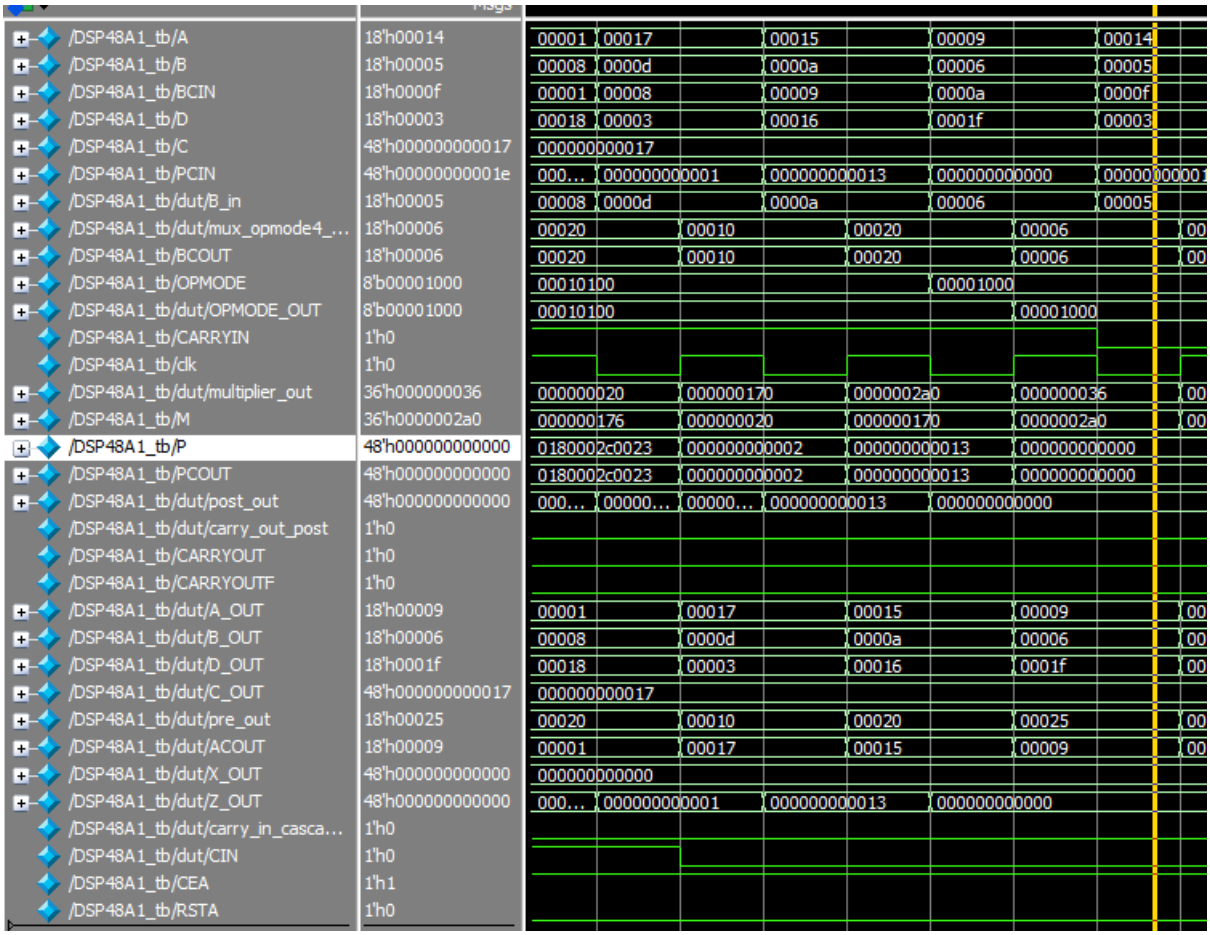
- **Case 3 :**


/DSP48A1_tb/A 18'h00013
/DSP48A1_tb/B 18'h00005
/DSP48A1_tb/BCIN 18'h0000e
/DSP48A1_tb/D 18'h0000f
/DSP48A1_tb/C 48'h000000000017
/DSP48A1_tb/PCIN 48'h000000000019
/DSP48A1_tb/dut/B_in 18'h00005
/DSP48A1_tb/dut/mux_opmode4_... 18'h00007
/DSP48A1_tb/BCOUT 18'h00007
/DSP48A1_tb/OPMODE 8'b00110011
/DSP48A1_tb/dut/OPMODE_OUT 8'b00110011
/DSP48A1_tb/CARRYIN 1'h1
/DSP48A1_tb/clk 1'h0
/DSP48A1_tb/dut/multiplier_out 36'h0000000a8
/DSP48A1_tb/M 36'h00000011e
/DSP48A1_tb/P 48'h00000000024d
/DSP48A1_tb/PCOUT 48'h00000000024d
/DSP48A1_tb/dut/post_out 48'h00f000600008
/DSP48A1_tb/dut/carry_out_post 1'h0
/DSP48A1_tb/CARRYOUT 1'h1
/DSP48A1_tb/CARRYOUTF 1'h1
/DSP48A1_tb/dut/A_OUT 18'h00018
/DSP48A1_tb/dut/B_OUT 18'h00005
/DSP48A1_tb/dut/D_OUT 18'h00002
/DSP48A1_tb/dut/C_OUT 48'h000000000017
/DSP48A1_tb/dut/pre_out 18'h00007
/DSP48A1_tb/dut/ACOUT 18'h00018
/DSP48A1_tb/dut/X_OUT 48'h00f000600007
/DSP48A1_tb/dut/Z_OUT 48'h000000000000
/DSP48A1_tb/dut/carry_in_casca... 1'h1
/DSP48A1_tb/dut/CIN 1'h1
/DSP48A1_tb/CEA 1'h1
/DSP48A1_tb/RSTA 1'h0

- **Case 4 :**


/DSP48A1_tb/A
/DSP48A1_tb/B
/DSP48A1_tb/BCIN
/DSP48A1_tb/D
/DSP48A1_tb/C
/DSP48A1_tb/PCIN
/DSP48A1_tb/dut/B_in
/DSP48A1_tb/dut/mux_opmode4_...
/DSP48A1_tb/BCOUT
/DSP48A1_tb/OPMODE
/DSP48A1_tb/dut/OPMODE_OUT
/DSP48A1_tb/CARRYIN
/DSP48A1_tb/clk
/DSP48A1_tb/dut/multiplier_out
/DSP48A1_tb/M
/DSP48A1_tb/P
/DSP48A1_tb/PCOUT
/DSP48A1_tb/dut/post_out
/DSP48A1_tb/dut/carry_out_post
/DSP48A1_tb/CARRYOUT
/DSP48A1_tb/CARRYOUTF
/DSP48A1_tb/dut/A_OUT
/DSP48A1_tb/dut/B_OUT
/DSP48A1_tb/dut/D_OUT
/DSP48A1_tb/dut/C_OUT
/DSP48A1_tb/dut/pre_out
/DSP48A1_tb/dut/ACOUT
/DSP48A1_tb/dut/X_OUT
/DSP48A1_tb/dut/Z_OUT
/DSP48A1_tb/dut/carry_in_casca...
/DSP48A1_tb/dut/CIN
/DSP48A1_tb/CEA
/DSP48A1_tb/RSTA

- **Case 5 :**


/DSP48A1_tb/A 18'h00014
/DSP48A1_tb/B 18'h00005
/DSP48A1_tb/BCIN 18'h0000f
/DSP48A1_tb/D 18'h00003
/DSP48A1_tb/C 48'h000000000017
/DSP48A1_tb/PCIN 48'h00000000001e
/DSP48A1_tb/dut/B_in 18'h00005
/DSP48A1_tb/dut/mux_opmode4_... 18'h00006
/DSP48A1_tb/BCOUT 18'h00006
/DSP48A1_tb/OPMODE 8'b00001000
/DSP48A1_tb/dut/OPMODE_OUT 8'b00001000
/DSP48A1_tb/CARRYIN 1'h0
/DSP48A1_tb/clk 1'h0
/DSP48A1_tb/dut/multiplier_out 36'h000000036
/DSP48A1_tb/M 36'h0000002a0
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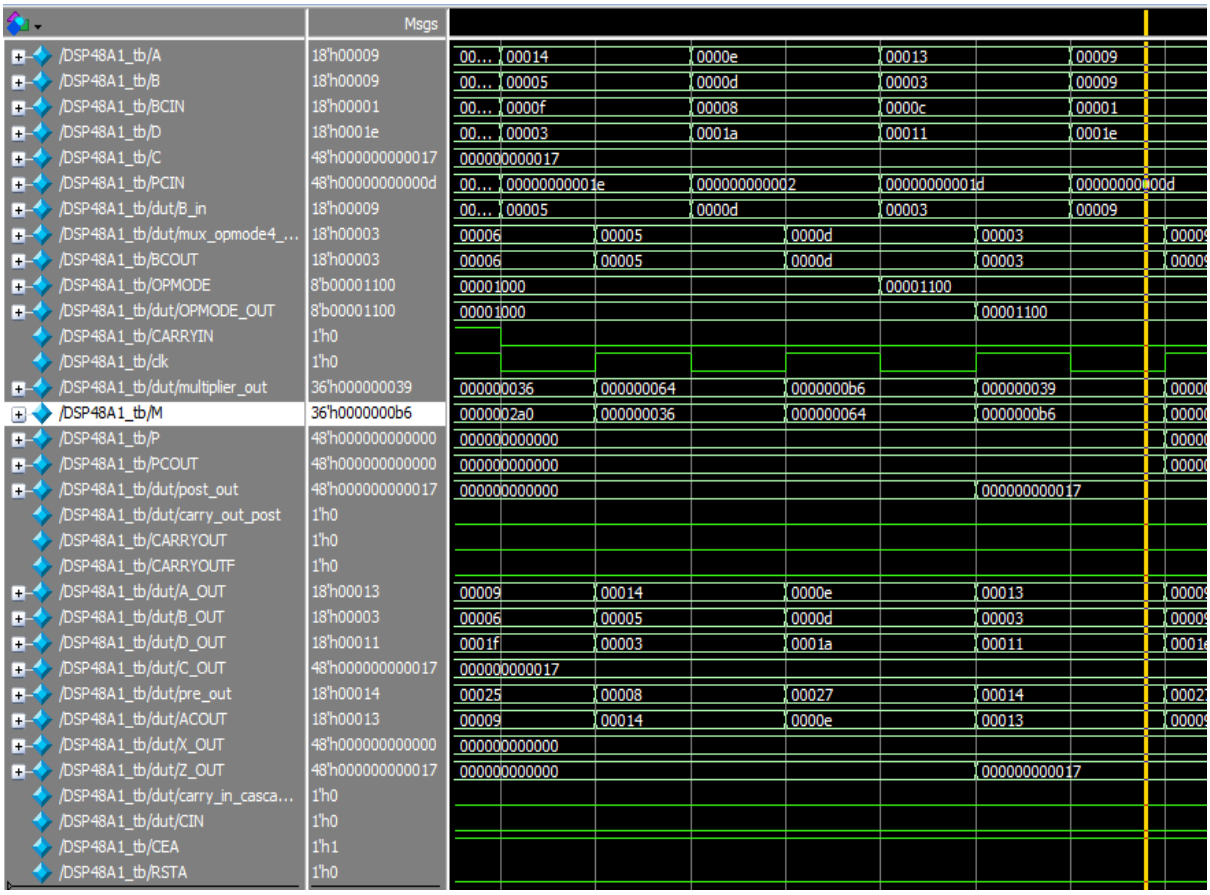
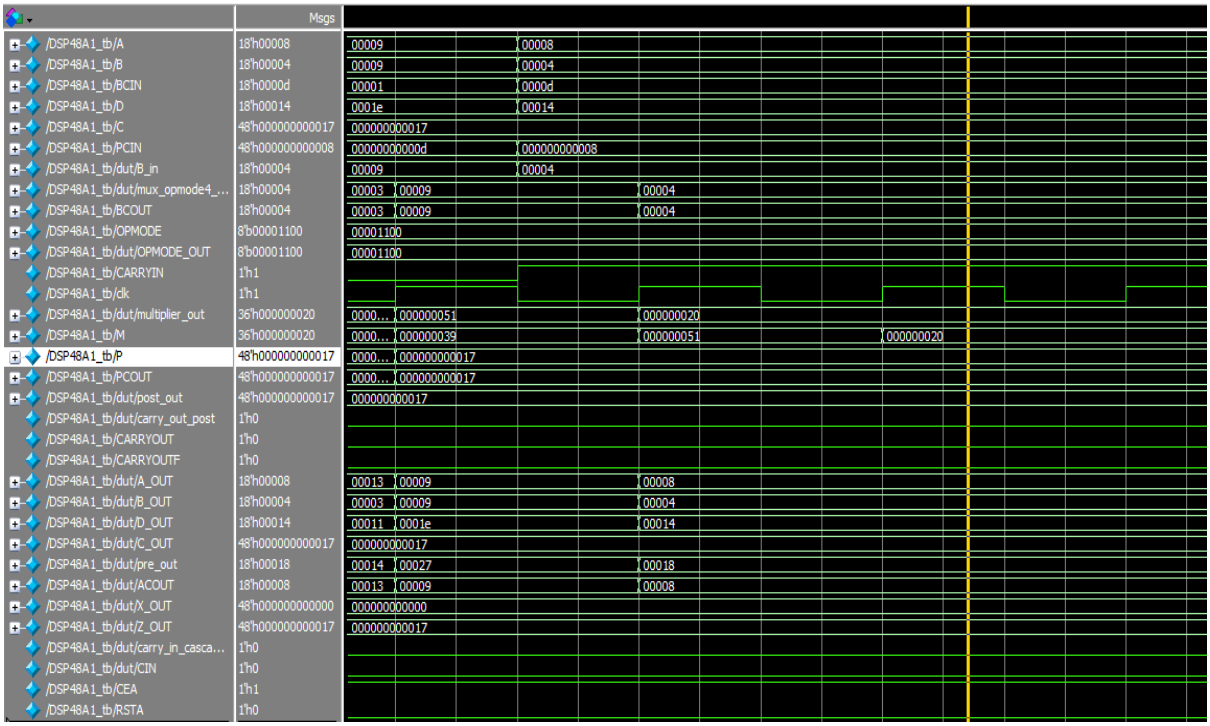
/DSP48A1_tb/PCOUT 48'h000000000000
/DSP48A1_tb/dut/post_out 48'h000000000000
/DSP48A1_tb/dut/carry_out_post 1'h0
/DSP48A1_tb/CARRYOUT 1'h0
/DSP48A1_tb/CARRYOUTF 1'h0
/DSP48A1_tb/dut/A_OUT 18'h00009
/DSP48A1_tb/dut/B_OUT 18'h00006
/DSP48A1_tb/dut/D_OUT 18'h0001f
/DSP48A1_tb/dut/C_OUT 48'h000000000017
/DSP48A1_tb/dut/pre_out 18'h00025
/DSP48A1_tb/dut/ACOUT 18'h00009
/DSP48A1_tb/dut/X_OUT 48'h000000000000
/DSP48A1_tb/dut/Z_OUT 48'h000000000000
/DSP48A1_tb/dut/carry_in_casca... 1'h0
/DSP48A1_tb/dut/CIN 1'h0
/DSP48A1_tb/CEA 1'h1
/DSP48A1_tb/RSTA 1'h0

- **Case 6 :**

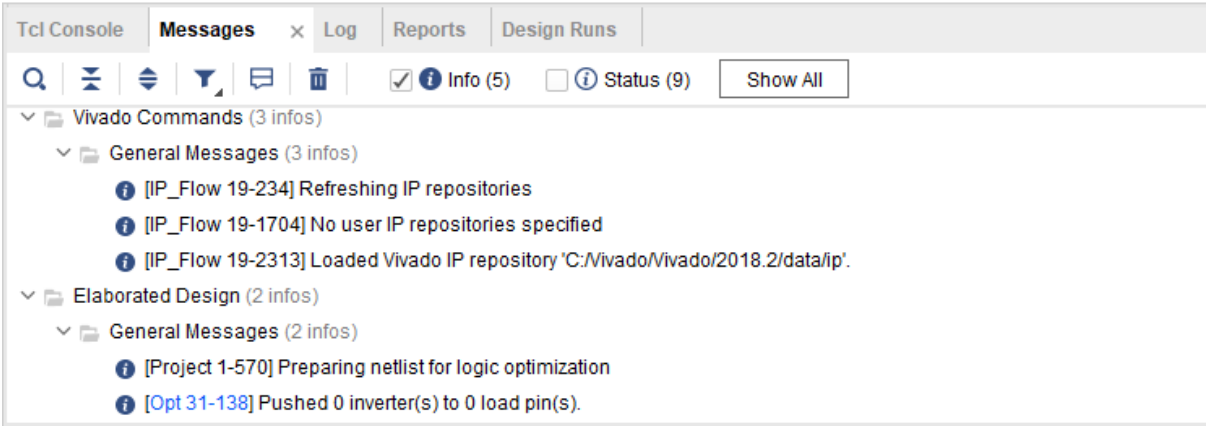

Msgs
/DSP48A1_tb/A
/DSP48A1_tb/B
/DSP48A1_tb/BCIN
/DSP48A1_tb/D
/DSP48A1_tb/C
/DSP48A1_tb/PCIN
/DSP48A1_tb/dut/B_in
/DSP48A1_tb/dut/mux_opmode4_...
/DSP48A1_tb/BCOUT
/DSP48A1_tb/OPMODE
/DSP48A1_tb/dut/OPMODE_OUT
/DSP48A1_tb/CARRYIN
/DSP48A1_tb/clk
/DSP48A1_tb/dut/multiplier_out
/DSP48A1_tb/M
/DSP48A1_tb/P
/DSP48A1_tb/PCOUT
/DSP48A1_tb/dut/post_out
/DSP48A1_tb/dut/carry_out_post
/DSP48A1_tb/CARRYOUT
/DSP48A1_tb/CARRYOUTF
/DSP48A1_tb/dut/A_OUT
/DSP48A1_tb/dut/B_OUT
/DSP48A1_tb/dut/D_OUT
/DSP48A1_tb/dut/C_OUT
/DSP48A1_tb/dut/pre_out
/DSP48A1_tb/dut/ACOUT
/DSP48A1_tb/dut/X_OUT
/DSP48A1_tb/dut/Z_OUT
/DSP48A1_tb/dut/carry_in_casca...
/DSP48A1_tb/dut/CIN
/DSP48A1_tb/CEA
/DSP48A1_tb/RSTA

- **Case 7 :**

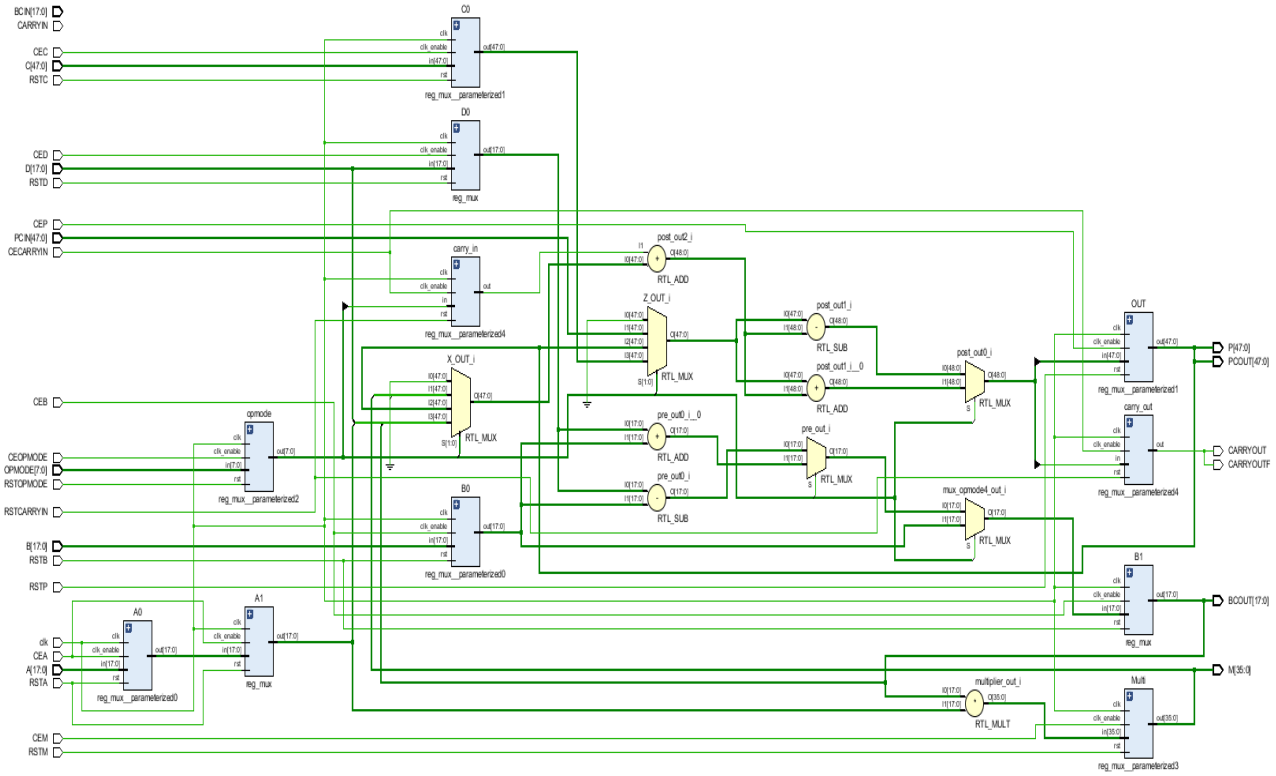

Msgs
/DSP48A1_tb/A
/DSP48A1_tb/B
/DSP48A1_tb/BCIN
/DSP48A1_tb/D
/DSP48A1_tb/C
/DSP48A1_tb/PCIN
/DSP48A1_tb/dut/B_in
/DSP48A1_tb/dut/mux_opmode4_...
/DSP48A1_tb/BCOUT
/DSP48A1_tb/OPMODE
/DSP48A1_tb/dut/OPMODE_OUT
/DSP48A1_tb/CARRYIN
/DSP48A1_tb/clk
/DSP48A1_tb/dut/multiplier_out
/DSP48A1_tb/M
/DSP48A1_tb/P
/DSP48A1_tb/PCOUT
/DSP48A1_tb/dut/post_out
/DSP48A1_tb/dut/carry_out_post
/DSP48A1_tb/CARRYOUT
/DSP48A1_tb/CARRYOUTF
/DSP48A1_tb/dut/A_OUT
/DSP48A1_tb/dut/B_OUT
/DSP48A1_tb/dut/D_OUT
/DSP48A1_tb/dut/C_OUT
/DSP48A1_tb/dut/pre_out
/DSP48A1_tb/dut/ACOUT
/DSP48A1_tb/dut/X_OUT
/DSP48A1_tb/dut/Z_OUT
/DSP48A1_tb/dut/carry_in_casca...
/DSP48A1_tb/dut/CIN
/DSP48A1_tb/CEA
/DSP48A1_tb/RSTA

Elaboration:

- ## Messages:

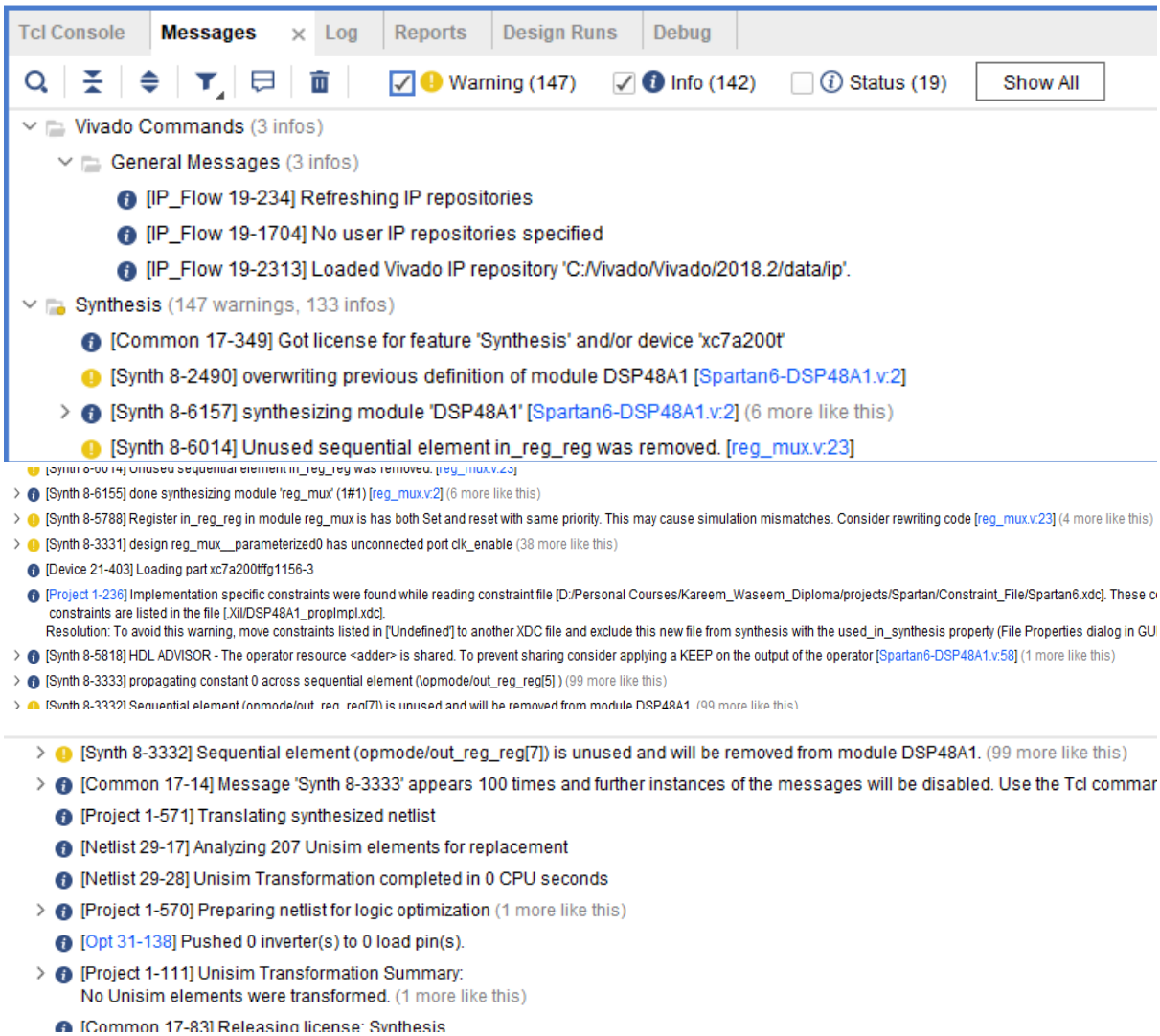


- ## Schematic:

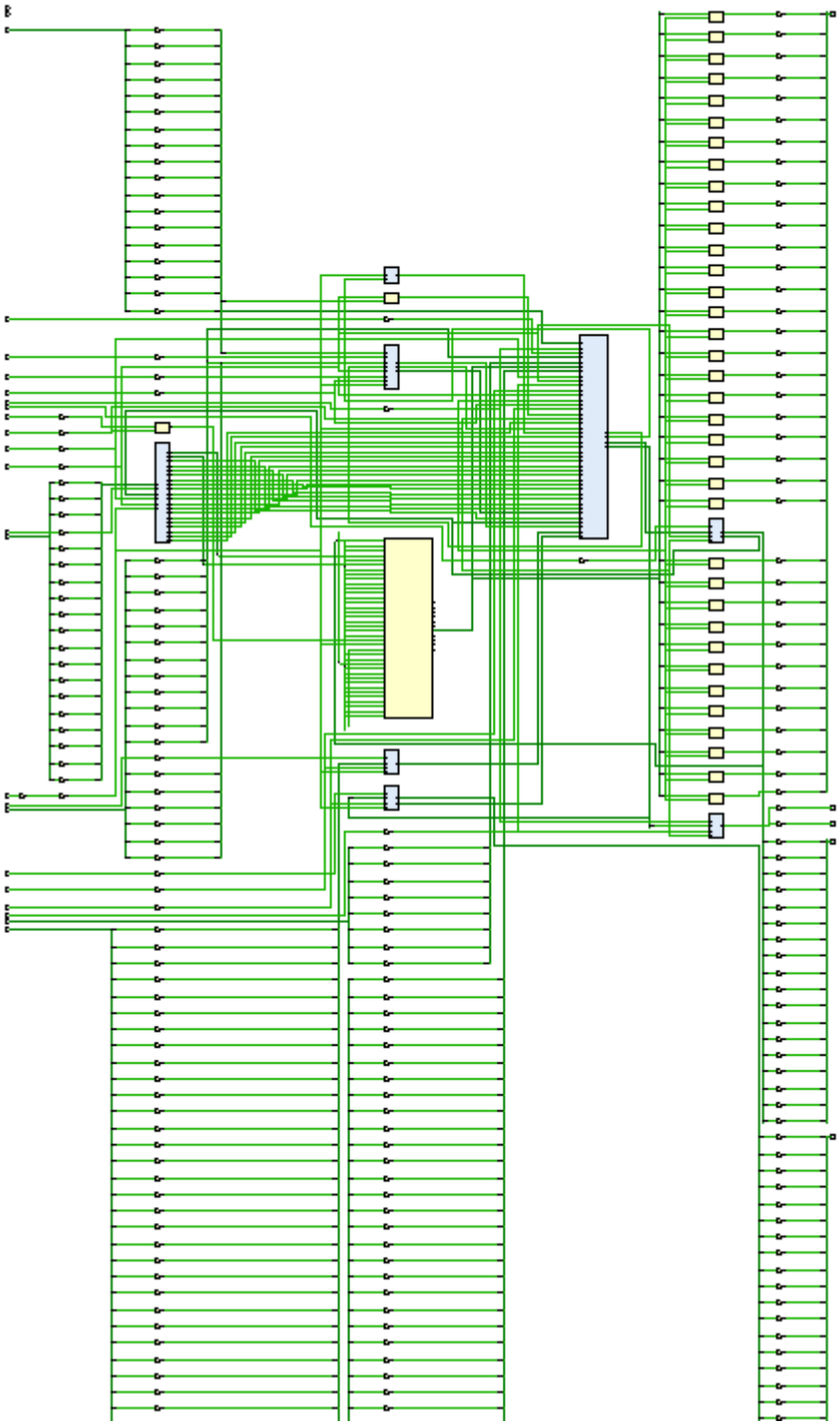


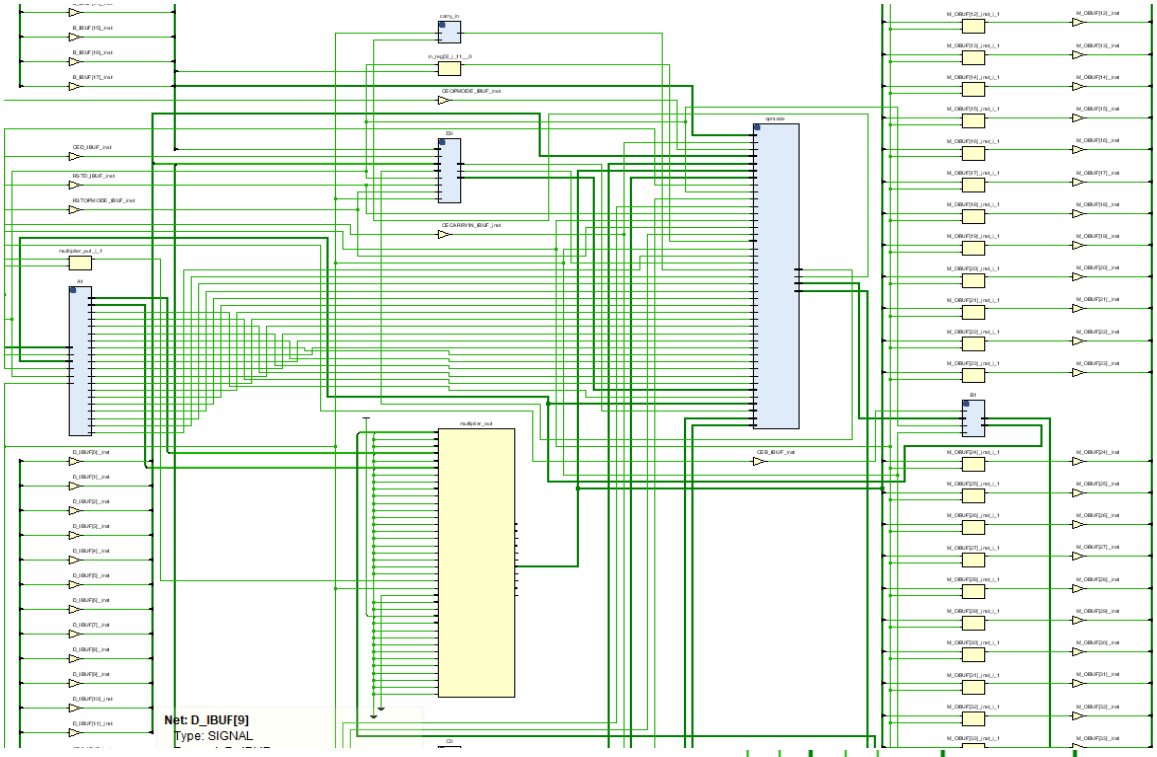
Synthesis:

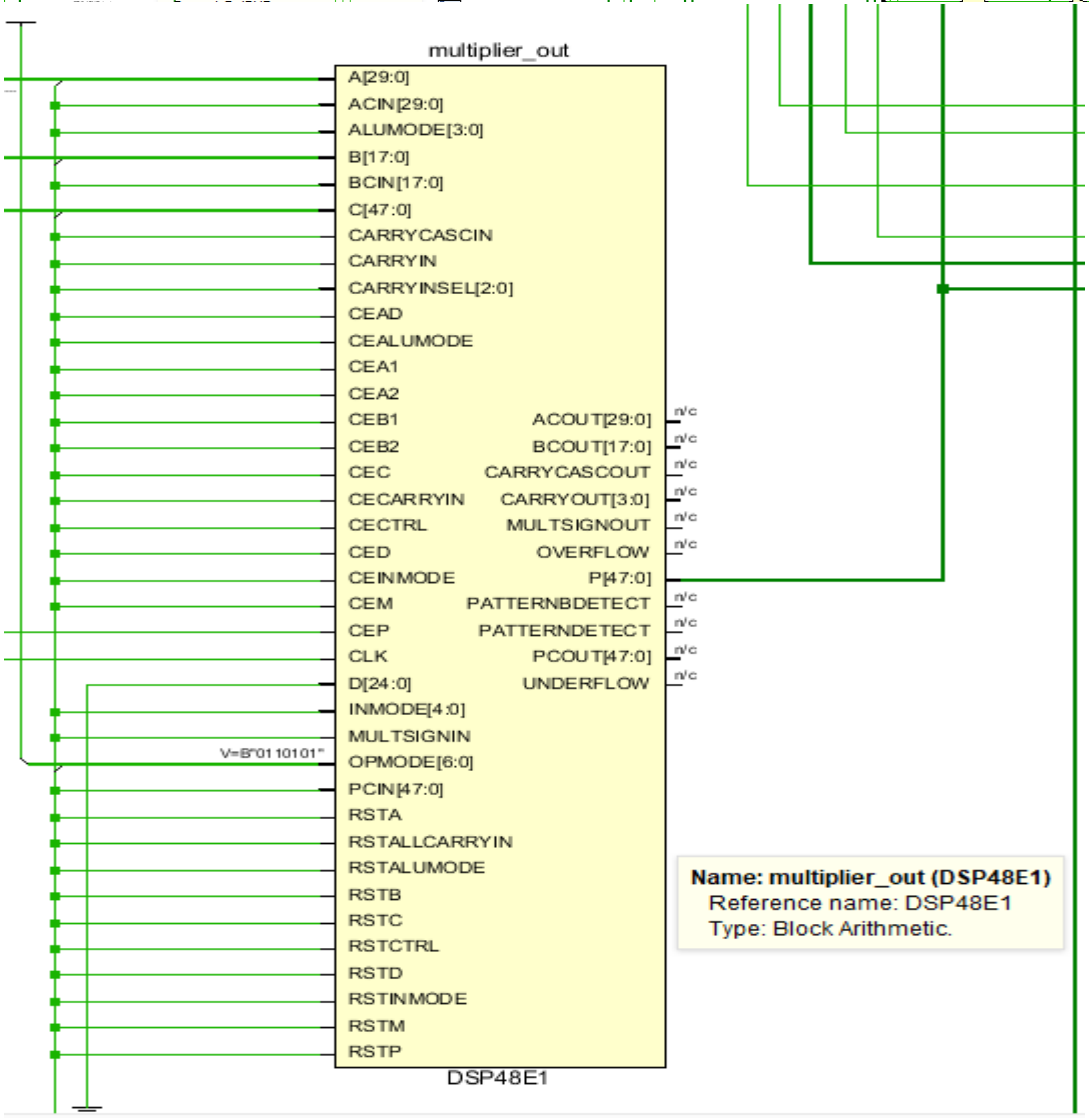
- **Messages:**



- **Schematic:**




Net: D_IBUF[9]
Type: SIGNAL


multiplier_out
A[29:0]
ACIN[29:0]
ALUMODE[3:0]
B[17:0]
BCIN[17:0]
C[47:0]
CARRYCASCIN
CARRYIN
CARRYINSEL[2:0]
CEAD
CEALUMODE
CEA1
CEA2
CEB1
CEB2
CEC
CECARRYIN
CECTRL
CED
CEINMODE
CEM
CEP
CLK
D[24:0]
INMODE[4:0]
MULTSIGNIN
V=B"0110101"
OPMODE[6:0]
PCIN[47:0]
RSTA
RSTALLCARRYIN
RSTALUMODE
RSTB
RSTC
RSTCTRL
RSTD
RSTINMODE
RSTM
RSTP
ACOUT[29:0]
BCOUT[17:0]
CARRYCASCOUT
CARRYOUT[3:0]
MULTSIGNOUT
OVERFLOW
P[47:0]
PATTERNBDETECT
PATTERNDETECT
PCOUT[47:0]
UNDERFLOW
n/c
DSP48E1
Name: multiplier_out (DSP48E1)
Reference name: DSP48E1
Type: Block Arithmetic.

- # Utilization Report:

Tcl Console | Messages | Log | Reports | Design Runs | Utilization | Debug

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<1%)
- Memory
- DSP
  - DSPs (<1%)
    - DSP48E1 only
- IO and GT Specific
  - Bonded IOB (65%)

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	313	160	1	327	1
A1 (reg_mux)	37	18	0	0	0
B1 (reg_mux_0)	19	18	0	0	0
C0 (reg_mux__param...	1	48	0	0	0
carry_in (reg_mux__pa...	0	1	0	0	0
carry_out (reg_mux__p...	2	1	0	0	0
D0 (reg_mux_1)	3	18	0	0	0
opmode (reg_mux__p...	207	8	0	0	0
OUT (reg_mux__para...	25	48	0	0	0

- # Timing Report:

Tcl Console | Messages | Log | Reports | Design Runs | Timing | Utilization | Debug

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (326)
- Intra-Clock Paths
  - sys_clk_pin
    - Setup 4.471 ns (10)
    - Hold 0.131 ns (10)
    - Pulse Width 4.500 ns (30)

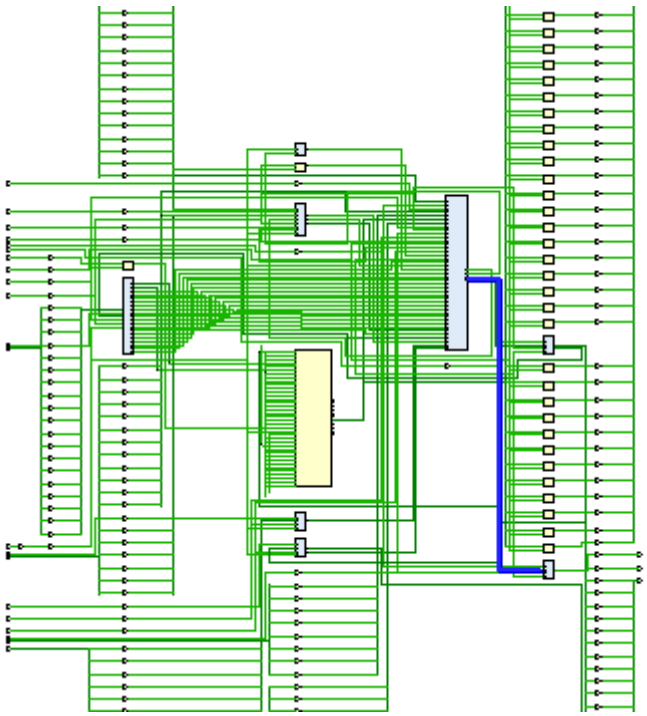
Timing Summary - timing_Spartan6

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.471 ns	Worst Hold Slack (WHS):	0.131 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	121	Total Number of Endpoints:	121	Total Number of Endpoints:	162

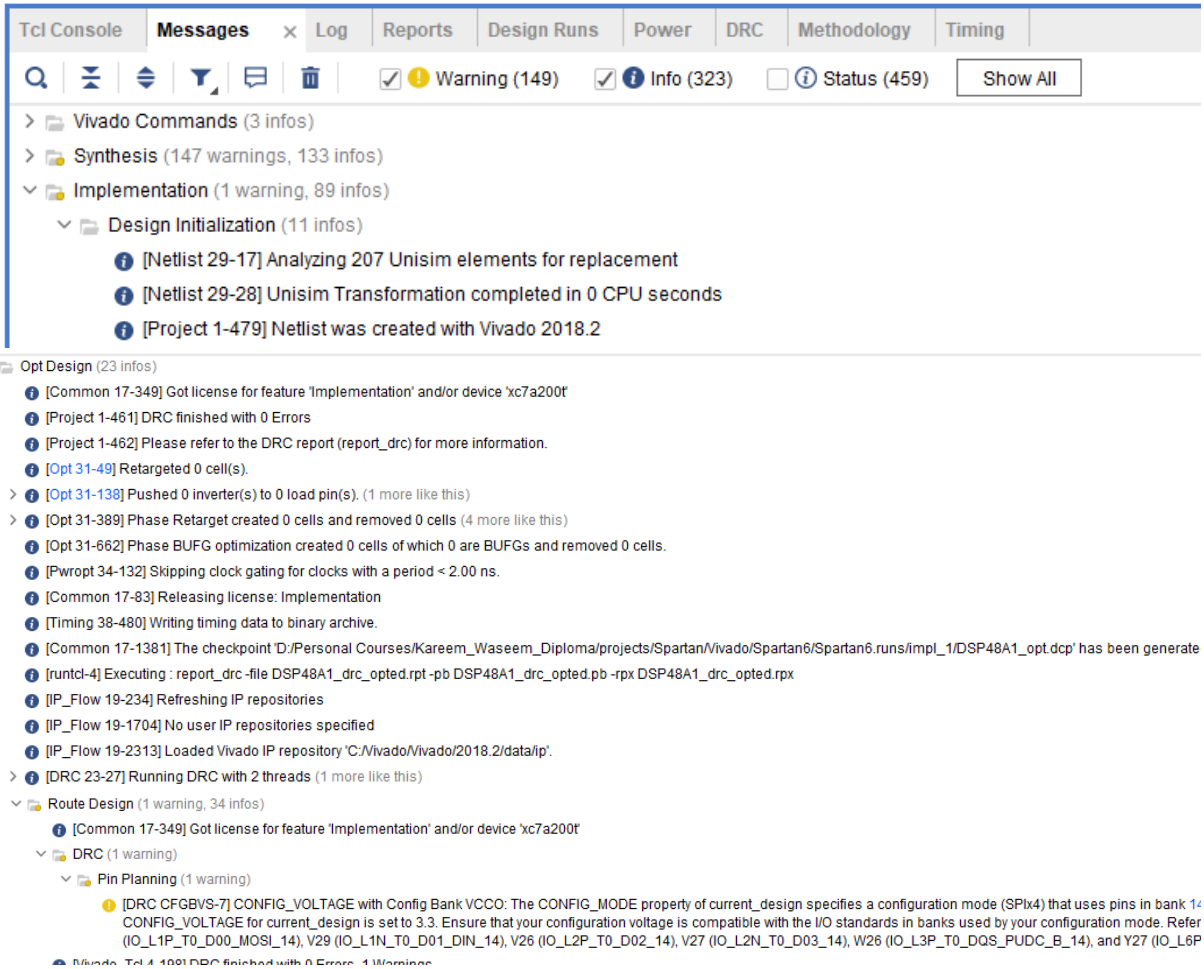
All user specified timing constraints are met.

Worst –ve slack:



Implementation:

- ## Messages:



Place Design (21 infos)

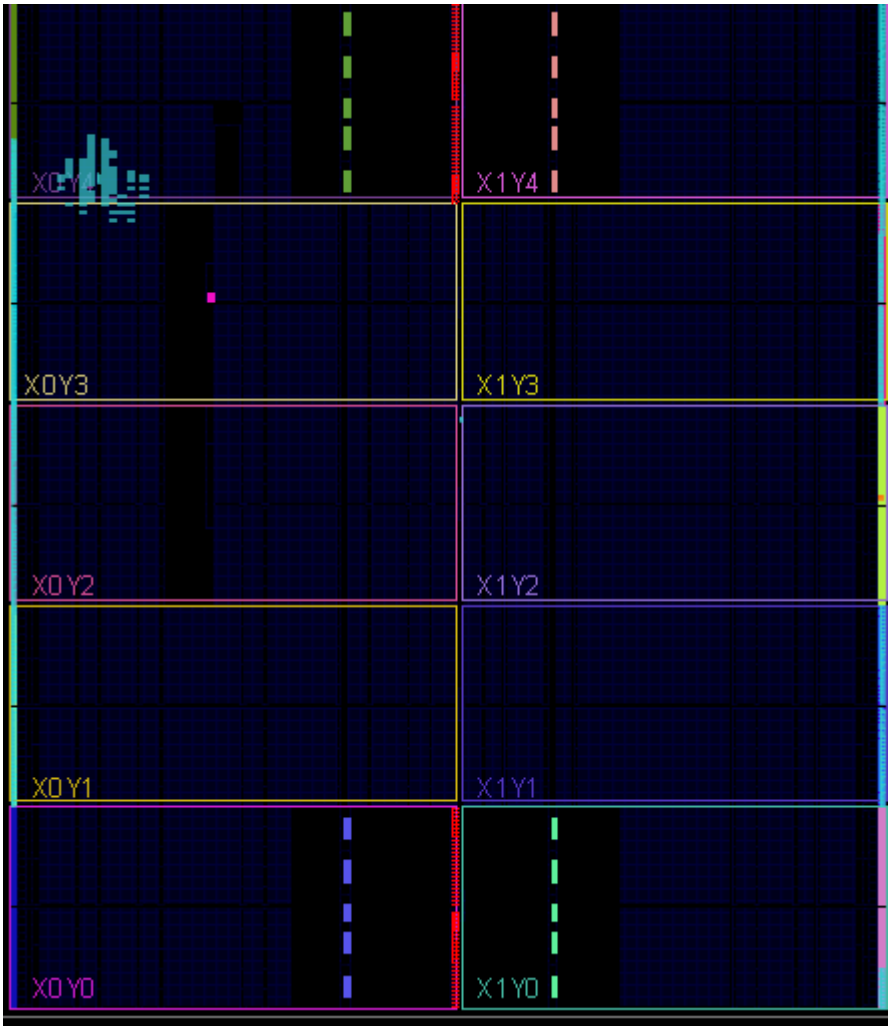
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a200t'
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
- [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
- [Physopt 32-65] No nets found for high-fanout optimization.
- [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- [Place 30-746] Post Placement Timing Summary WNS=4.061. For the most accurate timing information please run report_timing.
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/Personal Courses/Kareem_Waseem_Diploma/projects/Spartan/Vivado/Spartan6/Spartan6.runs/impl_1/DSP48A1_plac
- [runtcl-4] Executing : report_io -file DSP48A1_io_placed.rpt (2 more like this)

Implemented Design (9 infos)

General Messages (9 infos)

- [Netlist 29-17] Analyzing 207 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
  No Unisim elements were transformed.

- **Schematic:**



- **Utilization Report:**

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<1%)
- Slice Logic Distribution
  - Slice (1%)
    - SLICEM
    - SLICEL
  - LUT Flip Flop Pairs (<1%)
    - LUT-FF pairs with one unused LU
    - LUT-FF pairs with one unused Fli

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	303	160	115	303	68	1	327	1
A1 (reg_mux)	33	18	21	33	0	0	0	0
B1 (reg_mux_0)	19	18	18	19	0	0	0	0
C0 (reg_mux__param...	1	48	20	1	0	0	0	0
carry_in (reg_mux__pa...	0	1	1	0	0	0	0	0
carry_out (reg_mux__p...	2	1	2	2	0	0	0	0
D0 (reg_mux_1)	3	18	7	3	0	0	0	0
opmode (reg_mux__p...	207	8	76	207	0	0	0	0
OUT (reg_mux__para...	25	48	27	25	0	0	0	0

- # Timing Report: