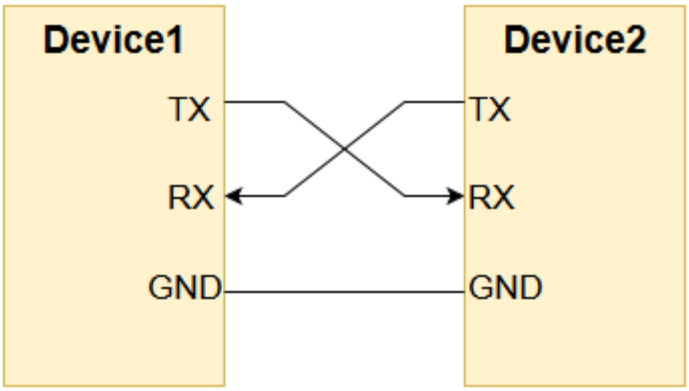
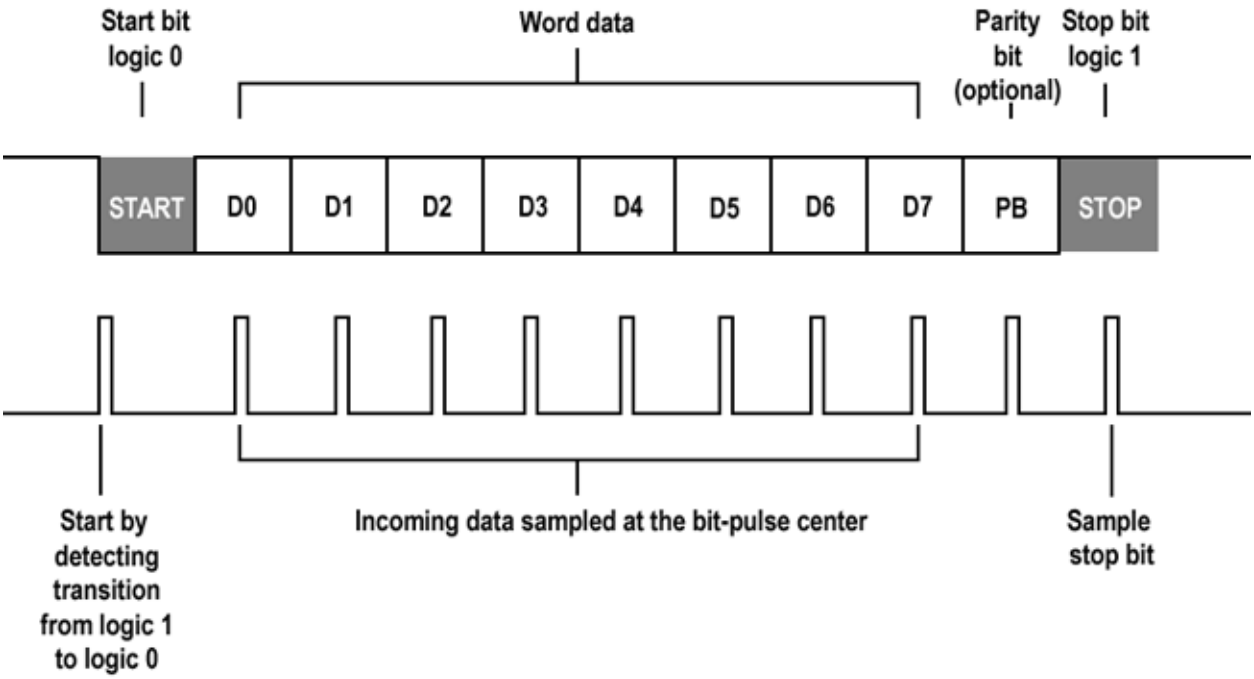
UART Receiver Project

UART is a communication protocol that uses a single connection to send or receive data from another device. For a full duplex connection, two connections are needed between the two devices, each for every direction of transmission. The connection is demonstrated in following diagram:



Data is divided into bytes that are sent using UART frames. These frames are demonstrated in the following diagram:



In an idle state, the connection wire between the two devices is kept at a **logic one** voltage. Start of the UART frame is indicated by the detection of the START bit (**logic zero**). Then the data is serialized bit by bit on the transmission line. Then, there is an optional PARITY bit that is used to detect bit-flips and transmission errors. Then finally there is a STOP bit (**logic one**).

Parity can be odd or even parity depending on the connection specification between the two connected devices.

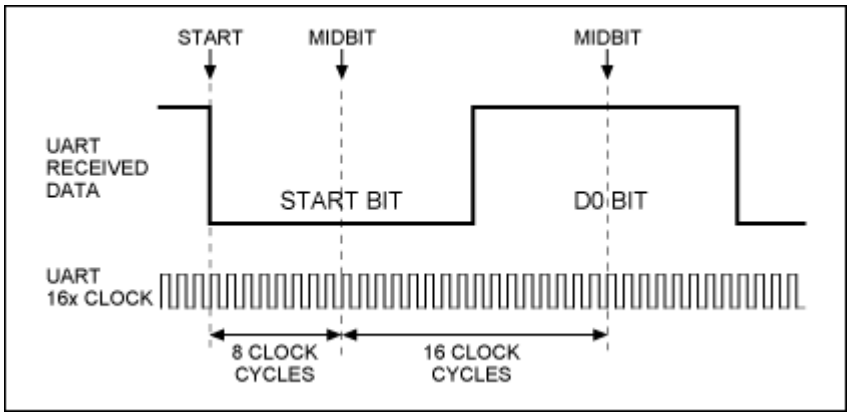
UART RX

When designing a UART receiver, we need to consider sampling using a higher frequency to determine the start of the incoming UART frame. This is not usually done between communicating modules in the same device. However, when it comes to inter-device communication, connection wires (or traces on a PCB) are much more likely to experience interference and possible glitches due to external signals.

In the case of UART receiver, a sampling signal that 16 times the baud rate is usually used by the receiver.

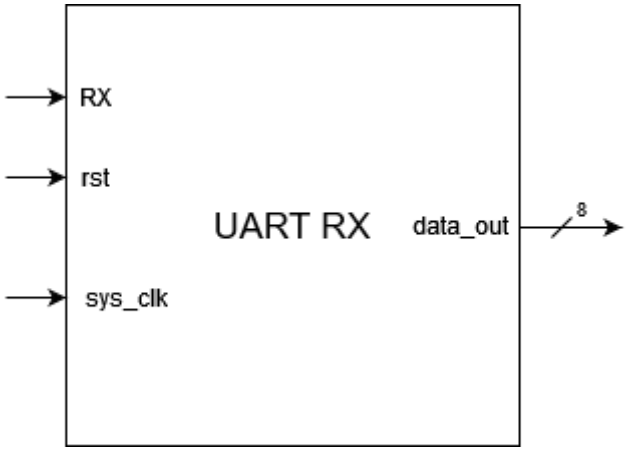
Once the receiver detects the start of a UART frame, it waits for 8 clock periods to sample the middle of the incoming bit (to make sure it is not a glitch). Then, we can now sample the incoming data every 16 clock periods.

This is illustrated in the following timing diagram:



Project Details

It is required to implement a receiver that follows the illustrated diagram:



Signal Name	Description
RX	The data line that will receive transmitted UART frames from the other device
rst	Global asynchronous reset
sys_clk	System clock
data_out	8-bit wide bus showing the last received byte of data from the RX port

It is also required that the design is parameterized to work with different data baud rates. So, the parameters needed in the design shall be illustrated in the following table:

Parameter Name	Description
pBAUD_RATE	Intended baud rate for receiver instance (in bits/sec)
pSYS_CLK_FREQ	Input sys_clk frequency (in Hz)

Deliverables

- ISE project that is ready to be programmed on our SP-605 evaluation kit.